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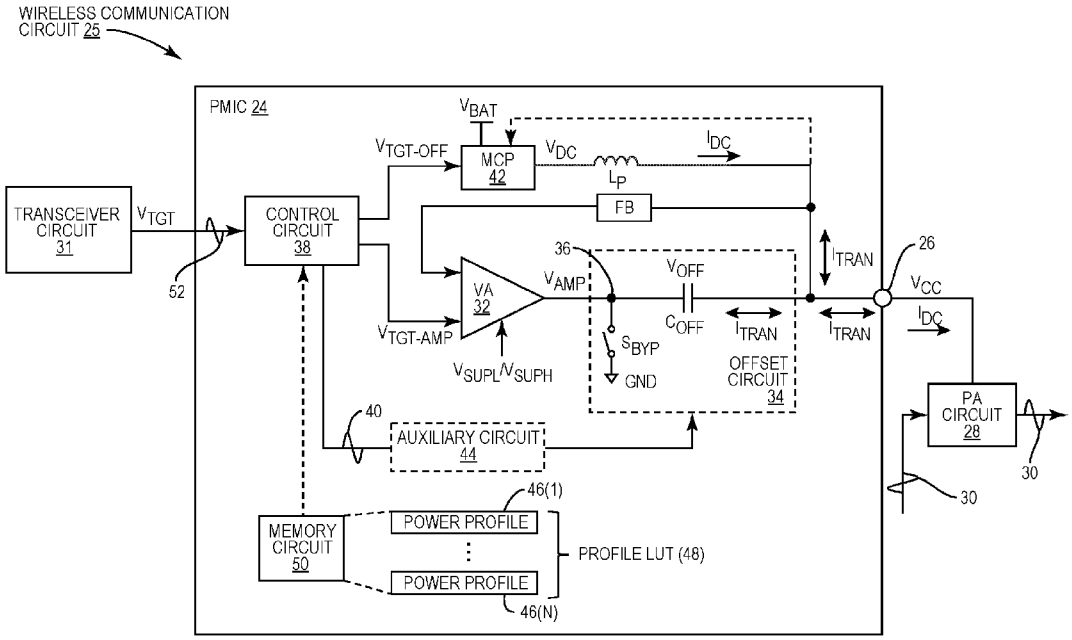

FIG. 2

(57) **Abstract:** A fast-switching power management integrated circuit (PMIC) is provided. The PMIC is configured to provide an average power tracking (APT) voltage to a power amplifier circuit for amplifying a radio frequency (RF) signal modulated in multiple time intervals. Herein, the PMIC is configured to increase or decrease the APT voltage from a present voltage level in a present one of the time intervals to a future voltage level in an upcoming one of the time intervals with very short switching interval (e.g., < 20 nanoseconds). When the APT voltage transitions from the present voltage level to the future voltage level, the PMIC opportunistically activates a voltage amplifier to help ensure proper operation of the power amplifier circuit (e.g., maintain the APT voltage at the present level and reduce ripple in the APT voltage). As a result, the PMIC can switch the APT voltage frequently and rapidly with reduced inrush current.

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FAST-SWITCHING POWER MANAGEMENT INTEGRATED CIRCUIT

Related Applications

[0001] This application claims the benefit of U.S. provisional patent application serial number 63/352,301, filed on June 15, 2022, the disclosure of which is hereby incorporated herein by reference in its entirety.

Field of the Disclosure

[0002] The technology of the disclosure relates generally to a power management integrated circuit (PMIC).

Background

[0003] Fifth-generation (5G) new radio (NR) (5G-NR) has been widely regarded as the next generation of wireless communication technology beyond the current third-generation (3G) and fourth-generation (4G) technologies. In this regard, a wireless communication device capable of supporting the 5G-NR wireless communication technology is expected to achieve higher data rates, improved coverage range, enhanced signaling efficiency, and reduced latency across a wide range of radio frequency (RF) bands, which include a low-band (below 1 GHz), a mid-band (1 GHz to 6 GHz), and a high-band (above 24 GHz).

[0004] Downlink and uplink transmissions in a 5G-NR system are widely based on orthogonal frequency division multiplexing (OFDM). In this regard, Figure 1 is a schematic diagram of an exemplary OFDM time-frequency grid 10 illustrating at least one resource block (RB) 12 for physical resource allocation in the 5G-NR system. The OFDM time-frequency grid 10 includes a frequency axis 14 representing a frequency domain and a time axis 16 representing a time domain. Along the frequency axis 14, there are multiple subcarriers 18(1)-18(M). The subcarriers 18(1)-18(M) are orthogonally separated from each other by a subcarrier spacing (SCS) (e.g., 15 KHz). Along the time axis 16, there are multiple OFDM symbols 20(1)-20(N). The OFDM symbols 20(1)-20(N) may be modulated either as data symbols to carry data payload and/or reference

symbols to carry such reference signals as demodulation reference signals (DMRS), sounding reference signals (SRS), and so on. Each of the OFDM symbols 20(1)-20(N) is separated by a cyclic prefix (CP) (not shown) configured to act as a guard band to help overcome inter-symbol interference (ISI) between the OFDM symbols 20(1)-20(N). In the OFDM time-frequency grid 10, each intersection of the subcarriers 18(1)-18M) and the OFDM symbols 20(1)-20(N) defines a resource element (RE) 22.

[0005] In a 5G-NR communication system, an RF signal can be modulated into multiple subcarriers among the subcarriers 18(1)-18(N) in the frequency domain (along the frequency axis 14) and multiple OFDM symbols among the OFDM symbols 20(1)-20(N) in the time domain (along the time axis 16). The table (Table 1) below summarizes OFDM configurations supported by the 5G-NR communication system.

Table 1

SCS (KHz)	Slot Length (μs)	# of Slots per Subframe	CP (μs)	OFDM Symbol Duration (μs)	Modulation Bandwidth (MHz)
15	1000	1	4.69	71.43	50
30	500	2	2.34	35.71	100
60	250	4	1.17	17.86	200
120	125	8	0.59	8.93	400

[0006] In the 5G-NR communication system, the RF signal is typically modulated with a high modulation bandwidth in excess of 200 MHz. In this regard, according to Table 1, the SCS will be 120 KHz and a transition settling time between two consecutive OFDM symbols among the OFDM symbols 20(1)-20(N) (e.g., amplitude change of the RF signal) needs to be less than or equal to the CP duration of 0.59 μs.

[0007] In addition, the wireless communication device may also need to support such internet-of-things (IoT) applications as keyless car entry, remote garage door opening, contactless payment, mobile boarding pass, and so on. Needless to say, the wireless communication device must also always make

911/E911 service accessible under emergency situations. As such, it is critical that the wireless communication device remains operable whenever needed.

[0008] Notably, the wireless communication device relies on a battery cell (e.g., Li-Ion battery) to power its operations and services. Despite recent advancement in battery technologies, the wireless communication device can run into a low battery situation from time to time. In this regard, it is desirable to prolong battery life concurrent to enabling fast voltage changes between the OFDM symbols 20(1)-20(N).

Summary

[0009] Embodiments of the disclosure relate to a fast-switching power management integrated circuit (PMIC). The PMIC is configured to provide an average power tracking (APT) voltage to a power amplifier circuit for amplifying a radio frequency (RF) signal modulated in multiple time intervals. Herein, the PMIC is configured to increase or decrease the APT voltage from a present voltage level in a present one of the time intervals to a future voltage level in an upcoming one of the time intervals with a very short switching interval (e.g., < 20 nanoseconds). When the APT voltage transitions from the present voltage level to the future voltage level, the PMIC opportunistically activates a voltage amplifier to help ensure proper operation of the power amplifier circuit (e.g., maintain the APT voltage at the present level and reduce ripple in the APT voltage). As a result, the PMIC can switch the APT voltage frequently and rapidly with reduced inrush current.

[0010] In one aspect, a PMIC is provided. The PMIC includes a voltage output that outputs an APT voltage to a power amplifier circuit for amplifying an RF signal modulated in a plurality of modulation units each comprising a plurality of time intervals. The PMIC also includes an offset circuit. The offset circuit is coupled to the voltage output and configured to change the APT voltage from a present voltage level in a present time interval among the plurality of time intervals to a future voltage level in an upcoming time interval among the plurality of time intervals during a transition interval that falls within one of the present

time interval and the upcoming time interval. The PMIC also includes a voltage amplifier. The voltage amplifier is coupled to an input of the offset circuit. The voltage amplifier is activated at a start of the transition interval and deactivated at an end of the transition interval to generate a modulated voltage at the input of the offset circuit based on an amplifier target voltage determined to cause the modulated voltage to be higher than or equal to a headroom voltage at the end of the transition interval.

[0011] In another aspect, a wireless communication circuit is provided. The wireless communication circuit includes a PMIC. The PMIC includes a voltage output that outputs an APT voltage for amplifying an RF signal modulated in a plurality of modulation units each comprising a plurality of time intervals. The PMIC also includes an offset circuit. The offset circuit is coupled to the voltage output and configured to change the APT voltage from a present voltage level in a present time interval among the plurality of time intervals to a future voltage level in an upcoming time interval among the plurality of time intervals during a transition interval that falls within one of the present time interval and the upcoming time interval. The PMIC also includes a voltage amplifier. The voltage amplifier is coupled to an input of the offset circuit. The voltage amplifier is activated at a start of the transition interval and deactivated at an end of the transition interval to generate a modulated voltage at the input of the offset circuit based on an amplifier target voltage determined to cause the modulated voltage to be higher than or equal to a headroom voltage at the end of the transition interval.

[0012] Those skilled in the art will appreciate the scope of the present disclosure and realize additional aspects thereof after reading the following detailed description of the preferred embodiments in association with the accompanying drawing figures.

Brief Description of the Drawing Figures

[0013] The accompanying drawing figures incorporated in and forming a part of this specification illustrate several aspects of the disclosure, and together with the description serve to explain the principles of the disclosure.

[0014] Figure 1 is a schematic diagram of an exemplary orthogonal frequency division multiplexing (OFDM) time-frequency grid illustrating at least one resource block (RB) for physical resource allocation;

[0015] Figure 2 is a schematic diagram of an exemplary power management integrated circuit (PMIC) configured according to embodiments of the present disclosure to support fast average power tracking (APT) voltage switching;

[0016] Figure 3 is a timing diagram providing an exemplary illustration of the PMIC of Figure 2 configured according to an embodiment of the present disclosure to increase the APT voltage from a present voltage level to a future voltage level;

[0017] Figure 4 is a timing diagram providing an exemplary illustration of the PMIC of Figure 2 configured according to an embodiment of the present disclosure to decrease the APT voltage from a present voltage level to a future voltage level;

[0018] Figure 5 is a timing diagram providing an exemplary illustration of the PMIC of Figure 2 configured according to another embodiment of the present disclosure to decrease the APT voltage from a present voltage level to a future voltage level;

[0019] Figures 6A and 6B are block diagrams providing exemplary illustrations of some power profiles that may be used by the PMIC of Figure 2 for enabling fast APT voltage switching; and

[0020] Figure 7 is a schematic diagram of an exemplary user element wherein the PMIC of Figure 2 can be provided.

Detailed Description

[0021] The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the embodiments and illustrate the

best mode of practicing the embodiments. Upon reading the following description in light of the accompanying drawing figures, those skilled in the art will understand the concepts of the disclosure and will recognize applications of these concepts not particularly addressed herein. It should be understood that these concepts and applications fall within the scope of the disclosure and the accompanying claims.

[0022] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present disclosure. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0023] It will be understood that when an element such as a layer, region, or substrate is referred to as being "on" or extending "onto" another element, it can be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or extending "directly onto" another element, there are no intervening elements present. Likewise, it will be understood that when an element such as a layer, region, or substrate is referred to as being "over" or extending "over" another element, it can be directly over or extend directly over the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly over" or extending "directly over" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

[0024] Relative terms such as "below" or "above" or "upper" or "lower" or "horizontal" or "vertical" may be used herein to describe a relationship of one

element, layer, or region to another element, layer, or region as illustrated in the Figures. It will be understood that these terms and those discussed above are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures.

[0025] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the disclosure. As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes," and/or "including" when used herein specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0026] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms used herein should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0027] Embodiments of the disclosure relate to a fast-switching power management integrated circuit (PMIC). The PMIC is configured to provide an average power tracking (APT) voltage to a power amplifier circuit for amplifying a radio frequency (RF) signal modulated in multiple time intervals. Herein, the PMIC is configured to increase or decrease the APT voltage from a present voltage level in a present one of the time intervals to a future voltage level in an upcoming one of the time intervals with a very short switching interval (e.g., < 20 nanoseconds). When the APT voltage transitions from the present voltage level to the future voltage level, the PMIC opportunistically activates a voltage amplifier to help ensure proper operation of the power amplifier circuit (e.g., maintain the APT voltage at the present level and reduce ripple in the APT voltage). As a

result, the PMIC can switch the APT voltage frequently and rapidly with reduced inrush current.

[0028] In this regard, Figure 2 is a schematic diagram of an exemplary PMIC 24, which is provided in a wireless communication circuit 25 and configured according to embodiments of the present disclosure to support fast APT voltage switching. The PMIC 24 includes a voltage output 26 that outputs an APT voltage V_{CC} to a power amplifier circuit 28 in the wireless communication circuit 25. The power amplifier circuit 28 is configured to amplify an RF signal 30 based on the APT voltage V_{CC}. The RF signal 30, which may be generated by a transceiver circuit 31 in the wireless communication circuit 25, is modulated in multiple modulation units, each of which is further divided into multiple time intervals. In the context of the present disclosure, the modulation units are equivalent to time-division duplex (TDD) time slots or mini time slots, and the time intervals inside each of the modulation units are equivalent to orthogonal frequency division multiplexing (OFDM) symbols, such as the OFDM symbols 20(1)-20(N) in Figure 1. In this regard, each of the time intervals can be modulated to carry a data payload (referred herein as "a data symbol") and a reference signal (referred herein as "a reference symbol"), such as a demodulation reference signal (DMRS), a sounding reference signal (SRS), and so on.

[0029] Given that the power amplifier circuit 28 needs to amplify the data symbols and the reference symbols to different power levels, the PMIC 24 may need to adapt (increase or decrease) the APT voltage V_{CC} on a per-symbol basis. Moreover, as previously described in Figure 1, the PMIC 24 must complete the APT voltage V_{CC} within the respective cyclic prefix (CP) in each of the OFDM symbols 20(1)-20(N).

[0030] The PMIC 24 includes a voltage amplifier 32 (denoted as "VA") and an offset circuit 34. The voltage amplifier 32 is coupled to an input 36 of the offset circuit 34 and the offset circuit 34 is coupled to the voltage output 26. In the context of the present disclosure, the power amplifier circuit 28 is assumed to have a much higher bandwidth than that of the offset circuit 34. As described in

detail below, the offset circuit 34 is configured to change (increase or decrease) the APT voltage V_{CC} from a present voltage level (denoted as "$V_{CC(N-1)}$" in Figures 3 to 5) to a future voltage level (denoted as "$V_{CC(N)}$" in Figures 3 to 5) between a pair of adjacent time intervals (denoted as "S_{N-1}" and "S_N" in Figures 3 to 5). For the sake of distinction, the time intervals S_{N-1} and S_N are also referred to as a "present time interval" and an "upcoming time interval," respectively.

[0031] More specifically, the offset circuit 34 will cause the APT voltage V_{CC} to change from the present voltage level $V_{CC(N-1)}$ in the present time interval S_{N-1} to the future voltage level $V_{CC(N)}$ in the upcoming time interval S_N during a transition interval (denoted as "TP" in Figures 3 to 5). Depending on whether the APT voltage V_{CC} is increasing or decreasing from the present time interval S_{N-1} to the upcoming time interval S_N, the transition interval TP can be located either in the present time interval S_{N-1} or in the upcoming time interval S_N to ensure that the APT voltage V_{CC} can reach the future voltage level $V_{CC(N)}$ by the CP of the upcoming time interval S_N.

[0032] As further illustrated in Figures 3 to 5, while the APT voltage V_{CC} transitions from the present voltage level $V_{CC(N-1)}$ to the future voltage level $V_{CC(N)}$ during the transition interval TP, the voltage amplifier 32 is activated at a start of the transition interval TP (denoted as "T_1") and deactivated at an end of the transition interval TP (denoted as "T_2") to ensure proper operation of the power amplifier circuit 28. According to an embodiment of the present disclosure, the voltage amplifier 32 will provide a modulated voltage V_{AMP} at an input 36 of the offset circuit 34. In a non-limiting example, the voltage amplifier 32 is configured to generate the modulated voltage V_{AMP} based on an amplifier target voltage $V_{TGT-AMP}$ and one of a lower supply voltage V_{SUPL} and a higher supply voltage V_{SUPH} ($V_{SUPH} > V_{SUPL}$).

[0033] As discussed in detailed examples in Figures 3 to 5, the amplifier target voltage $V_{TGT-AMP}$ is so determined to ensure that the voltage amplifier 32 can maintain the modulated voltage V_{AMP} at or above a headroom voltage (denoted as "V_{NHEAD}" in Figures 3 to 5), which is greater than 0 V, at the end T_2 of the transition interval TP. As a result, the voltage amplifier 32 can maintain the

APT voltage V_{CC} at the present voltage level $V_{CC(N-1)}$ and suppress ripple in the APT voltage V_{CC} during the transition interval TP to thereby ensure the proper operation of the power amplifier circuit 28 during the transition interval TP.

[0034] According to an embodiment of the present disclosure, the PMIC 24 can include a control circuit 38, which can be a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC), as an example. In one aspect, the control circuit 38 may be configured to determine whether the transition interval TP should be within the present time interval S_{N-1} or the upcoming time interval S_N based on a differential ΔV_{CC} between the present voltage level $V_{CC(N-1)}$ and the future voltage level $V_{CC(N)}$ ($\Delta V_{CC} = V_{CC(N-1)} - V_{CC(N)}$). Understandably, the differential ΔV_{CC} will be positive when the present voltage level $V_{CC(N-1)}$ is higher than the future voltage level $V_{CC(N)}$ or negative when the present voltage level $V_{CC(N-1)}$ is lower than the future voltage level $V_{CC(N)}$. In a non-limiting example, the control circuit 38 can receive a modulated target voltage V_{TGT}, which indicates the future voltage level $V_{CC(N)}$ in the upcoming time interval S_N, from the transceiver circuit 31. Accordingly, the control circuit 38 may control the offset circuit 34 (e.g., via a control signal 40) to transition from the present voltage level $V_{CC(N-1)}$ to the future voltage level $V_{CC(N)}$ during the transition interval TP.

[0035] In another aspect, the control circuit 38 may also be configured to determine the amplifier target voltage $V_{TGT-AMP}$ based on the determined differential ΔV_{CC}. In a non-limiting example, when the future voltage level $V_{CC(N)}$ is higher than the present voltage level $V_{CC(N-1)}$, as illustrated in Figure 3, the amplifier target voltage $V_{TGT-AMP}$ is equal to a sum of the future voltage level $V_{CC(N)}$ and a markup voltage (denoted as "V_{DIFF}"), as shown in equation (Eq. 1) below. In another non-limiting example, when the future voltage level $V_{CC(N)}$ is lower than the present voltage level $V_{CC(N-1)}$, as illustrated in Figures 4 and 5, the amplifier target voltage $V_{TGT-AMP}$ is equal to a sum of the present voltage level $V_{CC(N-1)}$ and the markup voltage V_{DIFF}, as shown in equation (Eq. 2) below.

$$V_{TGT-AMP} = V_{CC(N)} + V_{DIFF} \qquad \text{(Eq. 1)}$$

$$V_{TGT\text{-}AMP} = V_{CC(N-1)} + V_{DIFF} \qquad \text{(Eq. 2)}$$

[0036] In the equations (Eq. 1 and Eq. 2), the markup voltage V_{DIFF} can be of different values depending on how the APT voltage V_{CC} will change from the present time interval S_{N-1} to the upcoming time interval S_N. In this regard, by changing the amplifier target voltage $V_{TGT\text{-}AMP}$ and, more specifically the markup voltage V_{DIFF}, the control circuit 38 can cause the voltage amplifier 32 to generate the modulated voltage V_{AMP} at appropriate levels during the transition interval TP to maintain proper operation of the power amplifier circuit 28.

[0037] In yet another aspect, the control circuit 38 may be further configured to activate the voltage amplifier 32 at the start T_1 of the transition interval TP and deactivate the voltage amplifier 32 at the end T_2 of the transition interval TP. In a non-limiting example, the control circuit 38 can cause the voltage amplifier 32 to be deactivated in response to receiving the lower supply voltage V_{SUPL} or activated in response to receiving the higher supply voltage V_{SUPH}. By controlling the offset circuit 34 to change the APT voltage V_{CC} and opportunistically activating/deactivating the voltage amplifier 32 to ensure proper operation of the power amplifier circuit 28 during the transition interval TP, the PMIC 24 can switch the APT voltage V_{CC} efficiently under the increasingly stringent switching time requirements (e.g., < 20 ns).

[0038] The PMIC 24 also includes a multi-level charge pump (MCP) 42. The MCP 42, which may be a direct current (DC)-DC buck-boost converter, is configured to generate a low-frequency voltage V_{DC} (e.g., DC voltage) based on a battery voltage V_{BAT}. Specifically, the MCP 42 may operate in a buck mode to generate the low-frequency voltage V_{DC} at $0\times V_{BAT}$ or $1\times V_{BAT}$, or in a boost mode to generate the low-frequency voltage V_{DC} at $2\times V_{BAT}$. The MCP 42 may be configured to toggle between the buck mode and the boost mode based on a particular duty cycle (e.g., 20%@$0\times V_{BAT}$, 30%@$1\times V_{BAT}$, and 50%@$2\times V_{BAT}$). As such, the MCP 42 may be controlled to generate the low-frequency voltage V_{DC} at a desired level.

[0039] In an embodiment, the control circuit 38 may be further configured to generate an offset target voltage $V_{TGT\text{-}OFF}$ based on the modulated target voltage V_{TGT}. The offset target voltage $V_{TGT\text{-}OFF}$ may indicate the future voltage level $V_{CC(N)}$ of the APT voltage V_{CC}. Accordingly, the MCP 42 may determine and operate based on a corresponding duty cycle to generate the low-frequency voltage V_{DC} at the desired level as indicated by the offset target voltage $V_{TGT\text{-}OFF}$.

[0040] The PMIC 24 also includes a power inductor L_P. The power inductor L_P is coupled between the MCP 42 and the voltage output 26 and is configured to induce a low-frequency current I_{DC} (e.g., a DC current) based on the low-frequency voltage V_{DC}. Understandably, the low-frequency current I_{DC} that may be induced is a function of the low-frequency voltage V_{DC} and an inductance of the power inductor L_P. Accordingly, the control circuit 38 may further change the low-frequency current I_{DC} based on the offset target voltage $V_{TGT\text{-}OFF}$. In an embodiment, the MCP 42 may receive feedback from the APT voltage V_{CC}.

[0041] Herein, the offset circuit 34 includes an offset capacitor C_{OFF} and a bypass switch S_{BYP}. The offset capacitor C_{OFF} is coupled between the input 36 and the voltage output 26, and the bypass switch S_{BYP} is coupled between the input 36 and a ground (GND).

[0042] Under one operating scenario, the APT voltage V_{CC} is set to increase from the present voltage level $V_{CC(N-1)}$ in the present time interval S_{N-1} to the future voltage level $V_{CC(N)}$ in the upcoming time interval S_N ($V_{CC(N-1)} < V_{CC(N)}$). In this regard, the control circuit 38 will set the offset target voltage $V_{TGT\text{-}OFF}$ to the future voltage level $V_{CC(N)}$ of the APT voltage V_{CC} to cause the low-frequency current I_{DC} to be generated at a desired amount to thereby charge the offset capacitor C_{OFF} to the future voltage level $V_{CC(N)}$.

[0043] The control circuit 38 will open the bypass switch S_{BYP} and activate the voltage amplifier 32 at the start of the transition interval TP to generate the amplifier target voltage $V_{TGT\text{-}AMP}$ at a level higher than the future voltage level $V_{CC(N)}$ such that a current I_{TRAN} can flow from the MCP 42 through the offset capacitor C_{OFF} and sink in the voltage amplifier 32. In a non-limiting example, the PMIC 24 can include an auxiliary circuit 44, which can provide additional current

to help maintain the modulated voltage V_{AMP} in the presence of the current I_{TRAN}. As a result, the current I_{TRAN} will gradually charge the offset capacitor C_{OFF} to the future voltage level $V_{CC(N)}$ during the transition interval TP. When the offset capacitor C_{OFF} is charged up to the future voltage level $V_{CC(N)}$ at the end of the transition interval TP, the control circuit 38 deactivates the voltage amplifier 32 and closes the bypass switch S_{BYP}. Thereafter, the offset capacitor C_{OFF} and the MCP 42 will maintain the APT voltage V_{CC} at the future voltage level $V_{CC(N)}$ in the remainder of the upcoming time interval S_N.

[0044] The operating scenario described above can be graphically illustrated in Figure 3. Figure 3 is a timing diagram providing an exemplary illustration as to how the PMIC 24 of Figure 2 operates under the above-described operating scenario to increase the APT voltage V_{CC}. Elements in Figure 2 are referenced in Figure 3 and will not be re-described herein.

[0045] As illustrated, the transition interval TP falls completely within the upcoming time interval S_N, wherein the start T_1 of the transition interval TP is aligned with a boundary T_0 (a.k.a. a starting time of the CP in the upcoming time interval S_N) between the present time interval S_{N-1} and the upcoming time interval S_N, and the end T_2 of the transition interval TP comes after time T_3 (a.k.a. an ending time of the CP in the upcoming time interval S_N). Understandably, the CP is typically much shorter than the transition interval TP. Herein, the modulated target voltage V_{TGT} indicates that the APT voltage V_{CC} will increase from the present voltage level $V_{CC(N-1)}$ (e.g., 2.3 V) in the present time interval S_{N-1} to the future voltage level $V_{CC(N)}$ (e.g., 2.9 V) in the upcoming time interval S_N. Accordingly, the control circuit 38 determines the offset target voltage $V_{TGT-OFF}$ to be equal to the future voltage level $V_{CC(N)}$.

[0046] As for the amplifier target voltage $V_{TGT-AMP}$, the control circuit 38 is configured to set the markup voltage V_{DIFF} in the equation (Eq. 1) to be equal to the headroom voltage V_{NHEAD} ($V_{TGT-AMP} = V_{CC(N)} + V_{NHEAD}$). At time T_1, the control circuit 38 opens the bypass switch S_{BYP} and activates the voltage amplifier 32 (e.g., by coupling the higher supply voltage V_{SUPH} to the voltage amplifier 32). Accordingly, the voltage amplifier 32 will generate the modulated voltage V_{AMP} at

the input 36 in accordance with the amplifier target voltage $V_{TGT-AMP}$. In a non-limiting example, the voltage amplifier 32, with assistance from the auxiliary circuit 44, can quickly drive the modulated voltage V_{AMP} from a GND level to the differential ΔV_{CC} ($\Delta V_{CC} < 0$) at time T_3 to help stabilize the APT voltage V_{CC} during the transition interval TP. Thereafter, the voltage amplifier 32 gradually decreases the modulated voltage V_{AMP} to the headroom voltage V_{NHEAD} at time T_2.

[0047] Starting at time T_1, the offset capacitor C_{OFF} is gradually charged up to reach the future voltage level $V_{CC(N)}$ at time T_2. Accordingly, at time T_2, the control circuit 38 closes the bypass switch S_{BYP} and deactivates the voltage amplifier 32 to let the modulated voltage V_{AMP} return to the GND level. The APT voltage V_{CC}, which equals a sum of the modulated voltage V_{AMP} and the offset voltage V_{OFF}, will settle at the future voltage level $V_{CC(N)}$ at time T_3. Notably, since the voltage amplifier 32 maintains the modulated voltage V_{AMP} at or above the headroom voltage V_{NHEAD} while the bypass switch S_{BYP} is toggled, the APT voltage V_{CC} will not drop below the headroom voltage V_{NHEAD}, thus ensuring proper operation of the power amplifier circuit 28.

[0048] With reference back to Figure 2, under another operating scenario, the APT voltage V_{CC} is set to decrease from the present voltage level $V_{CC(N-1)}$ in the present time interval S_{N-1} to the future voltage level $V_{CC(N)}$ in the upcoming time interval S_N ($V_{CC(N-1)} > V_{CC(N)}$). In this regard, the control circuit 38 will set the offset target voltage $V_{TGT-OFF}$ to the future voltage level $V_{CC(N)}$ of the APT voltage V_{CC} to cause the low-frequency current I_{DC} to be generated at a desired amount to thereby cause the offset capacitor C_{OFF} to be discharged to the future voltage level $V_{CC(N)}$.

[0049] The control circuit 38 will open the bypass switch S_{BYP} and activate the voltage amplifier 32 at the start of the transition interval TP to generate the amplifier target voltage $V_{TGT-AMP}$ at the present voltage level $V_{CC(N-1)}$ such that the current I_{TRAN} can flow from the voltage amplifier 32 through the offset capacitor C_{OFF} and return to the MCP 42 and/or the power amplifier circuit 28. In a non-limiting example, the auxiliary circuit 44 can provide additional current to help

maintain the modulated voltage V_{AMP} in the presence of the current I_{TRAN}. As a result, the offset capacitor C_{OFF} will be gradually discharged to the future voltage level $V_{CC(N)}$ during the transition interval TP. When the offset capacitor C_{OFF} is discharged to the future voltage level $V_{CC(N)}$ at the end of the transition interval TP, the control circuit 38 deactivates the voltage amplifier 32 and closes the bypass switch S_{BYP}. Thereafter, the offset capacitor C_{OFF} and the MCP 42 will maintain the APT voltage V_{CC} at the future voltage level $V_{CC(N)}$ in the remainder of the upcoming time interval S_N.

[0050] The operating scenario described above can be graphically illustrated in Figures 4 and 5. Figure 4 is a timing diagram providing an exemplary illustration as to how the PMIC 24 of Figure 2 operates under one possibility of the above-described operating scenario to decrease the APT voltage V_{CC}. More specifically, Figure 4 illustrates a situation where the headroom voltage V_{NHEAD} (e.g., 0.4 V) is lower than the differential ΔV_{CC} (e.g., 0.6 V) between the present voltage level $V_{CC(N-1)}$ and the future voltage level $V_{CC(N)}$ ($V_{NHEAD} < \Delta V_{CC}$). Elements in Figure 2 are referenced in Figure 4 and will not be re-described herein.

[0051] As illustrated, the transition interval TP falls completely within the present time interval S_{N-1}, wherein the start T_1 of the transition interval TP begins prior to a boundary T_0 between the present time interval S_{N-1} and the upcoming time interval S_N, and the end T_2 of the transition interval TP is aligned with the boundary T_0 (a.k.a. a starting time of the CP in the upcoming time interval S_N). Understandably, the CP is typically much shorter than the transition interval TP. Herein, the modulated target voltage V_{TGT} indicates that the APT voltage V_{CC} will decrease from the present voltage level $V_{CC(N-1)}$ (e.g., 2.9 V) in the present time interval S_{N-1} to the future voltage level $V_{CC(N)}$ (e.g., 2.3 V) in the upcoming time interval S_N. Accordingly, the control circuit 38 determines the offset target voltage $V_{TGT-OFF}$ to be equal to the future voltage level $V_{CC(N)}$.

[0052] As for the amplifier target voltage $V_{TGT-AMP}$, the control circuit 38 is configured to set the markup voltage V_{DIFF} in the equation (Eq. 2) to 0 V ($V_{TGT-AMP} = V_{CC(N-1)} + 0$). At time T_1, the control circuit 38 opens the bypass switch S_{BYP}

and activates the voltage amplifier 32 (e.g., by coupling the higher supply voltage V_{SUPH} to the voltage amplifier 32). Accordingly, the voltage amplifier 32 will generate the modulated voltage V_{AMP} at the input 36 in accordance with the amplifier target voltage $V_{TGT\text{-}AMP}$. In a non-limiting example, the voltage amplifier 32, with assistance from the auxiliary circuit 44, can instantly drive the modulated voltage V_{AMP} from a GND level to the headroom voltage V_{NHEAD} at time T_1. Thereafter, the voltage amplifier 32 will continue to drive the modulated voltage V_{AMP} up to the voltage differential ΔV_{CC} at time T_2.

[0053] Starting at time T_1, the offset capacitor C_{OFF} is gradually discharged to reach the future voltage level $V_{CC(N)}$ at time T_2. Accordingly, at time T_2, the control circuit 38 closes the bypass switch S_{BYP} and deactivates the voltage amplifier 32 to let the modulated voltage V_{AMP} return to the GND level at time T_3. The APT voltage V_{CC}, which equals a sum of the modulated voltage V_{AMP} and the offset voltage V_{OFF}, will settle at the future voltage level $V_{CC(N)}$ at time T_3. Notably, since the voltage amplifier 32 maintains the modulated voltage V_{AMP} at or above the headroom voltage V_{NHEAD} while the bypass switch S_{BYP} is toggled, the APT voltage V_{CC} will not drop below the headroom voltage V_{NHEAD}, thus ensuring proper operation of the power amplifier circuit 28.

[0054] Figure 5 is a timing diagram providing an exemplary illustration as to how the PMIC 24 of Figure 2 operates under another possibility of the above-described operating scenario to decrease the APT voltage V_{CC}. More specifically, Figure 5 illustrates a situation where the headroom voltage V_{NHEAD} (e.g., 0.4 V) is higher than or equal to the differential ΔV_{CC} (e.g., 0.1 V) between the present voltage level $V_{CC(N-1)}$ and the future voltage level $V_{CC(N)}$ ($V_{NHEAD} \geq \Delta V_{CC}$). Elements in Figure 2 are referenced in Figure 5 and will not be re-described herein.

[0055] As illustrated, the transition interval TP falls completely within the present time interval S_{N-1}, wherein the start T_1 of the transition interval TP begins prior to a boundary T_0 between the present time interval S_{N-1} and the upcoming time interval S_N, and the end T_2 of the transition interval TP is aligned with the boundary T_0 (a.k.a. a starting time of the CP in the upcoming time interval S_N).

Understandably, the CP is typically much shorter than the transition interval TP. Herein, the modulated target voltage V_{TGT} indicates that the APT voltage V_{CC} will decrease from the present voltage level $V_{CC(N-1)}$ (e.g., 2.9 V) in the present time interval S_{N-1} to the future voltage level $V_{CC(N)}$ (e.g., 2.8 V) in the upcoming time interval S_N. Accordingly, the control circuit 38 determines the offset target voltage $V_{TGT-OFF}$ to be equal to the future voltage level $V_{CC(N)}$.

[0056] As for the amplifier target voltage $V_{TGT-AMP}$, the control circuit 38 is configured to set the markup voltage V_{DIFF} in the equation (Eq. 2) to equal the headroom voltage V_{NHEAD} minus the differential ΔV_{CC} between the present voltage level $V_{CC(N-1)}$ and the future voltage level $V_{CC(N)}$ ($V_{TGT-AMP} = V_{CC(N-1)} + V_{NHEAD} - \Delta V_{CC}$). At time T_1, the control circuit 38 opens the bypass switch S_{BYP} and activates the voltage amplifier 32 (e.g., by coupling the higher supply voltage V_{SUPH} to the voltage amplifier 32). Accordingly, the voltage amplifier 32 will generate the modulated voltage V_{AMP} at the input 36 in accordance with the amplifier target voltage $V_{TGT-AMP}$. In a non-limiting example, the voltage amplifier 32, with assistance from the auxiliary circuit 44, can instantly drive the modulated voltage V_{AMP} from a GND level to the differential ΔV_{CC} at time T_1. Thereafter, the voltage amplifier 32 will continue to drive the modulated voltage V_{AMP} up to the headroom voltage V_{NHEAD} at time T_2.

[0057] Starting at time T_1, the offset capacitor C_{OFF} is gradually discharged to reach the future voltage level $V_{CC(N)}$ at time T_2. Accordingly, at time T_2, the control circuit 38 closes the bypass switch S_{BYP} and deactivates the voltage amplifier 32 to let the modulated voltage V_{AMP} return to the GND level at time T_3. The APT voltage V_{CC}, which equals a sum of the modulated voltage V_{AMP} and the offset voltage V_{OFF}, will settle at the future voltage level $V_{CC(N)}$ at time T_3. Notably, since the voltage amplifier 32 maintains the modulated voltage V_{AMP} at or above the headroom voltage V_{NHEAD} while the bypass switch S_{BYP} is toggled, the APT voltage V_{CC} will not drop below the headroom voltage V_{NHEAD}, thus ensuring proper operation of the power amplifier circuit 28.

[0058] With reference back to Figure 2, in examples describe above, the control circuit 38 is configured to receive the modulated target voltage V_{TGT} on a

per time interval (a.k.a. per OFDM symbol) basis. In other words, the transceiver circuit 31 must communicate the future voltage level $V_{CC(N)}$ in the upcoming time interval S_N during, or even before, the present time interval S_{N-1}. As previously described in Figure 1, in a time-division duplex (TDD) system, multiple time intervals (a.k.a. OFDM symbols) can be include in a modulation unit (a.k.a. TDD time slot or mini time slot). As such, it may be possible for the control circuit 38 to receive the modulated target voltage V_{TGT} on a per modulation unit (a.k.a. TDD time slot or mini time slot) basis.

[0059] In this regard, the PMIC 24 may be preconfigured to include multiple power profiles 46(1)-46(N). In a non-limiting example, the power profiles 46(1)-46(N) can be organized into a profile lookup table (LUT) 48 and stored in a memory circuit 50. The power profiles 46(1)-46(N) may be stored in the memory circuit 50 by the transceiver circuit 31 via, for example, an RF front-end (RFFE) interface (not shown).

[0060] Figures 6A and 6B are block diagrams providing exemplary illustrations of the power profiles 46(1)-46(N) that may be employed by the PMIC 24 of Figure 2 for enabling fast switching of the APT voltage V_{CC}. Herein, each of the power profiles 46(1)-46(N) corresponds to a TDD time slot.

[0061] Figure 6A shows an exemplary power profile 46A among the power profiles 46(1)-46(N). As shown, the power profile 46A may be determined to indicate the future voltage levels of one or more data symbols and one or more SRS symbols.

[0062] Figure 6B shows an exemplary power profile 46B among the power profiles 46(1)-46(N). As shown, the power profile 46B may be determined to indicate the future voltage levels of one or more data symbols and one or more DMRS symbols.

[0063] With reference back to Figure 2, in an embodiment, the transceiver circuit 31 may communicate a profile indication 52 to indicate a selected power profile among the power profiles 46(1)-46(N) to be used for an upcoming modulation unit (e.g., TDD time slot) during, or prior to, a present modulation unit

(e.g., TDD time slot). Accordingly, the control circuit 38 may retrieve the selected power profile from the profile LUT 48 based on the received profile indication 52.

[0064] The PMIC 24 of Figure 2 can be provided in a user element to enable fast voltage switching. Figure 7 is a schematic diagram of an exemplary user element 100 wherein the PMIC of Figure 2 can be provided.

[0065] Herein, the user element 100 can be any type of user elements, such as mobile terminals, smart watches, tablets, computers, navigation devices, access points, and like wireless communication devices that support wireless communications, such as cellular, wireless local area network (WLAN), Bluetooth, and near field communications. The user element 100 will generally include a control system 102, a baseband processor 104, transmit circuitry 106, receive circuitry 108, antenna switching circuitry 110, multiple antennas 112, and user interface circuitry 114. In a non-limiting example, the control system 102 can be a field-programmable gate array (FPGA), as an example. In this regard, the control system 102 can include at least a microprocessor(s), an embedded memory circuit(s), and a communication bus interface(s). The receive circuitry 108 receives radio frequency signals via the antennas 112 and through the antenna switching circuitry 110 from one or more base stations. A low noise amplifier and a filter cooperate to amplify and remove broadband interference from the received signal for processing. Downconversion and digitization circuitry (not shown) will then downconvert the filtered, received signal to an intermediate or baseband frequency signal, which is then digitized into one or more digital streams using analog-to-digital converter(s) (ADC).

[0066] The baseband processor 104 processes the digitized received signal to extract the information or data bits conveyed in the received signal. This processing typically comprises demodulation, decoding, and error correction operations, as will be discussed in greater detail below. The baseband processor 104 is generally implemented in one or more digital signal processors (DSPs) and application specific integrated circuits (ASICs).

[0067] For transmission, the baseband processor 104 receives digitized data, which may represent voice, data, or control information, from the control system

102, which it encodes for transmission. The encoded data is output to the transmit circuitry 106, where a digital-to-analog converter(s) (DAC) converts the digitally encoded data into an analog signal and a modulator modulates the analog signal onto a carrier signal that is at a desired transmit frequency or frequencies. A power amplifier will amplify the modulated carrier signal to a level appropriate for transmission, and deliver the modulated carrier signal to the antennas 112 through the antenna switching circuitry 110. The multiple antennas 112 and the replicated transmit and receive circuitries 106, 108 may provide spatial diversity. Modulation and processing details will be understood by those skilled in the art.

[0068] Those skilled in the art will recognize improvements and modifications to the preferred embodiments of the present disclosure. All such improvements and modifications are considered within the scope of the concepts disclosed herein and the claims that follow.

Claims

What is claimed is:

1. A power management integrated circuit, PMIC, (24) comprising:

a voltage output (26) that outputs an average power tracking, APT, voltage (V_{CC}) to a power amplifier circuit (28) for amplifying a radio frequency, RF, signal (30) modulated in a plurality of modulation units each comprising a plurality of time intervals (S_{N-1}, S_N);

an offset circuit (34) coupled to the voltage output (26) and configured to change the APT voltage (V_{CC}) from a present voltage level ($V_{CC(N-1)}$) in a present time interval (S_{N-1}) among the plurality of time intervals to a future voltage level ($V_{CC(N)}$) in an upcoming time interval (S_N) among the plurality of time intervals during a transition interval (TP) that falls within one of the present time interval (S_{N-1}) and the upcoming time interval (S_N); and

a voltage amplifier (32) coupled to an input (36) of the offset circuit (34), the voltage amplifier (32) is activated at a start of the transition interval (TP) and deactivated at an end of the transition interval (TP) to generate a modulated voltage (V_{AMP}) at the input (36) of the offset circuit (34) based on an amplifier target voltage ($V_{TGT-AMP}$) determined to cause the modulated voltage (V_{AMP}) to be higher than or equal to a headroom voltage (V_{HEAD}) at the end of the transition interval (TP).

2. The PMIC of claim 1, further comprising a control circuit configured to:

determine the start and the end of the transition interval based on the present voltage level and the future voltage level of the APT voltage;

determine the amplifier target voltage to be equal to a sum of the future voltage level and a markup voltage;

activate the voltage amplifier at the start of the transition interval; and

deactivate the voltage amplifier at the end of the transition interval.

3. The PMIC of claim 2, wherein the control circuit is further configured to:
determine that the future voltage level of the APT voltage is higher than the present voltage level of the APT voltage;
determine the start of the transition interval to be at a boundary between the present time interval and the upcoming time interval;
determine the end of the transition interval to be later than the boundary between the present time interval and the upcoming time interval;
determine the markup voltage to be equal to the headroom voltage; and
cause the offset circuit to increase the APT voltage from the present voltage level to the future voltage level by the end of the transition interval.

4. The PMIC of claim 2, wherein the control circuit is further configured to:
determine that the future voltage level of the APT voltage is lower than the present voltage level of the APT voltage and the headroom voltage is lower than a differential between the present voltage level and the future voltage level;
determine the start of the transition interval to be earlier than a boundary between the present time interval and the upcoming time interval;
determine the end of the transition interval to be at the boundary between the present time interval and the upcoming time interval;
determine the markup voltage to be equal to zero; and
cause the offset circuit to decrease the APT voltage from the present voltage level to the future voltage level by the end of the transition interval.

5. The PMIC of claim 2, wherein the control circuit is further configured to:
determine that the future voltage level of the APT voltage is lower than the present voltage level of the APT voltage and the headroom voltage

is higher than or equal to a differential between the present voltage level and the future voltage level;

determine the start of the transition interval to be earlier than a boundary between the present time interval and the upcoming time interval;

determine the end of the transition interval to be at the boundary between the present time interval and the upcoming time interval;

determine the markup voltage to be equal to the headroom voltage subtracted by the differential between the present voltage level and the future voltage level; and

cause the offset circuit to decrease the APT voltage from the present voltage level to the future voltage level by the end of the transition interval.

6. The PMIC of claim 2, wherein the control circuit is further configured to receive, during the present time interval, an indication that indicates the future voltage level of the APT voltage in the upcoming time interval.

7. The PMIC of claim 2, wherein the control circuit is further configured to receive, during a present one of the plurality of modulation units, a profile indication that indicates a selected power profile for an upcoming one of the plurality of modulation units, the selected power profile comprises a plurality of future voltage levels each corresponding to a respective one of the plurality of time intervals in the upcoming one of the plurality of modulation units.

8. The PMIC of claim 7, further comprising a memory circuit configured to store a profile lookup table, LUT, (48) comprising a plurality of predetermined power profiles (46(1)-46(N)), wherein the control circuit is further configured to retrieve the selected power profile from the profile LUT based on the received indication.

9. The PMIC of claim 1, wherein:

the plurality of modulation units each corresponds to a time division duplex, TDD, time slot; and

the plurality of time intervals in each of the plurality of modulation units corresponds to an orthogonal frequency division multiplexing, OFDM, symbol.

10. A wireless communication circuit (25) comprising a power management integrated circuit, PMIC, (24) comprising:

a voltage output (26) that outputs an average power tracking, APT, voltage (V_{CC}) for amplifying a radio frequency, RF, signal (30) modulated in a plurality of modulation units each comprising a plurality of time intervals (S_{N-1}, S_N);

an offset circuit (34) coupled to the voltage output (26) and configured to change the APT voltage (V_{CC}) from a present voltage level ($V_{CC(N-1)}$) in a present time interval (S_{N-1}) among the plurality of time intervals to a future voltage level ($V_{CC(N)}$) in an upcoming time interval (S_N) among the plurality of time intervals during a transition interval (TP) that falls within one of the present time interval (S_{N-1}) and the upcoming time interval (S_N); and

a voltage amplifier (32) coupled to an input (36) of the offset circuit (34), the voltage amplifier (32) is activated at a start of the transition interval (TP) and deactivated at an end of the transition interval (TP) to generate a modulated voltage (V_{AMP}) at the input (36) of the offset circuit (34) based on an amplifier target voltage ($V_{TGT-AMP}$) determined to cause the modulated voltage (V_{AMP}) to be higher than or equal to a headroom voltage (V_{HEAD}) at the end of the transition interval (TP).

11. The wireless communication circuit of claim 10, wherein the PMIC further comprises a control circuit configured to:

determine the start and the end of the transition interval based on the present voltage level and the future voltage level of the APT voltage;

determine the amplifier target voltage to be equal to a sum of the future voltage level and a markup voltage;

activate the voltage amplifier at the start of the transition interval; and

deactivate the voltage amplifier at the end of the transition interval.

12. The wireless communication circuit of claim 11, wherein the control circuit is further configured to:

determine that the future voltage level of the APT voltage is higher than the present voltage level of the APT voltage;

determine the start of the transition interval to be at a boundary between the present time interval and the upcoming time interval;

determine the end of the transition interval to be later than the boundary between the present time interval and the upcoming time interval;

determine the markup voltage to be equal to the headroom voltage; and

cause the offset circuit to increase the APT voltage from the present voltage level to the future voltage level by the end of the transition interval.

13. The wireless communication circuit of claim 11, wherein the control circuit is further configured to:

determine that the future voltage level of the APT voltage is lower than the present voltage level of the APT voltage and the headroom voltage is lower than a differential between the present voltage level and the future voltage level;

determine the start of the transition interval to be earlier than a boundary between the present time interval and the upcoming time interval;

determine the end of the transition interval to be at the boundary between the present time interval and the upcoming time interval;

determine the markup voltage to be equal to zero; and

cause the offset circuit to decrease the APT voltage from the present voltage level to the future voltage level by the end of the transition interval.

14. The wireless communication circuit of claim 11, wherein the control circuit is further configured to:

determine that the future voltage level of the APT voltage is lower than the present voltage level of the APT voltage and the headroom voltage is higher than or equal to a differential between the present voltage level and the future voltage level;

determine the start of the transition interval to be earlier than a boundary between the present time interval and the upcoming time interval;

determine the end of the transition interval to be at the boundary between the present time interval and the upcoming time interval;

determine the markup voltage to be equal to the headroom voltage subtracted by the differential between the present voltage level and the future voltage level; and

cause the offset circuit to decrease the APT voltage from the present voltage level to the future voltage level by the end of the transition interval.

15. The wireless communication circuit of claim 11, wherein the control circuit is further configured to receive, during the present time interval, an indication that indicates the future voltage level of the APT voltage in the upcoming time interval.

16. The wireless communication circuit of claim 11, wherein the control circuit is further configured to receive, during a present one of the plurality of modulation units, a profile indication that indicates a selected power profile for an upcoming one of the plurality of modulation units, the selected power profile comprises a

plurality of future voltage levels each corresponding to a respective one of the plurality of time intervals in the upcoming one of the plurality of modulation units.

17. The wireless communication circuit of claim 16, wherein the PMIC further comprises a memory circuit configured to store a profile lookup table, LUT, (48) comprising a plurality of predetermined power profiles (46(1)-46(N)), wherein the control circuit is further configured to retrieve the selected power profile from the profile LUT based on the received indication.

18. The wireless communication circuit of claim 10, wherein:

the plurality of modulation units each corresponds to a time division duplex, TDD, time slot; and

the plurality of time intervals in each of the plurality of modulation units corresponds to an orthogonal frequency division multiplexing, OFDM, symbol.

19. The wireless communication circuit of claim 10, further comprising a transceiver circuit (31) configured to:

generate the RF signal and modulate the RF signal in the plurality of modulation units each comprising the plurality of time intervals; and

provide a modulated target voltage to the PMIC to indicate the future voltage level in the upcoming time interval among the plurality of time intervals.

20. The wireless communication circuit of claim 10, further comprising a power amplifier circuit (28) configured to amplify the RF signal in each of the plurality of time intervals based on the APT voltage.

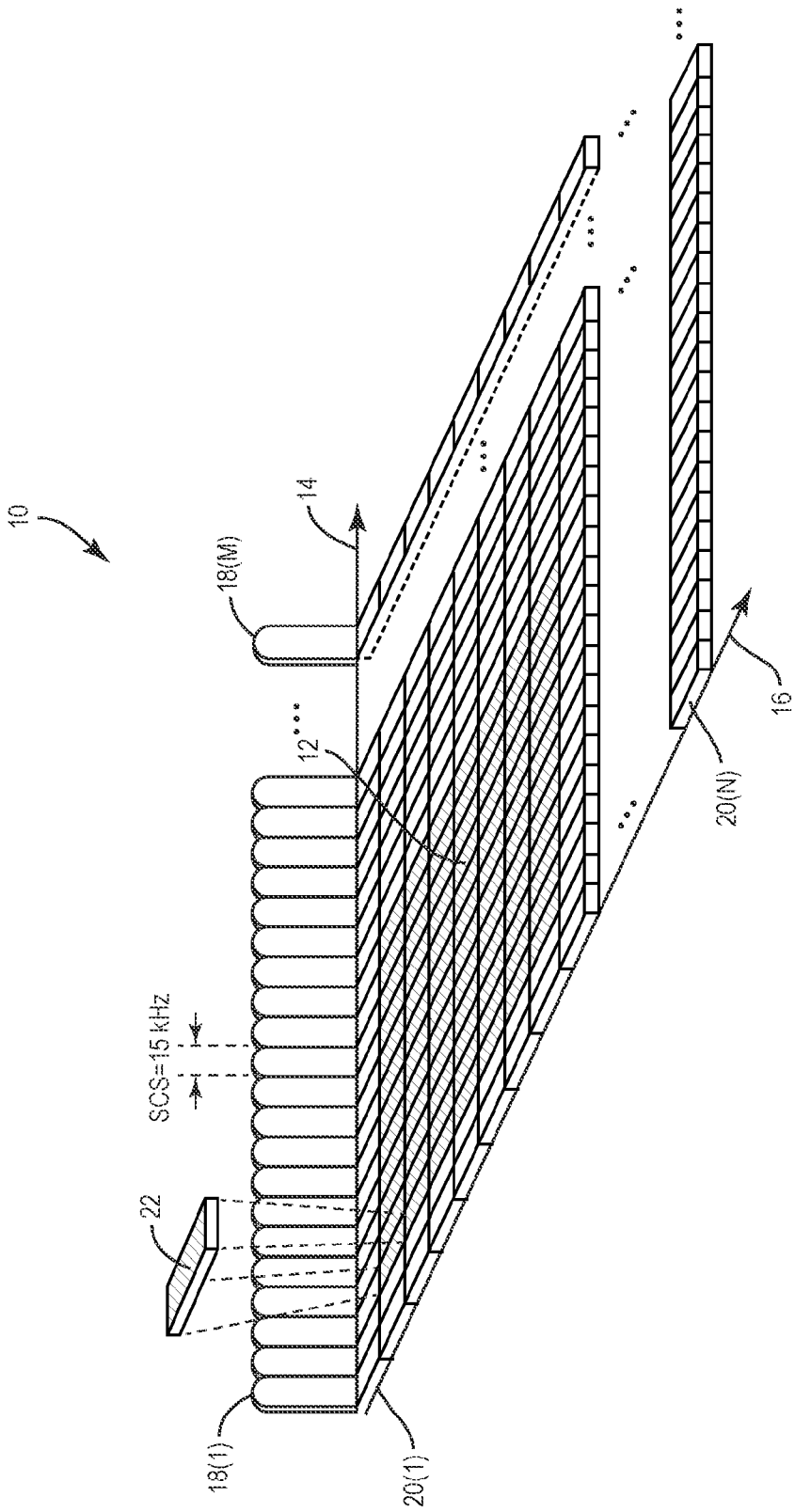

FIG. 1
(PRIOR ART)

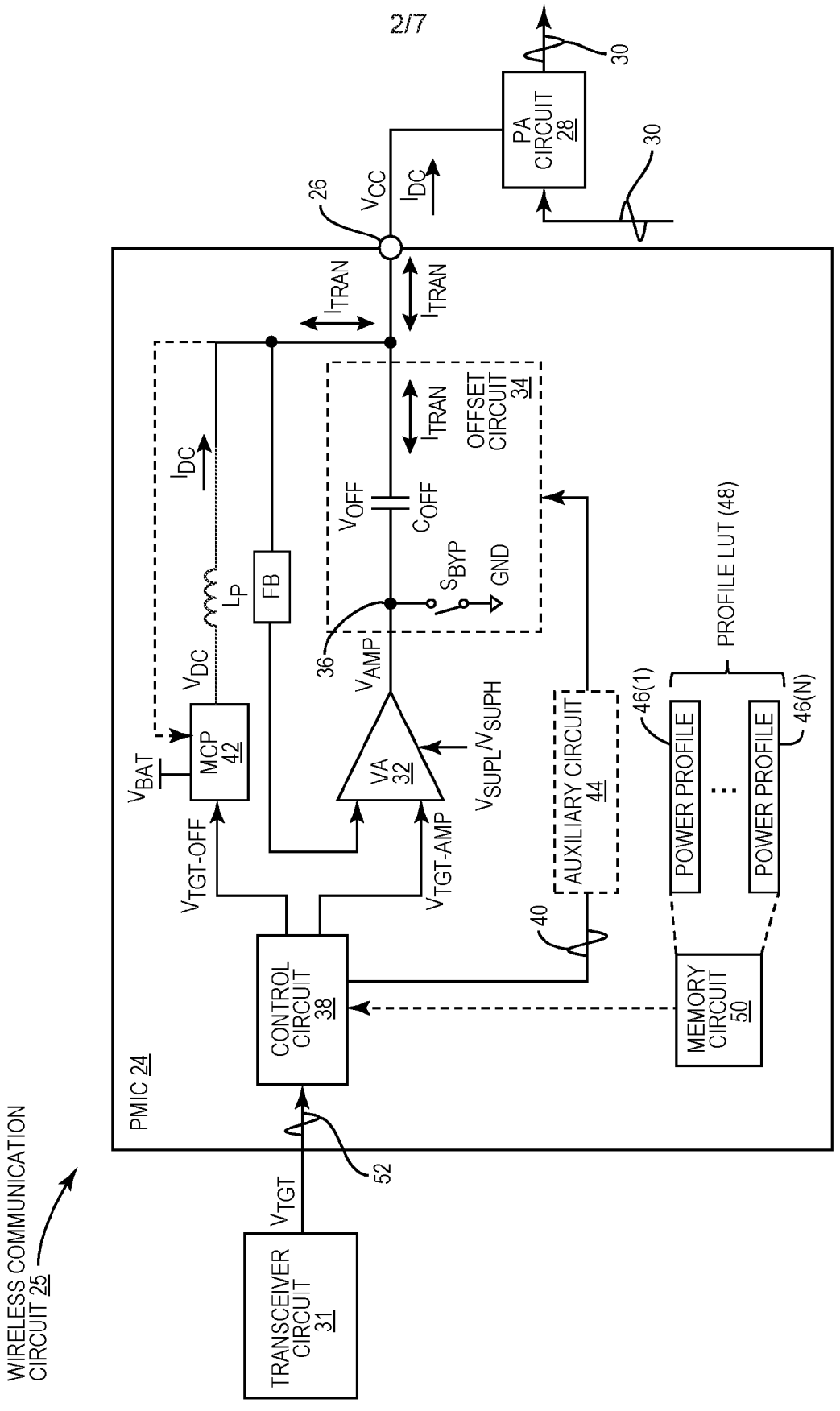
WIRELESS COMMUNICATION CIRCUIT 25
TRANSCEIVER CIRCUIT 31
V_{TGT}
52
PMIC 24
CONTROL CIRCUIT 38
$V_{TGT-OFF}$
$V_{TGT-AMP}$
MCP 42
V_{BAT}
V_{DC}
I_P
FB
I_{DC}
VA 32
V_{SUPL}/V_{SUPH}
36
V_{AMP}
OFFSET CIRCUIT 34
V_{OFF}
C_{OFF}
S_{BYP}
GND
I_{TRAN}
AUXILIARY CIRCUIT 44
40
MEMORY CIRCUIT 50
PROFILE LUT (48)
46(1)
46(N)
POWER PROFILE
POWER PROFILE
26
V_{CC}
I_{DC}
PA CIRCUIT 28
30
30

FIG. 2

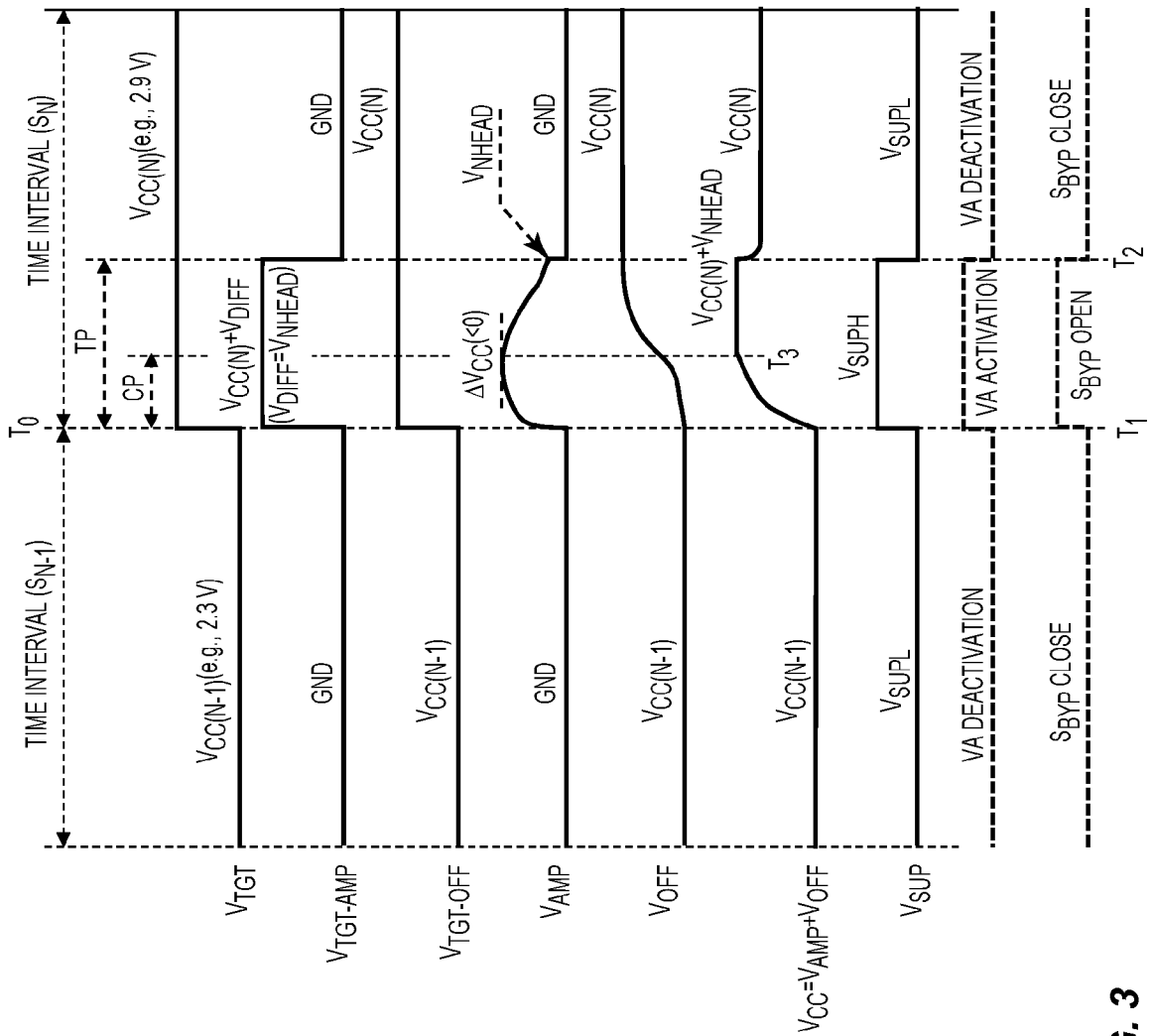
TIME INTERVAL (S_N)
TIME INTERVAL (S_{N-1})
TP
CP
T_0
T_1
T_2
T_3
$V_{CC(N)}$(e.g., 2.9 V)
$V_{CC(N-1)}$(e.g., 2.3 V)
$V_{CC(N)}$+V_{DIFF}
(V_{DIFF}=V_{NHEAD})
V_{NHEAD}
ΔV_{CC}(<0)
$V_{CC(N)}$+V_{NHEAD}
V_{SUPH}
V_{SUPL}
GND
$V_{CC(N)}$
$V_{CC(N-1)}$
VA DEACTIVATION
VA ACTIVATION
S_{BYP} CLOSE
S_{BYP} OPEN
V_{TGT}
$V_{TGT-AMP}$
$V_{TGT-OFF}$
V_{AMP}
V_{OFF}
V_{CC}=V_{AMP}+V_{OFF}
V_{SUP}

FIG. 3

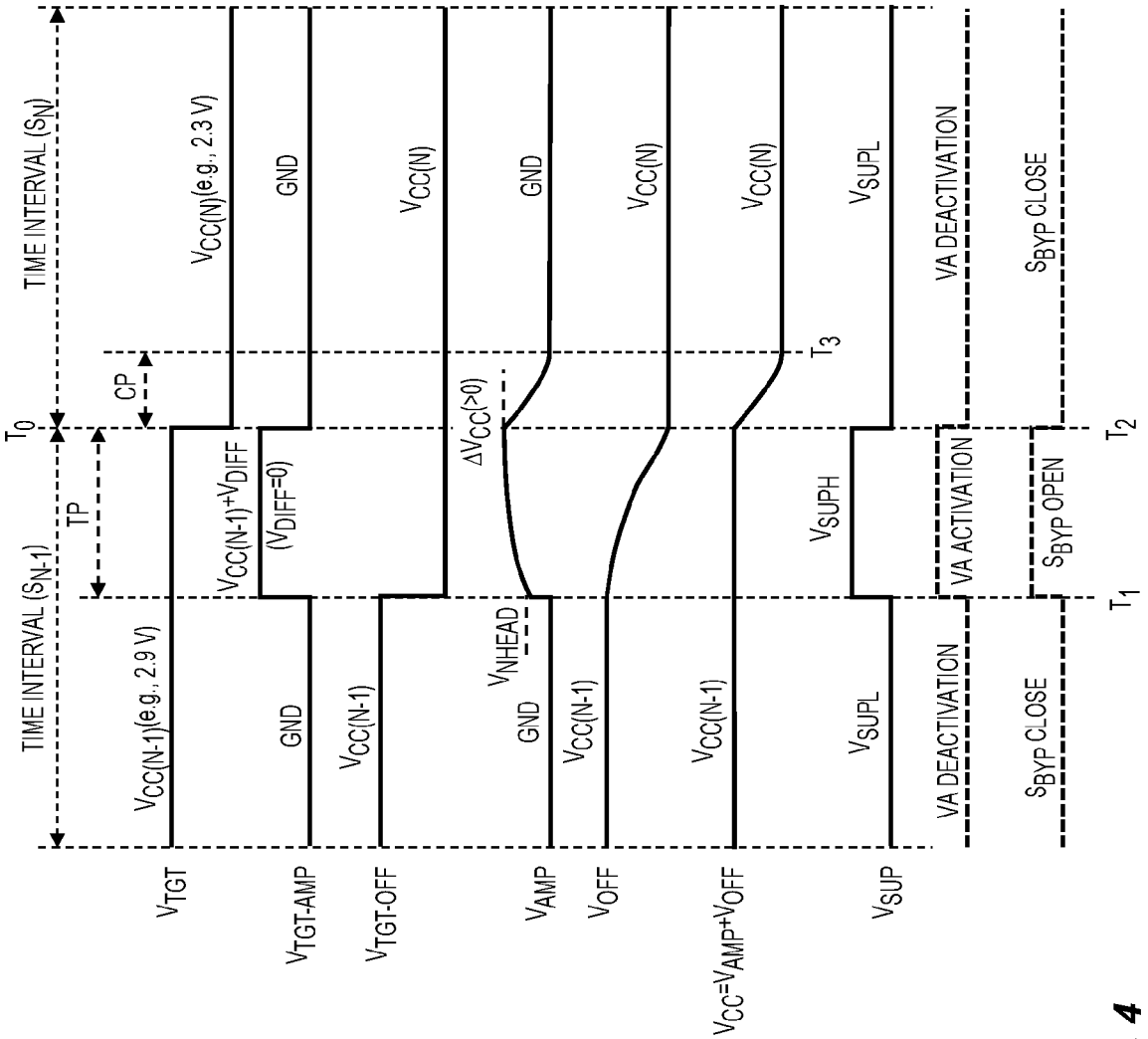
TIME INTERVAL (S_N)
TIME INTERVAL (S_{N-1})
CP
TP
T_0
T_1
T_2
T_3
$V_{CC(N)}$(e.g., 2.3 V)
$V_{CC(N-1)}$(e.g., 2.9 V)
$V_{CC(N-1)}+V_{DIFF}$
(V_{DIFF}=0)
GND
$V_{CC(N)}$
$V_{CC(N-1)}$
ΔV_{CC}(>0)
V_{NHEAD}
V_{SUPH}
V_{SUPL}
VA DEACTIVATION
VA ACTIVATION
S_{BYP} CLOSE
S_{BYP} OPEN
V_{TGT}
$V_{TGT-AMP}$
$V_{TGT-OFF}$
V_{AMP}
V_{OFF}
$V_{CC}=V_{AMP}+V_{OFF}$
V_{SUP}

FIG. 4

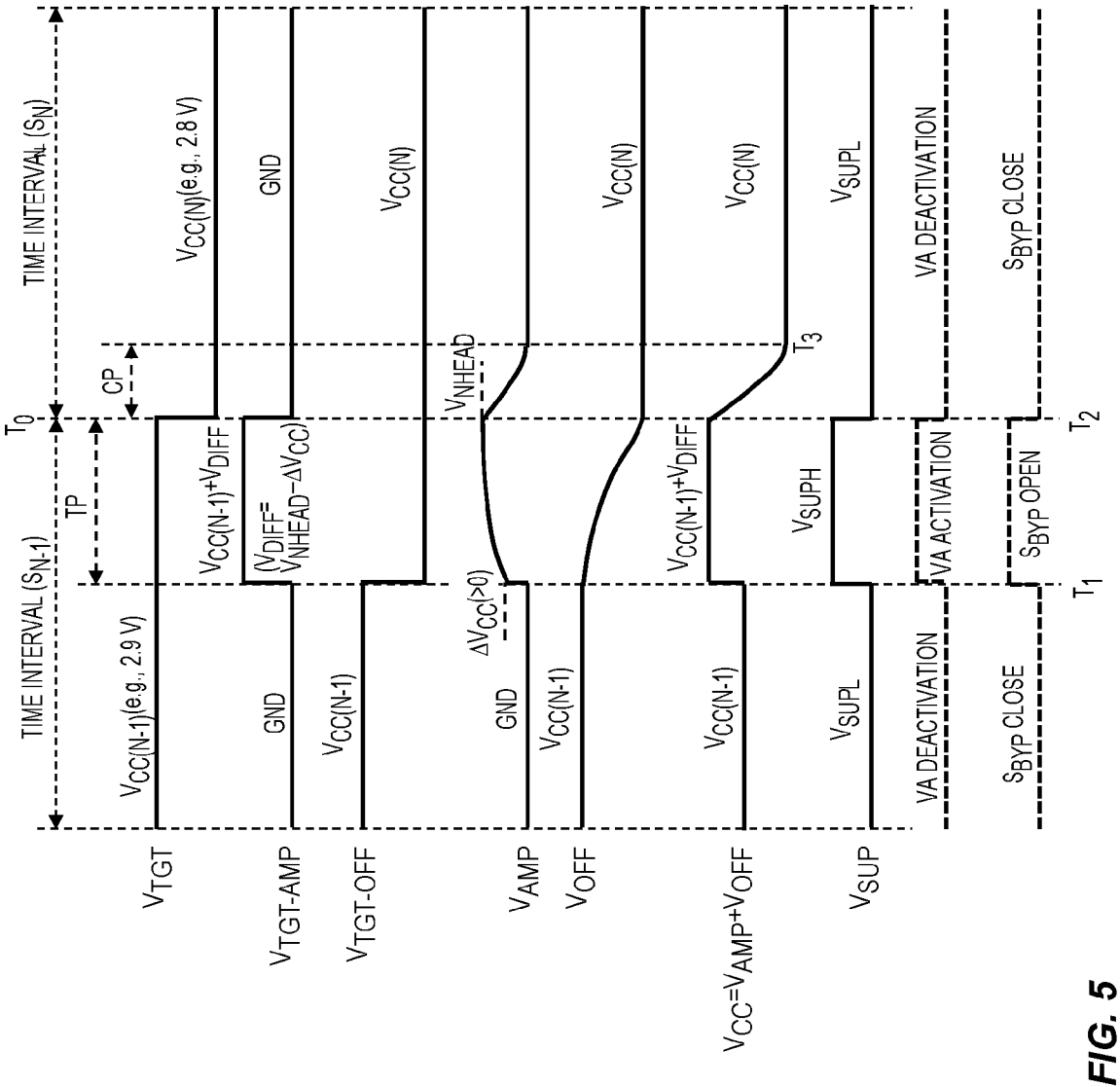
TIME INTERVAL (S_{N-1})
TIME INTERVAL (S_N)
TP
CP
T_0
T_1
T_2
T_3
$V_{CC(N-1)}$(e.g., 2.9 V)
$V_{CC(N)}$(e.g., 2.8 V)
GND
$V_{CC(N-1)}$
$V_{CC(N)}$
$V_{CC(N-1)}+V_{DIFF}$
(V_{DIFF}= $V_{NHEAD}-\Delta V_{CC}$)
V_{NHEAD}
ΔV_{CC}(>0)
V_{SUPH}
V_{SUPL}
VA DEACTIVATION
VA ACTIVATION
S_{BYP} CLOSE
S_{BYP} OPEN
V_{TGT}
$V_{TGT-AMP}$
$V_{TGT-OFF}$
V_{AMP}
V_{OFF}
$V_{CC}=V_{AMP}+V_{OFF}$
V_{SUP}

FIG. 5

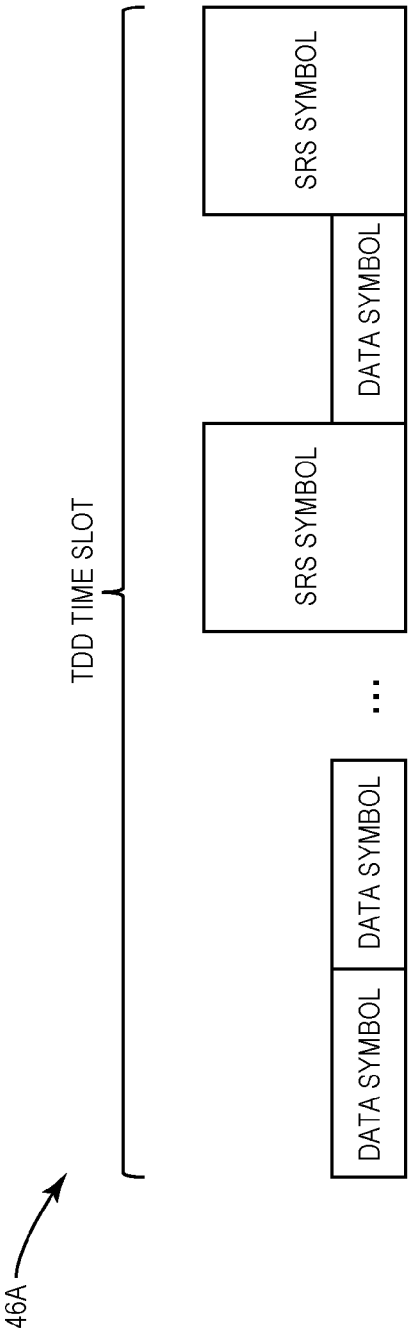
46A
TDD TIME SLOT
DATA SYMBOL
DATA SYMBOL
...
SRS SYMBOL
SRS SYMBOL
DATA SYMBOL

FIG. 6A

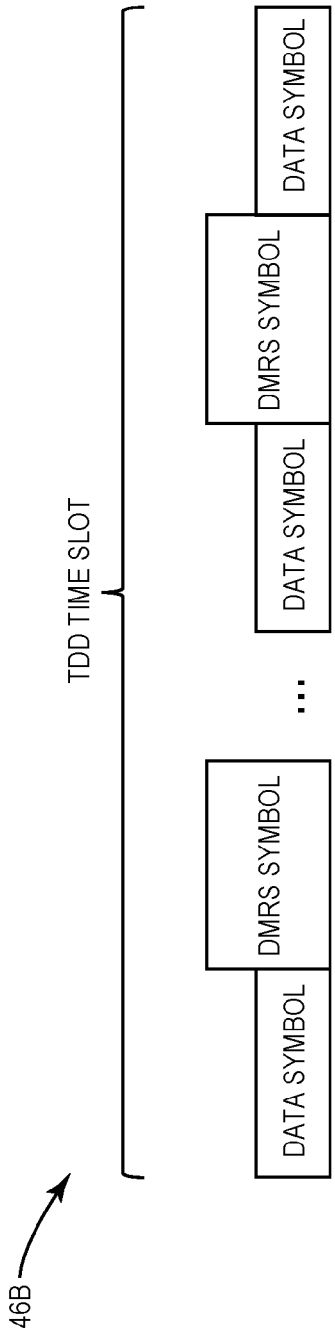
46B
TDD TIME SLOT
DATA SYMBOL
DMRS SYMBOL
...
DATA SYMBOL
DMRS SYMBOL
DATA SYMBOL

FIG. 6B

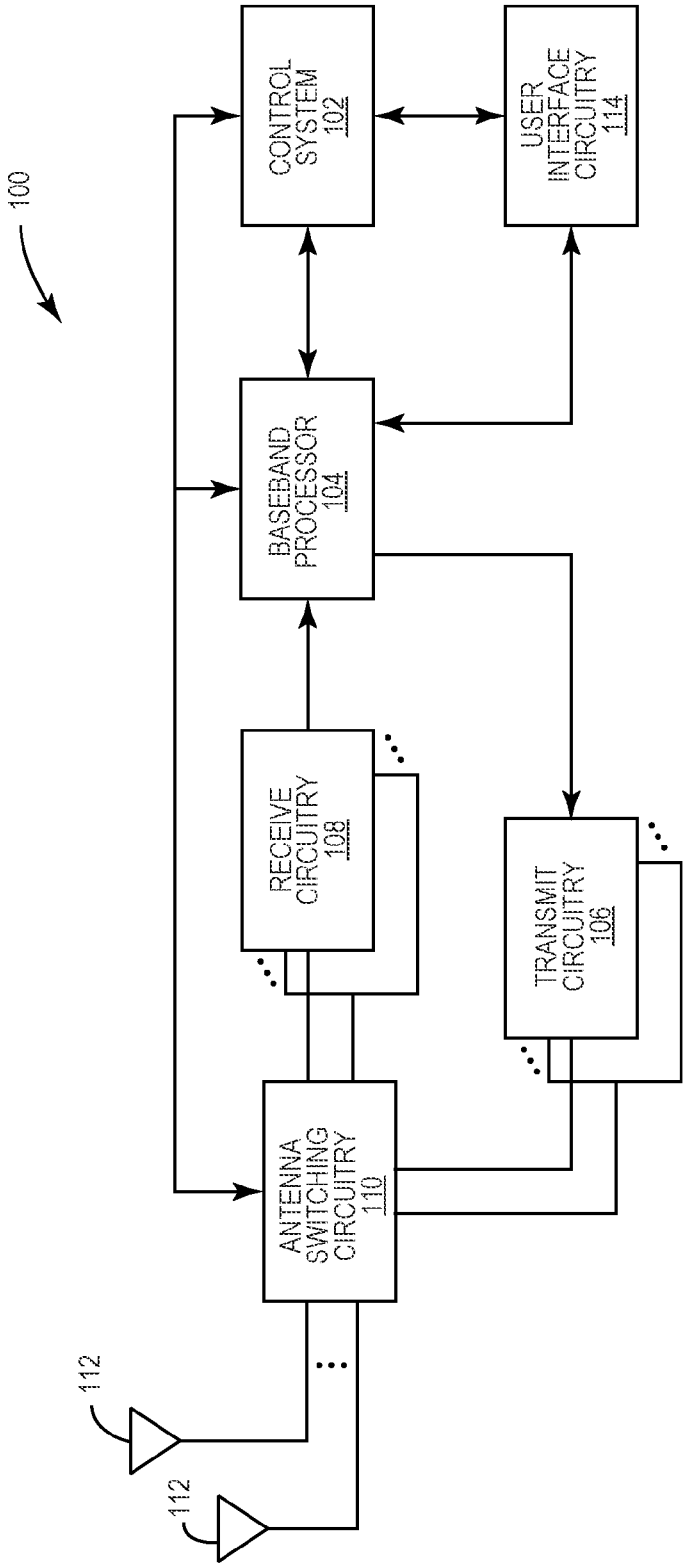
100
CONTROL SYSTEM 102
USER INTERFACE CIRCUITRY 114
BASEBAND PROCESSOR 104
RECEIVE CIRCUITRY 108
TRANSMIT CIRCUITRY 106
ANTENNA SWITCHING CIRCUITRY 110
112
112

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2023/022317

A. CLASSIFICATION OF SUBJECT MATTER

INV. H03F1/02 H03F3/195 H03F3/213 H03F3/24 H03F3/72
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2020/336111 A1 (KHLAT NADIM [FR]) 22 October 2020 (2020-10-22) the whole document -----	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 August 2023	08/09/2023

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Jespers, Michaël

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2023/022317

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2020336111 A1	22-10-2020	NONE	

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专利代理师 刘倜
(51)Int.Cl.
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H03F 3/213(2006.01)
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H03F 3/72(2006.01)

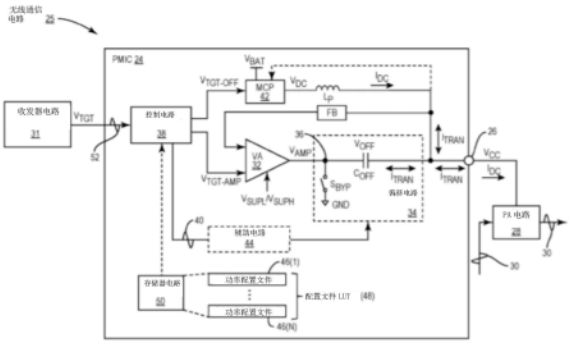
权利要求书4页 说明书10页 附图8页

(54)发明名称

快速切换电源管理集成电路

(57)摘要

提供了一种快速切换电源管理集成电路(PMIC)。PMIC被配置成向功率放大器电路提供平均功率跟踪(APT)电压,以用于放大在多个时间间隔中调制的射频(RF)信号。在本文中,PMIC被配置成以非常短的切换间隔(例如,<20纳秒)将APT电压从时间间隔中的当前一个时间间隔中的当前电压电平增大或减小到时间间隔中的即将到来的一个时间间隔中的将来电压电平。当APT电压从当前电压电平转变到将来电压电平时,PMIC适时地激活电压放大器以帮助确保功率放大器电路的正常运行(例如,将APT电压维持在当前电平并减少APT电压中的波动)。因此,PMIC可以随着涌入电流的减小而频繁且快速地切换APT电压。



CN 119054197 A

1.一种电源管理集成电路PMIC(24),包括:

电压输出(26),所述电压输出将平均功率跟踪APT电压(V_{CC})输出到功率放大器电路(28)以用于放大在多个调制单元中调制的射频RF信号(30),所述多个调制单元各自包括多个时间间隔(S_{N-1},S_N);

偏移电路(34),所述偏移电路耦接到所述电压输出(26),并且被配置成在过渡间隔(TP)期间将所述APT电压(V_{CC})从所述多个时间间隔中的当前时间间隔(S_{N-1})中的当前电压电平($V_{CC(N-1)}$)改变为所述多个时间间隔中的即将到来的时间间隔(S_N)中的将来电压电平($V_{CC(N)}$),所述过渡间隔落在所述当前时间间隔(S_{N-1})和所述即将到来的时间间隔(S_N)中的一者内;以及

耦接到所述偏移电路(34)的输入(36)的电压放大器(32),所述电压放大器(32)在所述过渡间隔(TP)开始时被激活,并且在所述过渡间隔(TP)结束时被去活,以基于确定为使所述调制电压(V_{AMP})在所述过渡间隔(TP)结束时高于或等于净空电压(V_{HEAD})的放大器目标电压($V_{TGT-AMP}$)在所述偏移电路(34)的所述输入(36)处生成调制电压(V_{AMP})。

2.根据权利要求1所述的PMIC,还包括控制电路,所述控制电路被配置成:

基于所述APT电压的所述当前电压电平和所述将来电压电平来确定所述过渡间隔的所述开始和所述结束;

确定所述放大器目标电压等于所述将来电压电平和标记电压的总和;

在所述过渡间隔开始时激活所述电压放大器;以及

在所述过渡间隔结束时去活所述电压放大器。

3.根据权利要求2所述的PMIC,其中,所述控制电路还被配置成:

确定所述APT电压的所述将来电压电平高于所述APT电压的所述当前电压电平;

确定所述过渡间隔的所述开始在所述当前时间间隔与所述即将到来的时间间隔之间的边界处;

确定所述过渡间隔的所述结束晚于所述当前时间间隔与所述即将到来的时间间隔之间的所述边界;

确定所述标记电压等于所述净空电压;以及

使所述偏移电路在所述过渡间隔结束之前将所述APT电压从所述当前电压电平增大到所述将来电压电平。

4.根据权利要求2所述的PMIC,其中,所述控制电路还被配置成:

确定所述APT电压的所述将来电压电平低于所述APT电压的所述当前电压电平,并且所述净空电压低于所述当前电压电平与所述将来电压电平之间的差分;

确定所述过渡间隔的所述开始早于所述当前时间间隔与所述即将到来的时间间隔之间的边界;

确定所述过渡间隔的所述结束在所述当前时间间隔与所述即将到来的时间间隔之间的所述边界处;

确定所述标记电压等于零;以及

使所述偏移电路在所述过渡间隔结束之前将所述APT电压从所述当前电压电平减小到所述将来电压电平。

5.根据权利要求2所述的PMIC,其中,所述控制电路还被配置成:

确定所述APT电压的所述将来电压电平低于所述APT电压的所述当前电压电平,并且所述净空电压高于或等于所述当前电压电平与所述将来电压电平之间的差分;

确定所述过渡间隔的所述开始早于所述当前时间间隔与所述即将到来的时间间隔之间的边界;

确定所述过渡间隔的所述结束在所述当前时间间隔与所述即将到来的时间间隔之间的所述边界处;

确定所述标记电压等于所述净空电压减去所述当前电压电平与所述将来电压电平之间的所述差分;以及

使所述偏移电路在所述过渡间隔结束之前将所述APT电压从所述当前电压电平减小到所述将来电压电平。

6.根据权利要求2所述的PMIC,其中,所述控制电路还被配置成在所述当前时间间隔期间接收指示所述即将到来的时间间隔中的所述APT电压的所述将来电压电平的指示。

7.根据权利要求2所述的PMIC,其中,所述控制电路还被配置成在所述多个调制单元中的当前一个调制单元期间接收配置文件指示,所述配置文件指示指示所述多个调制单元中的即将到来的一个调制单元的所选功率配置文件,所选功率配置文件包括多个将来电压电平,所述多个将来电压电平各自对应于所述多个调制单元中的即将到来的一个调制单元中的所述多个时间间隔中的相应一个时间间隔。

8.根据权利要求7所述的PMIC,还包括存储器电路,所述存储器电路被配置成存储配置文件查找表LUT(48),所述配置文件查找表包括多个预定功率配置文件(46(1)-46(N)),其中,所述控制电路还被配置成基于所接收的指示从所述配置文件LUT检索所选功率配置文件。

9.根据权利要求1所述的PMIC,其中:

所述多个调制单元各自对应于时分双工TDD时隙;并且

所述多个调制单元中的每一个调制单元中的所述多个时间间隔对应于正交频分复用OFDM符号。

10.一种无线通信电路(25),包括电源管理集成电路PMIC(24),所述电源管理集成电路包括:

电压输出(26),所述电压输出输出平均功率跟踪APT电压(V_{CC})以用于放大在多个调制单元中调制的射频RF信号(30),所述多个调制单元各自包括多个时间间隔(S_{N-1},S_N);

偏移电路(34),所述偏移电路耦接到所述电压输出(26),并且被配置成在过渡间隔(TP)期间将所述APT电压(V_{CC})从所述多个时间间隔中的当前时间间隔(S_{N-1})中的当前电压电平($V_{CC(N-1)}$)改变为所述多个时间间隔中的即将到来的时间间隔(S_N)中的将来电压电平($V_{CC(N)}$),所述过渡间隔落在所述当前时间间隔(S_{N-1})和所述即将到来的时间间隔(S_N)中的一者内;以及

耦接到所述偏移电路(34)的输入(36)的电压放大器(32),所述电压放大器(32)在所述过渡间隔(TP)开始时被激活,并且在所述过渡间隔(TP)结束时被去活,以基于确定为使所述调制电压(V_{AMP})在所述过渡间隔(TP)结束时高于或等于净空电压(V_{HEAD})的放大器目标电压($V_{TGT-AMP}$)在所述偏移电路(34)的所述输入(36)处生成调制电压(V_{AMP})。

11.根据权利要求10所述的无线通信电路,其中,所述PMIC还包括控制电路,所述控制

电路被配置成:

基于所述APT电压的所述当前电压电平和所述将来电压电平来确定所述过渡间隔的所述开始和所述结束;

确定所述放大器目标电压等于所述将来电压电平和标记电压的总和;

在所述过渡间隔开始时激活所述电压放大器;以及

在所述过渡间隔结束时去活所述电压放大器。

12.根据权利要求11所述的无线通信电路,其中,所述控制电路还被配置成:

确定所述APT电压的所述将来电压电平高于所述APT电压的所述当前电压电平;

确定所述过渡间隔的所述开始在所述当前时间间隔与所述即将到来的时间间隔之间的边界处;

确定所述过渡间隔的所述结束晚于所述当前时间间隔与所述即将到来的时间间隔之间的所述边界;

确定所述标记电压等于所述净空电压;以及

使所述偏移电路在所述过渡间隔结束之前将所述APT电压从所述当前电压电平增大到所述将来电压电平。

13.根据权利要求11所述的无线通信电路,其中,所述控制电路还被配置成:

确定所述APT电压的所述将来电压电平低于所述APT电压的所述当前电压电平,并且所述净空电压低于所述当前电压电平与所述将来电压电平之间的差分;

确定所述过渡间隔的所述开始早于所述当前时间间隔与所述即将到来的时间间隔之间的边界;

确定所述过渡间隔的所述结束在所述当前时间间隔与所述即将到来的时间间隔之间的所述边界处;

确定所述标记电压等于零;以及

使所述偏移电路在所述过渡间隔结束之前将所述APT电压从所述当前电压电平减小到所述将来电压电平。

14.根据权利要求11所述的无线通信电路,其中,所述控制电路还被配置成:

确定所述APT电压的所述将来电压电平低于所述APT电压的所述当前电压电平,并且所述净空电压高于或等于所述当前电压电平与所述将来电压电平之间的差分;

确定所述过渡间隔的所述开始早于所述当前时间间隔与所述即将到来的时间间隔之间的边界;

确定所述过渡间隔的所述结束在所述当前时间间隔与所述即将到来的时间间隔之间的所述边界处;

确定所述标记电压等于所述净空电压减去所述当前电压电平与所述将来电压电平之间的所述差分;以及

使所述偏移电路在所述过渡间隔结束之前将所述APT电压从所述当前电压电平减小到所述将来电压电平。

15.根据权利要求11所述的无线通信电路,其中,所述控制电路还被配置成在所述当前时间间隔期间接收指示所述即将到来的时间间隔中的所述APT电压的所述将来电压电平的指示。

16.根据权利要求11所述的无线通信电路,其中,所述控制电路还被配置成在所述多个调制单元中的当前一个调制单元期间接收配置文件指示,所述配置文件指示指示所述多个调制单元中的即将到来的一个调制单元的所选功率配置文件,所选功率配置文件包括多个将来电压电平,所述多个将来电压电平各自对应于所述多个调制单元中的即将到来的一个调制单元中的所述多个时间间隔中的相应一个时间间隔。

17.根据权利要求16所述的无线通信电路,其中,所述PMIC还包括存储器电路,所述存储器电路被配置成存储配置文件查找表LUT(48),所述配置文件查找表包括多个预定功率配置文件(46(1)-46(N)),其中,所述控制电路还被配置成基于所接收的指示从所述配置文件LUT检索所选功率配置文件。

18.根据权利要求10所述的无线通信电路,其中:

所述多个调制单元各自对应于时分双工TDD时隙;并且

所述多个调制单元中的每一个调制单元中的所述多个时间间隔对应于正交频分复用OFDM符号。

19.根据权利要求10所述的无线通信电路,还包括收发器电路(31),所述收发器电路被配置成:

在所述多个调制单元中生成所述RF信号并调制所述RF信号,所述多个调制单元各自包括所述多个时间间隔;以及

向所述PMIC提供调制目标电压以指示所述多个时间间隔中的所述即将到来的时间间隔中的所述将来电压电平。

20.根据权利要求10所述的无线通信电路,还包括功率放大器电路(28),所述功率放大器电路被配置成基于所述APT电压在所述多个时间间隔中的每一个时间间隔中放大所述RF信号。

快速切换电源管理集成电路

[0001] 相关申请

[0002] 本申请要求于2022年6月15日提交的序列号为63/352,301的美国临时专利申请的权益,所述临时专利申请的公开内容以全文引用的方式并入本文中。

技术领域

[0003] 本公开的技术大体上涉及电源管理集成电路(PMIC)。

背景技术

[0004] 第五代(5G)新空口(NR)(5G-NR)被广泛认为是超越当前第三代(3G)和第四代(4G)技术的下一代无线通信技术。在这点上,能够支持5G-NR无线通信技术的无线通信装置预期会实现数据速率更高、覆盖范围改进、信号传递效率增强,以及跨广泛范围的射频(RF)频带的时延减少,所述频带包含低频带(低于1GHz)、中频带(1GHz到6GHz)和高频带(高于24GHz)。

[0005] 5G-NR系统中的下行和上行传输广泛基于正交频分复用(OFDM)。就此而言,图1是示范性OFDM时频网格10的示意图,示出了用于5G-NR系统中的物理资源分配的至少一个资源块(RB)12。OFDM时频网格10包括表示频域的频率轴14和表示时域的时间轴16。沿着频率轴14,存在多个副载波18(1)-18(M)。副载波18(1)-18(M)彼此正交地分开副载波间距(SCS)(例如,15KHz)。沿着时间轴16,存在多个OFDM符号20(1)-20(N)。OFDM符号20(1)-20(N)可以被调制为数据符号以承载数据有效载荷和/或参考符号以承载诸如解调参考信号(DMRS)、探测参考信号(SRS)等的参考信号。OFDM符号20(1)-20(N)中的每一个由循环前缀(CP)(未示出)分开,所述循环前缀被配置成充当防护带以帮助克服OFDM符号20(1)-20(N)之间的符号间干扰(ISI)。在OFDM时频网格10中,副载波18(1)-18M)和OFDM符号20(1)-20(N)的每个交点定义资源元素(RE)22。

[0006] 在5G-NR通信系统中,RF信号可以被调制成频域(沿着频率轴14)中的副载波18(1)-18(N)中的多个副载波和时域(沿着时间轴16)中的OFDM符号20(1)-20(N)中的多个OFDM符号。下表(表1)汇总了由5G-NR通信系统支持的OFDM配置。

[0007] 表1

[0008]

SCS (KHz)	时隙长度 (μs)	每子帧的时隙编号	CP (μs)	OFDM符号持续时间 (μs)	调制带宽 (MHz)
15	1000	1	4.69	71.43	50
30	500	2	2.34	35.71	100
60	250	4	1.17	17.86	200
120	125	8	0.59	8.93	400

[0009] 在5G-NR系统中,RF信号通常以超过200MHz的高调制带宽调制。就此而言,根据表

1,SCS将为120KHz,并且OFDM符号20(1)-20(N)中两个连续OFDM符号之间的过渡稳定时间(例如,PF信号的幅值变化)需要小于或等于0.59μs的CP持续时间。

[0010] 另外,无线通信装置可能还需要支持此类物联网(IoT)应用,例如无钥匙上车、远程车库门打开、非接触式支付、移动登机牌等。毋庸置疑,无线通信装置还必须始终使911/E911服务在紧急情况下可访问。这样一来,无线通信装置在需要时保持可操作是至关重要的。

[0011] 值得注意的是,无线通信装置依赖于电池单元(例如,Li离子电池)为其操作和服务供电。尽管电池技术最近取得了进展,但无线通信装置可能不时地处于低电量状态。就此而言,期望延长电池寿命,同时使得OFDM符号20(1)-20(N)之间能够实现快速电压变化。

发明内容

[0012] 本公开的实施例涉及快速切换电源管理集成电路(PMIC)。PMIC被配置成向功率放大器电路提供平均功率跟踪(APT)电压,以用于放大在多个时间间隔中调制的射频(RF)信号。在本文中,PMIC被配置成以非常短的切换间隔(例如,<20纳秒)将APT电压从时间间隔中的当前一个时间间隔中的当前电压电平增大或减小到时间间隔中的即将到来的一个时间间隔中的将来电压电平。当APT电压从当前电压电平转变到将来电压电平时,PMIC适时地激活电压放大器以帮助确保功率放大器电路的正常运行(例如,将APT电压维持在当前电平并减少APT电压中的波动)。因此,PMIC可以随着涌入电流的减小而频繁且快速地切换APT电压。

[0013] 在一个方面中,提供了一种PMIC。所述PMIC包括电压输出,所述电压输出将APT电压输出到功率放大器电路以用于放大在多个调制单元中调制的RF信号,所述多个调制单元各自包括多个时间间隔。所述PMIC还包括偏移电路。所述偏移电路耦接到所述电压输出,并且被配置成在过渡间隔期间将所述APT电压从所述多个时间间隔中的当前时间间隔中的当前电压电平改变为所述多个时间间隔中的即将到来的时间间隔中的将来电压电平,所述过渡间隔落在所述当前时间间隔和所述即将到来的时间间隔中的一者内。所述PMIC还包括电压放大器。所述电压放大器耦接到偏移电路的输入。所述电压放大器在所述过渡间隔开始时被激活,并且在所述过渡间隔结束时被去活,以基于确定为使所述调制电压在所述过渡间隔结束时高于或等于净空电压的放大器目标电压在所述偏移电路的所述输入处生成调制电压。

[0014] 在另一方面中,提供了一种无线通信电路。所述无线通信电路包括PMIC。所述PMIC包括电压输出,所述电压输出输出APT电压以用于放大在多个调制单元中调制的RF信号,所述多个调制单元各自包括多个时间间隔。所述PMIC还包括偏移电路。所述偏移电路耦接到所述电压输出,并且被配置成在过渡间隔期间将所述APT电压从所述多个时间间隔中的当前时间间隔中的当前电压电平改变为所述多个时间间隔中的即将到来的时间间隔中的将来电压电平,所述过渡间隔落在所述当前时间间隔和所述即将到来的时间间隔中的一者内。所述PMIC还包括电压放大器。所述电压放大器耦接到偏移电路的输入。所述电压放大器在所述过渡间隔开始时被激活,并且在所述过渡间隔结束时被去活,以基于确定为使所述调制电压在所述过渡间隔结束时高于或等于净空电压的放大器目标电压在所述偏移电路的所述输入处生成调制电压。

[0015] 在阅读以下与附图有关的优选实施例的详细说明之后,所属技术领域中具有通常知识者将会了解本公开的范围,并明白其额外的方面。

附图说明

[0016] 并入本说明书中并形成本说明书的一部分的附图说明了本公开的几个方面,并且连同说明书一起用于解释本公开的原理。

[0017] 图1是示出用于物理资源分配的至少一个资源块(RB)的示范性正交频分复用(OFDM)时频网格的示意图;

[0018] 图2是根据本公开的实施例被配置成支持快速平均功率跟踪(APT)电压切换的示范性电源管理集成电路(PMIC)的示意图;

[0019] 图3是提供根据本公开的实施例配置以将APT电压从当前电压电平增加到将来电压电平的图2的PMIC的示范性图示的时序图;

[0020] 图4是提供根据本公开的实施例配置以将APT电压从当前电压电平减小到将来电压电平的图2的PMIC的示范性图示的时序图;

[0021] 图5是提供根据本公开的另一实施例配置以将APT电压从当前电压电平减小到将来电压电平的图2的PMIC的示范性图示的时序图;

[0022] 图6A和6B是提供可以由图2的PMIC用于实现快速APT电压切换的一些功率配置文件的示范性图示的框图;以及

[0023] 图7是其中可以提供图2的PMIC的示范性用户元件的示意图。

具体实施方式

[0024] 下文阐述的实施例表示使本领域技术人员能够实践实施例并且示出实践实施例的最佳模式所必需的信息。在参照附图阅读以下说明之后,所属技术领域中具有通常知识者将了解本公开的概念,并将会明白未在本文中具体阐述的这些概念的应用。应了解,这些概念和应用属于本公开和随附权利要求书的范围之内。

[0025] 将了解,虽然本文中可能使用第一、第二等用语来描述各种元件,但这些元件不应受到这些用语的限制。这些用语仅用于区分不同的元件。例如,在不脱离本公开的范围的情况下,第一元件可以被称为第二元件,并且类似地,第二元件可以被称为第一元件。如本文所用,术语“和/或”包含相关联所列项目中的一个或多个项目的任何和所有组合。

[0026] 应当理解,当例如层、区域或衬底的元件被称为“在另一元件上”或“延伸到”另一元件上时,其可以直接在另一元件上或直接延伸到另一元件上,或者也可以存在中间元件。相反,当元件被称为“直接在另一元件上”或“直接延伸到另一元件上”时,不存在中间元件。同样,应理解,当例如层、区域或衬底的元件被称为“在另一元件上方”或“在另一元件上方延伸”时,其可以直接在另一元件上方或直接在另一元件上方延伸,或者也可以存在中间元件。相反,当元件被称为“直接在另一元件上方”或“直接在另一元件上方”延伸时,不存在中间元件。还将理解,当元件被称为“连接”或“耦合”到另一元件时,其可以直接连接或耦合到另一元件,或者可以存在中间元件。相反,当元件被称为“直接连接”或“直接耦合”到另一元件时,不存在中间元件。

[0027] 例如“以下”或“以上”或“上”或“下”或“水平”或“竖直”的相对术语在本文中可以

用于描述一个元件、层或区域与如图所示的另一元件、层或区域的关系。应理解,这些术语和上面讨论的那些旨在包括除附图中描绘的朝向之外的装置的不同朝向。

[0028] 本文所用的术语仅用于描述特定实施例的目的,并且不旨在限制本公开。如本文所用,除非上下文另外明确指示,否则单数形式“一(a)”、“一(an)”和“所述”也旨在包含复数形式。还应理解,当在本文中使用时,术语“包括(comprises)”、“包括(comprising)”、“包含(includes)”和/或“包含(including)”指定存在所述特征、整数、步骤、操作、元件和/或部件,但不排除存在或添加一个或多个其它特征、整数、步骤、操作、元件、部件和/或它们的群组。

[0029] 除非另外定义,否则本文使用的所有术语(包含技术和科学术语)具有与本公开所属领域的普通技术人员通常理解的相同含义。更将了解,本文中所使用的用语应解译为具有与本说明书的背景和相关前案中的意义一致的意义,且除非在本文中明确定义,否则不应以理想化或过度正式的含义来阐释。

[0030] 本公开的实施例涉及快速切换电源管理集成电路(PMIC)。PMIC被配置成向功率放大器电路提供平均功率跟踪(APT)电压,以用于放大在多个时间间隔中调制的射频(RF)信号。在本文中,PMIC被配置成以非常短的切换间隔(例如,<20纳秒)将APT电压从时间间隔中的当前一个时间间隔中的当前电压电平增大或减小到时间间隔中的即将到来的一个时间间隔中的将来电压电平。当APT电压从当前电压电平转变到将来电压电平时,PMIC适时地激活电压放大器以帮助确保功率放大器电路的正常运行(例如,将APT电压维持在当前电平并减少APT电压中的波动)。因此,PMIC可以随着涌入电流的减小而频繁且快速地切换APT电压。

[0031] 就此而言,图2是示范性PMIC 24的示意图,该PMIC设置在无线通信电路25中并且根据本公开的实施例被配置成支持快速APT电压切换。PMIC 24包括电压输出26,其将APT电压V_{CC}输出到无线通信电路25中的功率放大器电路28。功率放大器电路28被配置成基于APT电压V_{CC}放大RF信号30。可以由无线通信电路25中的收发器电路31生成的RF信号30分多个调制单元被调制,每个调制单元被进一步划分成多个时间间隔。在本公开的上下文中,调制单元等价于时分双工(TDD)时隙或微时隙,并且调制单元中的每一个内部的时间间隔等价于正交频分复用(OFDM)符号,例如图1中的OFDM符号20(1)-20(N)。就此而言,可以调制时间间隔中的每一个以承载数据有效载荷(在本文中称为“数据符号”)和参考信号(在本文中称为“参考符号”),例如解调参考信号(DMRS)、探测参考信号(SRS)等。

[0032] 鉴于功率放大器电路28需要将数据符号和参考符号放大到不同的功率电平,PMIC 24可能需要基于每符号调适(增大或减小)APT电压V_{CC}。此外,如图1中先前所述,PMIC 24必须在OFDM符号20(1)-20(N)中的每一个中的相应循环前缀(CP)内完成APT电压V_{CC}。

[0033] PMIC 24包括电压放大器32(表示为“VA”)和偏移电路34。电压放大器32耦接到偏移电路34的输入36,并且偏移电路34耦接到电压输出26。在本公开的上下文中,假设功率放大器电路28具有比偏移电路34的带宽高得多的带宽。如下文详细所述,偏移电路34被配置成在一对相邻时间间隔(在图3到5中表示为“S_{N-1}”和“S_N”)之间将APT电压V_{CC}从当前电压电平(在图3到5中表示为“$V_{CC(N-1)}$”)改变(增大或减小)到将来电压电平(在图3到5中表示为“$V_{CC(N)}$”)。为了区分,时间间隔S_{N-1}和S_N分别也称为“当前时间间隔”和“即将到来的时间间隔”。

[0034] 更具体地,偏移电路34将使APT电压V_{CC}在过渡间隔(在图3到5中表示为"TP")期间从当前时间间隔S_{N-1}中的当前电压电平$VCC_{(N-1)}$改变到即将到来的时间间隔S_N中的将来电压电平$V_{CC(N)}$。取决于APT电压V_{CC}从当前时间间隔S_{N-1}到即将到来的时间间隔$S_{N是}$增加还是减小,过渡间隔TP可以位于当前时间间隔S_{N-1}中还是位于即将到来的时间间隔S_N中,以确保APT电压V_{CC}可以通过即将到来的时间间隔S_N的CP达到将来电压电平$V_{CC(N)}$。

[0035] 如图3到5中进一步所示,虽然APT电压V_{CC}在过渡间隔TP期间从当前电压电平$V_{CC(N-1)}$转变到将来电压电平$V_{CC(N)}$,但电压放大器32在过渡间隔TP开始时(表示为"T_1")激活且在过渡间隔TP结束时(表示为"T_2")去活以确保功率放大器电路28的正确操作。根据本公开的实施例,电压放大器32将在偏移电路34的输入36处提供调制电压V_{AMP}。在非限制性示例中,电压放大器32被配置成基于放大器目标电压$V_{TGT-AMP}$以及较低电源电压V_{SUPL}和较高电源电压V_{SUPH}($V_{SUPH}>V_{SUPL}$)中的一个生成调制电压V_{AMP}。

[0036] 如图3到5中的详细示例中所论述的,如此确定放大器目标电压$V_{TGT-AMP}$以确保电压放大器32可在过渡间隔TP的末端T_2处将调制电压V_{AMP}维持在净空电压(在图3到5中表示为"V_{NHEAD}")或高于净空电压,所述净空电压大于0V。因此,电压放大器32可以将APT电压V_{CC}维持在当前电压电平$V_{CC(N-1)}$,并且在过渡间隔TP期间抑制APT电压V_{CC}中的波动,从而确保在过渡间隔TP期间功率放大器电路28的正确操作。

[0037] 根据本公开的实施例,PMIC 24可以包括控制电路38,例如,所述控制电路可以是现场可编程门阵列(FPGA)或专用集成电路(ASIC)。在一个方面中,控制电路38可以被配置成基于当前电压电平$V_{CC(N-1)}$与将来电压电平$V_{CC(N)}$之间的差分ΔV_{CC}($\Delta V_{CC}=V_{CC(N-1)}-V_{CC(N)}$)来确定过渡间隔TP应在当前时间间隔$S_{N-1}$还是在即将到来的时间间隔$S_N$内。可以理解的是,当当前电压电平$V_{CC(N-1)}$高于将来电压电平$V_{CC(N)}$时,差分$\Delta V_{CC}$将为正,或者当当前电压电平$V_{CC(N-1)}$低于将来电压电平$V_{CC(N)}$时,差分$\Delta V_{CC}$将为负。在非限制性示例中,控制电路38可以从收发器电路31接收指示即将到来的时间间隔S_N中的将来电压电平$V_{CC(N)}$的调制目标电压V_{TGT}。因此,控制电路38可以(例如,经由控制信号40)控制偏移电路34以在过渡间隔TP期间从当前电压电平$V_{CC(N-1)}$转变到将来电压电平$V_{CC(N)}$。

[0038] 在另一方面中,控制电路38还可以被配置成基于所确定的差分ΔV_{CC}来确定放大器目标电压$V_{TGT-AMP}$。在非限制性示例中,当将来电压电平$V_{CC(N)}$高于当前电压电平$V_{CC(N-1)}$时,如图3中所示,放大器目标电压$V_{TGT-AMP}$等于将来电压电平$V_{CC(N)}$和标记电压(表示为"V_{DIFF}")之和,如下文方程(方程1)中所示。在另一非限制性示例中,当将来电压电平$V_{CC(N)}$低于当前电压电平$V_{CC(N-1)}$时,如图4和5中所示,放大器目标电压$V_{TGT-AMP}$等于当前电压电平$V_{CC(N-1)}$和标记电压V_{DIFF}之和,如下文方程(方程2)中所示。

[0039] $V_{TGT-AMP}=V_{CC(N)}+V_{DIFF}$ (方程1)

[0040] $V_{TGT-AMP}=V_{CC(N-1)}+V_{DIFF}$ (方程2)

[0041] 在方程(方程1和方程2)中,取决于APT电压V_{CC}从当前时间间隔S_{N-1}到即将到来的时间间隔S_N将如何变化,标记电压V_{DIFF}可以具有不同的值。就此而言,通过改变放大器目标电压$V_{TGT-AMP}$,并且更具体地改变标记电压V_{DIFF},控制电路38可以使电压放大器32在过渡间隔TP期间在适当电平下生成调制电压V_{AMP},以维持功率放大器电路28的正常运行。

[0042] 在又一方面中,控制电路38可进一步被配置成在过渡间隔TP的开始T_1处激活电压放大器32,并且在过渡间隔TP的结束T_2处去活电压放大器32。在非限制性示例中,控制电路

38可以响应于接收到较低电源电压V_{SUPL}而使电压放大器32被去活或响应于接收到较高电源电压V_{SUPH}而被激活。通过控制偏移电路34以改变APT电压V_{CC}并且适时地激活/去活电压放大器32以确保功率放大器电路28在过渡间隔TP期间正常运行,PMIC 24可以在越来越严格的切换时间要求(例如,<20ns)下有效地切换APT电压V_{CC}。

[0043] PMIC 24还包括多级电荷泵(MCP)42。MCP 42可以是直流(DC)到DC降压-升压转换器,其被配置成基于电池电压V_{BAT}生成低频电压V_{DC}(例如,DC电压)。具体地,MCP 42可以在降压模式下操作以生成处于$0\times V_{BAT}$或$1\times V_{BAT}$的低频电压V_{DC},或者在升压模式下操作以生成处于$2\times V_{BAT}$的低频电压V_{DC}。MCP 42可以被配置成基于特定占空比(例如,20%@$0\times V_{BAT}$、30%@$1\times V_{BAT}$和50%@$2\times V_{BAT}$)在降压模式与升压模式之间切换。这样一来,MCP 42可以被控制以在期望电平下生成低频电压V_{DC}。

[0044] 在实施例中,控制电路38可进一步被配置成基于调制目标电压V_{TGT}生成偏移目标电压$V_{TGT-OFF}$。偏移目标电压$V_{TGT-OFF}$可以指示APT电压V_{CC}的将来电压电平$V_{CC(N)}$。因此,MCP 42可以基于对应的占空比来确定并操作以在如由偏移目标电压$V_{TGT-OFF}$指示的期望电平下生成低频电压V_{DC}。

[0045] PMIC 24还包括功率电感器L_P。功率电感器L_P耦接于MCP 42和电压输出26之间并被配置成基于低频电压V_{DC}而感生低频电流I_{DC}(例如,DC电流)。可以理解的是,可以感生的低频电流I_{CD}是低频电压V_{DC}和功率电感器L_P的电感的函数。因此,控制电路38可进一步基于偏移目标电压$V_{TGT-OFF}$改变低频电流I_{DC}。在实施例中,MCP 42可以从APT电压V_{CC}接收反馈。

[0046] 在本文中,偏移电路34包括偏移电容器C_{OFF}和旁路开关S_{BYP}。偏移电容器C_{OFF}耦接于输入36与电压输出26之间,并且旁路开关S_{BYP}耦接于输入36与地(GND)之间。

[0047] 在一种操作情境下,将APT电压V_{CC}设置为从当前时间间隔S_{N-1}中的当前电压电平$V_{CC(N-1)}$增大到即将到来的时间间隔S_N中的将来电压电平$V_{CC(N)}$($V_{CC(N-1)}<V_{CC(N)}$)。就此而言,控制电路38将偏移目标电压$V_{TGT-OFF}$设置为APT电压V_{CC}的将来电压电平$V_{CC(N)}$,以使得以期望量生成低频电流I_{CD},从而将偏移电容器C_{OFF}充电到将来电压电平$V_{CC(N)}$。

[0048] 控制电路38将断开旁路开关S_{BYP}并在过渡间隔TP开始时激活电压放大器32,以在高于将来电压电平$V_{CC(N)}$的电平下生成放大器目标电压$V_{TGT-AMP}$,使得电流I_{TRAN}可以从MCP 42流动通过偏移电容器C_{OFF}并在电压放大器32中汇集。在非限制性示例中,PMIC 24可以包括辅助电路44,所述辅助电路可以提供额外电流以帮助在存在电流I_{TRAN}的情况下维持调制电压V_{AMP}。结果,电流I_{TRAN}将在过渡间隔TP期间将偏移电容器C_{OFF}逐渐充电到将来电压电平$V_{CC(N)}$。当偏移电容器C_{OFF}在过渡间隔TP结束时充电到将来电压电平$V_{CC(N)}$时,控制电路38去活电压放大器32并闭合旁路开关S_{BYP}。此后,偏移电容器C_{OFF}和MCP 42将在即将到来的时间间隔S_N的剩余时间内将APT电压V_{CC}维持在将来电压电平$V_{CC(N)}$。

[0049] 上述操作情境可以在图3中以图形方式示出。图3是提供关于图2的PMIC 24在上述操作情境下如何操作以增大APT电压V_{CC}的示范性图示的时序图。图2中的元件在图3中被提及,且在本文中将不再描述。

[0050] 如图所示,过渡间隔TP完全落在即将到来的时间间隔S_N内,其中过渡间隔TP的开始T_1与当前时间间隔S_{N-1}与即将到来的时间间隔S_N之间的边界T_0(也称为即将到来的时间间隔S_N中的CP的开始时间)对准,并且过渡间隔TP的结束T_2在时间T_3(也称为即将到来的时间间隔S_N中的CP的结束时间)之后。可以理解的是,CP通常比过渡间隔TP短得多。在本文中,调

制目标电压V_{TGT}指示APT电压V_{CC}将从当前时间间隔S_{N-1}中的当前电压电平$V_{CC(N-1)}$(例如,2.3V)增大到即将到来的时间间隔S_N中的将来电压电平$V_{CC(N)}$(例如,2.9V)。因此,控制电路38确定偏移目标电压$V_{TGT-OFF}$等于将来电压电平$V_{CC(N)}$。

[0051] 关于放大器目标电压$V_{TGT-AMP}$,控制电路38被配置成将方程(方程1)中的标记电压V_{DIFF}设置为等于净空电压V_{NHEAD}($V_{TGT-AMP}=V_{CC(N)}+V_{NHEAD}$)。在时间$T_1$处,控制电路38断开旁路开关$S_{BYP}$并激活电压放大器32(例如,通过将较高电源电压$V_{SUPH}$耦接到电压放大器32)。因此,电压放大器32将根据放大器目标电压$V_{TGT-AMP}$在输入36处生成调制电压V_{AMP}。在非限制性示例中,电压放大器32在辅助电路44的辅助下可以在时间T_3处将调制电压V_{AMP}从GND电平快速驱动到差分ΔV_{CC}($\Delta V_{CC}<0$),以帮助在过渡间隔TP期间稳定APT电压V_{CC}。此后,电压放大器32在时间T_2将调制电压V_{AMP}逐渐减小到净空电压V_{NHEAD}。

[0052] 从时间T_1开始,偏移电容器C_{OFF}逐渐充电以在时间T_2达到将来电压电平$V_{CC(N)}$。因此,在时间T_2处,控制电路38闭合旁路开关S_{BYP}并去活电压放大器32以使调制电压V_{AMP}返回到GND电平。等于调制电压V_{AMP}和偏移电压V_{OFF}的总和的APT电压V_{CC}将在时间T_3处稳定于将来电压电平$V_{CC(N)}$。值得注意的是,由于电压放大器32在旁路开关S_{BYP}被切换时将调制电压V_{AMP}维持在净空电压V_{NHEAD}处或高于该净空电压,因此APT电压V_{CC}不会下降到净空电压V_{NHEAD}以下,从而确保功率放大器电路28的正常运行。

[0053] 返回图2,在另一种操作情境下,将APT电压V_{CC}设置为从当前时间间隔S_{N-1}中的当前电压电平$V_{CC(N-1)}$减小到即将到来的时间间隔S_N中的将来电压电平$V_{CC(N)}$($V_{CC(N-1)}>V_{CC(N)}$)。就此而言,控制电路38将偏移目标电压$V_{TGT-OFF}$设置为APT电压V_{CC}的将来电压电平$V_{CC(N)}$,以使得以期望量生成低频电流I_{CD},从而使得偏移电容器C_{OFF}被放电到将来电压电平$V_{CC(N)}$。

[0054] 控制电路38将断开旁路开关S_{BYP}并在过渡间隔TP开始时激活电压放大器32,以在当前电压电平$V_{CC(N-1)}$下生成放大器目标电压$V_{TGT-AMP}$,使得电流I_{TRAN}可以从电压放大器32流动通过偏移电容器C_{OFF}并返回到MCP 42和/或功率放大器电路28。在非限制性示例中,辅助电路44可以提供额外电流以帮助在存在电流I_{TRAN}的情况下维持调制电压V_{AMP}。结果,偏移电容器C_{OFF}将在过渡间隔TP期间逐渐被放电到将来电压电平$V_{CC(N)}$。当偏移电容器C_{OFF}在过渡间隔TP结束时放电到将来电压电平$V_{CC(N)}$时,控制电路38去活电压放大器32并闭合旁路开关S_{BYP}。此后,偏移电容器C_{OFF}和MCP 42将在即将到来的时间间隔S_N的剩余时间内将APT电压V_{CC}维持在将来电压电平$V_{CC(N)}$。

[0055] 上述操作情境可以在图4和图5中以图形方式示出。图4是提供关于图2的PMIC 24在上述操作情境的一种可能性下如何操作以减小APT电压V_{CC}的示范性图示的时序图。更具体地,图4示出了净空电压V_{NHEAD}(例如,0.4V)低于当前电压电平$V_{CC(N-1)}$与将来电压电平$V_{CC(N)}$之间的差分ΔV_{CC}(例如,0.6V)($V_{NHEAD}<\Delta V_{CC}$)的情况。图2中的元件在图4中被提及,且在本文中将不再描述。

[0056] 如图所示,过渡间隔TP完全落在当前时间间隔S_{N-1}内,其中过渡间隔TP的开始T_1开始于当前时间间隔S_{N-1}与即将到来的时间间隔S_N之间的边界T_0之前,并且过渡间隔TP的结束T_2与边界T_0(也称为即将到来的时间间隔S_N中的CP的开始时间)对准。可以理解的是,CP通常比过渡间隔TP短得多。在本文中,调制目标电压V_{TGT}指示APT电压V_{CC}将从当前时间间隔S_{N-1}中的当前电压电平$V_{CC(N-1)}$(例如,2.9V)减小到即将到来的时间间隔S_N中的将来电压电平$V_{CC(N)}$(例如,2.3V)。因此,控制电路38确定偏移目标电压$V_{TGT-OFF}$等于将来电压电平$V_{CC(N)}$。

[0057] 关于放大器目标电压$V_{TGT-AMP}$,控制电路38被配置成将方程(方程2)中的标记电压V_{DIFF}设置为0V($V_{TGT-AMP}=V_{CC(N-1)}+0$)。在时间$T_1$处,控制电路38断开旁路开关$S_{BYP}$并激活电压放大器32(例如,通过将较高电源电压$V_{SUPH}$耦接到电压放大器32)。因此,电压放大器32将根据放大器目标电压$V_{TGT-AMP}$在输入36处生成调制电压V_{AMP}。在非限制性示例中,电压放大器32在辅助电路44的辅助下可以在时间T_1处即刻将调制电压V_{AMP}从GND电平驱动到净空电压V_{NHEAD}。此后,电压放大器32将继续在时间T_2将调制电压V_{AMP}驱动到电压差分ΔV_{CC}。

[0058] 从时间T_1开始,偏移电容器C_{OFF}逐渐放电以在时间T_2达到将来电压电平$V_{CC(N)}$。因此,在时间T_2处,控制电路38闭合旁路开关S_{BYP}并去活电压放大器32以使调制电压V_{AMP}在时间T_3返回到GND电平。等于调制电压V_{AMP}和偏移电压V_{OFF}的总和的APT电压V_{CC}将在时间T_3处稳定于将来电压电平$V_{CC(N)}$。值得注意的是,由于电压放大器32在旁路开关S_{BYP}被切换时将调制电压V_{AMP}维持在净空电压V_{NHEAD}处或高于该净空电压,因此APT电压V_{CC}不会下降到净空电压V_{NHEAD}以下,从而确保功率放大器电路28的正常运行。

[0059] 图5是提供关于图2的PMIC 24在上述操作情境的另一种可能性下如何操作以减小APT电压V_{CC}的示范性图示的时序图。更具体地,图5示出了净空电压V_{NHEAD}(例如,0.4V)高于或等于当前电压电平$V_{CC(N-1)}$与将来电压电平$V_{CC(N)}$之间的差分ΔV_{CC}(例如,0.1V)($V_{NHEAD}\geq\Delta V_{CC}$)的情况。图2中的元件在图5中被提及,且在本文中将不再描述。

[0060] 如图所示,过渡间隔TP完全落在当前时间间隔S_{N-1}内,其中过渡间隔TP的开始T_1开始于当前时间间隔S_{N-1}与即将到来的时间间隔S_N之间的边界T_0之前,并且过渡间隔TP的结束T_2与边界T_0(也称为即将到来的时间间隔S_N中的CP的开始时间)对准。可以理解的是,CP通常比过渡间隔TP短得多。在本文中,调制目标电压V_{TGT}指示APT电压V_{CC}将从当前时间间隔S_{N-1}中的当前电压电平$V_{CC(N-1)}$(例如,2.9V)减小到即将到来的时间间隔S_N中的将来电压电平$V_{CC(N)}$(例如,2.8V)。因此,控制电路38确定偏移目标电压$V_{TGT-OFF}$等于将来电压电平$V_{CC(N)}$。

[0061] 关于放大器目标电压$V_{TGT-AMP}$,控制电路38被配置成将方程(方程2)中的标记电压V_{DIFF}设置为等于净空电压V_{NHEAD}减去当前电压电平$V_{CC(N-1)}$与将来电压电平$V_{CC(N)}$之间的差分ΔV_{CC}($V_{TGT-AMP}=V_{CC(N-1)}+V_{NHEAD}-\Delta V_{CC}$)。在时间$T_1$处,控制电路38断开旁路开关$S_{BYP}$并激活电压放大器32(例如,通过将较高电源电压$V_{SUPH}$耦接到电压放大器32)。因此,电压放大器32将根据放大器目标电压$V_{TGT-AMP}$在输入36处生成调制电压V_{AMP}。在非限制性示例中,电压放大器32在辅助电路44的辅助下可以在时间T_1处即刻将调制电压V_{AMP}从GND电平驱动到差分ΔV_{CC}。此后,电压放大器32将继续在时间T_2将调制电压V_{AMP}驱动到净空电压V_{NHEAD}。

[0062] 从时间T_1开始,偏移电容器C_{OFF}逐渐放电以在时间T_2达到将来电压电平$V_{CC(N)}$。因此,在时间T_2处,控制电路38闭合旁路开关S_{BYP}并去活电压放大器32以使调制电压V_{AMP}在时间T_3返回到GND电平。等于调制电压V_{AMP}和偏移电压V_{OFF}的总和的APT电压V_{CC}将在时间T_3处稳定于将来电压电平$V_{CC(N)}$。值得注意的是,由于电压放大器32在旁路开关S_{BYP}被切换时将调制电压V_{AMP}维持在净空电压V_{NHEAD}处或高于该净空电压,因此APT电压V_{CC}不会下降到净空电压V_{NHEAD}以下,从而确保功率放大器电路28的正常运行。

[0063] 返回参考图2,在上文描述的示例中,控制电路38被配置成在每个时间间隔(即,每个OFDM符号)接收调制目标电压V_{TGT}。换句话说,收发器电路31必须在当前时间间隔S_{N-1}期间或甚至之前在即将到来的时间间隔S_N中传送将来电压电平$V_{CC(N)}$。如图1中先前所述,在时分双工(TDD)系统中,多个时间间隔(又名OFDM符号)可以包括在调制单元(又名TDD时隙或迷

你时隙)中。这样一来,控制电路38可以在每个调制单元(又名TDD时隙或迷你时隙)接收调制目标电压V_{TGT}。

[0064] 就此而言,PMIC 24可以被预配置为包括多个功率配置文件46(1)-46(N)。在非限制性示例中,功率配置文件46(1)-46(N)可以被组织成配置文件查找表(LUT)48并存储在存储器电路50中。功率配置文件46(1)-46(N)可以由收发器电路31经由例如RF前端(RFFE)接口(未示出)存储在存储器电路50中。

[0065] 图6A和6B是提供功率配置文件46(1)-46(N)的示范性图示的框图,所述功率配置文件可以由图2的PMIC 24用于实现APT电压V_{CC}的快速切换。在本文中,功率配置文件46(1)-46(N)中的每一个对应于TDD时隙。

[0066] 图6A示出了功率配置文件46(1)-46(N)中的示范性功率配置文件46A。如图所示,可以确定功率配置文件46A以指示一个或多个数据符号和一个或多个SRS符号的将来电压电平。

[0067] 图6B示出了功率配置文件46(1)-46(N)中的示范性功率配置文件46B。如图所示,可以确定功率配置文件46B以指示一个或多个数据符号和一个或多个DMRS符号的将来电压电平。

[0068] 返回参考图2,在实施例中,收发器电路31可以传送配置文件指示52以指示在当前调制单元(例如,TDD时隙)期间或之前要用于即将到来的调制单元(例如,TDD时隙)的功率配置文件46(1)-46(N)中的选定功率配置文件。因此,控制电路38可以基于接收到的配置文件指示52从配置文件LUT 48检索选定的功率配置文件。

[0069] 图2的PMIC 24可以设于用户元件中以实现快速电压切换。图7是其中可以提供图2的PMIC的示范性用户元件100的示意图。

[0070] 本文中,用户元件100可以是任何类型的用户元件,例如移动终端、智能手表、平板计算机、计算机、导航装置、接入点和类似的支持无线通信的无线通信装置,例如蜂窝、无线局域网(WLAN)、蓝牙和近场通信。用户元件100通常将包含控制系统102、基带处理器104、发送电路系统106、接收电路系统108、天线开关电路系统110、多个天线112和用户接口电路系统114。在非限制性示例中,举例来说,控制系统102可以是现场可编程门阵列(FPGA)。在这点上,控制系统102可至少包含微处理器、嵌入式存储器电路和通信总线接口。接收电路系统108经由天线112并通过天线开关电路系统110从一个或多个基站接收射频信号。低噪声放大器和滤波器协作以放大和消除来自所接收信号的宽带干扰以进行处理。然后,降频转换和数字化电路(未示出)将滤波后的接收信号降转换为中间或基带频率信号,接着使用模/数转换器(ADC)将所述信号数字化为一个或多个数字流。

[0071] 基带处理器104处理数字化的所接收信号以提取在所接收信号中传送的信息或数据位。这种处理通常包括解调、解码和错误校正操作,这将在下文更详细地论述。基带处理器104通常在一个或多个数字信号处理器(DSP)和专用集成电路(ASIC)中实施。

[0072] 对于发送,基带处理器104从控制系统102接收可表示语音、数据或控制信息的数字化数据,所述基带处理器对所述数字化数据进行编码以用于发送。编码的数据被输出到发送电路系统106,其中数/模转换器(DAC)将数字编码的数据转换成模拟信号,并且调制器将模拟信号调制到处于所要发送频率或多个频率的载波信号上。功率放大器会将调制的载波信号放大到适于发送的电平,并通过天线开关电路系统110将调制的载波信号递送到天

线112。多个天线112和复制的发射电路系统106和接收电路系统108可以提供空间分集。本领域的技术人员将理解调制和处理细节。

[0073] 本领域技术人员将认识到对本公开的优选实施例的改进和修改。所有这种改进和修改都被认为是在本文所公开的概念和下文的权利要求的距离内。

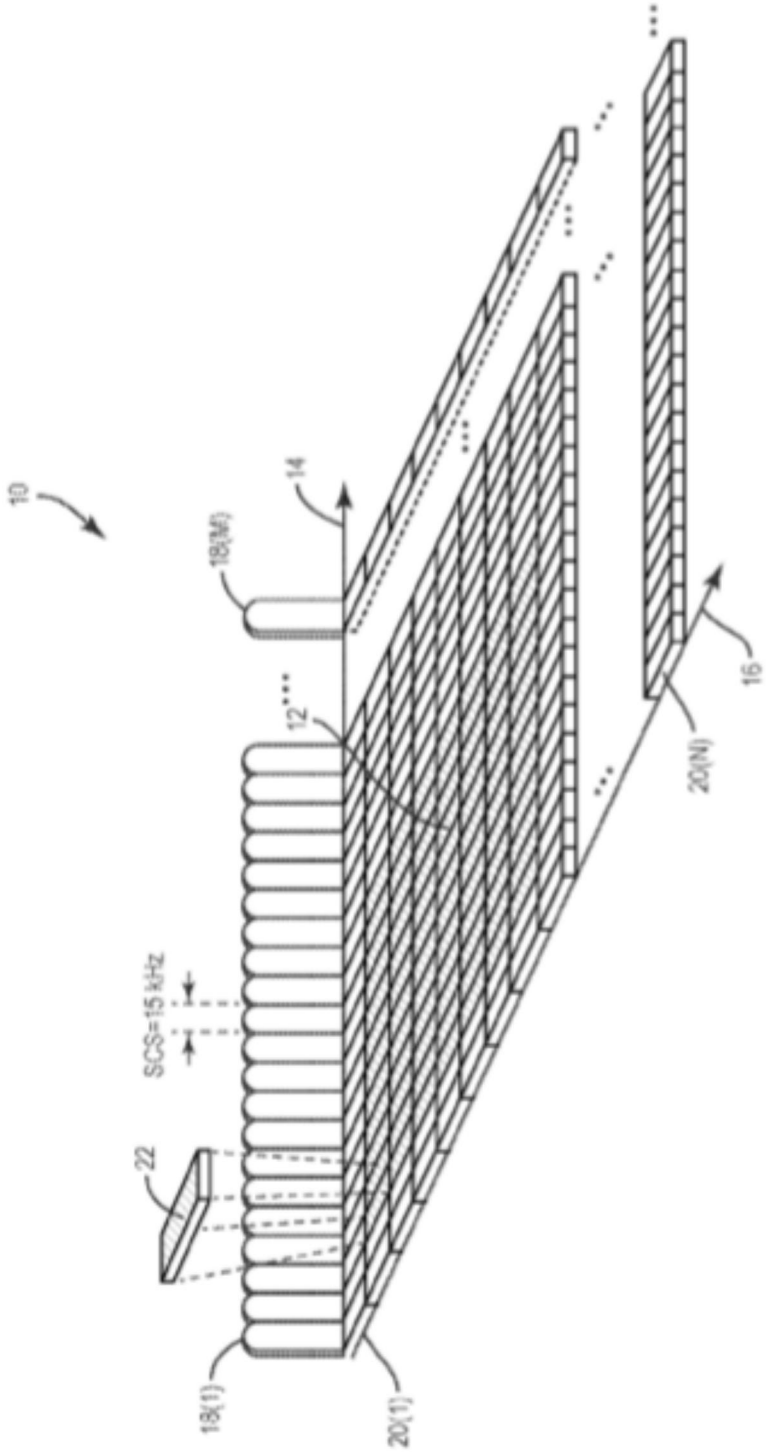


图1(现有技术)

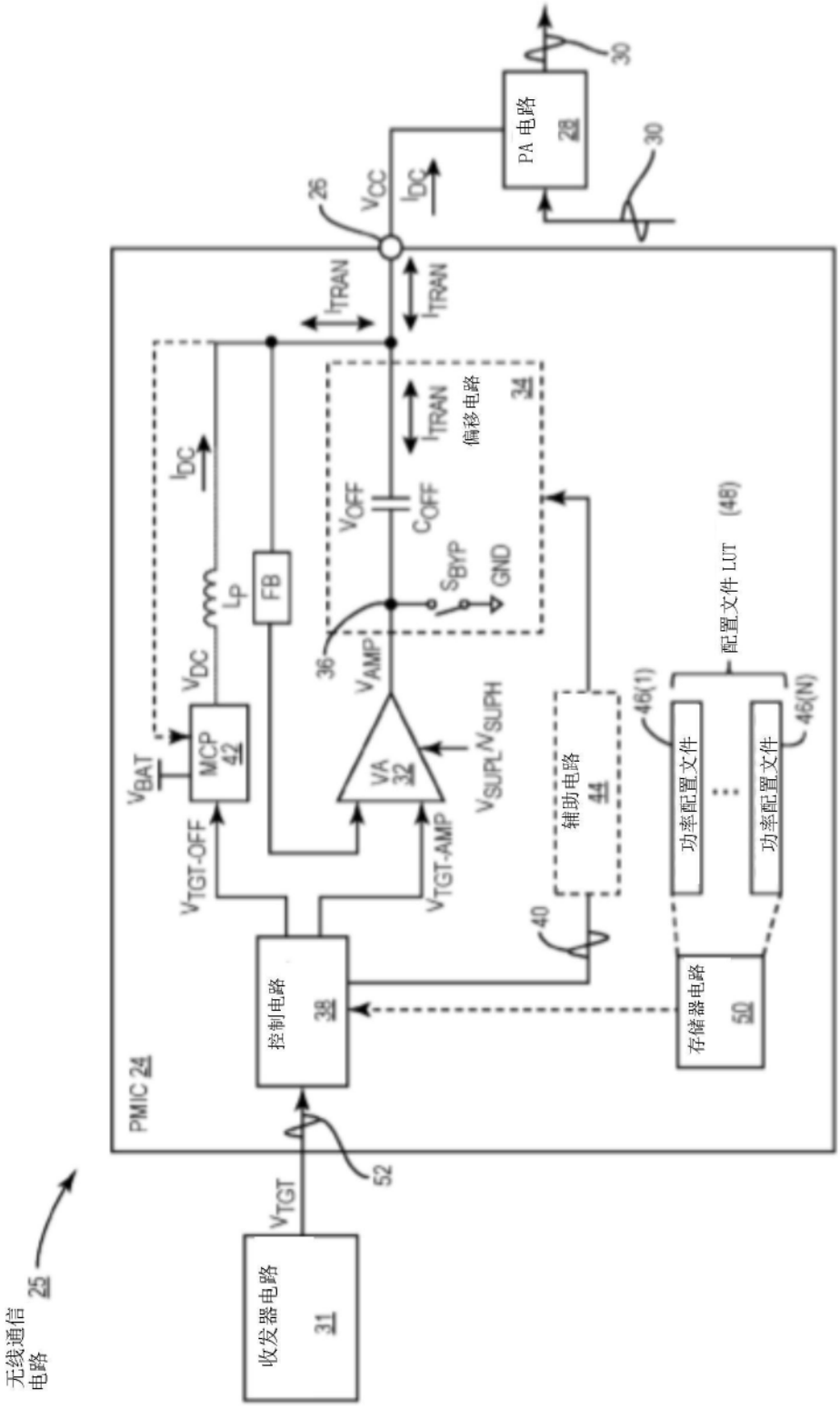

无线通信电路 25
收发器电路 31
V_{TGT}
52
PMIC 24
控制电路 38
40
存储器电路 50
辅助电路 44
46(1)
功率配置文件
功率配置文件
46(N)
配置文件 LUT (46)
$V_{TGT-OFF}$
$V_{TGT-AMP}$
V_{SUPL}/V_{SUPH}
VA 32
V_{AMP}
36
V_{BAT}
MCP 42
V_{DC}
L_P
FB
I_{DC}
V_{OFF}
C_{OFF}
S_{BYP}
GND
偏移电路 34
I_{TRAN}
I_{TRAN}
I_{TRAN}
26
V_{CC}
I_{DC}
PA 电路 28
30
30

图2

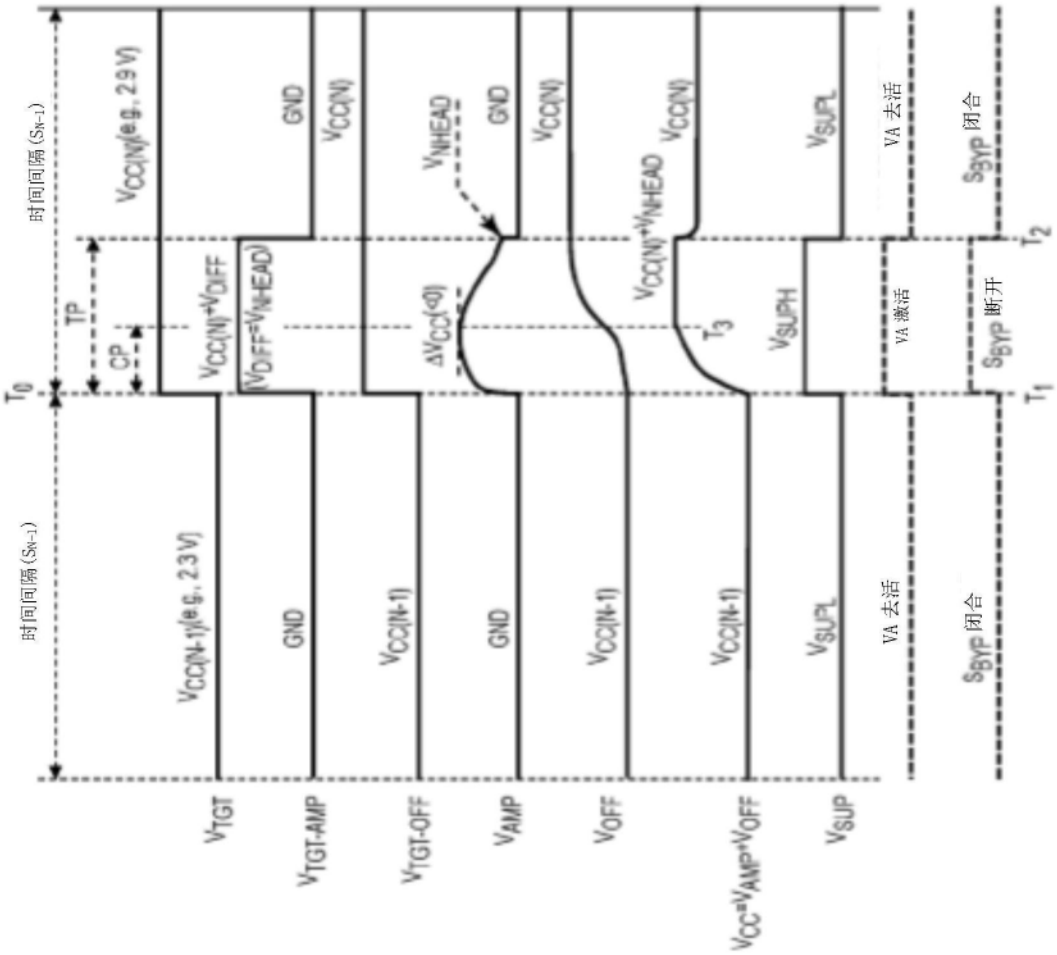

时间间隔(SN-1)
VCC(N)(e.g., 2.9 V)
GND
VCC(N)
VNHEAD
GND
VCC(N)
VCC(N)+VNHEAD
VCC(N)
VSUPL
VA 去活
SBYP 闭合
TP
CP
VCC(N)+VDIFF
|VDIFF|=VNHEAD
ΔVCC(<0)
T3
VSUPH
VA 激活
SBYP 断开
T2
T0
T1
时间间隔(SN-1)
VCC(N-1)(e.g., 2.3 V)
GND
VCC(N-1)
GND
VCC(N-1)
VCC(N-1)
VSUPL
VA 去活
SBYP 闭合
VTGT
VTGT-AMP
VTGT-OFF
VAMP
VOFF
VCC=VAMP+VOFF
VSUP

图3

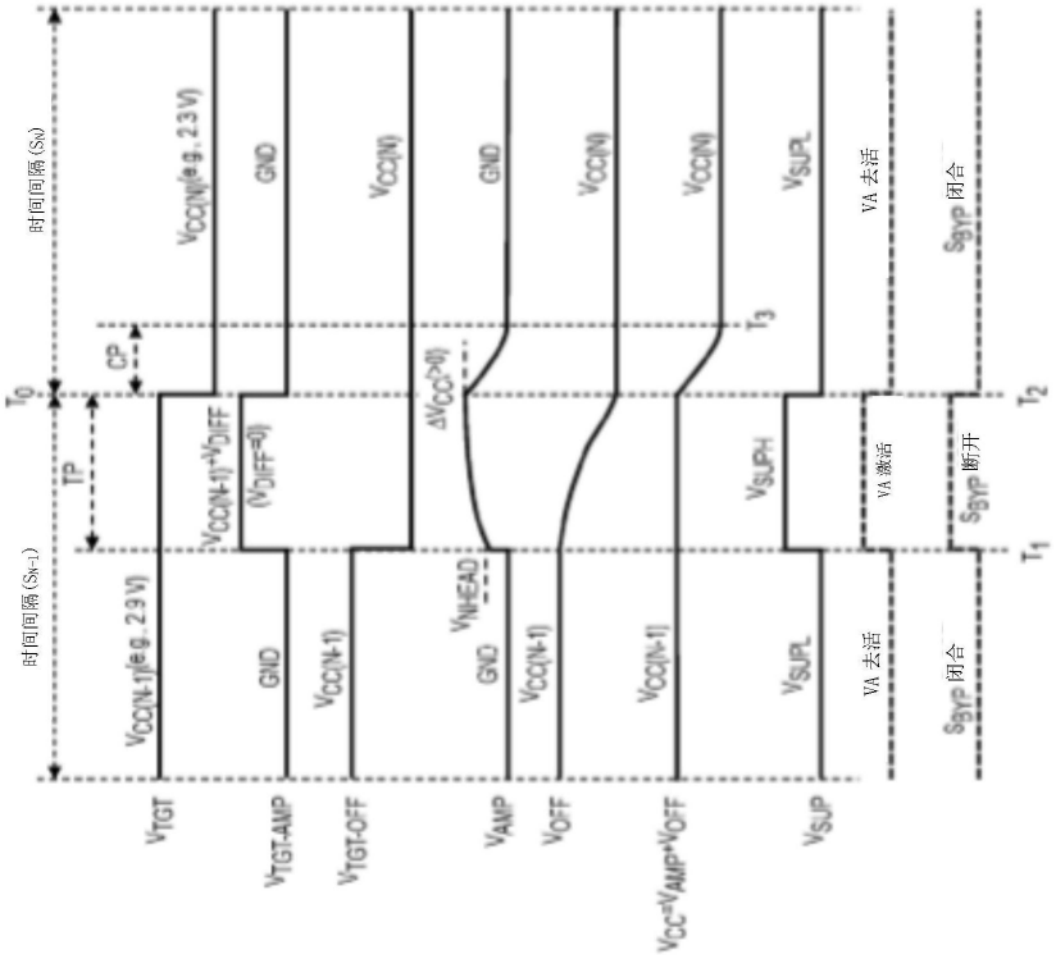

时间间隔(SN)
时间间隔(SN-1)
CP
TP
T0
T1
T2
T3
VCC(N)(e.g. 2.3 V)
VCC(N-1)(e.g. 2.9 V)
VCC(N-1)+VDIFF
(VDIFF>0)
GND
VCC(N)
VCC(N-1)
ΔVCC(>0)
VNHEAD
VCC(N)
VCC(N-1)
VCC(N)
VCC(N-1)
VSUPL
VSUPH
VSUPL
VA 去活
VA 激活
VA 去活
SgyP 闭合
SgyP 断开
SgyP 闭合
VTGT
VTGT-AMP
VTGT-OFF
VAMP
VOFF
VCC-VAMP+VOFF
VSUP

图4

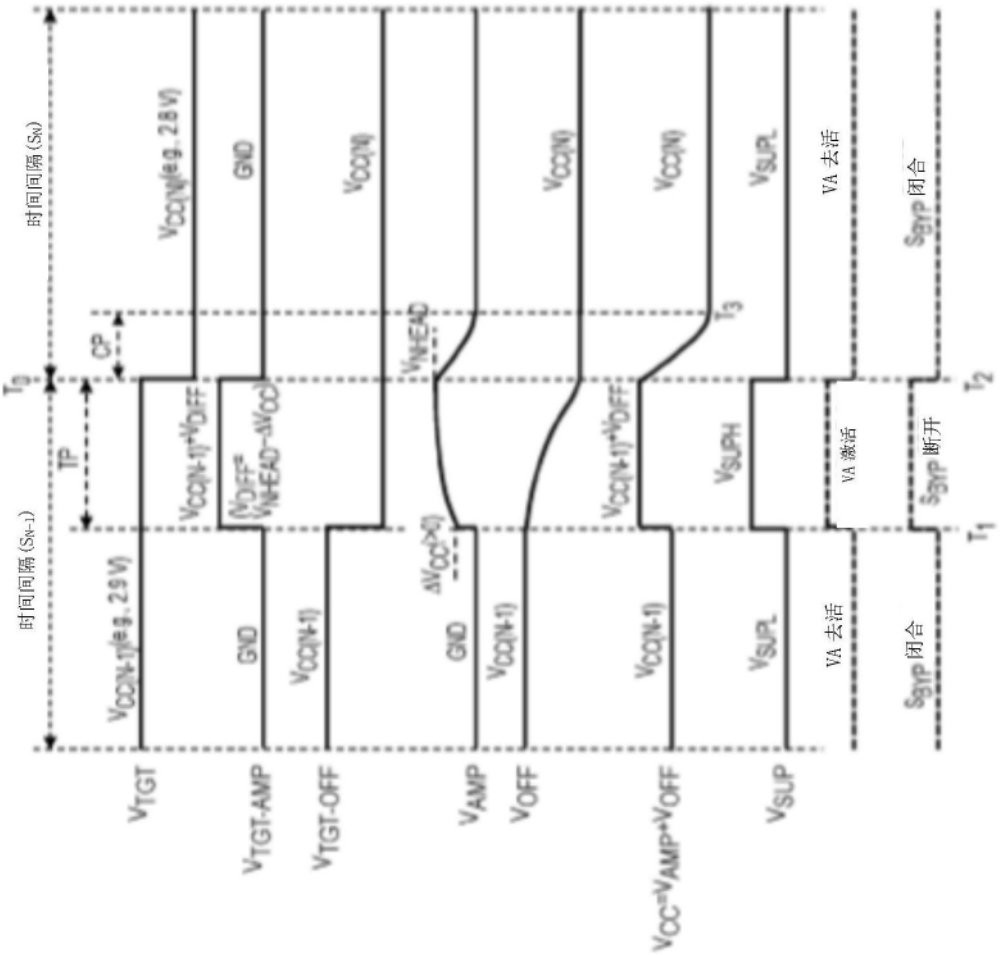

时间间隔(SN)
时间间隔(SN-1)
CP
TP
T0
T1
T2
T3
VCC(N)(e.g.,2.8 V)
VCC(N-1)(e.g.,2.5 V)
VCC(N-1)+VDIFF
(VDIFF=VHEAD-ΔVCC)
GND
VCC(N)
VCC(N-1)
VHEAD
ΔVCC(>0)
VCC(N)
VCC(N-1)+VDIFF
VCC(N-1)
VSUPL
VSUPH
VSUPL
VA 去活
VA 激活
VA 去活
SSYP 闭合
SSYP 断开
SSYP 闭合
VTGT
VTGT-AMP
VTGT-OFF
VAMP
VOFF
VCC=VAMP+VOFF
VSUP

图5

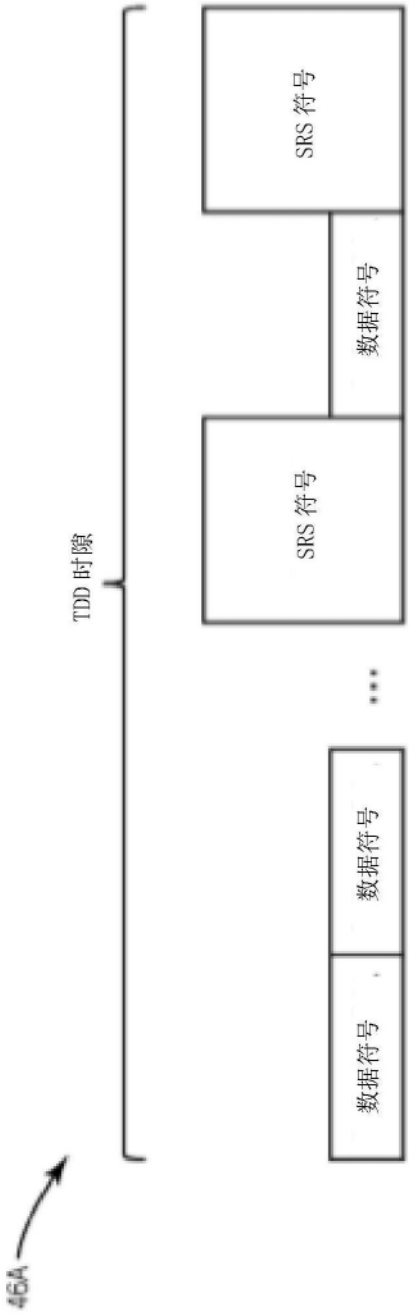


图6A

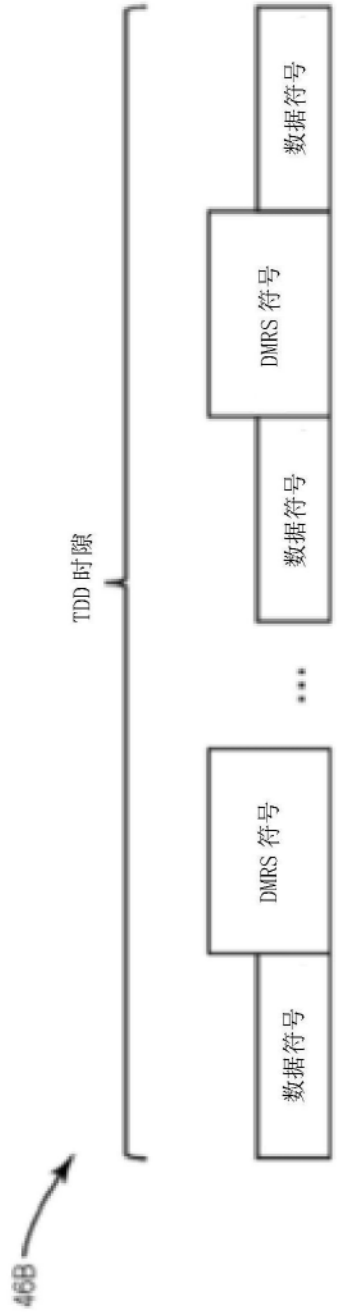


图6B

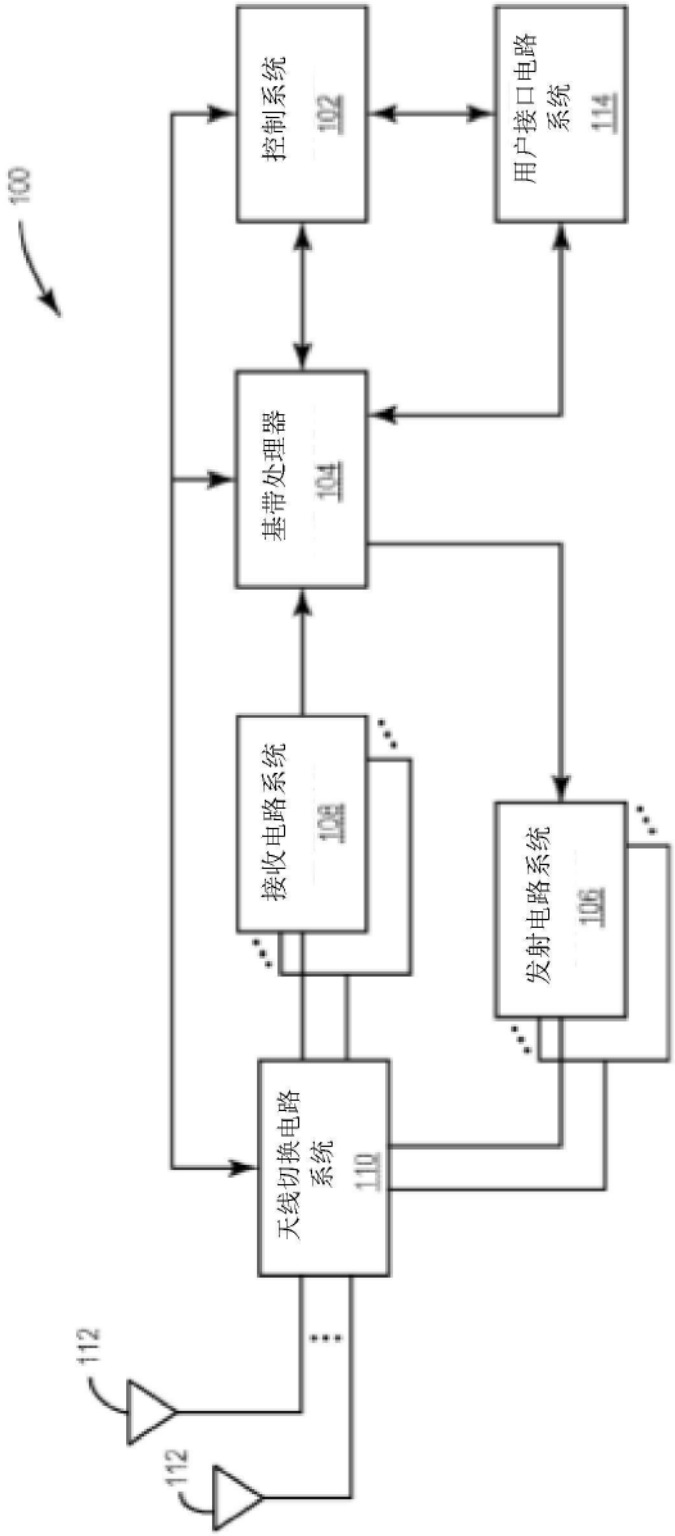

100
控制系统
102
用户接口电路系统
114
基带处理器
104
接收电路系统
108
发射电路系统
106
天线切换电路系统
110
112
112

图7