

(51) International Patent Classification:
H01L 27/04 (2006.01)(21) International Application Number:
PCT/US2013/030471(22) International Filing Date:
12 March 2013 (12.03.2013)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
13/423,720 19 March 2012 (19.03.2012) US

(71) Applicant: ANALOG DEVICES, INC. [US/US]; One Technology Way, Norwood, MA 02062 (US).

(72) Inventors: SALCEDO, Javier, A.; One Technology Way, Norwood, MA 02062 (US). PARTHASARATHY, Srivatsan; One Technology Way, Norwood, MA 02062 (US).

(74) Agent: CHRISTENSEN, Michael, R.; KNOBBE, MARTENS, OLSON & BEAR, LLP, 2040 Main Street, 14th Floor, Irvine, CA 92614 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,

HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

Published:

- with international search report (Art. 21(3))

(54) Title: APPARATUS AND METHOD FOR PROTECTION OF PRECISION MIXED-SIGNAL ELECTRONIC CIRCUITS

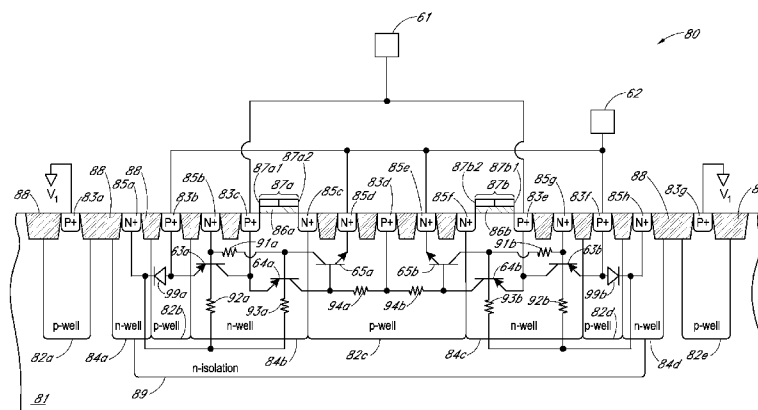


FIG. 3B

(57) Abstract: Apparatus and methods for precision mixed-signal electronic circuit protection are provided. In one embodiment, an apparatus includes a p-well, an n-well, a poly-active diode structure, a p-type active region, and an n-type active region. The poly-active diode structure is formed over the n-well, the p-type active region is formed in the n-well on a first side of the poly-active diode structure, and the n-type active region is formed along a boundary of the p-well and the n-well on a second side of the poly-active diode structure. During a transient electrical event the apparatus is configured to provide conduction paths through and underneath the poly-active diode structure to facilitate injection of carriers in the n-type active region. The protection device can further include another poly-active diode structure formed over the p-well to further enhance carrier injection into the n-type active region.

APPARATUS AND METHOD FOR PROTECTION OF PRECISION MIXED-SIGNAL ELECTRONIC CIRCUITS

BACKGROUND

Field

[0001] Embodiments of the invention relate to electronic systems, and more particularly, to protection devices for integrated circuits (ICs), such as precision mixed signal ICs associated with a low capacitance and high voltage tolerant interface.

Description of the Related Technology

[0002] Certain electronic systems can be exposed to a transient electrical event, or an electrical signal of a relatively short duration having rapidly changing voltage and high power. Transient electrical events can include, for example, electro static discharge (ESD) events arising from the abrupt release of charge from an object or person to an electronic system.

[0003] Transient electrical events can destroy an integrated circuit (IC) inside an electronic system due to overvoltage conditions and high levels of power dissipation over relatively small areas of the IC. High power dissipation can increase IC temperature and can lead to numerous problems, such as gate oxide punch-through, junction damage, metal damage, and surface charge accumulation. Moreover, transient electrical events can induce latch-up (in other words, inadvertent creation of a low-impedance path), thereby disrupting the functioning of the IC and potentially causing permanent damage to the IC. Processing technologies used for advanced mixed-signal applications can use nanoscale features, and conventional device architectures and topologies have proved insufficient to enable robust transient electrical event protection. Thus, there is a need to provide an IC with protection from such transient electrical events, such as during IC power-up and power-down conditions.

SUMMARY

[0004] In one embodiment an apparatus for providing protection from transient electrical events is provided. The apparatus includes a semiconductor substrate, a first well disposed in the semiconductor substrate, a second well disposed in the semiconductor substrate adjacent the first well, a first gate structure disposed over the

second well, a first active region disposed on a first side of the first gate structure along a boundary of the first and second wells, a second active region disposed on a second side of the first gate structure in the second well, and a third active region disposed in the first well. The second well has a doping type opposite a doping type of the first well, the second active region has a doping type opposite a doping type of the first active region, and the third active region has a doping type the same as the doping type of the first active region. During a transient overvoltage stress event the apparatus is configured to provide a first conduction path under the first gate structure and a second conduction path through the first gate structure to decrease a turn-on response time and reduce a transient breakdown voltage between the first and second wells during the transient overvoltage stress event.

[0005] In another embodiment, an apparatus for providing protection from transient electrical events is provided. The apparatus includes a semiconductor substrate, a first well disposed in the semiconductor substrate, a second well disposed in the semiconductor substrate adjacent the first well, a first means for implant blocking disposed over the second well, a first active region disposed on a first side of the first implant blocking means along a boundary of the first and second wells, a second active region disposed on a second side of the first implant blocking means in the second well, and a third active region disposed in the first well. The second well has a doping type opposite a doping type of the first well, the second active region has a doping type opposite a doping type of the first active region, and the third active region has a doping type the same as the doping type of the first active region. During a transient overvoltage stress event the apparatus is configured to provide a first conduction path under the first implant blocking means and a second conduction path through the first implant blocking means to decrease a turn-on response time and reduce a transient breakdown voltage between the first and second wells during the transient overvoltage stress event.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure 1 is a schematic block diagram of one example of an electronic system including an integrated circuit (IC) with low voltage circuitry, high voltage tolerant circuitry, and a protection system.

[0007] Figure 2 is a graph of IC protection device current versus transient electrical event voltage in accordance with one embodiment.

[0008] Figure 3A is a schematic perspective view of a protection device according to one embodiment.

[0009] Figure 3B is an annotated cross section view of the protection device of Figure 3A, taken along the lines 3B-3B.

[0010] Figure 4 is a cross section view of another implementation of the protection device of Figure 3A, taken along the lines 3B-3B.

[0011] Figure 5 is a cross section view of another embodiment of a protection device.

[0012] Figure 6A is a schematic perspective view of a protection device according to another embodiment.

[0013] Figure 6B is a cross section view of the protection device of Figure 6A, taken along the lines 6B-6B.

[0014] Figure 7 is a cross section view of another embodiment of a protection device.

[0015] Figure 8 is a schematic top plan layout view of a protection device according to one embodiment.

[0016] Figures 9A-9E are graphs of laboratory data for one implementation of the protection device of Figures 3A and 3B.

[0017] Figures 10A-10C are graphs of laboratory data for one implementation of the protection device of Figure 4.

DETAILED DESCRIPTION OF EMBODIMENTS

[0018] The following detailed description of certain embodiments presents various descriptions of specific embodiments of the invention. However, the invention can be embodied in a multitude of different ways as defined and covered by the claims. In this description, reference is made to the drawings where like reference numerals indicate identical or functionally similar elements.

[0019] Certain electronic systems are configured to protect circuits or components therein from transient electrical events. Furthermore, to help guarantee that an electronic system is reliable, manufacturers can test the electronic system under

defined stress conditions, which can be described by standards set by various organizations, such as the Joint Electronic Device Engineering Council (JEDEC), the International Electrotechnical Commission (IEC), and the Automotive Engineering Council (AEC). The standards can cover a wide multitude of transient electrical events as discussed above, including ESD events.

[0020] Electronic circuit reliability can be improved by providing protection circuits or devices for the pads of an IC. The protection devices can maintain the voltage level at the pad within a predefined safe range.

[0021] In certain applications, it can be desirable for a protection device to exhibit bidirectional operation such that a protection device transitions from a high-impedance state to a low-impedance state when the voltage of the transient electrical event exceeds a forward trigger voltage in the positive direction or falls below a reverse trigger voltage in the negative direction. The protection device can be configured to shunt a portion of the current associated with the transient electrical event when in the low-impedance state, so as to prevent the voltage of a transient electrical event from either reaching a forward or reverse failure voltage associated with damage to the IC. As will be described in detail later with reference to Figure 2, for transient electrical events having a positive voltage, the protection device can remain in the low-impedance state as long as the transient electrical event voltage remains above a forward holding voltage. Likewise, for negative transient signal events, the protection device can remain the low-impedance state as long as the transient electrical event voltage remains below a reverse holding voltage.

[0022] There is a need for a protection device that can be used to provide transient electrical event protection against both negative and positive transient signals. Additionally, there is a need for a low capacitance protection device that has fast operational speed, low static power dissipation, a small circuit area, and the ability to safely protect high-voltage tolerant pins. For example, these characteristics can be desirable in nanoscale ICs used in certain automotive, medical, and industrial processes, such as ICs used in high-speed signal processing, RF base stations, and/or in mixed voltage applications.

Overview of an Electronic System with a Protection System

[0023] Figure 1 is a schematic block diagram of an electronic system 10, which can include one or more protection devices described herein. The illustrated electronic system 10 includes an integrated circuit (IC) 4 that includes a protection system 12, low voltage circuitry 5, high voltage tolerant circuitry 6, first to third pins or pads 1-3, and first to third high voltage pins or pads 11-13.

[0024] Each of the first to third pads 1-3 and the first to third high voltage tolerant pads 11-13 can be, for example, one of power-high pads, power-low pads, or signal pads. However, the first to third high voltage tolerant pads 11-13 can be exposed to an electrical environment that is harsher than the electrical environment that the first to third pads 1-3 are exposed to. For example, the first to third high voltage tolerant pads 11-13 can be exposed to transient electrical signals having a greater voltage magnitude than transient electrical signals that reach the first to third pads 1-3. Although the IC 4 illustrates a configuration including three pads 1-3 and three high voltage tolerant pads 11-13, the IC 4 can be adapted to include more or fewer pads and/or more or fewer high voltage tolerant pads.

[0025] As illustrated in Figure 1, the low voltage circuitry 5 is electrically connected to the first to third pads 1-3, and the high voltage tolerant circuitry 6 is electrically connected to the first to third high voltage tolerant pads 11-13. In certain implementations, the high voltage tolerant circuitry 6 includes devices having a higher voltage tolerance than devices of the low voltage circuitry 5. For example, the high voltage tolerant circuitry 6 can include transistors having greater gate-to-source and/or gate-to-drain breakdown voltages. Additionally, in certain implementations, the high voltage tolerant circuitry 6 can include passive circuits, such as matching networks. As shown in Figure 1, the low voltage circuitry 5 can be configured to electrically communicate with the high voltage tolerant circuitry 6. In certain implementations, the high voltage tolerant circuitry 6 is electrically connected to the low voltage circuitry 5 using one or more transformers.

[0026] The IC 4 can be exposed to transient electrical events, such as ESD events, which can cause IC damage or induce latch-up during normal operation. For example, as illustrated in Figure 1, the third pad 3 can receive a transient electrical event 9, which can travel along electrical connections of the IC 4 and reach the low voltage

circuitry 5. The transient electrical event 9 can produce overvoltage conditions and can dissipate high levels of power, which can disrupt the functioning of the low voltage circuitry 5 and potentially cause permanent damage to the IC 4. Although Figure 1 illustrates the transient electrical event 9 reaching the third pad 3, the first and second pads 1, 2 and/or the first to third high voltage tolerant pads 11-13 can also be exposed to transient electrical events.

[0027] The protection system 12 can be provided to ensure reliability of the IC 4 by maintaining the voltage level at the pads of the IC 4 within a particular range of voltage, which can vary from pad to pad. The protection system 12 can include one or more protection circuits or devices, which can be configured to divert a current associated with a transient electrical event received on a pad of the IC to other nodes or pads of the IC, thereby providing transient electrical event protection, as will be described in further detail below.

[0028] Protection devices can be placed, for example, between a power-high pad and a signal pad, between a signal pad and a power-low pad, and/or between a power-high pad and a power-low pad. When no transient electrical event is present, the protection device can remain in a high-impedance/low-leakage state, thereby reducing static power dissipation resulting from leakage current. In the illustrated configuration, the protection system 12 has been configured to provide protection to the first to third pads 1-3 and to the first to third high voltage tolerant pads 11-13. However, other implementations are possible, such as configurations in which the protection system 12 protects the first to third pads 1-3, but not the first to third high-voltage pads 11-13, or configurations in which the protection system 12 protects the first to third high-voltage pads 11-13, but not the first to third pads 1-3.

[0029] As shown in Figure 1, the protection system 12 can be integrated on-chip with the IC 4. However, in other embodiments, the protection system 12 can be arranged external to the IC 4. For example, the protection system 12 can be included in a separately packaged IC, or it can be encapsulated in a common package with the IC 4. In such embodiments, one or more protection devices can be placed in a stand-alone IC, in a common package for system-on-a-package applications, or integrated with an IC in a common semiconductor substrate for system-on-a-chip applications.

[0030] Although the protection system 12 is illustrated in the context of the IC 4, the protection system 12 can be used in a wide array of ICs and other electronics having pads configured to operate over a single voltage domain or over a multitude of voltage domains.

[0031] Figure 2 is a graph 19 of IC protection device current versus transient electrical event voltage in accordance with one embodiment. As described above, a protection device can be configured to maintain the voltage level at a pad within a predefined safe range. Thus, the protection device can shunt a large portion of the current associated with the transient electrical event before the voltage of the transient signal $V_{\text{TRANSIENT}}$ reaches either a positive failure voltage $+V_F$ or a negative failure voltage $-V_F$ that would otherwise cause damage to the IC. Additionally, the protection device can conduct a relatively low amount of current at the normal operating voltage $+V_{\text{OP}}$, thereby reducing or minimizing static power dissipation resulting from the leakage current I_{LEAKAGE} , which enhances the energy efficiency of the IC.

[0032] Furthermore, as shown in the graph 19, the protection device can transition from a high-impedance state $+Z_H$ to a low-impedance state $+Z_L$ when the voltage of the transient signal $V_{\text{TRANSIENT}}$ reaches a positive trigger voltage $+V_{\text{TR}}$. Thereafter, the pad circuit can shunt a large amount of current over a wide range of transient signal voltage levels. The pad circuit can remain in the low-impedance state $+Z_L$ as long as the transient signal voltage level is above a positive holding voltage $+V_H$. By configuring the protection device to have a trigger voltage $+V_{\text{TR}}$ and a holding voltage $+V_H$, the protection device can have improved performance while having enhanced stability against unintended activation. In certain implementations, it can be specified for the holding voltage $+V_H$ to be above the operating voltage $+V_{\text{OP}}$ such that the protection device does not remain in the low-impedance state $+Z_L$ after passage of the transient signal event and a return to normal operating voltage levels.

[0033] In the illustrated embodiment, the protection device can also shunt a large amount of current for transient electrical events having a negative voltage, so that the protection device can provide transient electrical event protection against both negative and positive transient signals. The protection device can transition from a high-impedance state $-Z_H$ to a low-impedance state $-Z_L$ when the voltage of the transient signal $V_{\text{TRANSIENT}}$ reaches a negative trigger voltage $-V_{\text{TR}}$, thereby shunting a large negative

amount of current. The pad circuit can remain in the low-impedance state $-Z_L$ as long as the voltage magnitude of the negative transient signal is greater than the voltage magnitude of the negative holding voltage $-V_H$.

[0034] In Figure 2, voltage is expressed along a horizontal axis, and current is expressed along a vertical axis. In the illustrated embodiment, the protection device has I-V characteristics that are symmetrical. In other implementations, the protection devices described herein can have asymmetrical I-V characteristics. For example, protection devices can have different trigger voltages, holding voltages, and/or failure voltages with different I-V curves in the positive and negative regions of the graph.

[0035] It can be difficult to provide a protection device having a sufficiently high trigger voltage, particularly when providing the protection device on an IC fabricated using a low voltage semiconductor processing technology, for instance sub-nanoscale feature technologies. Additionally, it can be difficult to provide a protection device that has a relatively fast turn-on speed so as to prevent voltage overshoot from damaging low voltage devices. Furthermore, it can be difficult to provide a protection device that has a relatively small parasitic capacitance so as to provide protection from transient electrical events without substantially impacting signal bandwidth of high frequency signal pins. As will be described herein, protection devices are provided that can have a relatively low capacitance, a relatively fast operational speed, relatively low static power dissipation, high voltage tolerance, and a relatively small circuit area. Additionally, in certain implementations, protection devices are provided that can be made using semiconductor layers and regions associated with a typical low voltage semiconductor process, for instance, nanoscale complementary metal oxide semiconductor (CMOS) technologies.

Overview of Embodiments of Protection Devices

[0036] Figure 3A is a schematic perspective of a protection device 80 according to one embodiment. The protection device 80 includes a p-type doped (herein “p-type”) semiconductor substrate 81, first to fifth p-wells 82a-82e, first to seventh p-type active areas 83a-83g, first to fourth n-wells 84a-84d, first to eighth n-type doped (herein “n-type”) active areas 85a-85h, first and second gate oxide layers 86a, 86b, first and second gate regions 87a, 87b, oxide regions 88, and n-type isolation layer 89.

[0037] As illustrated in Figure 3A, the substrate 81 includes the first to fourth n-wells 84a-84d and the first to fifth p-wells 82a-82e formed therein. The second and third n-wells 84b, 84c are disposed on opposite sides of the third p-well 82c. The second p-well 82b is disposed on a side of the second n-well 84b opposite the third p-well 82c. The fourth p-well 82d is disposed on a side of the third n-well 84c opposite the third p-well 82c. The first n-well 84a is disposed on a side of the second p-well 82b opposite the second n-well 84b. The fourth n-well 84d is disposed on a side of the fourth p-well 82d opposite the third n-well 84c. The n-type isolation layer 89 is disposed beneath the second and third n-wells 84b, 84c, beneath the second to fourth p-wells 82b-82d, and beneath a portion of the first and fourth n-wells 84a, 84d. The first p-well 82a is formed adjacent the first n-well 84a on a side of the first n-well 84a opposite the second p-well 82b. The fifth p-well 82e is formed adjacent the fourth n-well 84d on a side of the fourth n-well 84d opposite the fourth p-well 82d.

[0038] In the illustrated configuration, the second p-well 82b abuts the first and second n-wells 84a, 84b, the third p-well 82c abuts the second and third n-wells 84b, 84c, the fourth p-well 82d abuts the third and fourth n-wells 84c, 84d, and the first and fifth p-wells 82a, 82e are spaced from the first and fourth n-wells 84a, 84d, respectively, such that the first p-well 82a does not abut the first n-well 84a and the fifth p-well 82e does not abut the fourth n-well 84d. However, other implementations are possible, including, for example, configurations in which the first p-well 82a abuts the first n-well 84a and the fifth p-well 82e abuts the fourth n-well 84d.

[0039] The first and seventh p-type active areas 83a, 83g are disposed in the first and fifth p-wells 82a, 82e, respectively. The second and sixth p-type active areas 83b, 83f are disposed in the second and fourth p-wells 82b, 82d, respectively. The first and eighth n-type active areas 85a, 85h are disposed in the first and fourth n-wells 84a, 84d, respectively. The fourth p-type active area 83d is disposed in the third p-well 82c. The fourth n-type active area 85d is disposed in the third p-well 82c on a side of the fourth p-type active area 83d facing the second n-well 84b. The fifth n-type active area 85e is disposed in the third p-well 82c on a side of the fourth p-type active area 83d facing the third n-well 84c.

[0040] The first and second gate oxide layers 86a, 86b are disposed on a surface 90 of the substrate 81 over the second and third n-wells 84b, 84c, respectively.

The first and second gate regions 87a, 87b are disposed over the first and second gate oxide layers 86a, 86b, respectively, and can be polysilicon layers. The third p-type active area 83c is disposed in the second n-well 84b on a first side of the first gate region 87a. The third n-type active area 85c is disposed on a second side of the first gate region 87a, and includes a first portion disposed in the second n-well 84b and a second portion disposed in the third p-well 82c. The second n-type active area 85b is disposed in the second n-well 84b on a side of the third p-type active area 83c opposite the first gate region 87a. The fifth p-type active area 83e is disposed in the third n-well 84c on a first side of the second gate region 87b. The sixth n-type active area 85f is disposed on a second side of the second gate region 87b, and includes a first portion disposed in the third n-well 84c and a second portion disposed in the third p-well 82c. The seventh n-type active area 85g is disposed in the third n-well 84c on a side of the fifth p-type active area 83e opposite the second gate region 87b.

[0041] The first gate region 87a includes a first p-type gate region or p-type doped poly-crystalline gate region 87a1 adjacent the third p-type active area 83c and a first n-type gate region or n-type doped poly-crystalline gate region 87a2 adjacent the third n-type active area 85c. Additionally, the second gate region 87b includes a second p-type gate region 87b1 adjacent the fifth p-type active area 83e and a second n-type gate region 87b2 adjacent the sixth n-type active area 85f. As will be described in detail below with respect to Figure 3B, configuring the first and second gate regions 87a, 87b to each include a p-type gate region and an n-type gate region can enhance the turn-on speed and/or amplify transient coupling of the protection device 80 during a transient electrical event.

[0042] In the illustrated embodiment, the protection device 80 is formed in the substrate 81, which can be a p-type substrate. In another embodiment, the substrate can include a p-type epitaxial layer formed on a silicon (Si) substrate. Although not illustrated in Figure 3A, the substrate 81 can also include other devices or structures formed therein.

[0043] In one embodiment, the first to fifth p-wells 82a-82e and the first to fourth n-wells 84a-84d can be similar to one another, and can have a depth ranging between about 1.5 μm and about 5.5 μm from the surface 90 of the substrate 81. In one implementation, the first to seventh p-type active areas 83a-83g and the first to eighth

n-type active areas 85a-85h have a depth that is about 15 times to about 25 times less than a depth of the well within which the active area is formed. The oxide regions 88 can have any suitable depth, such as depth that is about 5 times to about 15 times less than the depth of the first to fifth p-wells 82a-82e. In certain implementations, the oxide regions 88 can be relatively deeper than the first to seventh p-type active areas 83a-83g and the first to eighth n-type active areas 85a-85h.

[0044] The first and fourth n-wells 84a, 84d and the n-type isolation layer 89 can aid in electrically isolating the second to fourth p-wells 82b-82d from the substrate 81, thereby permitting the p-type substrate 81 and the second to fourth p-wells 82b-82d to operate at different electrical potentials. As used herein, and as will be understood by one of skill in the art, the term “n-type isolation layer” refers to any suitable n-type isolation layer, including, for example, those used in silicon-on-insulator (SOI) technologies, buried n-layer technologies, or in deep n-well technologies. Although the protection device 80 is illustrated as including the first and fourth n-wells 84a, 84d and the n-type isolation layer 89, in certain implementations, the protection device 80 can be isolated from a substrate in other ways. For example, isolation can be achieved when using silicon-on-insulator (SOI) processes by using dielectric structures. SOI processes can be employed in a variety of applications, including, for example, applications having high electrical robustness requirements. Although the protection device 80 is illustrated as including the first and fourth n-wells 84a, 84d and the n-type isolation layer 89, in certain implementations, such as high frequency configurations, the first and fourth n-wells 84a, 84d and the n-type isolation layer 89 can be omitted in favor of forming the second to third p-wells 82b-82d and the second and third n-wells 84b, 84c directly in the substrate 81.

[0045] The first and fifth p-wells 82a, 82e and the first and seventh p-type active areas 83a, 83g can form a guard ring around the protection device 80. The guard ring can be employed to eliminate the formation of unintended parasitic paths between the protection device 80 and surrounding semiconductor components when integrated on-chip.

[0046] The illustrated protection device 80 includes the oxide regions 88. Formation of the isolation regions can involve etching trenches in the substrate 81, filling the trenches with a dielectric, such as silicon dioxide (SiO₂), and removing the excess

dielectric using any suitable method, such as chemical-mechanical planarization. In certain implementations, the oxide regions 88 can be shallow trench regions, or any other suitable dielectric regions disposed between active areas.

[0047] The protection device 80 can undergo back end processing to form contacts and metallization. Skilled artisans will appreciate that these details have been omitted from this figure for clarity.

[0048] Figure 3B is an annotated cross section view of the protection device 80 of Figure 3A, taken along the lines 3B-3B. The protection device 80 includes the p-type substrate 81, the first to fifth p-wells 82a-82e, the first to seventh p-type active areas 83a-83g, the first to fourth n-wells 84a-84d, the first to eighth n-type active areas 85a-85h, the first and second gate oxide layers 86a, 86b, the first and second gate regions 87a, 87b, the oxide regions 88, and the n-type isolation layer 89, which can be as described above with respect to Figure 3A.

[0049] The cross section shows examples of equivalent circuit devices formed from the illustrated structure, such as first and second PNP bipolar transistors 64a, 64b, first and second NPN bipolar transistors 65a, 65b, first and second open-base PNP bipolar transistors 63a, 63b, a first resistor 91a, a second resistor 91b, a third resistor 92a, a fourth resistor 92b, a fifth resistor 93a, a sixth resistor 93b, a seventh resistor 94a, an eighth resistor 94b, and first and second diodes 99a, 99b. Additionally, the cross section has been annotated to show the first and second pads 61, 62 as well as electrical connections within the protection device 80 and to the pads.

[0050] The first pad 61 is electrically connected to the third and fifth p-type active areas 83c, 83e. The second pad 62 is electrically connected to the second and sixth p-type active areas 83b, 83f and to the fourth and fifth n-type active areas 85d, 85e. The first and seventh p-type active areas 83a, 83g are electrically connected to the first supply voltage V_1 , which can be, for example, a power-low or ground supply used to control the electrical potential of the substrate 81.

[0051] The first and second PNP bipolar transistors 64a, 64b can be formed from the third and fifth p-type active areas 83c, 83e, from the second and third n-wells 84b, 84c, and from the third p-well 82c, and can be lateral parasitic PNP bipolar devices. For example, the first PNP bipolar transistor 64a can have an emitter formed from the third p-type active area 83c, a base formed from the second n-well 84b, and a collector

formed from the third p-well 82c. Additionally, the second PNP bipolar transistor 64b can have an emitter formed from the fifth p-type active area 83e, a base formed from the third n-well 84c, and a collector formed from the third p-well 82c. The first and second NPN bipolar transistors 65a, 65b can be formed from the second and third n-wells 84b, 84c, the third p-well 82c, and the fourth and fifth n-type active areas 85d, 85e, and can be lateral parasitic NPN bipolar devices. For example, the first NPN bipolar transistor 65a can have an emitter formed from the fourth n-type active area 85d, a base formed from the third p-well 82c, and a collector formed from the second n-well 84b. Additionally, the second NPN bipolar transistor 65b can have an emitter formed from the fifth n-type active area 85e, a base formed from the third p-well 82c, and a collector formed from the third n-well 84c. The first and second open-base PNP bipolar transistors 63a, 63b can be formed from the second and fourth p-wells 82b, 82d, the second and third n-wells 84b, 84c, and the third and fifth p-type active areas 83c, 83e, and can be lateral parasitic PNP bipolar devices. For example, the first open-base PNP bipolar transistor 63a can have an emitter formed from the second p-well 82b, a base formed from the second n-well 84b, and a collector formed from the third p-type active area 83c. Additionally, the second open-base PNP bipolar transistor 63b can have an emitter formed from the fourth p-well 82d, a base formed from the third n-well 84c, and a collector formed from the fifth p-type active area 83e.

[0052] The first and second resistors 91a, 91b can be formed from the second and third n-wells 84b, 84c, respectively, utilizing the resistance therein. Additionally, the third and fifth resistors 92a, 93a can be formed from the first and second n-wells 84a, 84b and the n-type isolation layer 89, utilizing the resistance therein. Furthermore, the fourth and sixth resistors 92b, 93b can be formed from the third and fourth n-wells 84c, 84d and the n-type isolation layer 89, utilizing the resistance therein. Additionally, the seventh and eighth resistors 94a, 94b can be formed from the third p-well 82c, utilizing the resistance therein. The first diode 99a can have an anode formed from the second p-well 82b and a cathode formed from the first n-well 84a. The second diode 99b can have an anode formed from the fourth p-well 82d and a cathode formed from the second n-well 84b.

[0053] In the illustrated configuration, the protection device 80 does not include conventional metal oxide semiconductor (MOS) transistor formation, since active

areas of different doping polarities have been implanted on opposing sides of the first and second gate regions 87a, 87b. Rather, the gate regions 87a, 87b have been used as a self-aligned implant mask when doping the third and fifth p-type active areas 83c, 83e and the third and sixth n-type active areas 85c, 85f, which also creates a well-defined separation between the active areas implanted.

[0054] The protection device 80 can protect an IC from a transient electrical event having either positive or negative voltage amplitude. For example, when a negative transient electrical event causes the voltage of the first pad 61 to decrease relative to the voltage of the second pad 62, the first and second open-base PNP bipolar transistors 63a, 63b can operate as a reverse conduction path to provide protection to the IC. The reverse conduction path can have a breakdown voltage associated with a collector-emitter breakdown voltage of the first and second open-base PNP bipolar transistors 63a, 63b. By electrically floating the second and third n-wells 84b, 84c that operate as the bases of the first and second open-base PNP bipolar transistors 63a, 63b, respectively, the collector-emitter breakdown voltage of the first and second open-base PNP bipolar transistors 63a, 63b can be increased.

[0055] The first and second PNP bipolar transistors 64a, 64b and the first and second NPN bipolar transistors 65a, 65b can operate as a forward conduction path to provide protection against a positive transient electrical event that causes the voltage of the first pad 61 to increase relative to the voltage of the second pad 62. For example, as the voltage of the first pad 61 increases relative to the voltage of the second pad 62, the voltage across the first and second PNP bipolar transistors 64a, 64b and the voltage across the first and second NPN bipolar transistors 65a, 65b can increase. As skilled artisans will appreciate, the first PNP bipolar transistor 64a and the first NPN bipolar transistor 65a are cross-coupled in a feedback configuration, and at a certain level of voltage difference between the first and second pads 61, 62 the feedback between the first PNP bipolar transistor 64a and the first NPN bipolar transistor 65a can be regenerative and cause the first PNP bipolar transistor 64a and the first NPN bipolar transistor 65a to enter a low-impedance state. Likewise, at a certain level of voltage difference between the first and second pads 61, 62, the feedback between the second PNP bipolar transistor 64b and the second NPN bipolar transistor 65b can be regenerative and can cause the second PNP bipolar transistor 64b and the second NPN bipolar transistor 65b to enter a low-

impedance state. The transition of the cross-coupled bipolar transistors into the low-impedance state and the resulting conductivity modulation of the protection device 80 can be associated with high carrier injection relative to normal operating conditions. The injected carriers can be associated with, for example, the injection of holes from the third and fifth p-type active regions 83c, 83e into the second and third n-wells 84b, 84c and the injection of electrons from the fourth and fifth n-type active regions 85d, 85e into the third p-well 82c.

[0056] Inclusion of the first and second gate regions 87a, 87b aids in improving the transient performance of the protection device 80 by facilitating the injection of carriers into the third p-well 82c so as to decrease the response time and lower the voltage at which the cross-coupled PNP bipolar transistors 64a, 64b and NPN bipolar transistors 65a, 65a trigger. In particular, a transient signal event can be associated with fast rise and fall times (for example, from about 0.2 ns to about 15 ns) relative to the range of normal signal operating conditions. When a positive transient electrical event is received between the first and second pads 61, 62, a capacitance-driven displacement current can flow from the first pad 61 to the first and second gate regions 87a, 87b, which can increase the voltage of the first and second gate regions 87a, 87b and provide a conduction path under the first and second gate regions 87a, 87b for which carriers can reach the third and sixth n-type active areas 85c, 85f. Additionally, the first and second gate regions 87a, 87b themselves can operate as a conduction path for transient signals through which a capacitive-driven displacement current can flow from the first pad 61 to the third and sixth n-type active areas 85c, 85f.

[0057] Configuring the protection device 80 to include the first and second gate regions 87a, 87b aids in injecting carriers into the collector-base junctions of the PNP bipolar transistors 64a, 64b and into the collector-base junctions of the NPN bipolar transistors 65a, 65b. By enhancing feedback between the cross-coupled bipolar transistors in this manner can reduce a breakdown voltage between the third p-well 82c and the second and third n-wells 84b, 84c during stress conditions while beneficially maintaining relatively high quasi-static DC blocking voltage characteristics. Additionally, configuring the protection device 80 in this manner can provide a direct conduction path closer to the surface of the substrate 81 beneath the first and second gate regions 87a, 87b, thereby reducing the base transit time of the first and second PNP bipolar transistors

64a, 64b. Reducing base transit time can reduce the forward trigger voltage of the protection device 80 and improve the response time of the protection device 80 during a transient electrical event.

[0058] Accordingly, the first and second gate regions 87a, 87b can be used to help create direct carriers injection paths of the third and sixth n-type active areas 85c, 85f, thereby helping to activate the forward conduction path of the protection device 80 during a positive transient electrical event. However, during normal operating conditions, even at relatively high quasi-static voltages, the impedance between the first pad 61 and the third and sixth n-type active areas 85c, 85f can be relatively high, thereby providing enhanced protection against unintended activation of the protection device 80. Thus, the configuration illustrated in Figure 3B can be configured to provide a forward trigger voltage which decreases in response to rates of high power and voltage change associated with the conditions of a transient signal stress events such as electrostatic discharge events.

[0059] The performance of the protection device 80 can be further enhanced by configuring the first gate region 87a to include the first p-type gate region 87a1 and the first n-type gate region 87a2, and by configuring the second gate region 87b to include the second p-type gate region 87b1 and the second n-type gate region 87b2. In particular, the first and second n-type gate regions 87a2, 87b2, the first and second gate regions 87a, 87b can form p-n junction diodes that can reduce the response time at which direct lateral conduction paths are formed beneath the first and second gate regions 87a, 87b during a transient electrical event. Additionally, the highly-doped p-n junction poly structures formed can also increase the amount of capacitor-driven displacement current that flows from the first pad 81a to the third and sixth n-type active areas 85c, 85f by reducing the impedance of the first and second gate regions 87a, 87b to transient signals that have a positive voltage with respect to the first pad 61a.

[0060] The protection device 80 can protect an IC from a transient electrical event having either positive or negative voltage polarity. Using a single protection device 80 to provide protection against both positive and negative transient electrical events can permit a reduction in layout area relative to a design that uses separate structures for protection against positive and negative transient electrical events.

[0061] Although Figure 3B illustrates one embodiment of the connectivity of the protection device 80, other configurations are possible.

[0062] For example, in some embodiments the first and eighth n-type active areas 85a, 85h are electrically connected in other ways. For instance, in some implementations, the first and eighth n-type active areas 85a, 85h are electrically connected to a DC voltage source, such as a power-high supply. Connecting the n-type active areas 85a, 85h to a power-high voltage supply creates a stronger reverse-biased junction between the substrate 81 and the isolation structure formed from the n-wells 84a-84d and the n-type isolation layer 89. Additionally, biasing the first and eighth n-type active areas 85a, 85h also creates a stronger reverse-bias of the emitter-base junctions of the PNP bipolar transistors 64a, 64b, which increases the breakdown voltage and decreases the leakage current of the protection device during normal IC operation.

[0063] Additionally, in some implementations, the first and eighth n-type active areas 85a, 85h are electrically connected to the first pad 61. In such configurations, the first and second diodes 99a, 99b can aid in providing protection against negative transient electrical events. However, electrically connecting the first and eighth n-type active areas 85a, 85h to the first pad 61 also connects the fifth and sixth resistors 93a, 93b between the emitter-base junctions of the first and second PNP bipolar transistors 64a, 64b, respectively. Inclusion of these resistors assists in shifting the breakdown voltage of the first and second PNP bipolar transistors 64a, 64b from the lower open-base breakdown (herein, "BVCEO") to a slightly higher emitter-base-resistor driven breakdown (herein, "BVCEB"). Configuring the device in this manner allows for fine tuning of the blocking voltage characteristics of the device without addition of external discrete components, such as resistors. Additionally, increasing the blocking voltage in this manner allows for modification of the device characteristics to accommodate performance or specification requirements associated with high voltage tolerant pins, as will be discussed in connection with other embodiments for addressing specific design constraints in precision mixed-signals ICs.

[0064] Accordingly, configurations of the protection device 80 that connect the first pad 61 to the first and eighth n-type active areas 85a, 85h can have a higher forward breakdown between the first pad 61 and the second pad 62 and lower forward-biased diode for reverse conduction between the second pad 62 and the first pad 61. The

electrical potential of the bases of the PNP bipolar transistors 63a-63b, 64a-64b can be controlled through a resistor defined by the resistance of the first and second n-type active areas 85a, 85h, the resistance of the first to fourth n-wells 84a-84d, and the resistance of the n-type isolation layer 89. By tuning the doping and spacing of the regions defining this resistor, the breakdown voltages of the protection device 80 can be controlled while maintaining fast device response time upon stress.

[0065] Furthermore, in some embodiments, such as implementations associated with a relatively low reverse breakdown voltage, the second and fourth p-wells 82b, 82d can be omitted. In such configurations, the second and sixth p-type active areas 83b, 83f can be formed in second and third n-wells 84b, 84c, respectively, and can operate as the emitters of the first and second open-base PNP bipolar transistors 63a, 63b. Although positioning the second and sixth p-type active areas 83b, 83f in the second and third n-wells 84b, 84c can reduce the robustness of the reverse conduction path relative to the configuration shown in Figure 3B due to a lower reverse blocking voltage diode formation. Configuring the protection device in this manner can aid in reducing device layout area and reverse diode on-state resistance.

[0066] Additionally, in some embodiments, the isolation region defined by the n-type isolation layer 89 and the first and fourth n-wells 84a, 84d can be omitted in favor of isolating the protection device 80 from the substrate 81 in other ways, such as using a silicon on insulator (SOI) process.

[0067] In Figures 3A and 3B, the protection device 80 is symmetrical about the fourth p-type active area 83d to enhance device current handling capability per unit area. Persons having ordinary skill in the art will appreciate that the teachings herein are also applicable to asymmetric devices. For example, in certain implementations the wells, active areas, and/or other structures of the protection device 80 can be arranged in an asymmetric configuration in which the dimensions of the left-half of the device are different than the dimensions of the right-half of the device. Additionally, although configuring the protection device 80 to include both a left-half and a right-half can aid in reducing the area of the protection device 80 for a given amount of protection current, the teachings herein are applicable to structures including only a left-half or a right-half, such as implementations omitting the fifth to eighth n-type active areas 85e-85h, the fifth to seventh p-type active areas 83e-83g, the second gate oxide layer 86b, the second gate

region 87b, the third and fourth n-wells 87c, 87d, and the fourth and fifth p-wells 82d, 82e.

[0068] Figure 4 is a cross section view of another implementation of the protection device 80 of Figure 3A, taken along the lines 3B-3B. The protection device 100 of Figure 4 is similar to the protection device 80 of Figure 3B, except that the protection device 100 of Figure 4 illustrates a configuration in which the first pad 61 is further connected to the second and seventh n-type active areas 85b, 85g and in which the second pad 62 is further connected to the fourth p-type active area 83d.

[0069] Connecting the first pad 61 to the second and seventh n-type active areas 85b, 85g can reduce the reverse conduction voltage of the protection device 100 relative to the configuration shown in Figure 3B for negative stress conditions of the first pad 61 relative to the second pad 62. For example, rather than electrically floating the second and third n-wells 84b, 84c and using the first and second open-base PNP bipolar transistors 63a, 63b of Figure 3B to provide protection against negative transient electrical events, the protection device 100 uses emitter-base diode connected PNP bipolar transistor structures to provide protection against negative transient electrical events. For example, diode structures formed between the second p-well 82b and the second n-well 84b and between the fourth p-well 82d and the third n-well 84c can be used to control the reverse conduction voltage of the protection device 100. Since these diode structures can have a breakdown voltage that is less than a breakdown voltage of the first and second open-base PNP bipolar transistors 63a, 63b of Figure 3B, the protection device 100 of Figure 4 can have a lower reverse conduction voltage than the protection device 80 of Figure 3B. On the other hand, connecting the second and seventh n-type active areas 85b, 85g in this manner can reduce the resistance between the base and emitter of the PNP bipolar transistors 64a, 64b, respectively, thereby increasing the forward conduction voltage.

[0070] The protection device 100 also illustrates a configuration in which the second pad 62 is further connected to the fourth p-type active area 83d. Connecting the second pad 62 in this manner can be used to control the electrical potential of the bases of the first and second NPN bipolar transistors 65a, 65b shown in Figure 3B and to lower base-emitter resistance, which can lead to an increase in the forward trigger voltage of the protection device 100 of Figure 4 relative to the forward trigger voltage of the protection

device 80 of Figure 3B when the first pad 61 is stressed positive relative to the second pad 62. Connecting the protection device 100 in this manner can provide a high voltage tolerant protection device while maintaining fast response time during transient stress conditions.

[0071] Figure 5 is a cross section view of another embodiment of a protection device 110 in which the third p-well 82c has been configured to be electrically floating. The protection device 110 of Figure 5 is similar to the protection device 80 of Figure 3B, except that the protection device 110 of Figure 5 illustrates a configuration in which the fourth p-type active area 83d and the fifth n-type active area 85e have been omitted. Configuring the protection device 110 in this manner can increase the size of the emitter of the first and second NPN bipolar transistors 65a, 65b shown in Figure 3B, thereby enhancing current handling capability of the device. Additionally, by omitting the fourth p-type active area 83d and the fifth n-type active area 85e, the protection device 110 can be configured to have a smaller area.

[0072] Figure 6A is a schematic perspective of a protection device 120 according to another embodiment. The protection device 120 includes the p-type substrate 81, the first to fifth p-wells 82a-82e, the first to fourth n-wells 84a-84d, the oxide regions 88, and the n-type isolation layer 89, which can be as described earlier with respect to Figure 3A. The protection device 120 further includes first to eighth p-type active areas 123a-123h, first to seventh n-type active areas 125a-125g, first to fourth gate oxide layers 126a-126d, and first to fourth gate regions 127a-127d.

[0073] The first and eighth p-type active areas 123a, 123h are disposed in the first and fifth p-wells 82a, 82e, respectively. The second and seventh p-type active areas 123b, 123g are disposed in the second and fourth p-wells 82b, 82d, respectively. The first and seventh n-type active areas 125a, 125g are disposed in the first and fourth n-wells 84a, 84d, respectively.

[0074] The first and fourth gate oxide layers 126a, 126d are disposed on the surface 90 of the substrate 81 over the second and third n-wells 84b, 84c, respectively. The first and fourth gate regions 127a, 127d are disposed over the first and fourth gate oxide layers 126a, 126d, respectively, and can be polysilicon layers. The third p-type active area 123c is disposed in the second n-well 84b on a first side of the first gate region 127a. The third n-type active area 125c is disposed on a second side of the first

gate region 127a, and includes a first portion disposed in the second n-well 84b and a second portion disposed in the third p-well 82c. The second n-type active area 125b is disposed in the second n-well 84b on a side of the third p-type active area 123c opposite the first gate region 127a. The sixth p-type active area 123f is disposed in the third n-well 84c on a first side of the fourth gate region 127d. The fifth n-type active area 125e is disposed on a second side of the fourth gate region 127d, and includes a first portion disposed in the third n-well 84c and a second portion disposed in the third p-well 82c. The sixth n-type active area 125f is disposed in the third n-well 84c on a side of the sixth p-type active area 123f opposite the fourth gate region 127d.

[0075] The second and third gate oxide layers 126b, 126c are disposed on the surface 90 of the substrate 81 over the third p-well 82c. The second and third gate regions 127b, 127c are disposed over the second and third gate oxide layers 126b, 126c, respectively. The fourth p-type active area 123d is disposed in the third p-well 82c on a first side of the second gate region 127b. The third n-type active area 125c is disposed on a second side of the second gate region 127b. The fifth p-type active area 123e is disposed in the third p-well 82c on a first side of the third gate region 127c. The fifth n-type active area 125e is disposed on a second side of the third gate region 127c. The fourth n-type active area 125d is disposed in the third p-well 82c between the fourth and fifth p-type active areas 123d, 123e.

[0076] The first gate region 127a includes a first p-type gate region 127a1 adjacent the third p-type active area 123c and a first n-type gate region 127a2 adjacent the third n-type active area 125c. Additionally, the second gate region 127b includes a second p-type gate region 127b1 adjacent the fourth p-type active area 123d and a second n-type gate region 127b2 adjacent the third n-type active area 125c. Furthermore, the third gate region 127c includes a third p-type gate region 127c1 adjacent the fifth p-type active area 123e and a third n-type gate region 127c2 adjacent the fifth n-type active area 125e. Additionally, the fourth gate region 127d includes a fourth p-type gate region 127d1 adjacent the sixth p-type active area 123f and a fourth n-type gate region 127d2 adjacent the fifth n-type active area 125e. As will be described in detail below with respect to Figure 6B, configuring the first to fourth gate regions 127a-127d to each include a p-type gate region and an n-type gate region can reduce standing power dissipation by eliminating or decreasing surface leakage paths between critical adjacent

conduction path in the protection device. Configuring the device in this manner can enhance the turn-on speed of the protection device 120 during a transient electrical event by allowing more uniform current flow laterally without a need for deep inter-well isolations to separate critical active regions of opposite doping polarities.

[0077] The protection device 120 can undergo back end processing to form contacts and metallization. Skilled artisans will appreciate that these details have been omitted from this figure for clarity.

[0078] Figure 6B is a cross section view of the protection device 120 of Figure 6A, taken along the lines 6B-6B. The protection device 120 includes the p-type substrate 81, the first to fifth p-wells 82a-82e, the first to fourth n-wells 84a-84d, the oxide regions 88, the n-type isolation layer 89, the first to eighth p-type active areas 123a-123h, the first to seventh n-type active areas 125a-125g, the first to fourth gate oxide layers 126a-126d, and the first to fourth gate regions 127a-127d, which can be as described above with respect to Figure 6A. The cross section shows the first and second pads 61, 62 as well as electrical connections within the protection device 120 and to the pads.

[0079] The first pad 61 is electrically connected to the third and sixth p-type active areas 123c, 123f. The second pad 62 is electrically connected to the second and seventh p-type active areas 123b, 123g and to the fourth n-type active area 125d. The first and eighth p-type active areas 123a, 123h are electrically connected to the first supply voltage V_1 , which can be, for example, a power-low or ground supply.

[0080] The protection device 120 can protect an IC from a transient electrical event having either positive or negative voltage amplitude in a manner similar to that described earlier with respect to Figure 3B. However, in contrast to the protection device 80 of Figure 3B, the protection device 120 of Figure 6B further includes the second and third gate regions 127b, 127c disposed over the third p-well 82c. Including the second and third gate regions 127b, 127c enhances the turn-on speed of the protection device 120 of Figure 6B relative to the turn-on speed of the protection device 80 of Figure 3B by providing an additional path for carriers to reach the third and fifth n-type active areas 125c, 125e. In particular, during a transient signal event that is positive with respect to the first pad 61, the first to fourth gates 127a-127d can each be coupled upward, and conduction paths can be provided under and through each of these gate structures to

the third and fifth n-type active areas 125c, 125e. Configuring the protection device 120 to include a dual gate structure in which gates are provided on both sides of the third and fifth n-type active areas 125c, 125e can further enhance carrier injection and device turn-on speed. Additionally, the first to fourth gate regions 127a-127d can include the first to fourth p-type gate regions 127a1-127d1 and the first to fourth n-type gate regions 127a2-127d2, respectively, which can reduce gate resistance by providing a p-n junction diode formation, thereby further reducing the response time at which a lateral conduction path is formed beneath the gate region during a transient overvoltage electrical event.

[0081] Although Figure 6B illustrates one embodiment of the protection device 120, other configurations are possible. For example, in some implementations, the isolation region defined by the n-type isolation layer 89 and the first and fourth n-wells 84a, 84d can be omitted in favor of isolating the protection device 120 from the substrate 81 in other ways. In Figures 6A and 6B, the protection device 120 is symmetrical about the fourth n-type active area 125d. However, persons having ordinary skill in the art will appreciate that the teachings herein are also applicable to asymmetric devices.

[0082] Figure 7 is a cross section view of another embodiment of a protection device 130. The protection device 130 includes the p-type substrate 81, the first to fifth p-wells 82a-82e, the first to fourth n-wells 84a-84d, the oxide regions 88, and the n-type isolation layer 89, which can be as described earlier with respect to Figure 3A. The protection device 130 further includes first to ninth p-type active areas 133a-133i, first to sixth n-type active areas 135a-135f, first to fourth gate oxide layers 136a-136d and first to fourth gate regions 137a-137d. The cross section shows the first and second pads 61, 62 as well as electrical connections within the protection device 130 and to the pads.

[0083] The first and ninth p-type active areas 133a, 133i are disposed in the first and fifth p-wells 82a, 82e, respectively. The second and eighth p-type active areas 133b, 133h are disposed in the second and fourth p-wells 82b, 82d, respectively. The first and sixth n-type active areas 135a, 135f are disposed in the first and fourth n-wells 84a, 84d, respectively.

[0084] The first and fourth gate oxide layers 136a, 136d are disposed on the surface 90 of the substrate 81 over the second and third n-wells 84b, 84c, respectively. The first and fourth gate regions 137a, 137d are disposed over the first and fourth gate

oxide layers 136a, 136d, respectively, and can be polysilicon layers. The fourth p-type active area 133d is disposed on a first side of the first gate region 137a, and includes a first portion disposed in the second n-well 84b and a second portion disposed in the third p-well 82c. The second n-type active area 135b is disposed in the second n-well 84b on a second side of the first gate region 137a. The third p-type active area 133c is disposed in the second n-well 84b on a side of the second n-type active area 135b opposite the first gate region 137a. The sixth p-type active area 133f is disposed on a first side of the fourth gate region 137d, and includes a first portion disposed in the third n-well 84c and a second portion disposed in the third p-well 82c. The fifth n-type active area 135e is disposed in the third n-well 84c on a second side of the fourth gate region 137d. The seventh p-type active area 133g is disposed in the third n-well 84c on a side of the fifth n-type active area 135e opposite the fourth gate region 137d.

[0085] The second and third gate oxide layers 136b, 136c are disposed on the surface 90 of the substrate 81 over the third p-well 82c. The second and third gate regions 137b, 137c are disposed over the second and third gate oxide layers 136b, 136c, respectively. The fourth p-type active area 133d is disposed on a first side of the second gate region 137b. The third n-type active area 135c is disposed in the third p-well 82c on a second side of the second gate region 137b. The sixth p-type active area 133f is disposed on a first side of the third gate region 137c. The fourth n-type active area 135d is disposed in the third p-well 82c on a second side of the third gate region 137c. The fifth p-type active area 133e is disposed in the third p-well 82c between the third and fourth n-type active areas 135c, 135d.

[0086] The first gate region 137a includes a first p-type gate region 137a1 adjacent the fourth p-type active area 133d and a first n-type gate region 137a2 adjacent the second n-type active area 135b. Additionally, the second gate region 137b includes a second p-type gate region 137b1 adjacent the fourth p-type active area 133d and a second n-type gate region 137b2 adjacent the third n-type active area 135c. Furthermore, the third gate region 137c includes a third p-type gate region 137c1 adjacent the sixth p-type active area 133f and a third n-type gate region 137c2 adjacent the fourth n-type active area 135d. Additionally, the fourth gate region 137d includes a fourth p-type gate region 137d1 adjacent the sixth p-type active area 133f and a fourth n-type gate region 137d2 adjacent the fifth n-type active area 135e.

[0087] The first pad 61 is electrically connected to the third and seventh p-type active areas 133c, 133g. The second pad 62 is electrically connected to the second and eighth p-type active areas 133b, 133h and to the third and fourth n-type active areas 135c, 135d for low trigger operation, while other configurations can be used for higher trigger voltage operation as discussed earlier in connection with Fig. 4. The first and ninth p-type active areas 133a, 133i are electrically connected to the first supply voltage V_1 , which can be, for example, a power-low or ground supply.

[0088] The protection device 130 can protect an IC from a transient electrical event having either positive or negative voltage amplitude in a manner similar to that described earlier with respect to Figure 6B. For example, persons having ordinary skill in the art will appreciate that the protection device 130 of Figure 7 illustrates a complimentary configuration of the protection device 120 of Figure 6 in which the doping polarities of the active areas formed in the second and third n-wells 84b, 84c and the third p-well 82c has been reversed for blocking voltage adjustment. For example, in contrast to the configuration illustrated in Figure 6B which can define a highly doped n-type active to p-well blocking junction, the configuration illustrated in Figure 7 can define a highly doped p-type active to n-well blocking junction. Configuring the protection device in this manner can help protect IC pins in ultra low leakage applications, while maintaining robustness and fast response during transient stress conditions.

[0089] Skilled artisans will appreciate that lateral spacing defined for the different embodiments can be configured to follow minimum design rules of the technology they are fabricated in. Thus, device construction can vary depending on the technology node. For instance, for sub-60 nm technologies, minimum feature spacing between highly doped active regions can be, for example, in the range of about 0.18 μm to about 0.3 μm , for instance about 0.26 μm , and minimum gate length can be in the range of about 0.1 μm to about 0.5 μm , for instance about 0.36 μm .

[0090] Figure 8 is a schematic top plan layout view of a protection device 160 according to one embodiment. The protection device 160 includes a first pad 161a, a second pad 161b, first to third p-wells 162a-162c, and first and second n-wells 164a, 164b. Although only certain structures of the protection device 160 have been illustrated in Figure 8, the protection device 160 can include other structures, such as contacts and metallization, oxide regions, active areas, gate structures, shallow wells,

and/or deep wells. Skilled artisans will appreciate that these details have been omitted from Figure 8 for clarity.

[0091] As shown in Figure 8, the first p-well 162a has been configured as an island, and the first n-well 164a has been configured as a first ring that surrounds and abuts the first p-well 162a. Additionally, the second p-well 162b has been configured as a second ring that surrounds and abuts the first n-well 164a. Furthermore, the second n-well 164b has been configured as a third ring that surrounds and abuts the second p-well 162b. Additionally, the third p-well 162c has been configured as a fourth ring that surrounds, but does not abut, the second n-well 164b. The first pad 161a has been formed over a portion of the first n-well 164a and over a portion of the second p-well 162b. The second pad 161b has been formed over the first p-well 162a. Although Figure 8 illustrates one specific configuration of a protection device, other implementations are possible, such as rounded and single-side configurations adapted to chip-level layout, bonding, and/or packaging constraints can be practiced without departing from the teachings herein. It will be understood that the lines do not need to be straight or parallel.

[0092] The protection device 160 can be configured to provide protection to circuitry electrically connected to the first and second pads 161a, 161b. For example, in one implementation, the first pad 161 is a signal pad and the second pad is a power-low pad that is isolated from power-low pads used to control the electrical potential of the substrate that the protection device 160 is formed in. Although one configuration of the connectivity of the protection device 160 has been described, the protection device 160 can be connected to pads in other ways.

[0093] The protection device 160 of Figure 8 illustrates one example of an annular implementation of the protection devices described herein for low capacitance loading. For example, when the protection device 160 is viewed along the lines 170-170, the protection device 160 can have a similar cross section to the cross sections of the protection devices shown in Figures 3B, 4, 5, 6B, or 7. Accordingly, in certain implementations the first p-well 162a of Figure 8 can correspond to the third p-well 82c of Figures 3A, 3B, 4, 5, 6A, 6B, and 7, the first n-well 164a of Figure 8 can correspond to the second and third n-wells 84b, 84c of Figures 3A, 3B, 4, 5, 6A, 6B, and 7, and the second p-well 162b of Figure 8 can correspond to the second and fourth p-wells 82b, 82d of Figures 3A, 3B, 4, 5, 6A, 6B, and 7. Furthermore, the second n-well 164b of Figure 8

can correspond to the first and fourth n-wells 84a, 84d of Figures 3A, 3B, 4, 5, 6A, 6B, and 7, and the third p-well 162c of Figure 8 can correspond to the first and fifth p-wells 82a, 82e of Figures 3A, 3B, 4, 5, 6A, 6B, and 7.

[0094] As described above, the correspondence between wells of the protection device 160 of Figure 8 and the wells of the protection devices shown in Figures 3A, 3B, 4, 5, 6A, 6B, and 7 need not be one-to-one. For example the first n-well 164a of Figure 8 can be a ring that surrounds the first p-well 162a, and thus the first n-well 164a can operate as both the second and third n-wells 84b, 84c shown in Figures 3A, 3B, 4, 5, 6A, 6B, and 7. Configuring one or more wells as rings can help improve the current handling capability and/or reduce the footprint of the protection device.

[0095] In one embodiment, the footprint of the protection device 160 in sub 60-nm scale feature technology has a width W_1 in the range of about 35 μm to about 170 μm , for example, about 40 μm for sub 300 fF capacitive loading range, and a length W_2 in the range of about 10 μm to about 20 μm , for example, about 14 μm . However, other dimensions will be readily determined by one of skill in the art and process technology features.

[0096] Figures 9A-9E are graphs of laboratory demonstrating data for one implementations of the protection device 80 of Figures 3A and 3B. The graphs correspond to a configuration of the protection device 80 developed in a 180 nm CMOS process, capable of sustaining over 4 kV human body model (HBM), and having an area of about $74 \times 25 = 1850 \mu\text{m}^2$ including the device guard ring structures. Although Figures 9A-9E illustrate laboratory data for one implementation of the protection device 80, the protection device 80 can be configured to have different electrical characteristics, such as those suited for a particular electronic system or application.

[0097] Figure 9A is a graph 200 of leakage current versus DC voltage. The graph 200 includes three plots of leakage current versus voltage corresponding to laboratory data taken at temperatures of 25 °C, 85 °C, and 125 °C. A relatively small variation of leakage current across DC voltage can indicate the integrity and robustness of a protection device. As shown in Figure 9A, the illustrated embodiment of the protection device can sustain a DC voltage of about 6.5 V for temperatures up to about 125 °C while keeping the leakage below tens of nA at the highest operating temperature.

[0098] Figure 9B is a graph 210 of capacitance versus DC voltage. The graph 210 illustrates that the protection device can be configured to have a relatively small capacitance, such as a capacitance of less than about 300 fF even when configured to sustain over 4 kV HBM. Accordingly, the protection device can be used in various high speed applications, such as to protect signal pads operating at frequencies of up to about 5 GHz.

[0099] Figure 9C is a graph 220 of transmission line pulse (TLP) current versus TLP voltage for a negative transient electrical event. The measurements were taken at about room temperature, and each TLP measurement point can correspond to a voltage and a current measurement obtained by forcing a rectangular 100 ns current pulse having about a 10 ns rise time out of the protection device and measuring the voltage of the protection device between about 40% and about 90% of the current pulse width.

[0100] Figure 9D is a graph 230 of TLP laboratory data for a positive transient electrical event. The measurements were taken at about room temperature, and each TLP measurement point can correspond to a voltage and a current measurement obtained by forcing a rectangular 100 ns current pulse having about a 10 ns rise time into the protection device and measuring the voltage of the protection device between about 40% and about 90% of the current pulse width. The plot of leakage current corresponds to DC leakage at about 6 V after each TLP current pulse. As skilled artisans will appreciate, a relatively small variation in the leakage current value after each pulse can indicate the integrity of the IC. In contrast, drastic change in the leakage current can indicate IC damage. For the illustrated implementation, the protection device can have a trigger voltage of about 4.5 V and a holding voltage of about 2.5 V. Additionally, the leakage current of the protection device can be below about 100 pA at voltages as high as 6 V. Thus, the leakage current of the protection device and standing power dissipation can be relatively low and extend the battery lifetime in portable applications, and can have a relatively small variation across TLP current. This can indicate the integrity and robustness of the IC using the protection device after passage of transient electrical events.

[0101] Figure 9E illustrates a first graph 241 of voltage and current versus time and a second graph 242 of voltage and current versus time. The first graph 241 includes a first plot 245 of voltage versus time and a second plot 246 of current versus

time. A portion 243 of the first graph 241 has been expanded to form the second graph 242. The first and second graphs 241, 242 illustrate transient voltage and current versus time when a TLP stress condition correlating an HBM ESD event of about 5 kV is applied between the two pads of the device. The pulse starts at time 0 ns and ending at time 100 ns.

[0102] As shown in Figure 9E, the protection device can be configured to have a relatively fast response turn-on time. For example, the protection device has been configured to limit the voltage overshoot to about 12 V, and to have an activation time t_1 that is in the range of about 2 ns. In the illustrated configuration, the protection device provides a protection current of over 4 A of TLP current.

[0103] Figures 10A-10C are graphs of laboratory data for one implementation of the protection device 100 of Figure 4. The graphs correspond to a configuration of the protection device 100 developed in a 180 nm CMOS process, capable of sustaining over 4 kV human body model (HBM), and having an area of about $74 \times 25 = 1850 \mu\text{m}^2$ including the device guard ring structures. Although Figures 10A-10C illustrate laboratory data for one implementation of the protection device 100, the protection device 100 can be configured to have different electrical characteristics, such as those suited for a particular low capacitance, high ESD robustness and/or high voltage tolerant electronic system or application.

[0104] Figure 10A is a graph 250 of leakage current versus DC voltage. The graph 250 includes two corner temperature operation plots of leakage current versus voltage corresponding to laboratory data taken at temperatures of 25 °C and 125 °C. As shown in Figure 10A, the illustrated embodiment of the protection device can sustain a DC blocking voltage of about 9 V for temperatures up to about 125 °C. In contrast to the DC plots of Figure 9A, the DC breakdown voltage of the protection device increases for higher temperatures. This is caused by PNP bipolar transistor structures being connected to the pads rather than being used in open-base configurations. Accordingly, such structures control can be dominated by the reverse junction breakdown of the collector-base junctions of NPN bipolar transistor structures rather than by cross-coupled bipolar transistor action.

[0105] Figure 10B is a graph 260 of TLP laboratory data for a positive transient electrical event. The measurements were taken at about room temperature, and

each TLP measurement point can correspond to a voltage and a current measurement obtained by forcing a rectangular 100 ns current pulse having about a 10 ns rise time into the protection device and measuring the voltage of the protection device between about 40% and about 90% of the current pulse width. The plot of leakage current corresponds to DC leakage at about 6 V after each TLP current pulse. For the illustrated implementation, the protection device can have a trigger voltage of about 10 V and a holding voltage of about 2.5 V. Additionally, the leakage current of the protection device can be below about 10pA at voltages as high as 7V, allowing for ultra low leakage operation and higher voltage tolerant circuit input/output interface operation.

[0106] Figure 10C illustrates a first graph 271 of voltage and current versus time and a second graph 272 of voltage and current versus time. The first graph 271 includes a first plot 275 of voltage versus time and a second plot 276 of current versus time. A portion 273 of the first graph 271 has been expanded to form the second graph 272. The first and second graphs 271, 272 illustrate transient voltage and current versus time when a TLP stress condition corresponding to an HBM ESD event of about 5 kV is applied between two pads of the device. The pulse starts at time 0 ns and ending at time 100 ns.

[0107] As shown in Figure 10C, the protection device can be configured to have a relatively fast response turn-on time. For example, the protection device has been configured to limit the voltage overshoot to about 12 V, and to have an activation time t_2 that is in the range of about 2 ns when a high stress current is applied between the pads of the device. In the illustrated configuration, the protection device provides a protection current of over 5 A.

[0108] In contrast to the plots illustrated in Figures 9A-9E, the plots illustrated in Figures 10A-10C do not include plots of capacitance versus DC voltage and TLP current versus TLP voltage for a negative transient electrical event. Since the range and tendency of the specific laboratory data for the implementation of the protection device 100 associated with Figures 10A-10C provided similar results to those previously illustrated in Figures 9B and 9C, these details have been omitted for clarity.

[0109] While illustrated in the context of a p-type semiconductor substrate, the principles and advantages described herein are also applicable to an n-type configuration where the doping polarities are reversed. For example, an n-type substrate can be

provided rather than a p-type substrate, and wells and active areas of an opposite doping type can be provided in the n-type substrate. Furthermore, certain implementations described herein can be applicable to undoped substrates, such as substrates used in certain silicon-on-insulator (SOI) technologies.

[0110] The foregoing description and claims may refer to elements or features as being “connected” or “coupled” together. As used herein, unless expressly stated otherwise, “connected” means that one element/feature is directly or indirectly connected to another element/feature, and not necessarily mechanically. Likewise, unless expressly stated otherwise, “coupled” means that one element/feature is directly or indirectly coupled to another element/feature, and not necessarily mechanically. Thus, although the various schematics shown in the Figures depict example arrangements of elements and components, additional intervening elements, devices, features, or components may be present in an actual embodiment (assuming that the functionality of the depicted circuits is not adversely affected).

Applications

[0111] Devices employing the above described schemes can be implemented into various electronic devices. Examples of the electronic devices can include, but are not limited to, consumer electronic products, parts of the consumer electronic products, electronic test equipment, etc. Examples of the electronic devices can also include memory chips, memory modules, circuits of optical networks or other communication networks, and disk driver circuits. The consumer electronic products can include, but are not limited to, a mobile phone, a telephone, a television, a computer monitor, a computer, a hand-held computer, a personal digital assistant (PDA), a microwave, a refrigerator, an automobile, a stereo system, a cassette recorder or player, a DVD player, a CD player, a VCR, an MP3 player, a radio, a camcorder, a camera, a digital camera, a portable memory chip, a washer, a dryer, a washer/dryer, a copier, a facsimile machine, a scanner, a multi functional peripheral device, a wrist watch, a clock, etc. Further, the electronic device can include unfinished products, including those for industrial, medical and automotive applications.

[0112] Although this invention has been described in terms of certain embodiments, other embodiments that are apparent to those of ordinary skill in the art,

including embodiments that do not provide all of the features and advantages set forth herein, are also within the scope of this invention. Moreover, the various embodiments described above can be combined to provide further embodiments. In addition, certain features shown in the context of one embodiment can be incorporated into other embodiments as well. Accordingly, the scope of the present invention is defined only by reference to the appended claims.

WHAT IS CLAIMED IS:

1. An apparatus for providing protection from transient electrical events, the apparatus comprising:

a semiconductor substrate;

a first well disposed in the semiconductor substrate;

a second well disposed in the semiconductor substrate adjacent the first well, wherein the second well has a doping type opposite a doping type of the first well;

a first gate structure disposed over the second well;

a first active region disposed on a first side of the first gate structure along a boundary of the first and second wells;

a second active region disposed on a second side of the first gate structure in the second well, wherein the second active region has a doping type opposite a doping type of the first active region; and

a third active region disposed in the first well, wherein the third active region has a doping type the same as the doping type of the first active region;

wherein during a transient overvoltage stress event the apparatus is configured to provide a first conduction path under the first gate structure and a second conduction path through the first gate structure to decrease a turn-on response time and reduce a transient breakdown voltage between the first and second wells during the transient overvoltage stress event.

2. The apparatus of claim 1, wherein the first well is p-type doped, the second well is n-type doped, the first active region is n-type doped, the second active region is p-type doped, and the third active region is n-type doped.

3. The apparatus of claim 2, wherein the first gate structure comprises a p-type doped poly-crystalline gate region adjacent the second active region and an n-type doped poly-crystalline gate region adjacent the first active region.

4. The apparatus of claim 2, further comprising a fourth active region in the second well on a side of the second active region opposite the first gate structure, wherein the fourth active region is n-type doped.

5. The apparatus of claim 4, further comprising a third well disposed in the semiconductor substrate and a fifth active region disposed in the third well, wherein the fifth active region is p-type doped, and wherein the third well is p-type doped and disposed on a side of the second well opposite the first well.

6. The apparatus of claim 5, further comprising a first pad and a second pad disposed over the semiconductor substrate, wherein the first pad is electrically connected to the second active region and the second pad is electrically connected to the third active region and to the fifth active region.

7. The apparatus of claim 6, further comprising a sixth active region in the first well, wherein the sixth active region is p-type doped.

8. The apparatus of claim 7, further comprising a second gate structure over the first well, wherein the sixth active region is disposed between the first active region and the third active region, and wherein the second gate structure is disposed between the first active region and the sixth active region.

9. The apparatus of claim 7, wherein the sixth active region is disposed on a side of the third active region opposite the first active region, wherein the second pad is further connected to the sixth active region and the first pad is further connected to the fourth active region.

10. The apparatus of claim 5, wherein the second well is configured as a first ring that surrounds the first well, and wherein the third well is configured as a second ring that surrounds the second well.

11. The apparatus of claim 10, further comprising an isolation region enclosing the first well, the second well, and the third well, wherein the isolation region is n-type doped.

12. The apparatus of claim 11, further comprising a fourth well surround the third well, wherein the fourth well is n-type doped.

13. The apparatus of claim 12, wherein the second well, the fourth well, and the n-type doped isolation region are electrically floating.

14. The apparatus of claim 1, wherein the first well is p-type doped, the second well is n-type doped, the first active region is p-type doped, the second active region is n-type doped, and the third active region is p-type doped.

15. The apparatus of claim 14, further comprising a fourth active region in the second well on a side of the second active region opposite the first gate structure, wherein the fourth active region is p-type doped.

16. The apparatus of claim 15, further comprising a third well disposed in the semiconductor substrate and a fifth active region disposed in the third well, wherein the fifth active region is p-type doped, and wherein the third well is p-type doped and disposed on a side of the second well opposite the first well.

17. The apparatus of claim 16, further comprising a second gate structure over the first well and a sixth active region in the first well between the first active region and the third active region, wherein the second gate structure is disposed between the first active region and the sixth active region, and wherein the sixth active region is n-type doped.

18. An apparatus for providing protection from transient electrical events, the apparatus comprising:

a semiconductor substrate;

a first well disposed in the semiconductor substrate;

a second well disposed in the semiconductor substrate adjacent the first well, wherein the second well has a doping type opposite a doping type of the first well;

a first means for implant blocking disposed over the second well;

a first active region disposed on a first side of the first implant blocking means along a boundary of the first and second wells;

a second active region disposed on a second side of the first implant blocking means in the second well, wherein the second active region has a doping type opposite a doping type of the first active region; and

a third active region disposed in the first well, wherein the third active region has a doping type the same as the doping type of the first active region;

wherein during a transient overvoltage stress event the apparatus is configured to provide a first conduction path under the first implant blocking means and a second conduction path through the first implant blocking means to decrease a turn-on response time and reduce a transient breakdown voltage between the first and second wells during the transient overvoltage stress event.

19. The apparatus of claim 18, wherein the first well is p-type doped, the second well is n-type doped, the first active region is n-type doped, the second active region is p-type doped, and the third active region is n-type doped.

20. The apparatus of claim 19, further comprising a fourth active region in the second well on a side of the second active region opposite the first implant blocking means, wherein the fourth active region is n-type doped.

21. The apparatus of claim 20, further comprising a third well disposed in the semiconductor substrate and a fifth active region disposed in the third well, wherein the fifth active region is p-type doped, and wherein the third well is p-type doped and disposed on a side of the second well opposite the first well.

22. The apparatus of claim 21, wherein the second well is configured as a first ring that surrounds the first well, and wherein the third well is configured as a second ring that surrounds the second well.

23. The apparatus of claim 22, further comprising an isolation region enclosing the first well, the second well, and the third well, wherein the isolation layer is n-type doped.

24. The apparatus of claim 23, further comprising a fourth well surround the third well, wherein the fourth well is n-type doped.

25. The apparatus of claim 24, further comprising a first pad and a second pad disposed over the semiconductor substrate, wherein the first pad is electrically connected to the second active region and the second pad is electrically connected to the third active region and to the fifth active region.

26. The apparatus of claim 24, wherein the second well, the fourth well, and the n-type doped isolation region are electrically floating.

27. The apparatus of claim 24, further comprising a second means for implant block over the first well and a sixth active region in the first well between the first active region and the third active region, wherein the second implant blocking means is disposed between the first active region and the sixth active region, and wherein the sixth active region is p-type doped.

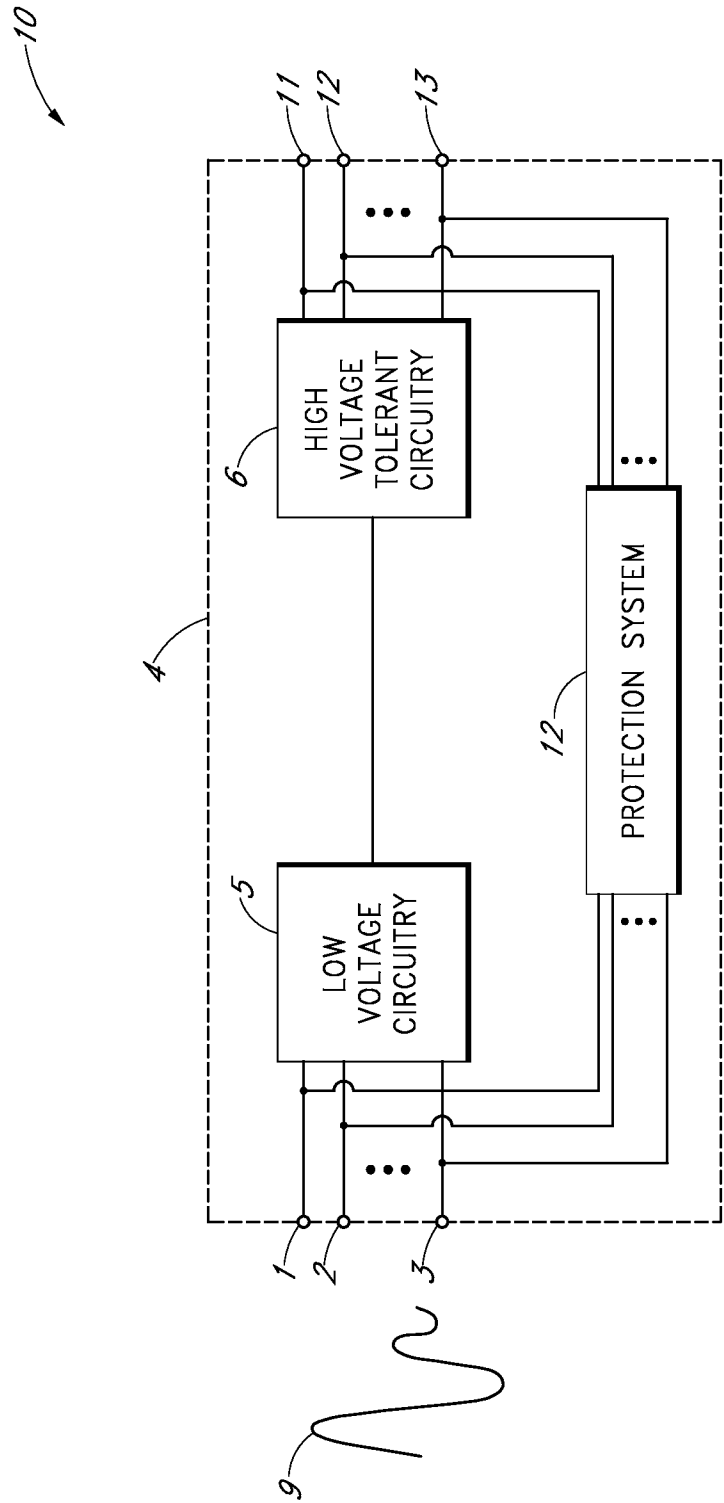


FIG. 1

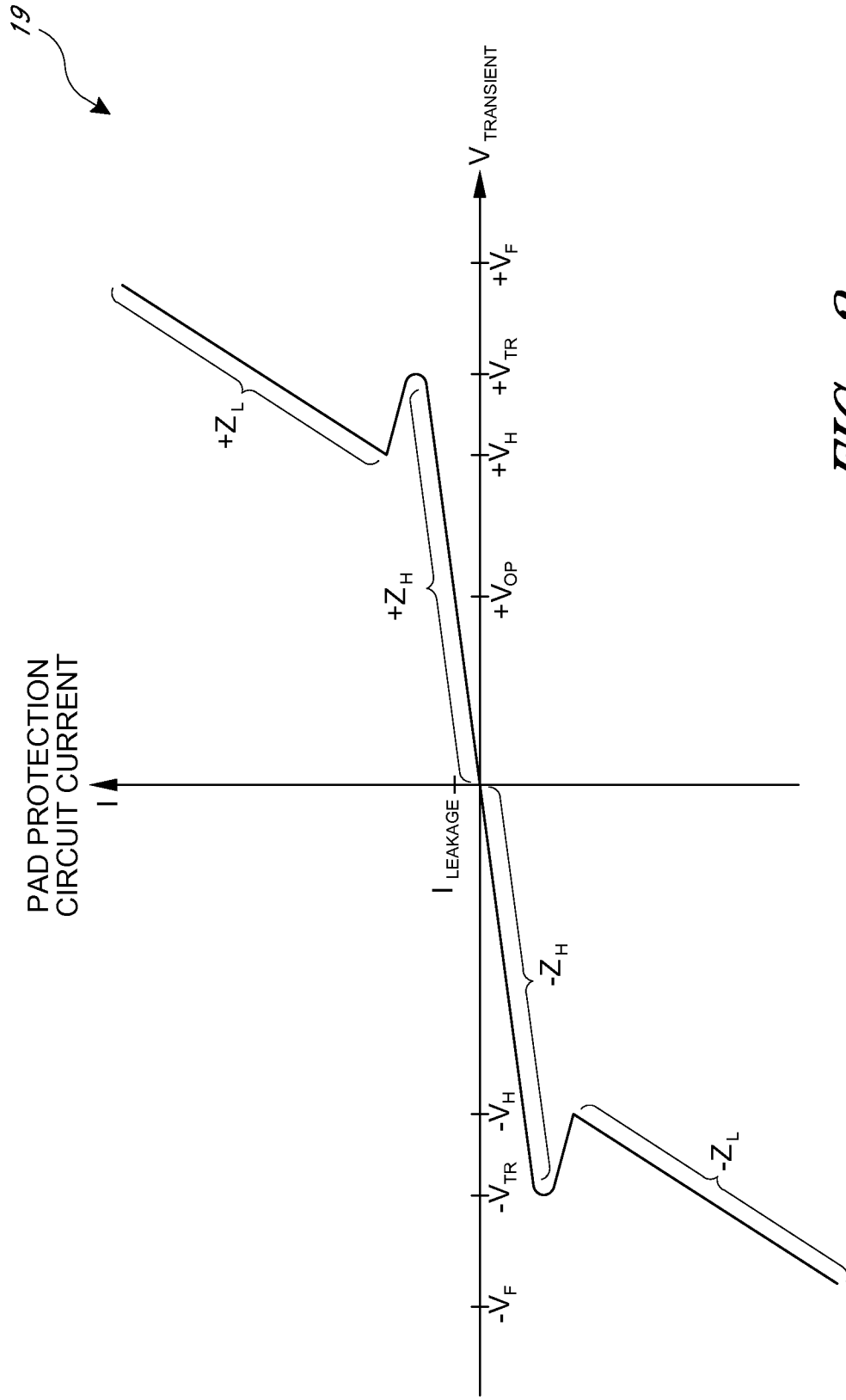


FIG. 2

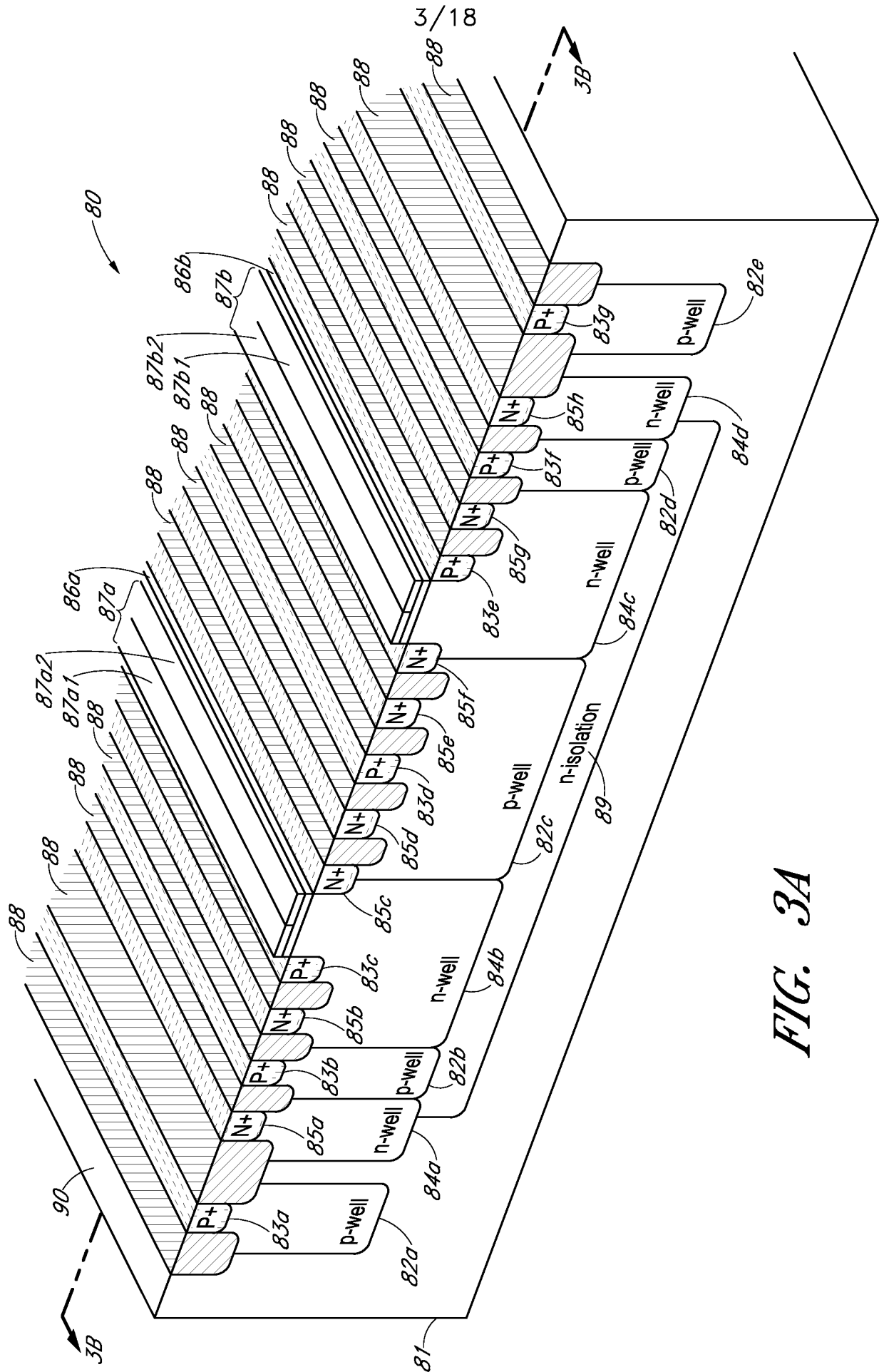
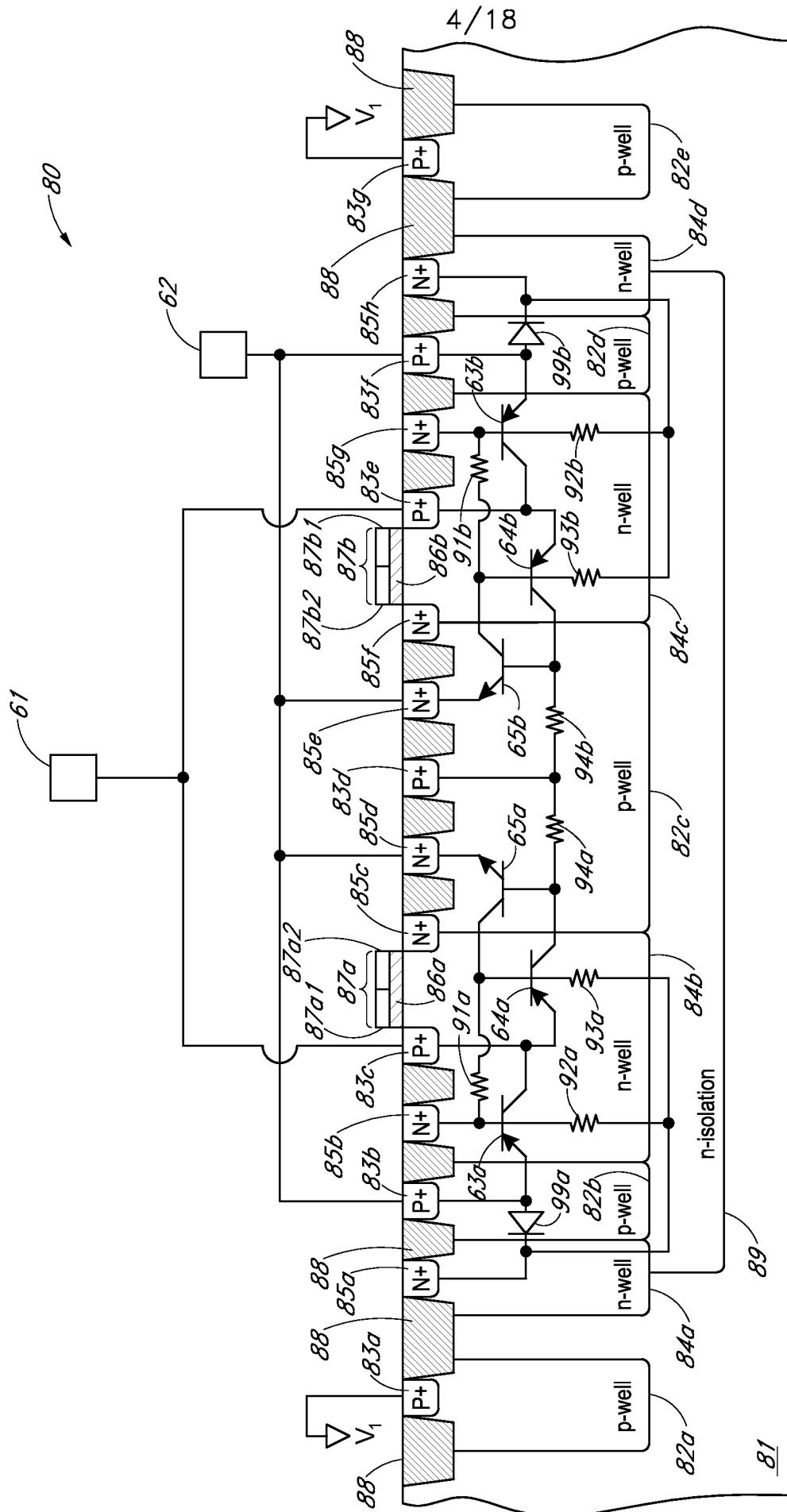


FIG. 3A



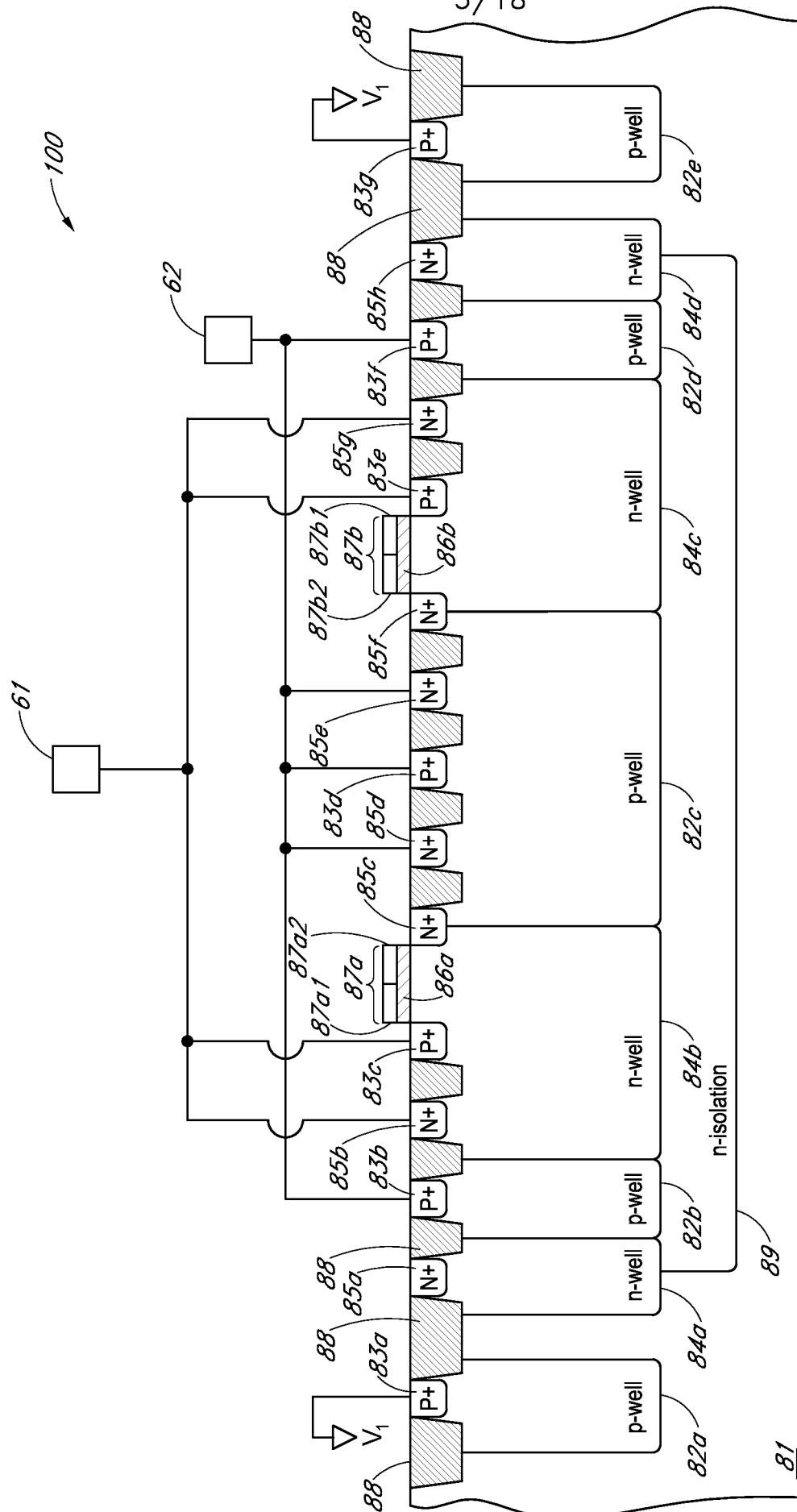


FIG. 4

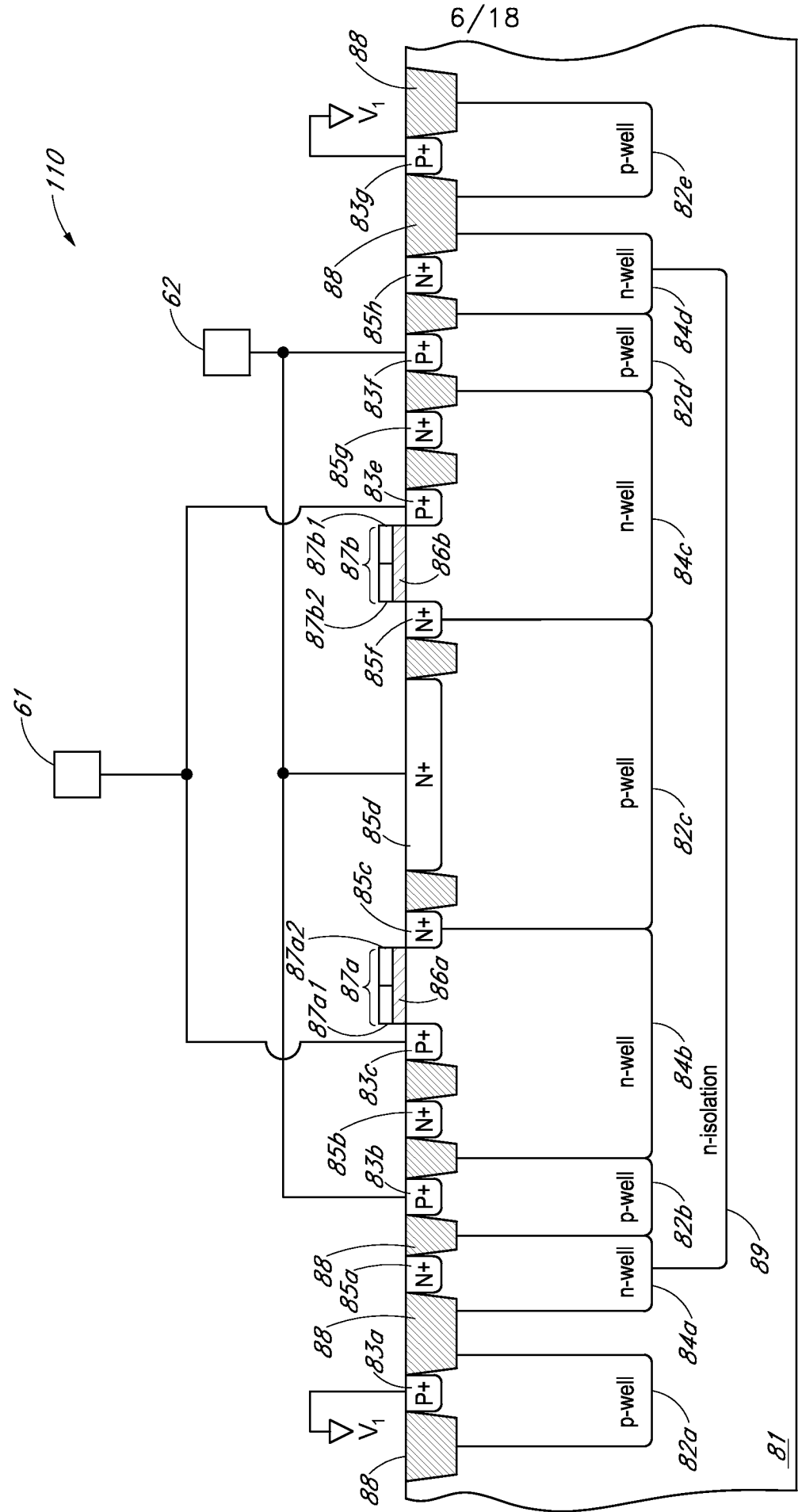
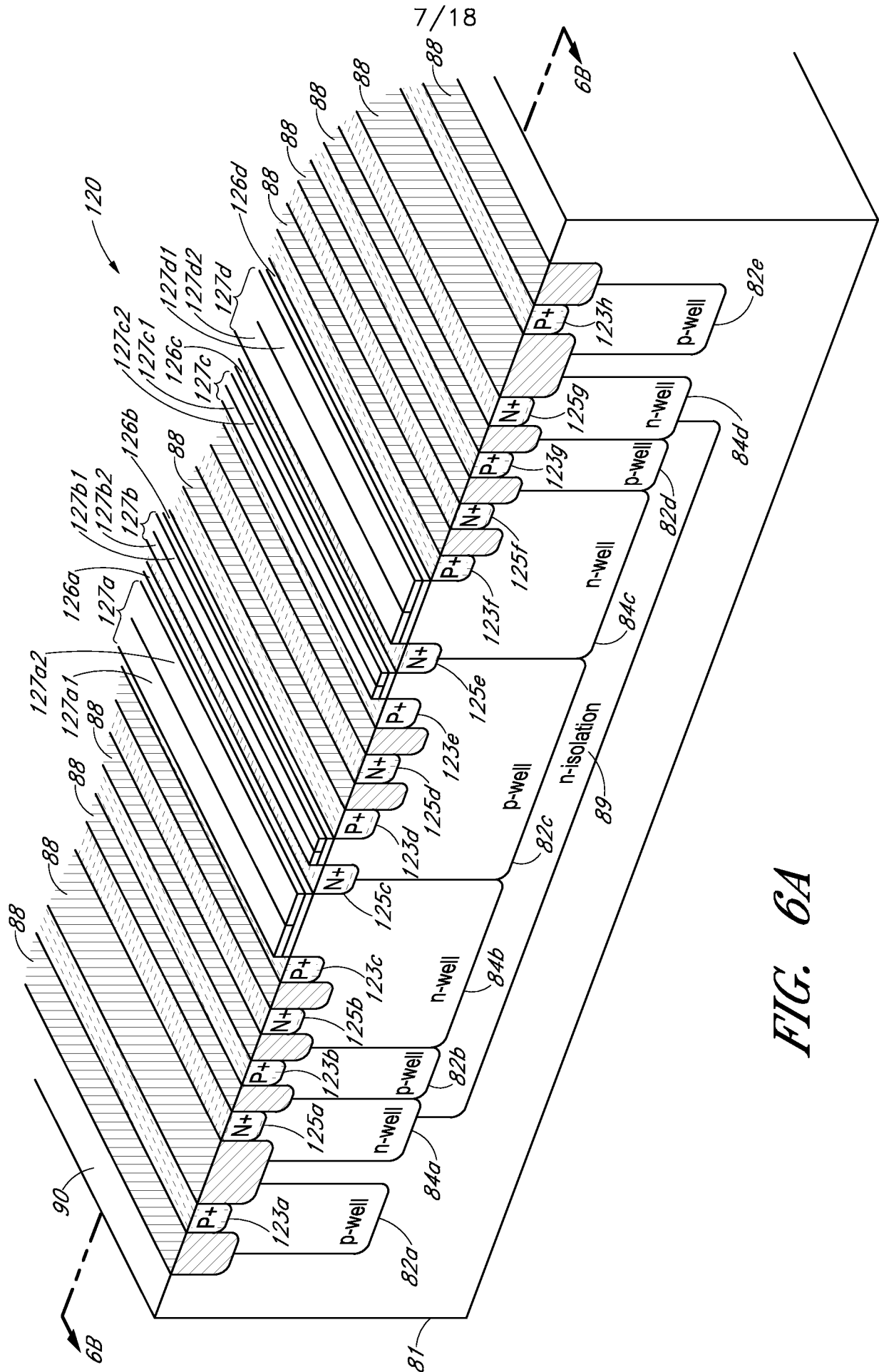


FIG. 5



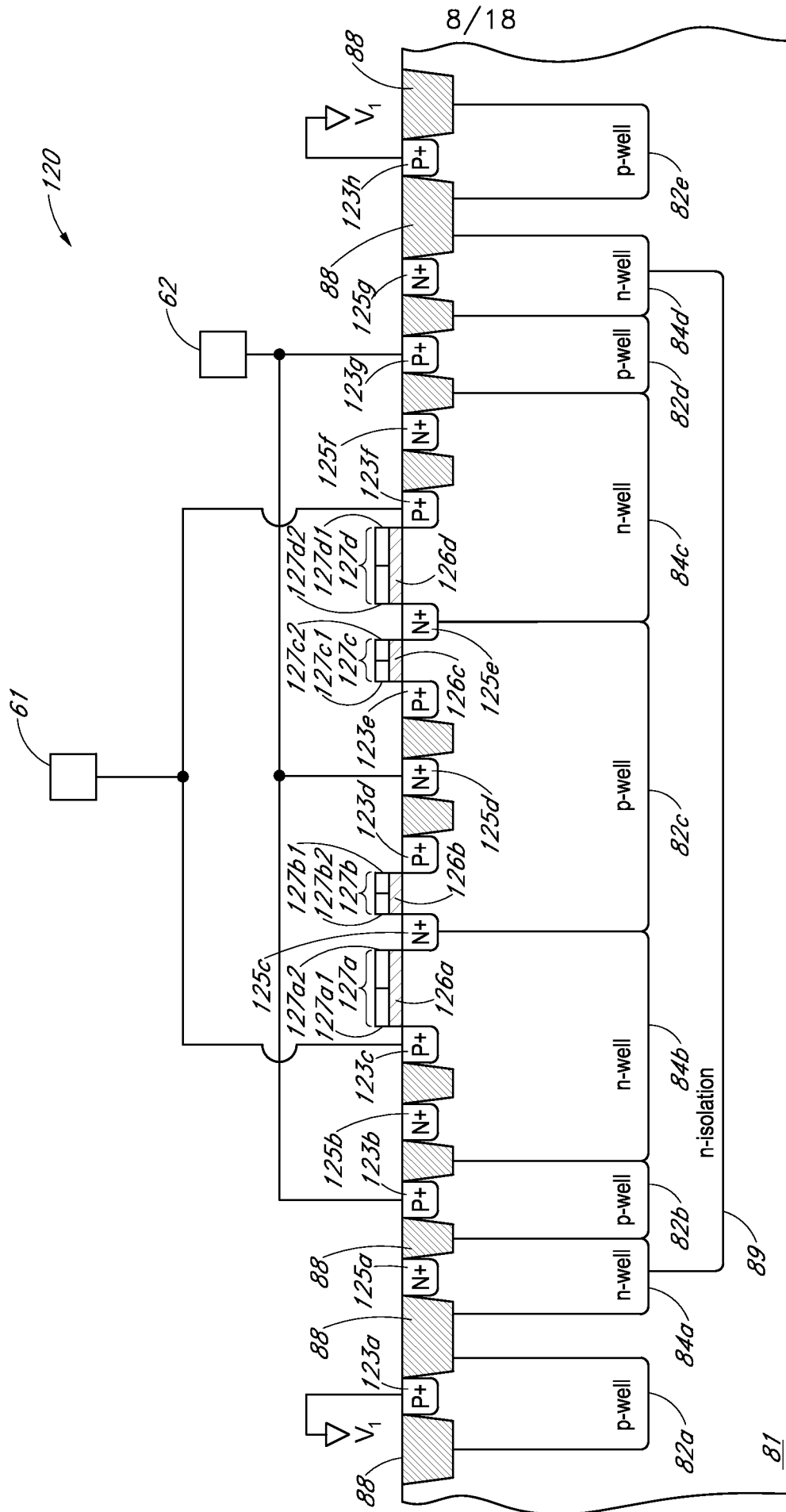


FIG. 6B

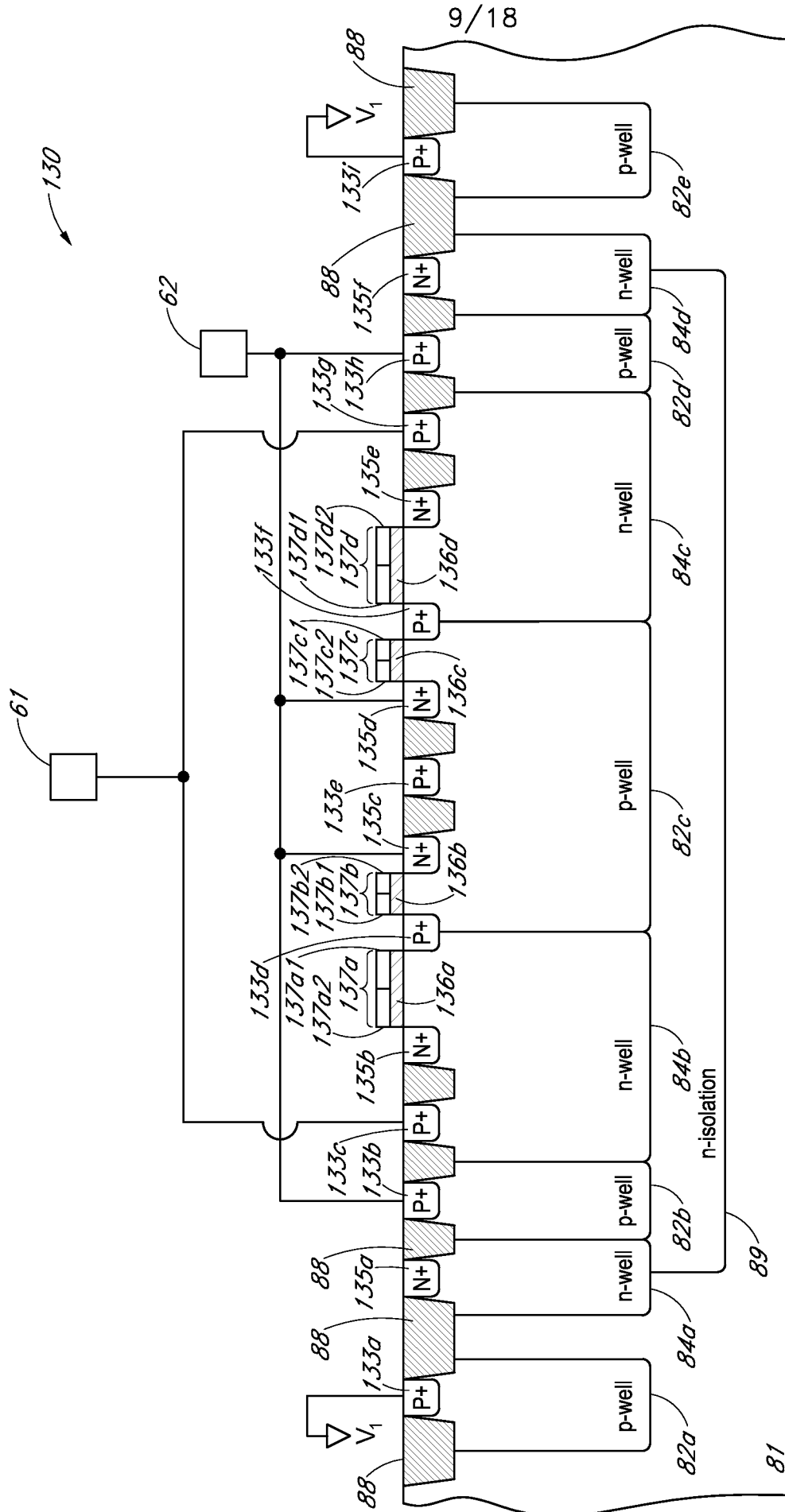


FIG. 7

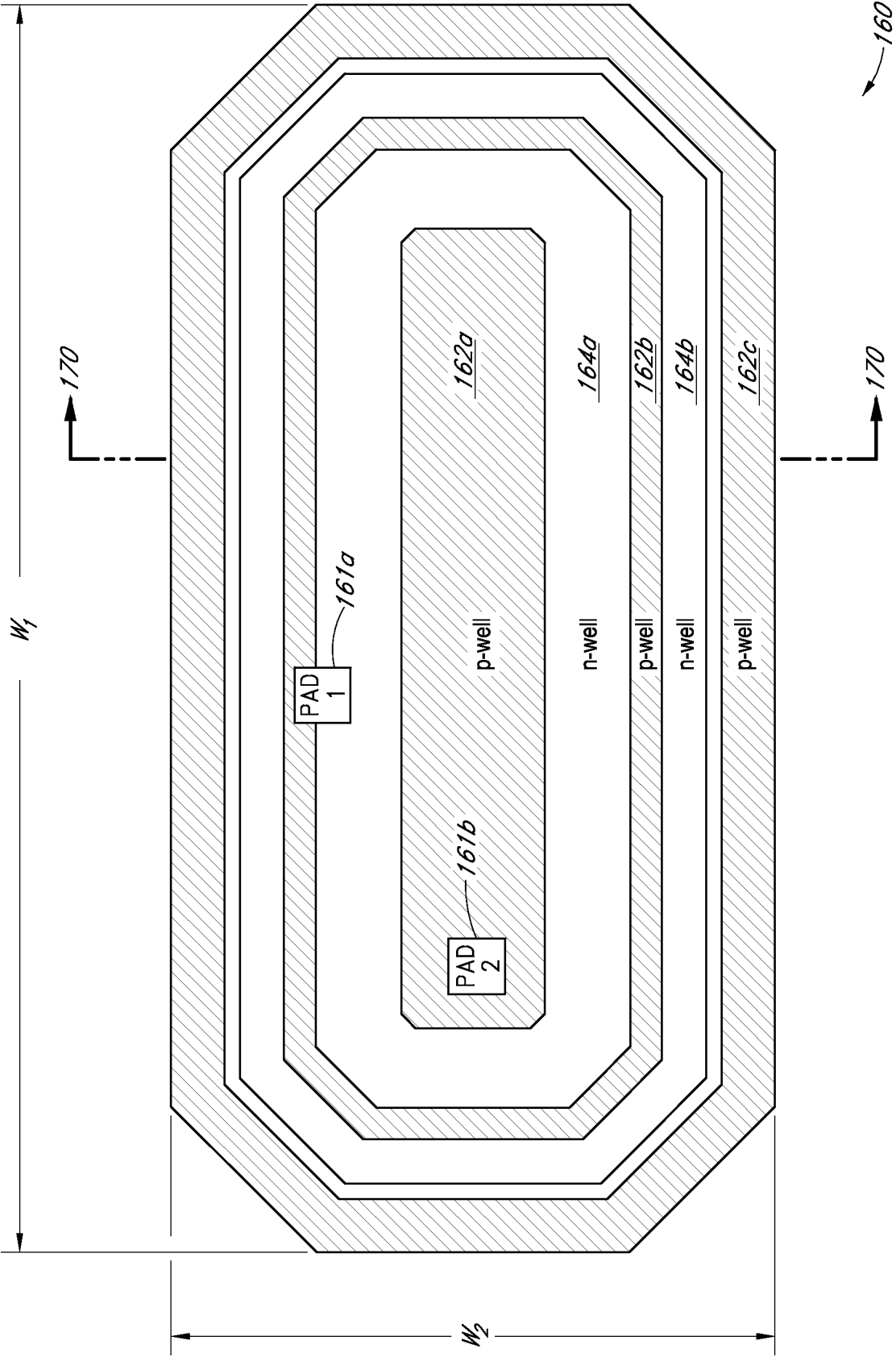


FIG. 8

200

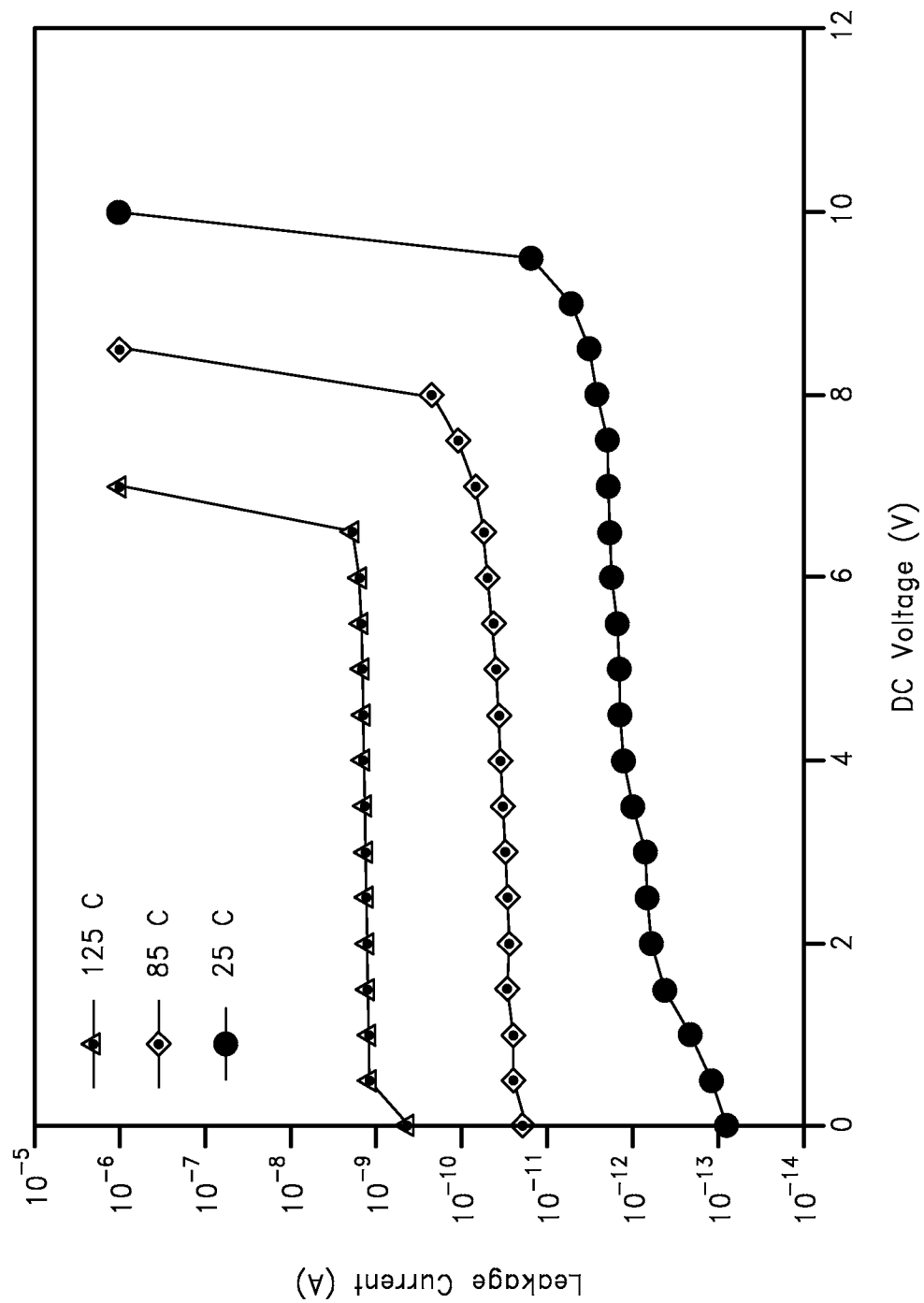


FIG. 9A

210

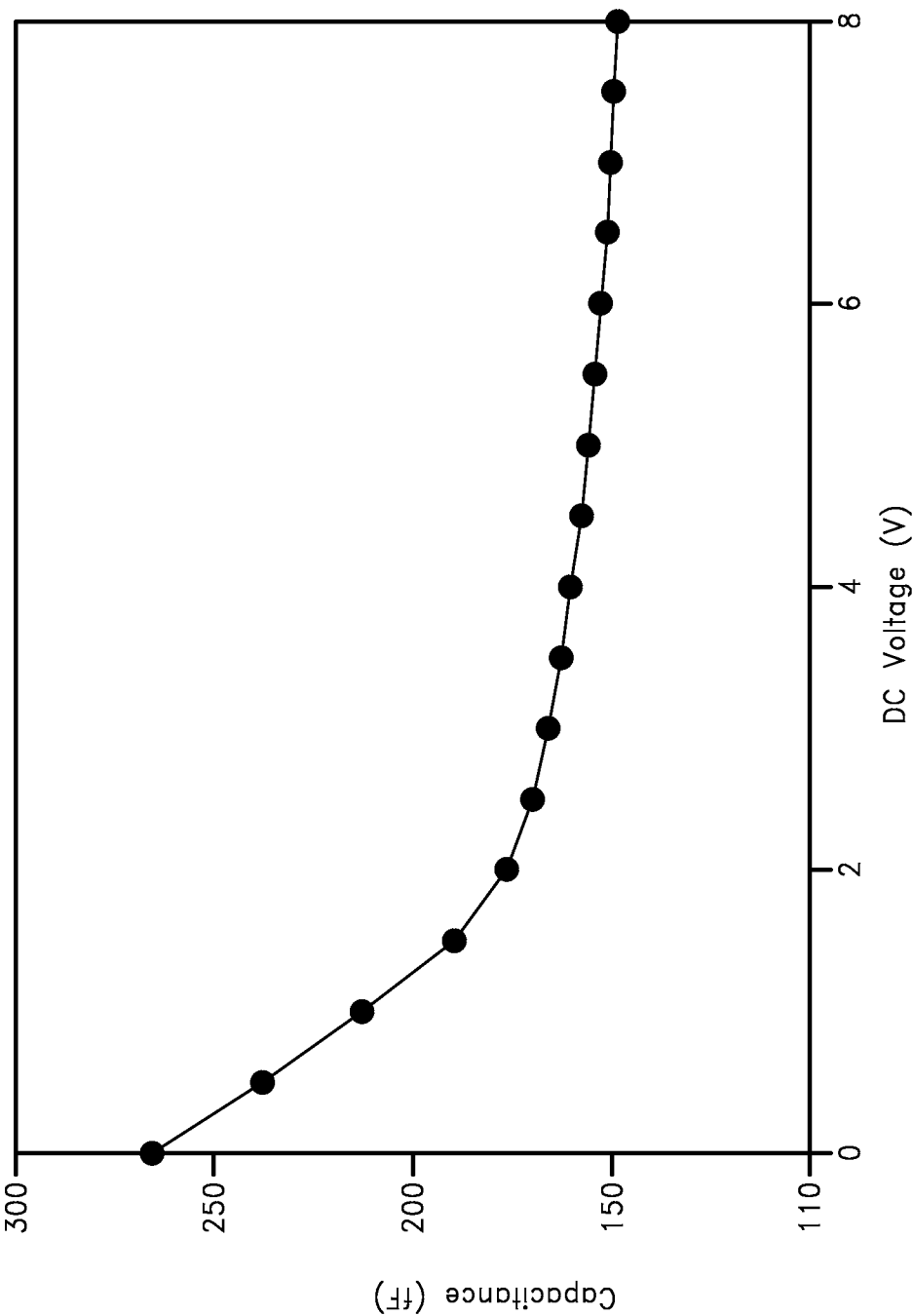


FIG. 9B

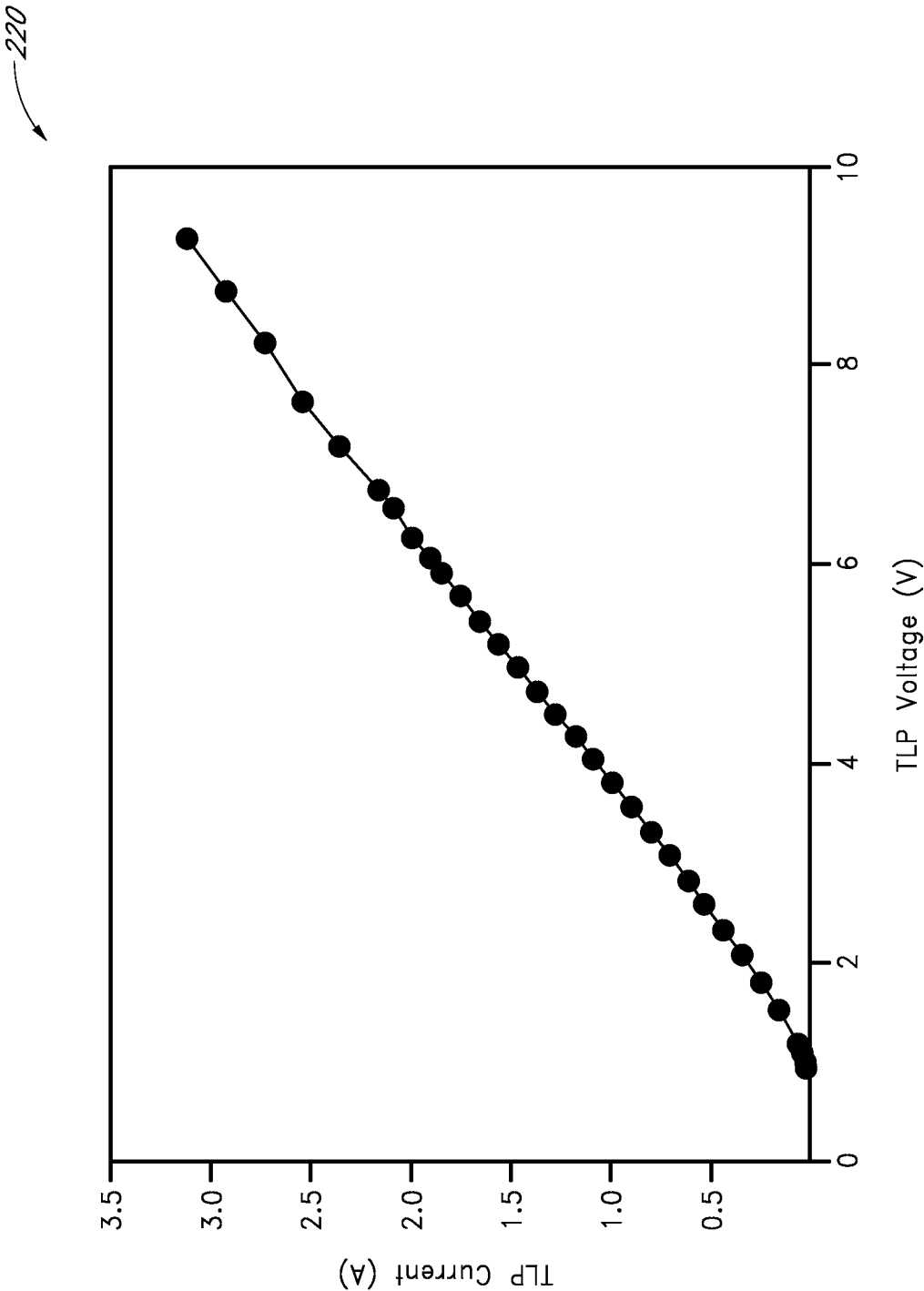
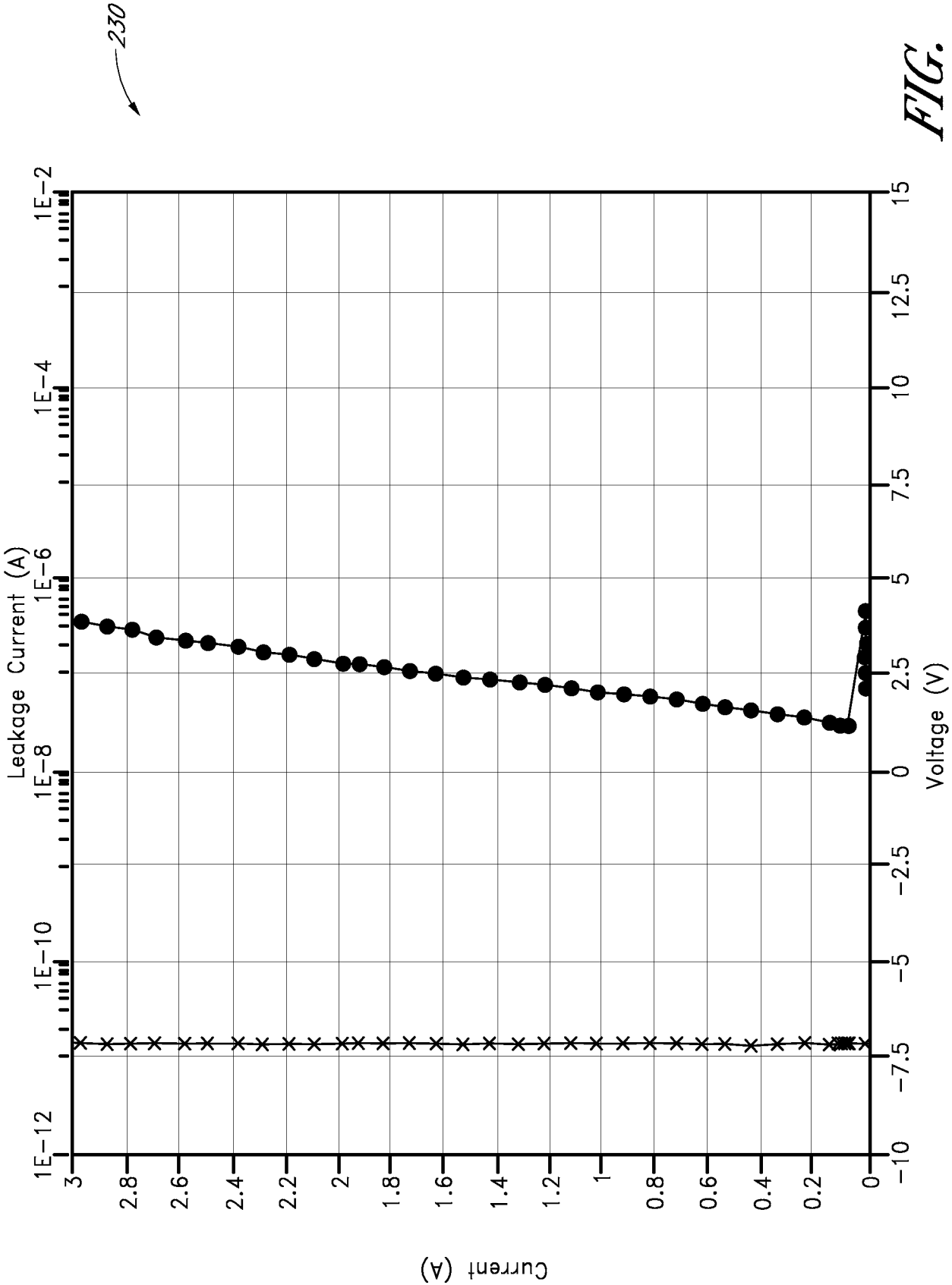
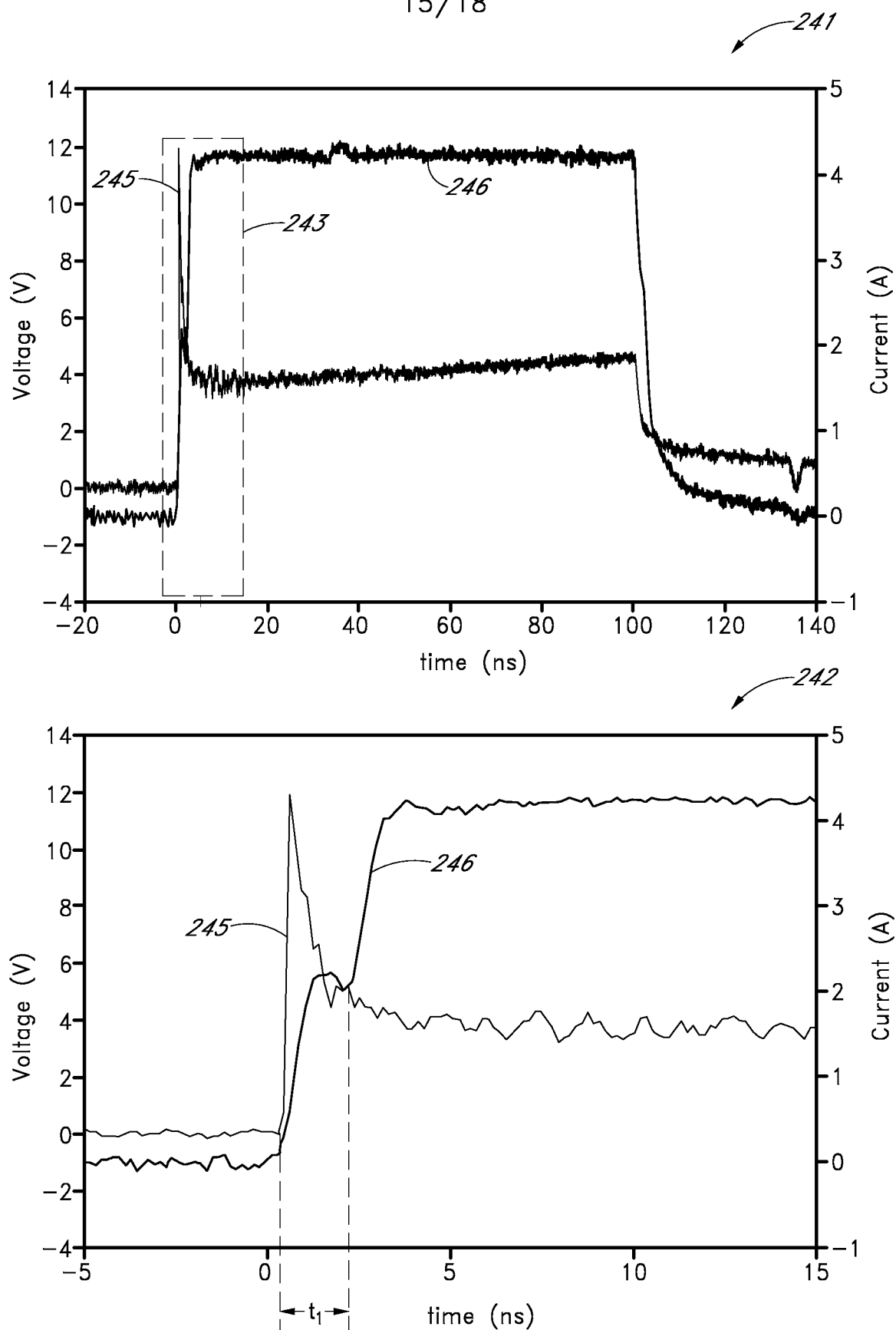


FIG. 9C

FIG. 9D



15/18

*FIG. 9E*

250

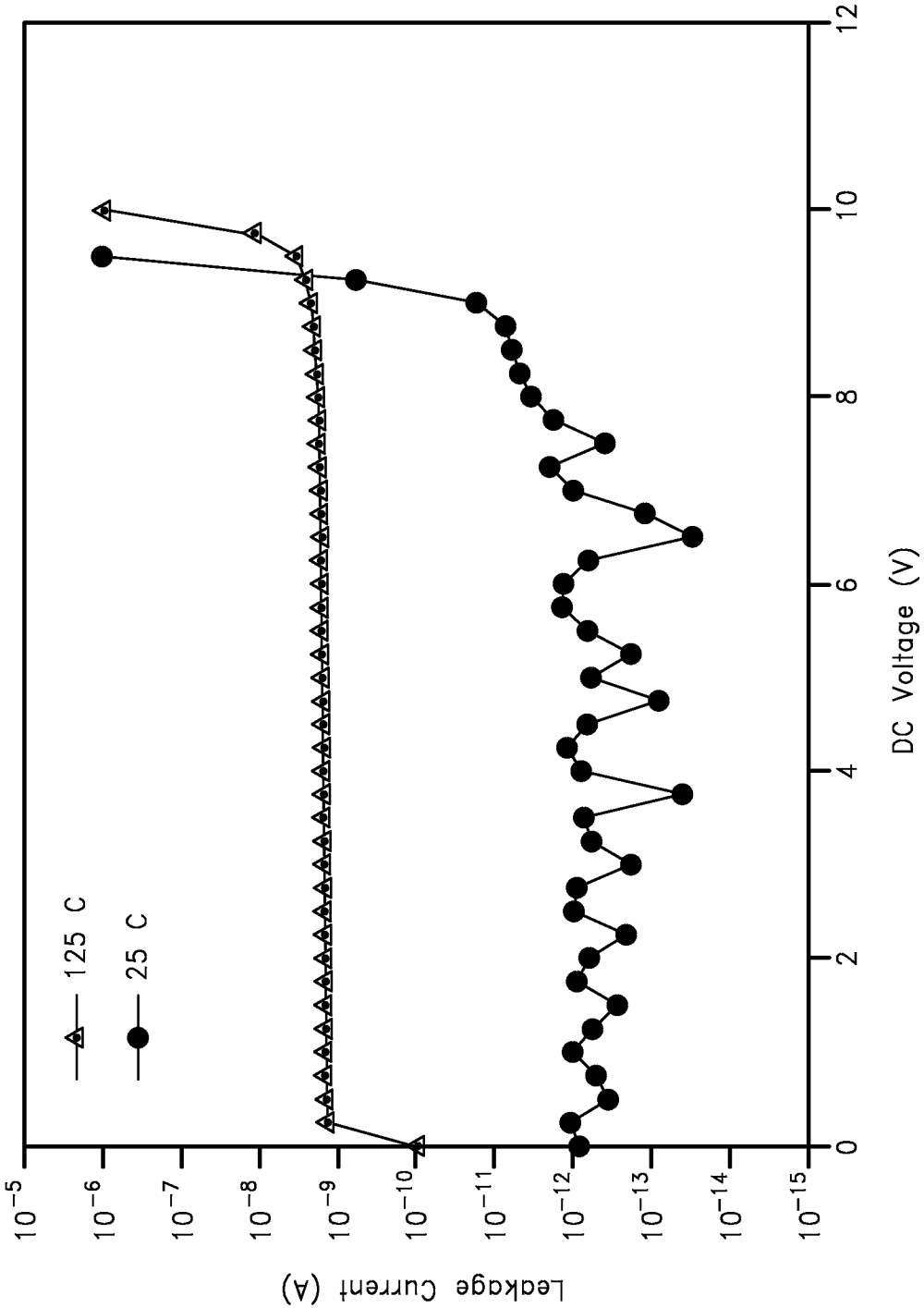


FIG. 10A

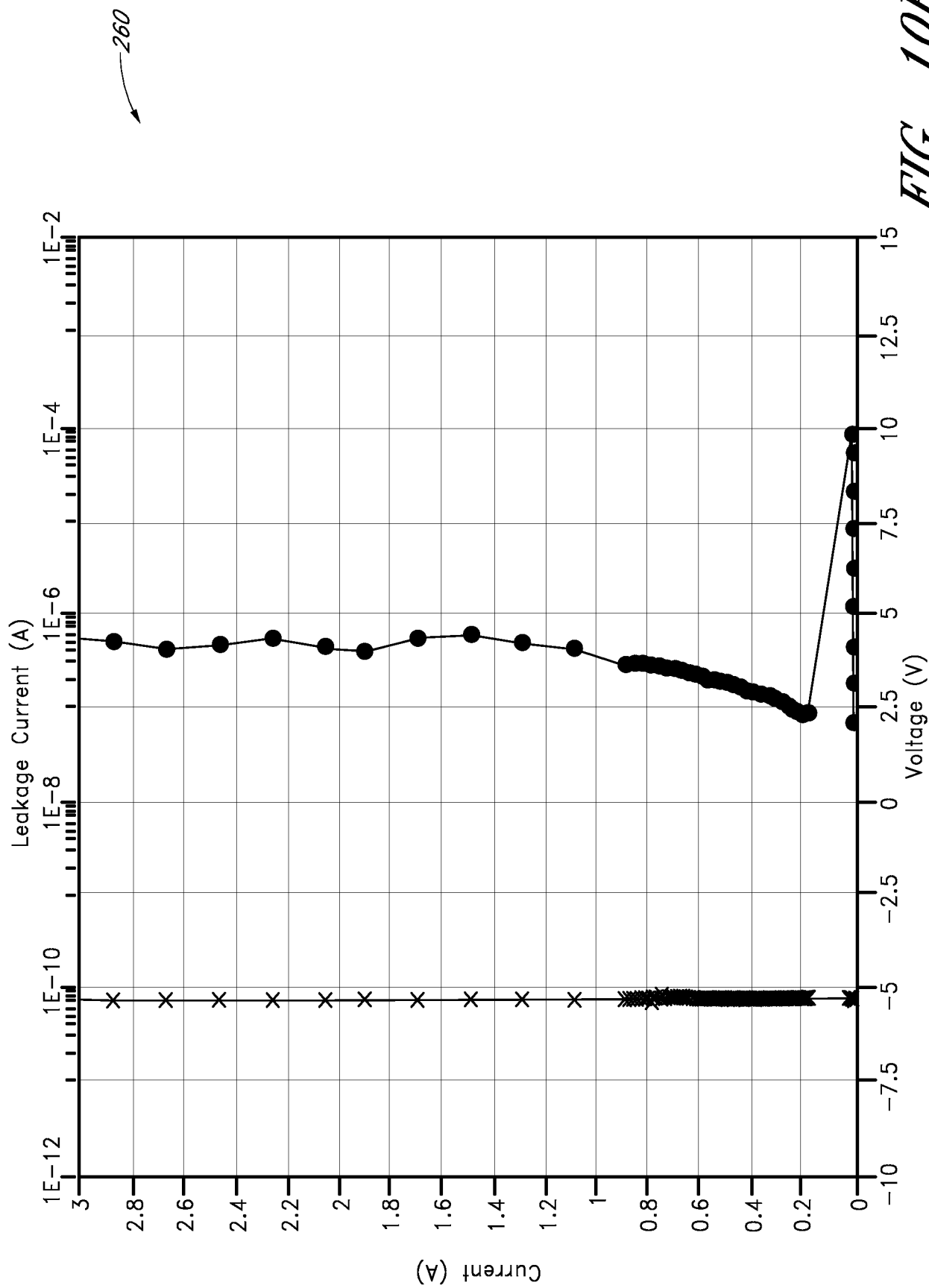


FIG. 10B

18/18

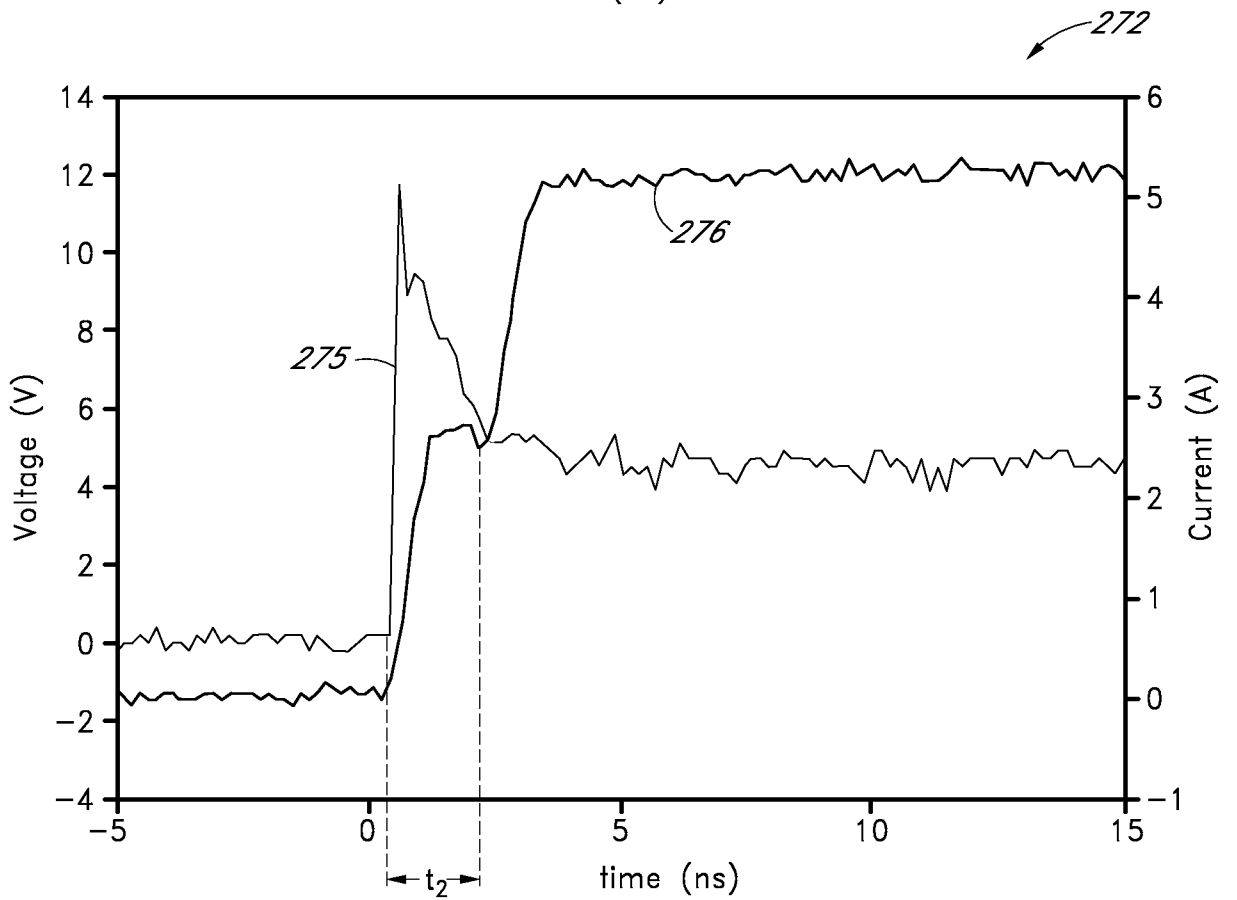
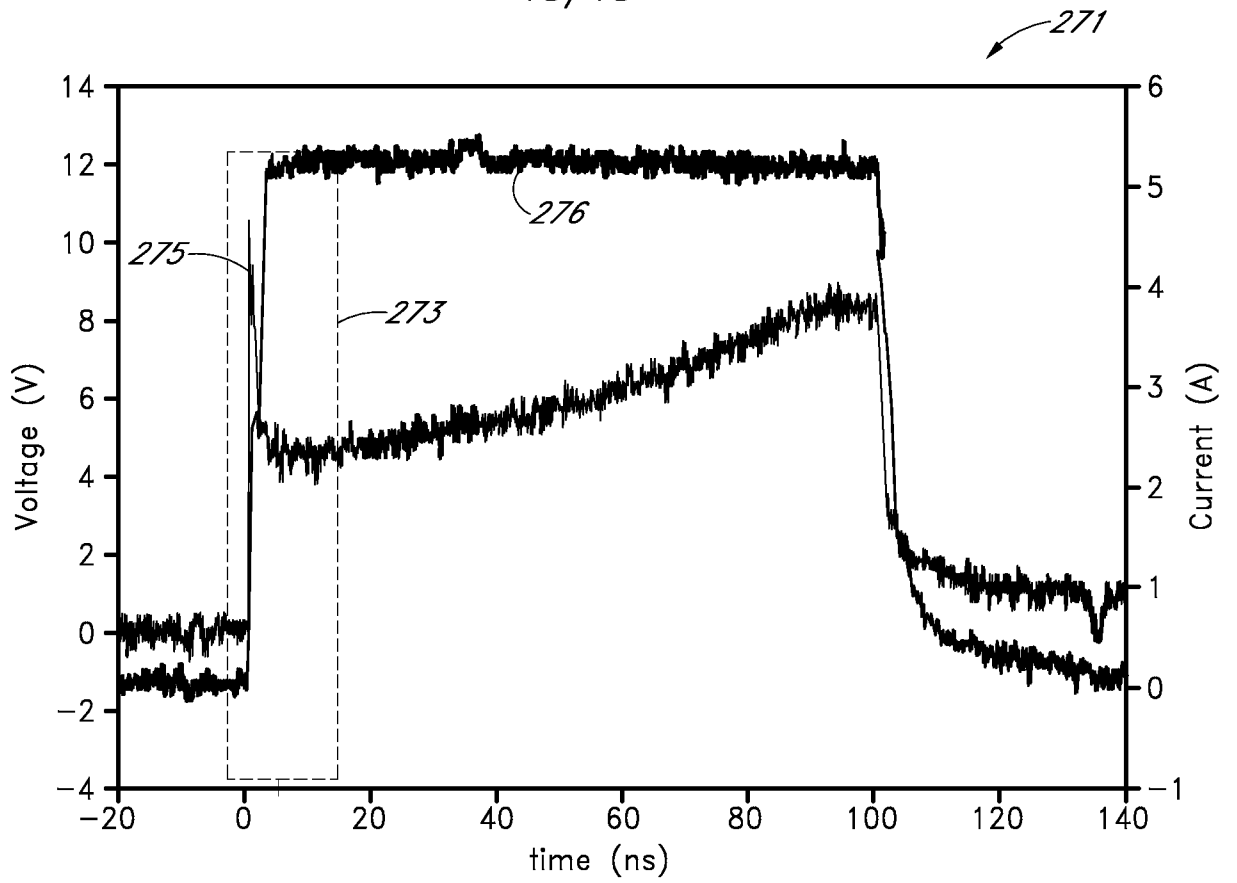


FIG. 10C

A. CLASSIFICATION OF SUBJECT MATTER**H01L 27/04(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 27/04; H01L 29/00; H01L 21/331; H01L 21/8222; H01L 29/78; H01L 29/735

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: transient, electrical, reduce, well, gate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 10-2006-0067100 A (ELECTRONICS AND TELECOMMUNICATIONS RESEARCH INSTITUTE) 19 June 2006 See abstract, pages 3-4 and figure 4.	1-27
A	US 2002-0109190 A1 (KER, MING-DOU et al.) 15 August 2002 See paragraph [0034] and figures 7A-7B.	1-27
A	US 2012-0007207 A1 (SALCEDO, JAVIER A.) 12 January 2012 See abstract, paragraphs [0067]-[0094], [0178]-[0181] and figures 2A-3C, 12.	1-27
A	KR 10-2009-0123683 A (HYNIX SEMICONDUCTOR INC.) 02 December 2009 See abstract, paragraphs [0045]-[0058], claims 1, 17-20 and figures 3-4.	1-27
A	KR 10-2010-0003569 A (INDUSTRY-UNIVERSITY COOPERATION FOUNDATION OF SEOKYEONG UNIVERSITY) 11 January 2010 See abstract, paragraphs [0029]-[0037], claims 1, 7 and figures 1-6.	1-27



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

26 June 2013 (26.06.2013)

Date of mailing of the international search report

27 June 2013 (27.06.2013)

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City,
302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

CHOI, Sang Won

Telephone No. 82-42-481-8291



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/030471

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR 10-2006-0067100 A	19.06.2006	US 2006-0125016 A1 US 2008-0128817 A1 US 7342281 B2 US 7576961 B2	15.06.2006 05.06.2008 11.03.2008 18.08.2009
US 2002-0109190 A1	15.08.2002	US 2002-0163009 A1 US 6498357 B2 US 6806160 B2	07.11.2002 24.12.2002 19.10.2004
US 2012-0007207 A1	12.01.2012	TW 201230295 A WO 2012-005940 A1	16.07.2012 12.01.2012
KR 10-2009-0123683 A	02.12.2009	US 2009-0294855 A1 US 8039899 B2	03.12.2009 18.10.2011
KR 10-2010-0003569 A	11.01.2010	None	