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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G05F 3/02, G01R 31/02

A1

(11) International Publication Number: **WO 99/56190**

(43) International Publication Date: 4 November 1999 (04.11.99)

(21) International Application Number: PCT/US99/08742

(22) International Filing Date: 20 April 1999 (20.04.99)

(30) Priority Data:
09/067,314 27 April 1998 (27.04.98) US

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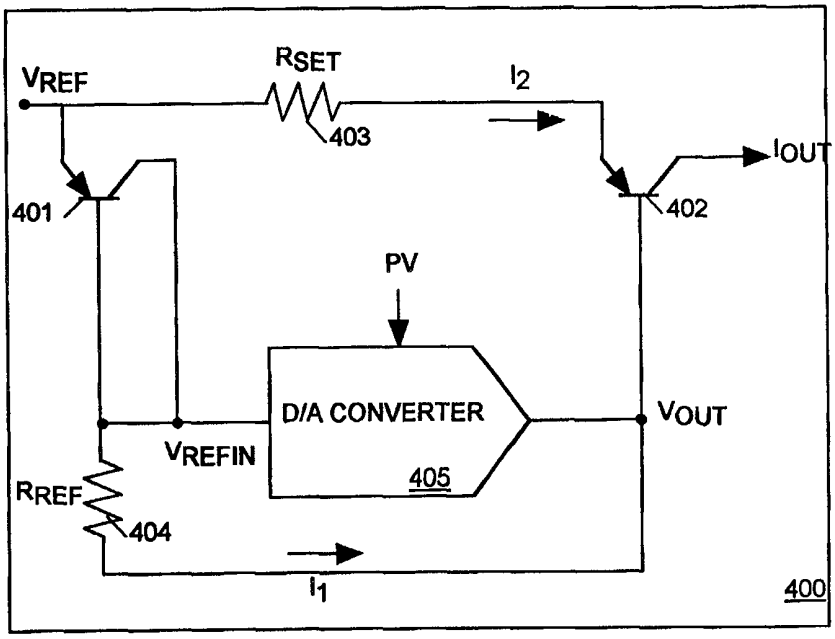
(81) Designated States: JP, KR, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: TEMPERATURE TRACKING VOLTAGE–TO–CURRENT CONVERTER



(57) Abstract

A programmable and precise voltage–to–current converter (i.e. current source) that tracks temperature variations. The voltage–to–current converter is implemented by placing a voltage reference circuit (405) between the bases of two transistors (401 and 402), or alternatively between a diode and a transistor. The voltage controlled current source circuit can be adjusted to track temperature variations. In one embodiment, the voltage reference circuit is a programmable digital–to–analog (D/A) converter. In a second embodiment, the voltage reference circuit is a differential amplifier.

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TEMPERATURE TRACKING VOLTAGE-TO-CURRENT CONVERTER

FIELD OF THE INVENTION

The invention generally relates to signal converters, and more particularly relates to voltage-to-current converters.

BACKGROUND OF THE INVENTION

As part of their quality assurance, semiconductor device makers systematically perform tests on their products to ensure that they meet or exceed all of their design parameters. Among the types of tests routinely performed include device parametric testing (a.k.a. DC testing), device logic function testing, and device timing testing (a.k.a. AC testing). While the semiconductor device being tested is often referred to as the Device Under Test, the test system used in conducting the above tests on the DUT is often referred to as Automatic Test Equipment (ATE).

The ATE is necessarily very precise to carry out the aforementioned tests on very sensitive DUT like semiconductor devices. In general, the ATE hardware is controlled by a computer which executes a test program to present the correct voltages, currents, timings, and functional states to the DUT and monitor the response from the device for each test. The result of each test is then compared to pre-defined limits and a pass/fail decision is made. As such, the ATE hardware normally include a collection of power-supplies, meters, signal generators, pattern generators, etc.

The Pin Electronics (PE) circuitry provides the interface between the ATE and the DUT. More particularly, the PE circuitry supplies input signals to the DUT and receives output signals from the DUT. As an example, in parametric testing, either an input voltage is sent to the DUT and an output current is received from the DUT or an input current is sent to the DUT and an output voltage is received from the DUT. Accordingly, a programmable current source is one of the PE's required components to drive desired currents to the DUT.

Figure 1 illustrates, as an example, a prior art current source used in a PE circuitry. As shown in Figure 1, prior art current source 100 comprises digital-to-analog (D/A) converter 101, bipolar transistors 102-103, and resistor R_{Iset}. D/A converter 101 receives as inputs an analog reference voltage V_{refin} and a digital programmed value PV from the test computer. In response, D/A converter 101 outputs an analog voltage V_{out}. The output of D/A converter 101 is connected to resistor R_{iset} which in turn is connected to the collector of transistor 102. The base of transistor 102 is connected to the base of transistor 103. Moreover, the base of transistor 102 is also connected to the collector of transistor 102. The emitter of transistor 102 is connected to a power voltage V_{ref}. While the emitter of transistor 103 is also connected to voltage V_{ref}, the collector of transistor 103 supplies the output current I_{out} of current source 100.

In so doing, transistors 102-103 and resistor R_{iset} form a current mirror wherein a current is drawn away from the collector of transistor 102 which causes an emitter-collector current to flow. Because transistors 102 and 103 are identical, a substantially equal emitter-collector current is provided as I_{out}. Examining transistor 102, from Kirchoff's voltage law:

$$V_{EB} + V_{BC} + V_{CE} = 0$$

Because the base is connected to the collector, $V_{BC} = 0$. As such, the above equation becomes

$$V_{CE} = - V_{EB} \quad (1)$$

From Ohm's law,

$$I_1 = (V_{ref} - V_{BE} - V_{out}) / R_{iset} \quad (2)$$

Well-known programmable D/A converter functional characteristics dictate that

$$V_{out} = V_{ref} * (PV/FS) \quad (3)$$

where PV is the digital programmed value and FS is the full scale digital value of the D/A converter.

Substituting equation (3) into equation (2),

$$I_1 = ((V_{ref} - V_{BE}) - (V_{ref} * (PV/FS))) / R_{iset}$$

$$= (V_{ref} * (1-(PV/FS)) - V_{BE}) / R_{iset} \quad (4)$$

From Kirchoff's current law,

$$I_{Emitter} + I_{Base} + I_{Collector} = 0$$

Current I_{Base} is approximately equal to $I_{Emitter}/H_{fe}$, where H_{fe} is the transistor gain which is typically in the range of 150-300. Therefore, I_{Base} is negligible compared to $I_{Emitter}$ and $I_{Collector}$. For this reason,

$$-I_{Emitter} = I_{Collector} = I_1 \quad (5)$$

Equation (5) is applicable to both transistors 102 and 103. Because I_E for both transistors 102 and 103 are the same,

$$I_1 = I_{out} \quad (6)$$

Since it is well known that V_{BE} is related to temperature according to the equation:

$$I_E \sim \exp(qV_{BE}/kT) \quad (7)$$

wherein q is the electronic charge, k is Boltzmann's constant, and T is temperature. Solving equation (7) for V_{BE},

$$V_{BE} \approx (kT/q)\ln(I_E) \quad (8)$$

As can be seen from equation (4), I_{out} depends on V_{BE}. Thus, under prior art current source 100, the output current I_{out} is affected by temperature variations which in turn affect the precision of the current source. Moreover, prior art current source 100 error ΔV_{BE} @ ΔT is constant over the full operating range, as shown in Figure 1A, making it impossible to accurately program small values. This can be illustrated by the following example. Assume that V_{Ref} = 5V, I_0 = 1mA, V_{BE} = 0.6V, and that the D/A converter is a 12-bit converter. The resolution for this 12-bit D/A converter is $5V/2^{12}$ bit = 1.22 mV/bit. From equation (8), the change ΔV_{BE} with respect to temperature variations can be determined. However, for silicon as a material, it is common knowledge that ΔV_{BE} = -2.5mV/°C. Thus, a change of 1°C represents a 200% error at the minimum current setting. Following this logic, a change of 25°C = -62.5mV which translates to an error equal in magnitude to the lower 6 bits of a 12-bit D/A converter.

Referring now to Figure 2 illustrating another prior art current source. As shown in Figure 2, prior art current

source 200 consists of a differential amplifier whose output is connected to the bases of the transistors in a current mirror circuit. The differential amplifier consists of operational amplifier (op-amp) 201, resistor R_I 202, resistor R_F 203, resistor R_I 204, and resistor R_F 205. Resistors R_I 202 and R_F 203 are connected in parallel to the non-inverted input of op-amp 201. Resistor R_I 202 is in turn connected to reference voltage V_{Ref}. Conversely, resistor R_F 203 is in turn connected to ground. Resistor R_I 204 and R_F 205 are connected in parallel to the inverted input of op-amp 201. Resistor R_I 204 is in turn connected to a voltage source V_I. Resistor R_F 205 is in turn connected to the output of op-amp 201.

The output of op-amp 201 is connected to resistor R_{set} 206 which in turn is connected to the collector of transistor 207 of the current mirror. The bases of transistors 207 and 208 are connected together as well as to the collector of transistor 207. The emitters of transistors 207 and 208 are connected together as well as to voltage V_+. Finally, the collector of transistor 208 provides the output current for current source 200.

An circuit analysis of current source 200 shows that:

$$I_1 \approx I_2 \approx I_{out}$$

$$I_{out} = (V_+ - V_{BE1} - V_{out}) / R_{set} \quad (9)$$

where V_{BE1} is the base-emitter voltage of transistor 207 and V_{out} is the output voltage of op-amp 201.

Since voltage V_{out} is also the output voltage of the differential amplifier,

$$V_{out} = (V_{Ref} - V_i) * (R_F/R_I) \quad (10)$$

Substituting equation (10) into equation (9), the output current is defined as:

$$I_{out} = (V_+ - V_{BE} - (V_{Ref} - V_i)) * (R_F/R_I) / R_{set} \quad (11)$$

where $V_{BE} = V_{BE1} = V_{BE2}$.

Accordingly, like prior art current source 100, prior art current source 200 depends on voltage V_{BE} which is subject to changes due to temperature variations which in turn greatly affect the precision of the current source. As demonstrated earlier, a change of 1°C represents a 200% error at the minimum current setting. Moreover, prior art current

source 200 error is constant over the full operating range making it impossible to accurately program small values.

On the other hand, U.S. Patent No. 4,251,743 issued February 17, 1981 to Hareyama (hereinafter Hareyama) discloses a current source designed for used in an Analog-to-Digital (A/D) converter which compensates for temperature variations as well as changes of components' characteristics such as aging. The current source disclosed in Hareyama also implements the current mirror concept. However, the current source disclosed in Hareyama implements feedback control (i.e., closed loop control) of its output current I_{out} to compensate for errors. As a result, in addition to requiring more hardware, the current source disclosed in Hareyama requires may not be as precise and responsive as desired due to the inherent characteristics (e.g., residual error and time lag) of feedback control.

Thus, a need exists for a precise current source circuit for use in a computer controlled ATE which has good dynamic range that is able to cancel out or compensate for current changes caused by temperature variations.

SUMMARY OF THE INVENTION

Accordingly, the present invention provides a precise voltage-to-current converter (current source) circuit for use in a computer controlled ATE which has that is able to cancel out or compensate for current changes induced by variations in the current source transistor's base-emitter voltage drop caused by temperature and process variations.

The present invention meets the above need with a current source circuit which comprises a voltage reference circuit and a voltage controlled current source. The voltage controlled current source circuit has a first and second transistor each having a base, a collector, and an emitter. In the preferred embodiment, the two transistors are co-located on a single substrate thereby insuring that they have similar electrical and thermal characteristics. The emitters of the first and second transistors are coupled to a first voltage. Moreover, the collector and the base of the first

transistor are connected together. The collector of the second transistor provides an output current for the current source circuit.

The voltage reference circuit is coupled between the bases of the first and second transistors. The voltage reference circuit can be adjusted either manually or automatically to set or program the desired output current. The first transistor provides a temperature tracking reference for the control element.

In one embodiment of the present invention, the voltage reference circuit is a programmable digital-to-analog (D/A) converter. In another embodiment of the present invention, the voltage reference circuit is a variable differential amplifier.

All the features and advantages of the present invention will become apparent from the following detailed description of its preferred embodiment whose description should be taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a first prior art current source circuit.

Figure 1A illustrates the I-V curves of the first prior art current source circuit with the $\Delta V_{BE}@\Delta T$ error band superimposed.

Figure 2 illustrates a second prior art current source circuit.

Figure 3 is a high-level block diagram illustrating a typical computer controlled Automatic Test Equipment (ATE) that implements the present invention.

Figure 4 is a block diagram illustrating a first embodiment of the current source circuit in accordance to the present invention.

Figure 4A illustrates the I-V curves of the first embodiment of the current source circuit in accordance to the present invention with the $\Delta V_{BE}@\Delta T$ error band superimposed.

Figure 5 is a block diagram illustrating a second embodiment of the current source circuit in accordance to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one skilled in the art that the present invention may be practiced without these specific details. In other instances well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention. Furthermore, while the following detailed description of the present invention describes its application primarily in Automatic Test Equipment (ATE), it is to be appreciated that the present invention can be used in any apparatus or system requiring a current source.

Figure 3 illustrates, for example, a high-level diagram of a computer controlled ATE 300 in which the present invention may be implemented or practiced. As shown in Figure 3, ATE 300 may comprise computer system 301, system clocks and calibration circuits 302, formatting-masking-timeset memory 303, pattern memory 304, system power supplies 305, special tester options unit 306, precision measurement unit 307, DUT reference & power supplies 308, test head 309, and bin box 310.

Computer system 301 is the system controller. Computer system 301 controls ATE 300 and supplies a means to transfer data to/from ATE 300. Hence, computer system 301 may generally include a central processing unit (CPU), input/output (I/O) interfaces such as parallel and serial ports, communications interface for networking and communicating with the outside world, video/graphics controller, a number of data storage devices such as hard drive and tape drive for locally storing information, I/O devices such as keyboard and video monitor to allow the operator to interact with ATE 300. It is to be appreciated

that computer system 300 can be any one of a number of different computer systems including desk-top computer systems, general purpose computer systems, embedded computer systems, and others.

System clocks and calibration circuits 302 provide the ATE system clocks for timing its operations and allow for ATE system calibrations. Pattern memory 304 is used to store test vector pattern data (i.e., a representation of the I/O states for the various logical functions that the DUT is designed to perform). Formatting-masking-timeset memory 303 is used to store formatting, masking, and timeset data which modify test vector pattern data before sending it to the DUT as well as create signal formats (wave shapes) and timing edge markers for input signals and strobe timing for sampling output signals. System power supplies 305 provide steady and uninterrupted alternating current (AC) power to ATE 300.

Special tester options unit 306 contains optional circuits to allow ATE 300 to be customized for carrying out predetermined tests. Precision measurement unit 307 allows ATE 300 to make accurate direct current (DC) measurements. DUT reference & power supplies 308 supply DC power (e.g., V_{DD}, V_{CC}, etc.) to the Device Under Test (DUT). Additionally, DUT reference & power supplies 308 supply input and output reference voltages (e.g., VIL/VIH, VOL/VOH) to the DUT. Test head 309 contains pin electronics (PU) circuitry and interfaces to the load board on which the DUT is placed. Bin box 310 is located near test head 309 and typically contains START and RESET buttons and displays pass/fail results.

Depending on its test purposes, it is to be appreciated that an ATE may have more or fewer than the components discussed above. Further, it should be clear that the components of the ATE discussed above are conventional and well known by people of ordinary skill in the art.

The voltage-to-current converter (the current source) under the present invention is implemented as part of the PE circuitry inside test head 309. In accordance to a first embodiment of the present invention, by implementing a programmable digital-to-analog (D/A) converter between the

bases of the two transistors in a voltage controlled current source circuit, a dynamic, programmable, and open-loop current source can be constructed. Under this embodiment, the current source can be programmed by computer system 301 to send the desired current to the DUT.

Reference is now made to Figure 4 illustrating the first embodiment of the current source in accordance to the present invention. As shown in Figure 4, current source 400 consists of bipolar transistors 401-402, resistor R_{set} 403, resistor R_{ref} 404, and programmable D/A converter 405. Preferably, transistors 401 and 402 are located on the same substrate so that their electrical and thermal characteristics are substantially matched. Also, resistor R_{set} 403 and resistor R_{ref} 404 are substantially equal. The emitter of transistor 401 receives a reference voltage V_{ref} and is also connected to resistor R_{set} 403. The base of transistor 401 is connected to resistor R_{ref} 404, the collector of transistor 401, and the voltage reference input of D/A converter 405. D/A converter 405 receives a programmable value PV from computer system 401. Its output is connected to the base of transistor 402 which is also connected to resistor R_{ref} 404. The emitter of transistor 402 is connected to resistor R_{set} 403. The collector of transistor 402 provides the output I_{out} for current source 400.

In so doing, transistors 401-402, resistor R_{set} 403, and resistor R_{ref} 404 make up a voltage controlled current source wherein transistor 401 provides the temperature tracking voltage reference and transistor 402 acts as a voltage-to-current converter. Further, it should be clear to a person of ordinary skill in the art that with its base connected to its collector, transistor 401 acts like a diode device. Hence, a diode device that has similar characteristics may replace transistor 401. Programmable D/A converter 405 is placed between the bases of transistors 401 and 402 to allow current source 400 to be programmable. As such, programmable D/A converter 405 acts as the voltage reference circuit. The D/A converter's voltage reference input and hence its output will now track transistor 402 ΔV_{BE}.

A circuit analysis of current source 400 is performed to determine an equation for the output current I_{out}. It is well known that the voltage V_{out} of a programmable D/A converter is equal to:

$$V_{out} = V_{RefIn} * (PV/FS) \quad (12)$$

where PV is the digital programmable value from controlled system computer 301 and FS is the digital full scale value of D/A converter 405.

Following the logic of the analysis in deriving equation (4) in the background section, current I_1 is determined to be:

$$I_1 = (V_{Ref} - V_{BE1} - V_{out})/R_{Ref} \quad (13)$$

where V_{BE1} is the voltage between the base and emitter of transistor 401. Similarly, current I_2 is:

$$I_2 = (V_{Ref} - V_{BE2} - V_{out})/R_{set} \quad (14)$$

Since $V_{BE1} = V_{BE2}$ (transistors 401 and 402 are substantially equivalent) and $R_{set} = R_{Ref}$, it can be shown that $I_1 \approx I_2$. From Kirchoff's current law:

$$I_2 = I_{out} + I_{Base} \quad (15)$$

where I_{Base} is the base current of transistor 402.

Current I_{Base} is approximately equal to I_2/H_{fe}, where H_{fe} is the transistor gain which is typically in the range of 150-300. Thus, I_{Base} is negligible and $I_2 \approx I_{out}$ under equation (15). Substituting equation (12) into equation (15):

$$I_2 \approx I_{out} = (V_{Ref} - V_{BE2} - (V_{Refin} * (PV/FS)))/R_{set} \quad (16)$$

By inspection, $V_{Refin} = V_{Ref} - V_{BE1} = V_{Ref} - V_{BE2}$. When this is substituted into equation (16), equation (16) becomes:

$$I_{out} = (V_{Ref} - V_{BE2} - ((V_{Ref} - V_{BE2}) * (PV/FS)))/R_{set} \quad (17)$$

Factoring out the term $((V_{Ref} - V_{BE2})/R_{set})$, equation (17) becomes:

$$I_{out} = ((V_{Ref} - V_{BE2})/R_{set}) * (1-(PV/FS)) \quad (18)$$

From equation (17), it can be seen that when the ratio (PV/FS) approaches unity, the V_{BE} terms cancel out as I_{out} approaches zero. The significance of this is that small values of current can be programmed with negligible temperature affect. Referring now to Figure 4A illustrating, as an example, the I-V curves of the first embodiment in accordance to the present invention. As shown in Figure 4A,

under the present invention, the error ΔV_{BE} @ ΔT is proportional to the current. Hence, at very low current values, the error ΔV_{BE} @ ΔT is essentially reduced to zero (0).

Moreover, under the present invention, there is no unusable range and no offset changes because V_{Refin} tracks the V_{BE} voltage of transistor 402. And, in accordance to the present invention, the whole voltage operating range of the current source is available. This can be illustrated by the considering the same example discussed earlier in the background. As before, assume that V_{Ref} = 5V, I_0 = 1mA, V_{BE} = 0.6V, and that the D/A converter is a 12-bit converter. The resolution for this 12-bit D/A converter is $5V/2^{12}$ bit = 1.22 mV/bit. Unlike the prior art example, the current I_{out} under equation (18) is maximum when PV is 0 and minimum when PV = FS. Hence, there is no unusable voltage range and no unusable D/A converter bit range in accordance to the present invention.

In accordance to a second embodiment of the present invention, by implementing a variable differential amplifier between the bases of the two transistors in a current mirror circuit, a dynamic, variable, and open-loop current source can be constructed. Under this embodiment, the current source can be varied by changing the values of resistors R_I and R_F to program the desired current to the DUT.

Referring now made to Figure 5 illustrating a second embodiment of the current source in accordance to the present invention. As shown in Figure 5, current source 500 consists of bipolar transistors 501-502, resistor R_{I1} 503, resistor R_{F1} 504, resistor R_{I2} 505, resistor R_{F2} 506, resistor R_{set} 507, and operational amplifier (op-amp) 508. Preferably, transistors 501 and 502 are located on the same substrate so that their electrical and thermal characteristics are substantially matched. Also, resistor R_{I1} 503 and resistor R_{F1} 504 are preferably equal to their counterparts resistor R_{I2} 505 and resistor R_{F2} 506. However, depending on needs, it is to be appreciated that resistor R_{I1} 503 can have a different value

than its counterpart resistor R_{I2} 505 and resistor R_{F1} 504 can have a different value than its counterpart resistor R_{F2} 506.

The emitter of transistor 501 receives a reference voltage V_{ref}. The base of transistor 501 is connected to resistor R_{I1} 503 and the collector of transistor 501. Resistor R_{I1} 503 is in turn connected to the non-inverted input of op-amp 508. Resistor R_{F1} 504, which is in parallel to resistor R_{I1} 503, is also connected to the non-inverted input of op-amp 508. The other end of resistor R_{F1} 504 is connected ground GND. The inverted input of op-amp 508 is connected to resistor R_{I2} 505 which in turn is connected to the voltage source V_i. The inverted input of op-amp 508 is also connected to R_{F2} 506 which in turn is connected to the output of op-amp 508. The output of op-amp 508 is connected to resistor R_{set} 507 which in turn is connected to the base of transistor 502. The emitter of transistor 502 receives voltage V_{Ref}. The collector of transistor 502 provides the output current I_{out} of current source 500.

In so doing, transistors 501 and 502 make up a voltage controlled current source circuit wherein transistor 501 provides temperature tracking voltage reference and transistor 502 is the voltage-to-current converter. Further, it should be clear to a person of ordinary skill in the art that with its base connected to its collector, transistor 501 acts like a diode device. Hence, a diode device with similar characteristics may replace transistor 501. On the other hand, op-amp 508, resistor R_{I1} 503, resistor R_{F1} 504, resistor R_{I2} 505, and resistor R_{F2} 506 make up a differential amplifier which together with resistor Rset 507 are placed between the bases of transistors 501 and 502 to act as a voltage reference circuit wherein the values of resistors R_{Ii} and R_{Fi} is used to program the desired current to the DUT. The voltage reference circuit's voltage reference input and hence its output will now track transistor 502 ΔV_{BE}.

A circuit analysis of the differential amplifier indicates that:

$$V_{out} = (R_F/R_I)*((V_{Ref} - V_{BE1}) - V_i) \quad (19)$$

where R_{I1} 503 = R_{I2} 505 = R_I and R_{F1} 504 = R_{F2} 506 = R_F and V_{BE1} is the base-emitter voltage of transistor 501.

The output current I_{out} is equal to:

$$I_{out} = (V_{Ref} - V_{BE2} - V_{out})/R_{set} \quad (20)$$

where V_{BE2} is the base-emitter voltage of transistor 502.

By substituting equation (19) into equation (20), equation (20) then becomes:

$$I_{out} = (V_{Ref} - V_{BE2} - ((V_{Ref} - V_{BE1}) - V_i)* (R_F/R_I))/R_{set} \quad (21)$$

If $R_F/R_I = 1$, then $V_{BE2} = V_{BE1}$ and equation (21) is reduced to:

$$I_{out} = V_i/R_{set} \quad (22)$$

According to equation (22), the output current I_{out} is not dependent on V_{BE} and therefore, is not subject to temperature variations. Therefore, the second embodiment of the present invention can operate with small values of current since the temperature affect is negligible. Moreover, under the present invention, there is no unusable range and no offset changes because V_{Refin} tracks the V_{BE} voltage of transistor 502.

The two embodiments of the present invention, a current source (a.k.a. voltage-to-current converter) circuit, are thus described. While the present invention has been described in particular embodiments, the present invention should not be construed as limited by such embodiments, but rather construed according to the below claims.

CLAIMS

What is claimed is:

1. A current source circuit comprising:

a voltage controlled current source circuit comprising a first and second transistor each having a base, a collector, and an emitter, the emitters of the first and second transistors coupled to a first voltage, the collector and the base of the first transistor connected together; the collector of the second transistor providing an output current for the current source circuit; and

a voltage reference circuit coupled between the bases of the first and second transistors wherein the voltage reference circuit can be adjusted to track temperature variations.

2. The current source circuit of claim 1, wherein the voltage reference circuit is a programmable digital-to-analog (D/A) converter.

3. The current source circuit of claim 2 further comprising:

a first resistor coupled between the bases of the first and second transistor; and

a second resistor coupled between the emitters of the first and second transistor.

4. The current source circuit of claim 3, wherein the output current is based on the equation:

$$I_{out} = ((V_{Ref} - V_{BE2})/R_{set})*(1-(PV/FS))$$

where V_{Ref} is the first voltage, V_{BE2} is the base-emitter voltage of the second transistor, R_{set} is the second resistor, PV is a digital programmable value of the D/A converter, and FS is a digital full scale value of the D/A converter.

5. The current source circuit of claim 1, wherein the voltage reference circuit is a variable differential amplifier.

6. The current source circuit of claim 5 further comprising a first resistor coupled between the variable differential amplifier and the base of the second transistor.

7. The current source circuit of claim 6, wherein the variable differential amplifier comprises:

an operational amplifier (op-amp) having an inverted input, a non-inverted input, and an output;

a second resistor connected to the non-inverted input of the op-amp;

a third resistor coupled between the non-inverted input of the op-amp and a second voltage; wherein the second and third resistors are parallel to each other;

a fourth resistor coupled between the inverted input of the op-amp and a voltage source; and

a fifth resistor coupled between the inverted input and the output of the op-amp, wherein the fourth and fifth resistors are parallel to each other.

8. The current source of claim 7, wherein the second and fourth resistors are substantially equal and the third and fifth resistors are substantially equal.

9. The current source of claim 8, wherein the output current is based on the equation:

$$I_{out} = (V_{Ref} - V_{BE2} - ((V_{Ref} - V_{BE1}) - V_i) * (R_F/R_I))/R_{set}$$

where V_{Ref} is the first voltage, V_{BE1} is the base-emitter voltage of the first transistor, V_{BE2} is the base-emitter voltage of the second transistor, V_i is the voltage output from the voltage source, R_F is the fourth resistor, R_I is the second resistor, and R_{set} is the first resistor.

10. An Automatic Test Equipment (ATE) comprising:

a computer system;

formatting-masking-timeset memory coupled to the computer system;

pattern memory coupled to the computer system;

a precision measurement unit coupled to the computer system; and

a test head unit coupled to the computer system, the precision measurement unit, and the bin box, the test head unit comprising a pin electronics (PE) circuit for supplying input signals to a device under test (DUT) and receives output signals from the DUT, the PE circuit comprising a current source circuit comprising:

a voltage controlled current source circuit comprising a first and second transistor each having a base, a collector, and an emitter, the emitters of the first and second transistors coupled to a first voltage, the collector and the base of the first transistor connected together; the collector of the second transistor providing an output current for the current source circuit; and

a voltage reference circuit coupled between the bases of the first and second transistors wherein the voltage reference circuit can be adjusted to track temperature variations.

11. The computer system of claim 10, wherein the voltage reference circuit is a programmable digital-to-analog (D/A) converter.

12. The ATE of claim 11, wherein the current source further comprising:

a first resistor coupled between the bases of the first and second transistor; and

a second resistor coupled between the emitters of the first and second transistor.

13. The ATE of claim 12, wherein the output current is based on the equation:

$$I_{out} = ((V_{Ref} - V_{BE2})/R_{set})*(1-(PV/FS))$$

where V_{Ref} is the first voltage, V_{BE2} is the base-emitter voltage of the second transistor, R_{set} is the second resistor, PV is a digital programmable value of the D/A converter, and FS is a digital full scale value of the D/A converter.

14. The ATE of claim 10, wherein the variable controlled device is a variable differential amplifier.

15. The ATE of claim 14 further comprising a first resistor coupled between the variable differential amplifier and the base of the second transistor.

16. The ATE of claim 15, wherein the variable differential amplifier comprises:

an operational amplifier (op-amp) having an inverted input, a non-inverted input, and an output;

a second resistor connected to the non-inverted input of the op-amp;

a third resistor coupled between the non-inverted input of the op-amp and a second voltage; wherein the second and third resistors are parallel to each other;

a fourth resistor coupled between the inverted input of the op-amp and a voltage source; and

a fifth resistor coupled between the inverted input and the output of the op-amp, wherein the fourth and fifth resistors are parallel to each other.

17. The ATE of claim 16, wherein the second and fourth resistors are substantially equal and the third and fifth resistors are substantially equal.

18. The ATE of claim 17, wherein the output current is based on the equation:

$$I_{out} = (V_{Ref} - V_{BE2} - ((V_{Ref} - V_{BE1}) - V_i) * (R_F/R_I))/R_{set}$$

where V_{Ref} is the first voltage, V_{BE1} is the base-emitter voltage of the first transistor, V_{BE2} is the base-emitter voltage of the second transistor, V_i is the voltage output from the voltage source, R_F is the fourth resistor, R_I is the second resistor, and R_{set} is the first resistor.

19. A method to convert voltage into current comprising the steps of:

in a voltage controlled current source circuit comprising a first and second transistor each having a base, a collector, and an emitter, the emitters of the first and second transistors coupled to a first voltage, the collector and the base of the first transistor connected together, providing an output current for the current mirror circuit at the collector of the second transistor; and

adjusting a voltage reference circuit coupled between the bases of the first and second transistors to track temperature variations.

20. The method of claim 19, wherein the voltage reference circuit is a programmable digital-to-analog (D/A) converter.

21. The method of claim 19, wherein the voltage reference circuit is a variable differential amplifier.

22. A current source circuit comprising:

a voltage controlled current source comprising a diode and a first transistor having a base, a collector, and an emitter, the input of the diode and the emitter of the first transistor coupled to a first voltage, the collector of the second transistor providing an output current for the current source circuit; and

a voltage reference circuit coupled between the output of the diode and the base of the first transistor wherein the voltage reference circuit can be adjusted using a reference voltage to track temperature variations.

23. The current source circuit of claim 22, wherein the voltage reference circuit is a programmable digital-to-analog (D/A) converter.

24. The current source circuit of claim 22, wherein the voltage reference circuit is a variable differential amplifier.

25. A temperature compensated transconductance circuit for generating an output current substantially proportional to a voltage indicative input, comprising:

a first circuit having a reference input, a control input, and an output, said first circuit reference input coupled to a voltage reference, said first circuit output providing said output current;

a second circuit having a reference input and an output, said second circuit reference input coupled to said voltage reference, wherein said second circuit generates temperature induced voltage changes on said second circuit output substantially equal to corresponding temperature induced voltage changes generated by said first circuit which affect said output current; and

a control element having a reference input, a voltage input, and an output, said reference input coupled to said second circuit output, said voltage input coupled to said voltage indicative input, and said control element output coupled to said first circuit control input so that said output current is substantially proportional to said voltage indicative input substantially without temperature induced offsets.

26. The temperature compensated transconductance circuit of claim 25, wherein said first circuit comprises a first transistor having an emitter coupled to said first circuit reference input, a base coupled to said first circuit control input, and a collector coupled to said first circuit output.

27. The temperature compensated transconductance circuit of claim 26, wherein said second circuit comprises a second transistor having an emitter coupled to said second circuit reference input, a base coupled to said second circuit output, and a collector coupled to said second circuit output.

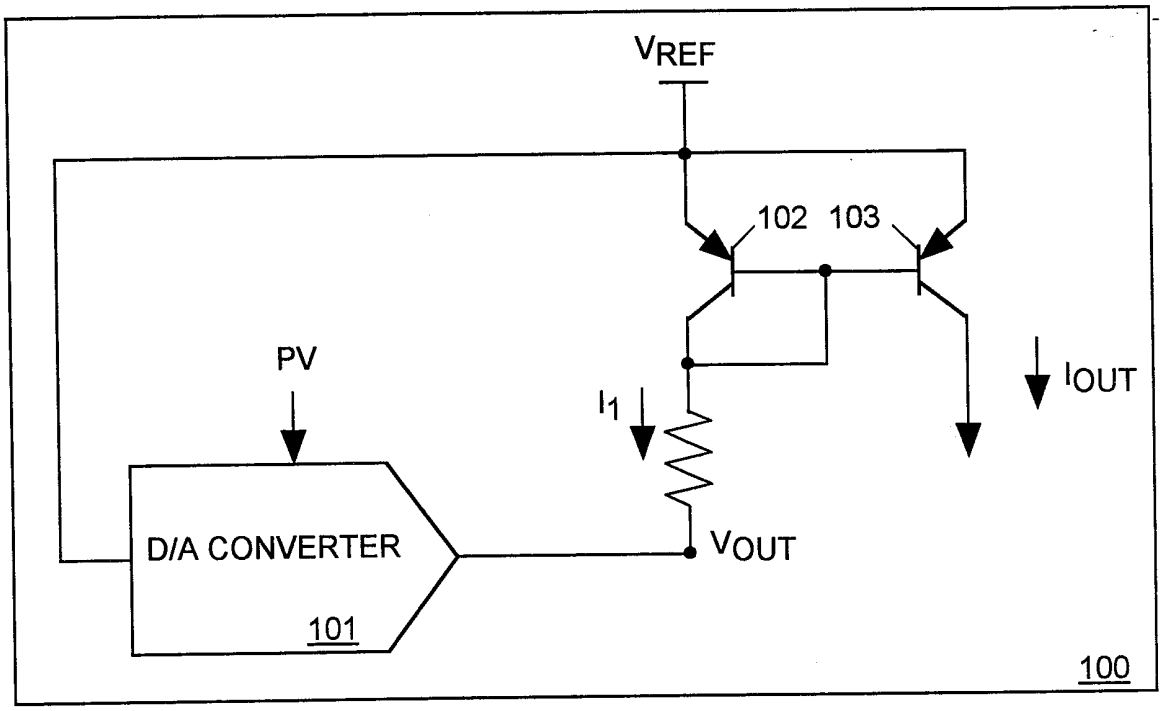


FIG. 1
(PRIOR ART)

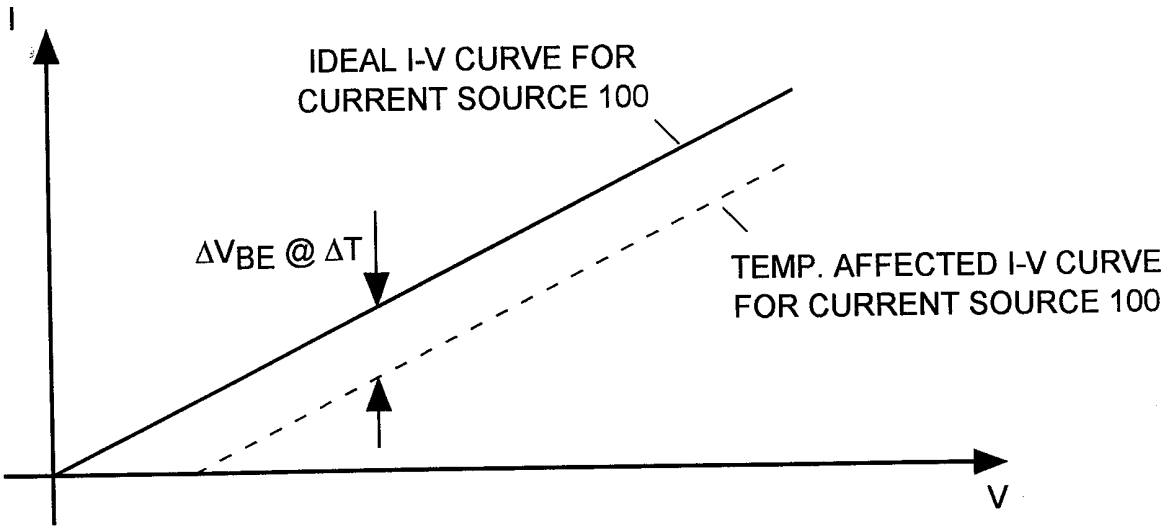


FIG. 1A
(PRIOR ART)

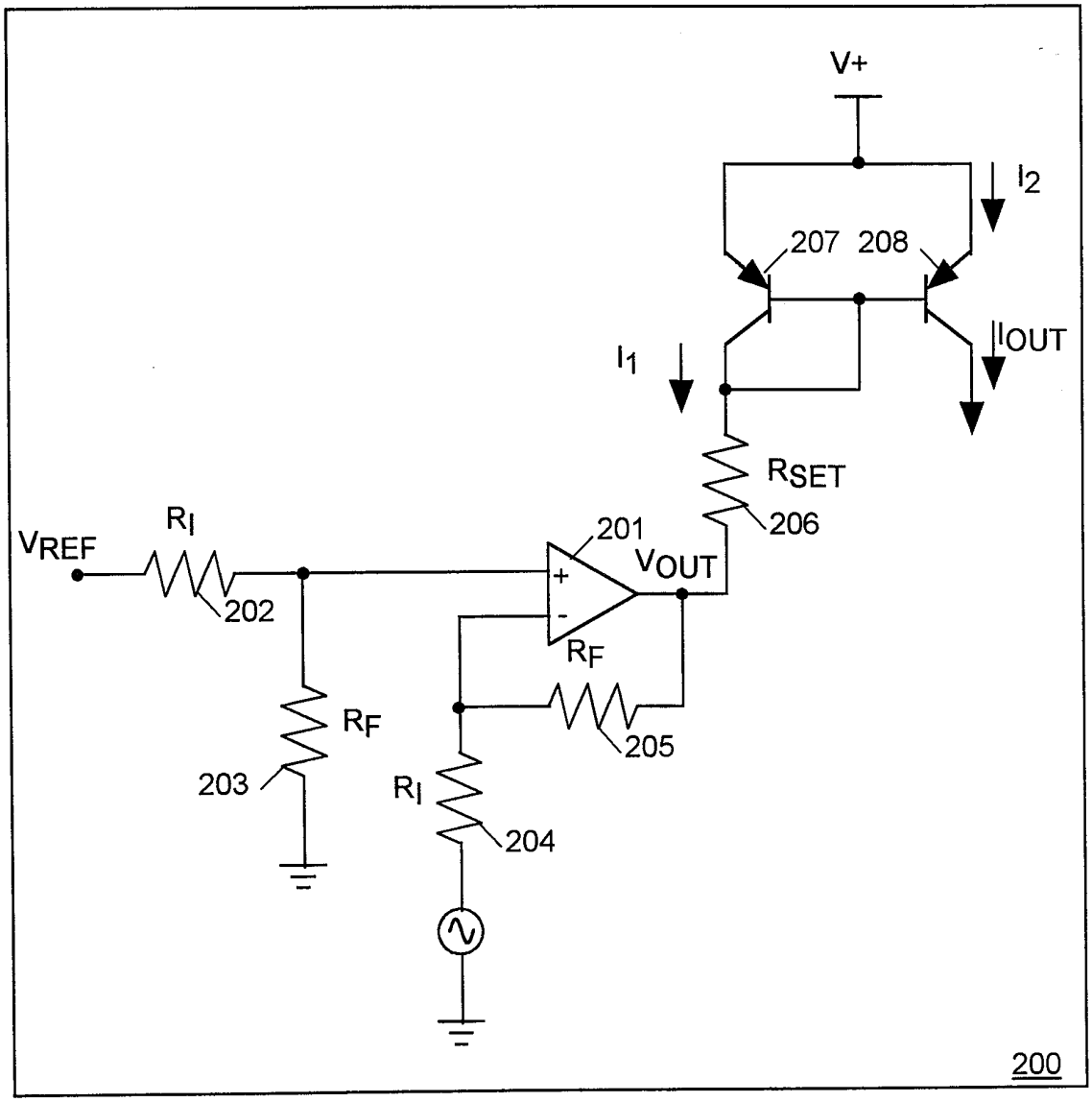
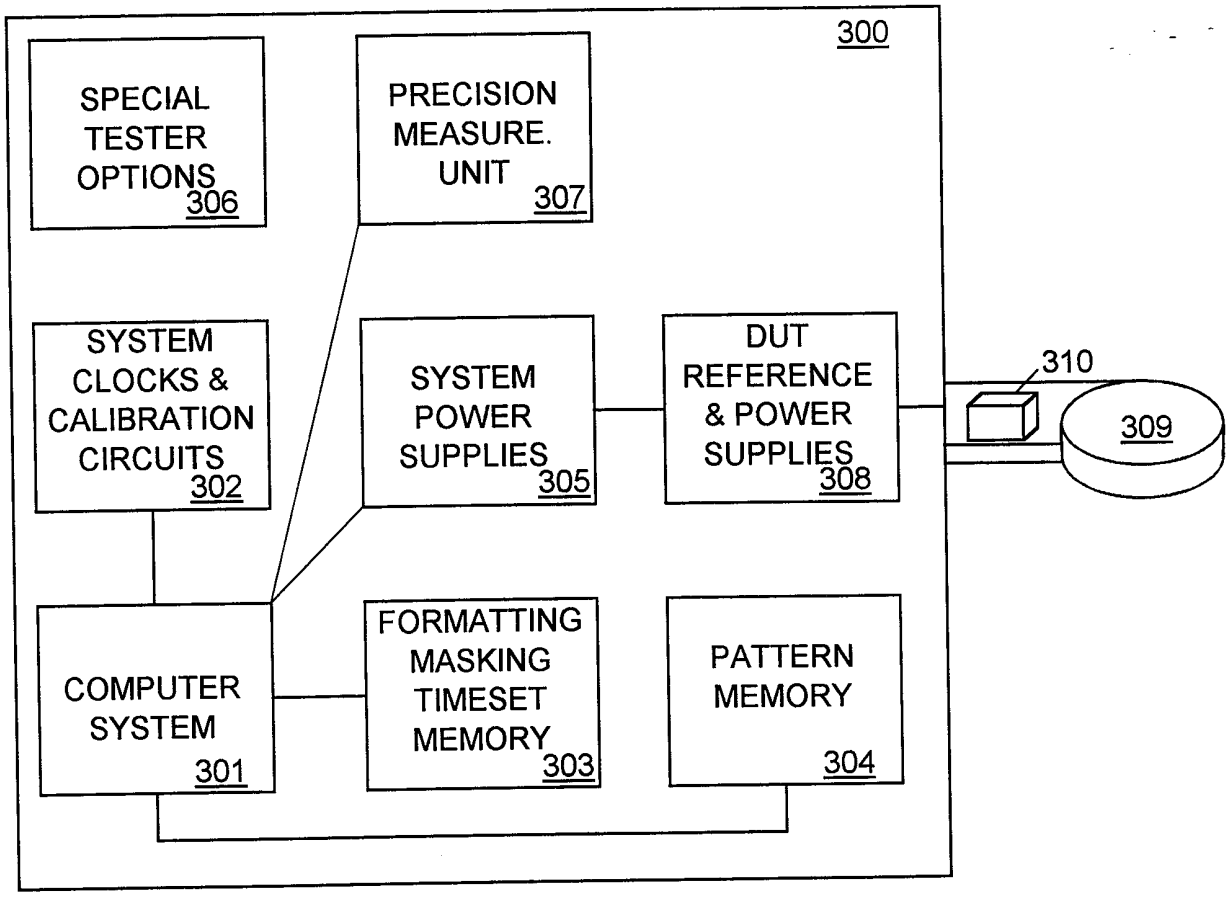


FIG. 2
(PRIOR ART)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SYSTEM CLOCKS & CALIBRATION CIRCUITS 302
SYSTEM POWER SUPPLIES 305
DUT REFERENCE & POWER SUPPLIES 308
310
309
COMPUTER SYSTEM 301
FORMATTING MASKING TIMESET MEMORY 303
PATTERN MEMORY 304

FIG. 3

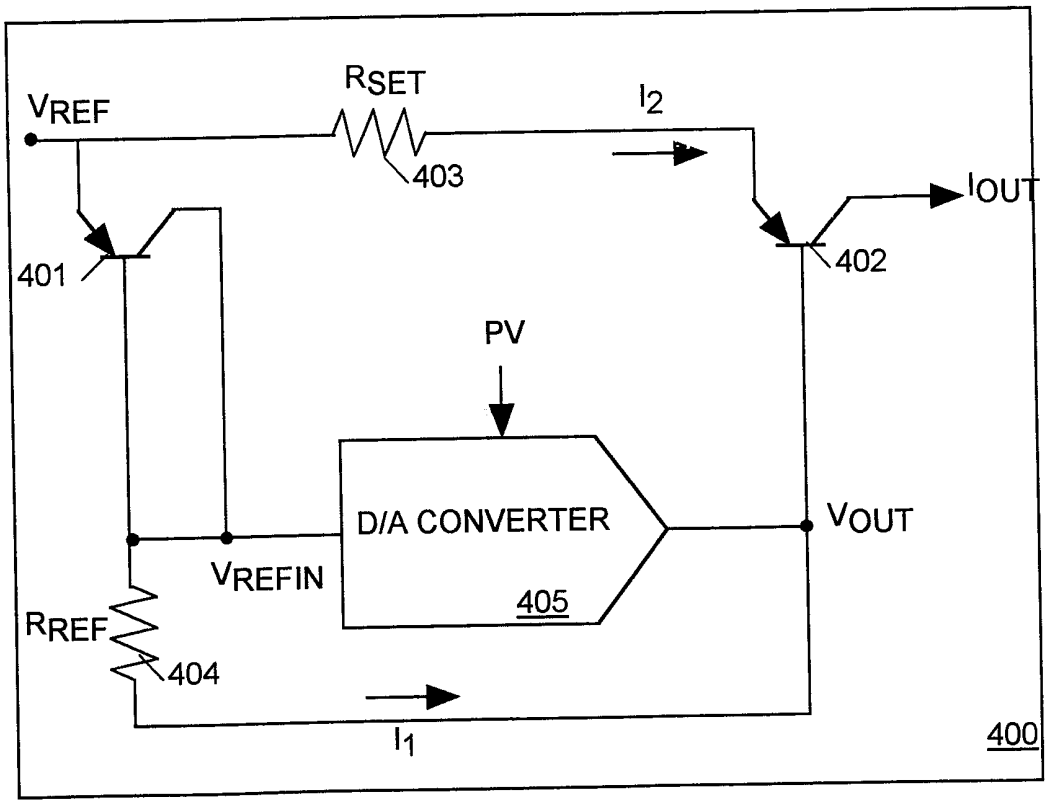
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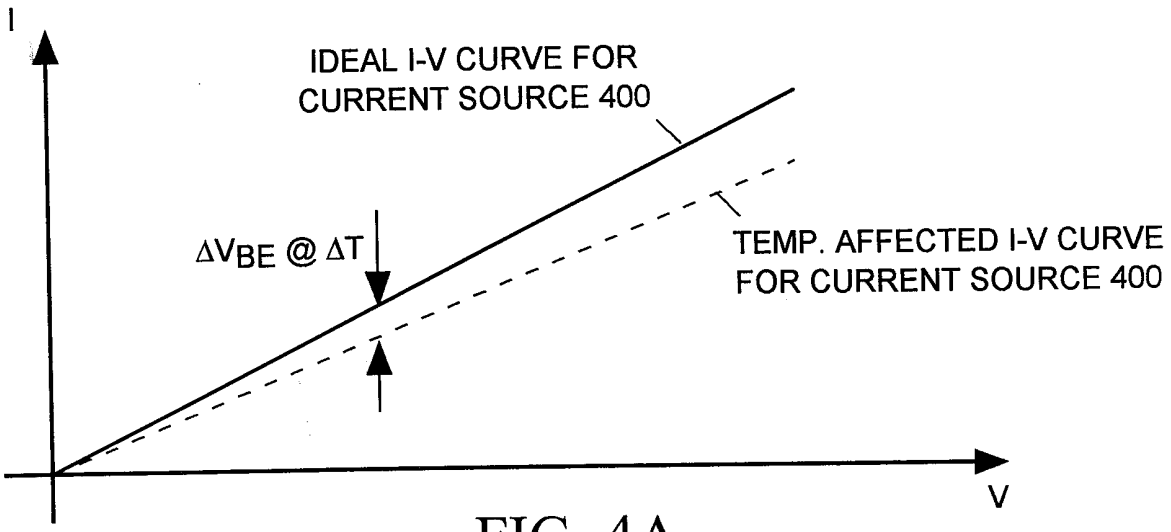
FIG. 4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ΔVBE @ ΔT
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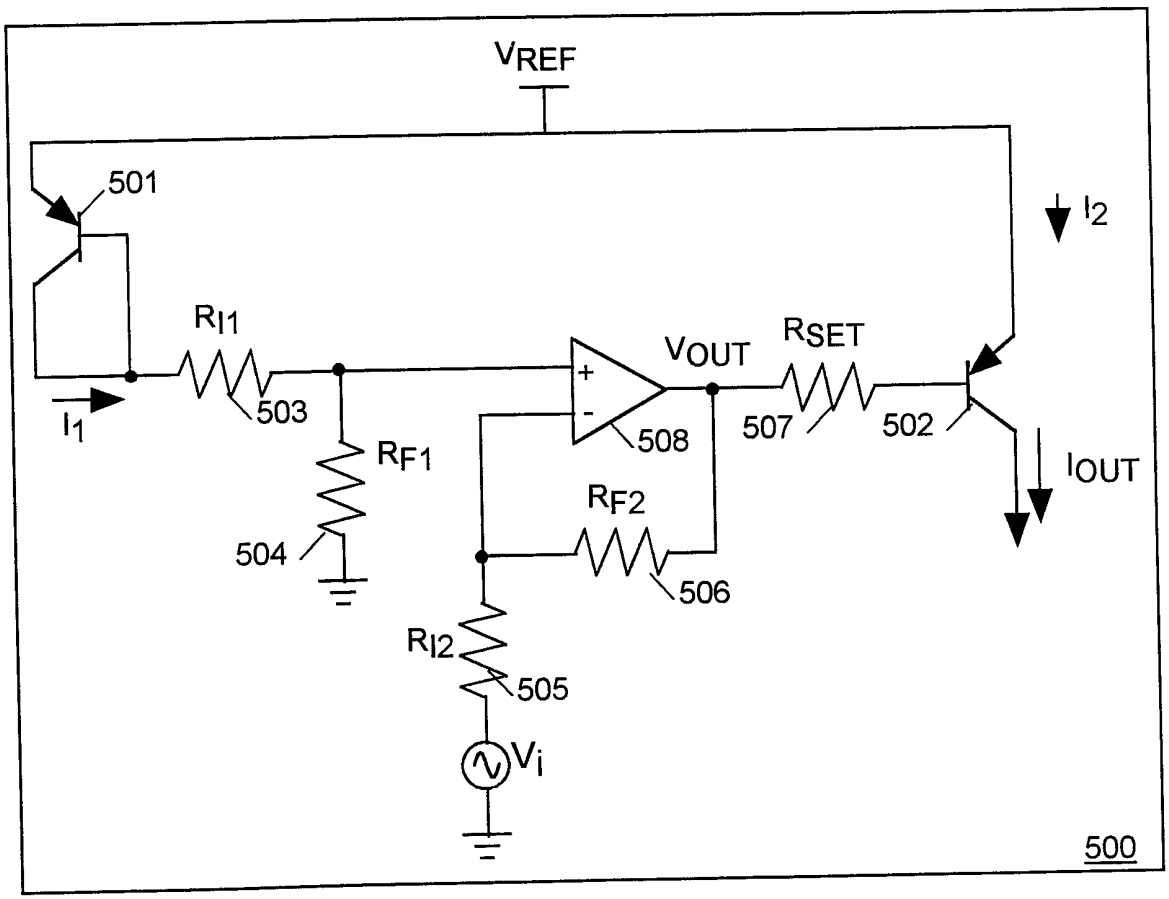
FOR CURRENT SOURCE 400
V

FIG. 4A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Vi
500

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/08742

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G05F 3/02; G01R 31/02
US CL :327/538, 324/73.1
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 327/538, 540, 323/312, 315; 324/73.1, 158.1

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

U.S. PTO APS
search terms: ate, "automatic test equipment", "pattern memory", computer, masking

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A, P	US 5,913,022 A (TINAZTEPE et al.) 15 June 1999 (15.06.99), Fig. 2.	10-21
A	US 5,107,199 A (VO et al.) 21 April 1992 (21.04.92), Fig. 2.	1-9 and 22-27
X	US 4,906,915 A (ABDI) 06 March 1990 (06.03.90), Fig. 1.	1, 5, 6, 22 and 24-27

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 29 JULY 1999	Date of mailing of the international search report 17 AUG 1999
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer TERRY D. CUNNINGHAM Telephone No. (703) 308-4872

Form PCT/ISA/210 (second sheet)(July 1992)*