United States Patent [19]

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[54] **CONTACT DELAY AND SELF-DESTRUCT CIRCUIT**

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[52] **U.S. Cl.** ..... **102/70.2 R**

[51] **Int. Cl.** **F42c 11/06**

[58] **Field of Search** 102/70.2

[56] **References Cited**

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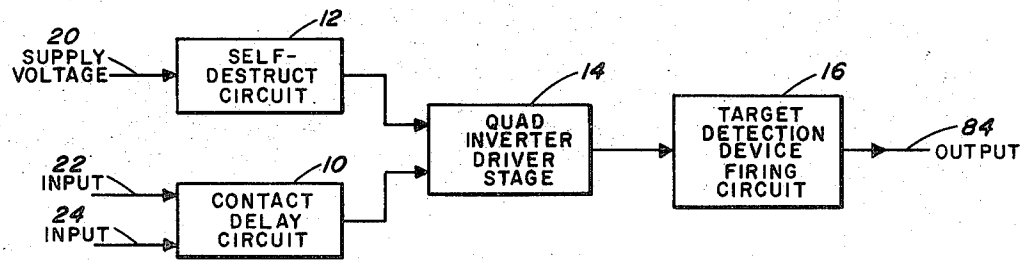
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[57] **ABSTRACT**

A circuit for providing a predetermined time delay after missile impact before detonation, and a self-destruct system controlled by the missile's operation. The circuit utilizes a quad inverter fed by the self-destruct system and the contact delay system, in parallel, driving a firing system. The contact delay system is basically a one-shot multivibrator, utilizing pulses from piezoelectric crystals as inputs, and having an RC timing circuit to trigger the firing system. The self-destruct system utilizes a reduced voltage resulting from an extinquished gas generator to trigger the firing system. The firing system has an SCR gate triggered by the quad inverter output.

7 Claims, 5 Drawing Figures



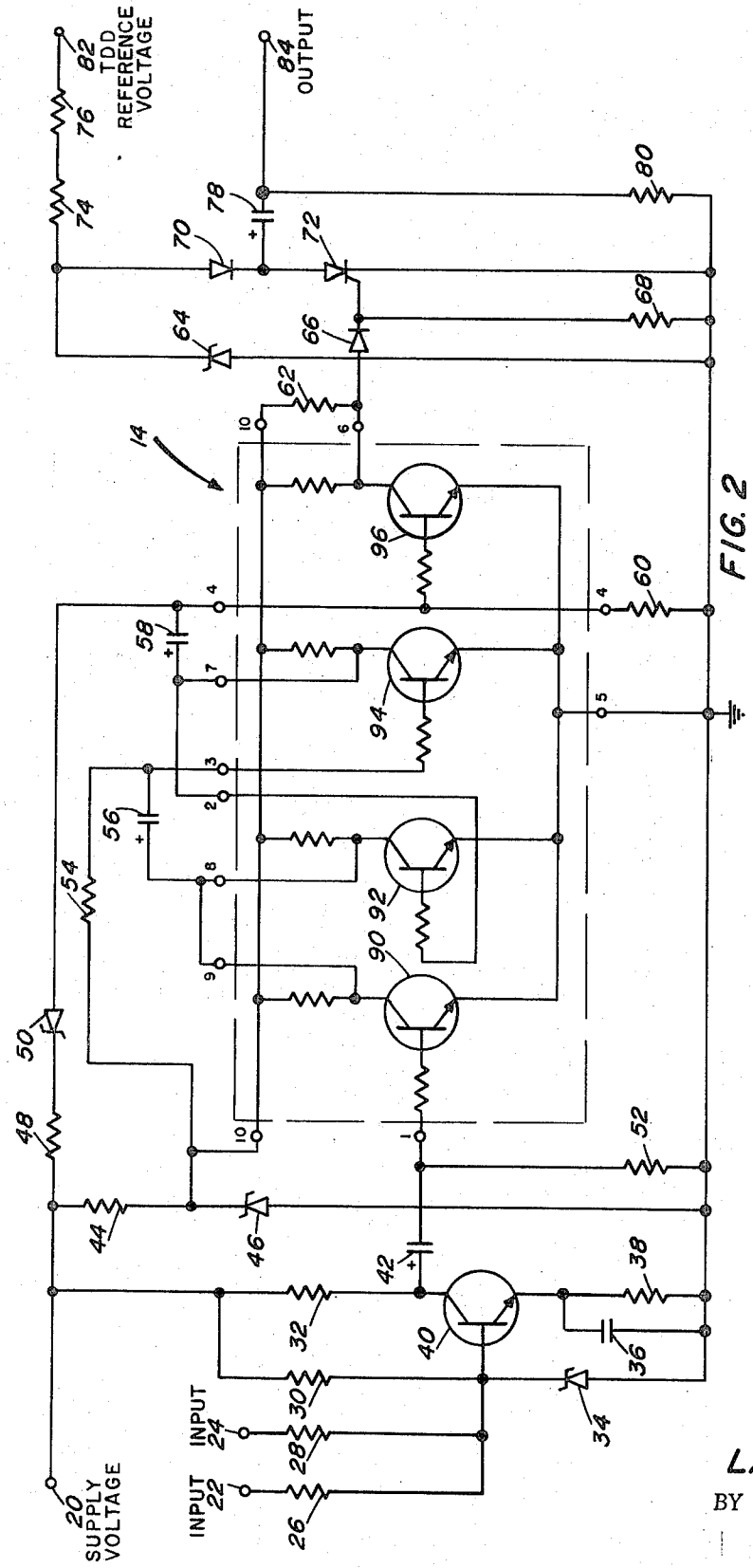


FIG. 2

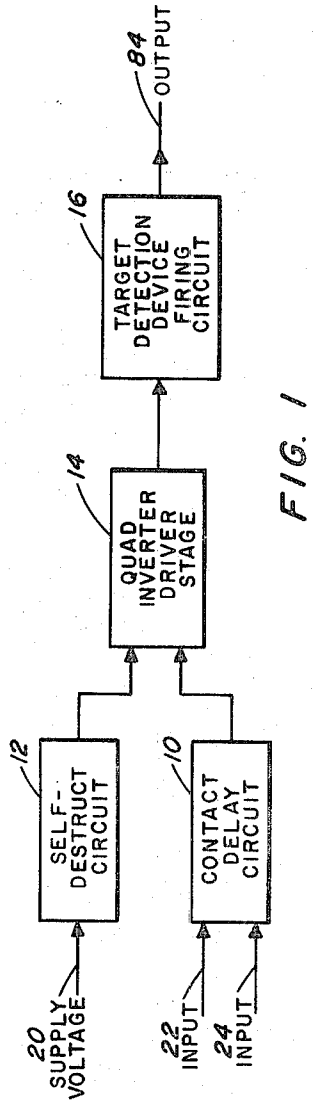


FIG. 1

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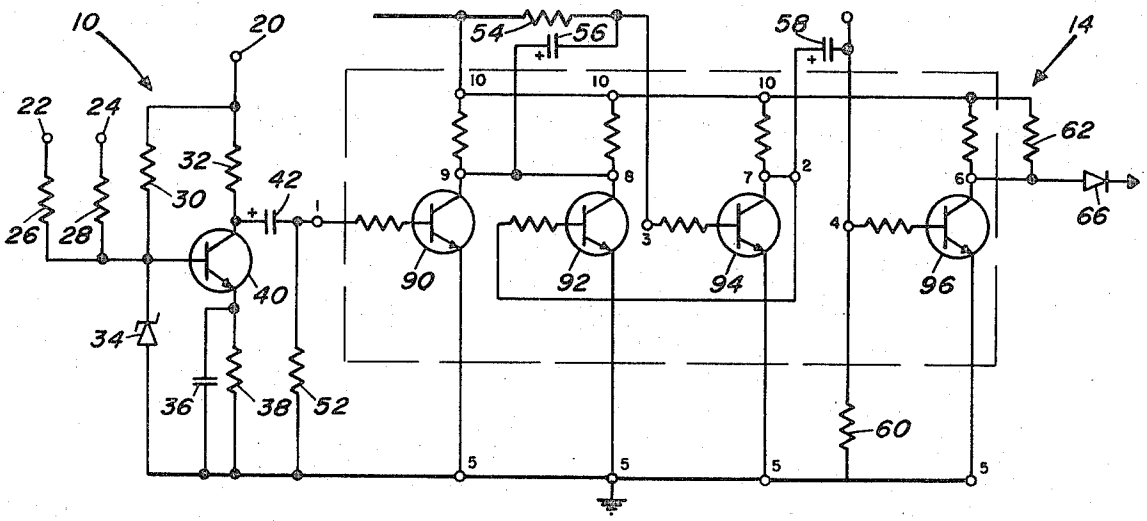


FIG. 3

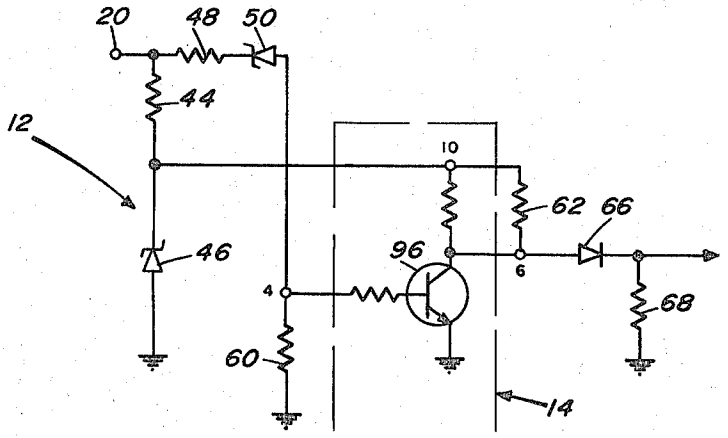


FIG. 4

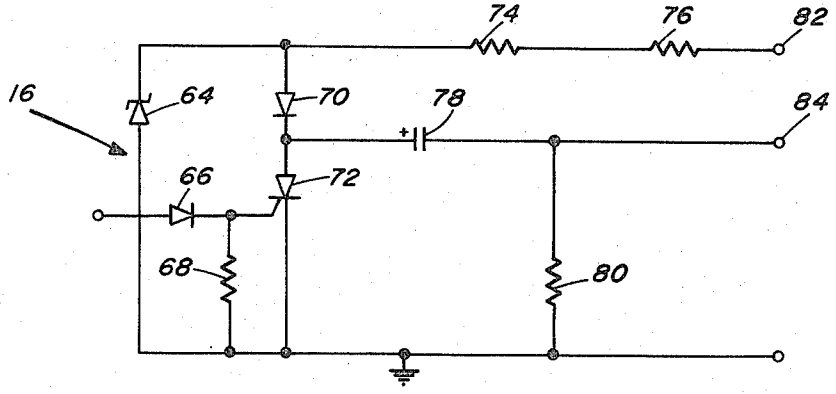


FIG. 5

CONTACT DELAY AND SELF-DESTRUCT CIRCUIT

GOVERNMENT INTEREST

The invention described herein may be manufactured and used by or for the Government of the United States of America for governmental purposes without the payment of any royalties thereon or therefor.

BACKGROUND OF THE INVENTION

The invention relates to the field of missile fuzing systems and, in particular, to the missile's hit and miss modes of operation.

Missile fuzing devices, prior to the present invention, gave a direct pulse to the target detecting device, and fired upon impact with no delay in time. The contact trigger circuits utilize transformer coupling, Shockley diodes and a relatively unregulated power supply. Inherent problems with the circuits are that Shockley diodes are difficult to obtain, and missile warhead misfiring caused by circuit transients can occur due to the relatively unregulated power supply and transformer coupling.

SUMMARY OF THE INVENTION

The present invention can be used anywhere a time-delay circuit is desired. The disclosed embodiment is designed for use in a missile system.

The contact delay system utilizes readily available components, no magnetic components and a well regulated power supply. After the missile experiences contact with the target a time delay, controllable by the selection of one resistor and one capacitor, prevents the circuit from delivering a destruct pulse to the target detection device firing circuit until after a predetermined time has expired. The self-destruct system takes advantage of a reduced voltage supply caused by a reduction in the revolutions per minute of the missile turbo-generator, resulting from the lack of fuel in the missile gas generator, to provide a trigger pulse to the firing circuit. The target detection device firing circuit was designed to allow broad silicon controlled rectifier selection without reducing effectiveness.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a block diagram of the complete circuit;

FIG. 2 is a schematic diagram of the complete circuit;

FIG. 3 is a schematic diagram of the contact delay circuit;

FIG. 4 is a schematic diagram of the self-destruct circuit; and

FIG. 5 is a schematic diagram of the target detection device firing circuit.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to FIGS. 1 and 2 wherein the contact delay and self-destruct circuit consists of a contact delay circuit **10**, a self-destruct circuit **12**, a quad inverter driver stage **14**, and a target detection device firing circuit **16**. The contact delay circuit **10**, the self-destruct circuit **12**, and the target detection device firing circuit **16** are shown individually in FIGS. **3**, **4** and **5**, and are not shown individually on FIG. **2** because certain components are shared by two or more of the circuits.

The following list is submitted by way of example to show component types and values for one embodiment of the invention. Using these examples the electronic time delay will be 0.82 ± 0.14 milliseconds over a design temperature range of −55° to +125° centigrade.

Symbol	Component	Value or type
14	Quad inverter	Motorola MC 927 G
20	(Supply Voltage)	+25 volts
26	Resistor	(as required)
28	Resistor	(as required)
30	Resistor	20 Kilohm
32	Resistor	6.8 Kilohm
34	Diode	1N751A
36	Capacitor	1 microfarad, 20 volt
38	Resistor	820 ohm
40	Transistor	2N929
42	Capacitor	0.1 microfarad
44	Resistor	430 ohm, 3 watt
46	Diode	1N750A, 4.7 volt
48	Resistor	10 Kilohm
50	Diode	1N753A, 6.2 volt
52	Resistor	2 Kilohm
54	Resistor	1.21 Kilohm, 1%, ⅛watt
56	Capacitor	1 microfarad
58	Capacitor	0.1 microfarad
60	Resistor	2 Kilohm
62	Resistor	1.5 Kilohm
64	Diode	1N973B, 33 volt
66	Diode	1N645
68	Resistor	221 Kilohm, 1%, ⅛ watt
70	Diode	1N645
72	Silicon Controlled Rectifier	2N1874A
74	Resistor	470 Kilohm, 1%
76	Resistor	33 Kilohm
78	Capacitor	10 microfarad, 75 volt
80	Resistor	1 Kilohm
82	(TDD reference voltage)	+165 volts

Referring now to FIG. **3** which shows the contact delay portion **10** of FIGS. **1** and **2**. The circuit is basically a one-shot multivibrator which is held "on" by the charge time of resistor **54** and capacitor **56**. A quad inverter **14** is used to develop the one-shot circuit. Transistor **40** is employed in the input circuit as a pulse inverter and crystal isolation stage, and provides a high level of rejection to noise on the missile supply line **20**. The crystals, or any other means desired for providing inputs **22** and **24**, are loaded by the as-required resistors **26** and **28** in series with the parallel combination of resistor **30**, diode **34**, and the input impedance of transistor **40**. This loading dampens the crystal output and reduces ringing. The switching sensitivity of the

input circuit is established by selecting the desired value of the as-required resistors **26** and **28.**

The final transistor **96** in the quad inverter **14** acts as a gate driver and transfers a positive pulse through diode **66** to the silicon controlled rectifier gate (SCR) **72.** This pulse is of sufficient amplitude to "fire" the SCR **72** over the design temperature range.

The timing of the circuit is described by equation (1) below.

$$t_1 = -K\ R\ C\ ln\ [1 - (e_c - e_o/E - e_o)] \quad (1)$$

where:

t_1 = charge time of capacitor **56** to voltage e_c

R = timing resistor **54**

C = timing capacitor **56**

e_c = final voltage required to switch transistor **94**

e_o = transistor **94** base voltage at $t = 0+$

E = supply volts at pin **10** of quad inverter **14**

K = 1.15

This equation maps the charging rate of capacitor **56** immediately after transistor **90** is switched on.

The total circuit delay can be computed by summing t_1 and the inherent contact crystal delay.

The operation is as follows: a negative pulse, generated by impulse stressing of the crystals, drives the base voltage of transistor **40** toward ground. This pulse is inverted through transistor **40** and appears at the collector as a positive pulse. The zener diode **34** holds the base of transistor **40** at a positive 5 volt potential when a negative pulse is not present. Negative pulses are limited by the forward characteristics of diode **34** which prevents reverse base-to-emitter (BVeb) breakdown of transistor **40** by limiting the negative excursion at ground potential.

The positive pulse at the collector of transistor **40** is then coupled by capacitor **42** to the base of transistor **90** which is normally cut-off. The combination of capacitor **42** and resistor **52** acts as a pulse shaping network. The positive pulse at transistor **90** will turn the transistor on if of adequate amplitude.

A low impedance path-to-ground is thereby supplied through transistor **90,** allowing capacitor **56** to discharge. The voltage at pin **3** of quad inverter **14** switches sharply negative and cuts off transistor **94.**

A positive voltage from the collector of transistor **94** is then fed to the base of transistor **92** (normally off) and turns it on. Transistor **92** now acts as the current path-to-ground. The positive voltage from the collector of transistor **94** is simultaneously fed to the differentiator consisting of capacitor **58** and resistor **60.** The differentiator produces a positive pulse at the base of transistor **96** (normally on) and simply turns transistor **96** on harder.

Meanwhile, capacitor **56** is charging at the time rate equal to t_1. As capacitor **56** charges, the circuit remains in the quasi-state described above and the voltage at pin **3** of quad inverter **14** swings slowly positive. When adequate base drive is achieved, transistor **94** turns on. The off time of transistor **94** is the circuit delay mechanism.

when transistor **94** switches on, transistor **92** switches off and the voltage at pin **3** of quad inverter **14** returns immediately to its original positive state. The input transistor **90** will remain off due to the absence of an input signal. This causes transistor **94** to saturate, producing a negative pulse out of the differentiator (capacitor **58** and resistor **60**). The pulse cuts transistor **96** off and drives the collector voltage of transistor **96** positive. This output pulse is then coupled to the SCR gate **72** through diode **66,** thus "firing", the SCR **72.** At the completion of the pulse, transistor **96** turns on and the entire circuit cycles back to its original state.

The output pulse width at pin **6** is determined by the differentiator (capacitor **58** and resistor **60**) discharge time. This pulse is always of adequate amplitude to fire the SCR **72.**

Referring now to FIG. **4** which shows the self-destruct portion **12** of FIGS. **1** and **2.** The circuit was designed to remove base drive voltage from transistor **96** upon reaching a reduced value of missile supply voltage **20.** As the missile gas generator burns out, the missile turbo generator slows down and causes a drop off in supply voltage **20.** This voltage reduction feature is used for missile self-destruct.

When the base drive voltage to transistor **96** is sufficiently reduced, the transistor cuts-off and produces a positive voltage at the collector. This positive voltage is then coupled through diode **66** to the SCR gate **72.** The amplitude of this gate voltage is sufficient to cause the SCR **72** to fire over the designed temperature range. The coupling diode **66** is necessary to prevent the saturation of transistor **96** from firing the SCR **72** at elevated temperatures. Using the components listed above, the operation of the self-destruct circuit **12** is as follows: with normal supply voltage applied transistor **96** is on and saturated. As the 25 volt supply **20** is lowered, transistor **96** starts out of saturation. When the supply is low enough the zener diode **50** goes out of regulation and passes very low current. The voltage drop across resistor **60** becomes insufficient to maintain transistor **96** on, therefore it shuts off. This causes the collector voltage of transistor **96** to go positive and thus fire the SCR **72.** The supply voltage reduction resistor **44** is such that adequate voltage is left across zener diode **46** to produce, at minimum, a 1-volt pulse across the SCR gate **72.** This circuit will produce an output pulse at supply voltages of 9 – 12 volts, depending on tolerances and temperatures. This represents a supply voltage reduction of at least 50 percent.

Referring now to FIG. **5** which shows the target detection device firing circuit **16** of FIGS. **1** and **2.** The principle of the target detection device (TDD) firing circuit is the same as in prior missile contact and self-destruct circuits.

The main advantage of the circuit is the reduction of holding current requirements to a point that special SCR selection is no longer necessary. This was accomplished by increasing the value of resistor **74** and placing zener diode **64** across the SCR **72** and diode **70.** During the charging of capacitor **78,** zener diode **64** acts as a high impedance, and the charge path is through resistors **76, 74,** and **80.** The time required to reach a minimum charge of 24 volts is below the maximum specified design value. Therefore, the use of the large series resistance **74** was justified. This large resistance lowered the anode current of the SCR **72** to a value which is below the SCR minimum holding current. The SCR gate resistor **68** was chosen as large as possible without jeopardizing the holding current requirements. Using the components listed above, the operation of the TDD firing circuit is as follows: upon application of the TDD battery voltage **82** to the circuit, capacitor **78** starts to charge toward a 33 volt final value. The SCR **72** is held off due to the lack of suffi-

cient gate voltage. The capacitor 78 will be charged to 24 volts (minimum) in less than 1.2 seconds.

A positive voltage pulse greater than 0.8 volts applied to the SCR gate 72 will turn the SCR 72 on over all conditions. The SCR, in the on state, acts as a low impedance path-to-ground and allows capacitor 78 to discharge through the SCR 72 and load attached to the output 84. This discharge forms a negative voltage pulse across the load.

Supply voltage 20, in this embodiment, is the missile system filament voltage supply. Prior devices utilize the system gyro power supply (+ 175 VDC) as the supply voltage 20, resulting in possible misfire due to circuit transients since the system gyro power is relatively unregulated. By using the missile system filament voltage supply the subject invention eliminates, or at least greatly reduces, the danger of warhead misfire since the filament voltage supply has better regulation.

What is claimed is:

1. A fuze system for use in a projectile, comprising;
first electrical means for providing a time delay after a first predetermined event before an electrical signal is provided as an output, wherein said first predetermined event is the projectile's contact with a target, including an input from a source responsive to said contact, a quad inverter coupled to the input and providing a time delayed output after the contact, and a time delay circuit coupled to said quad inverter for delaying the output of said quad inverter;
second electrical means for providing a time delay after a second predetermined event before an electrical signal is provided as an output; and
means for providing said electrical signal output after either said first or said second predetermined event.

2. The system of claim 1 wherein
said second electrical means is a means for detonating an explosive charge in said projectile at some time after said projectile's flight has been initiated.

3. The system of claim 1 wherein said time delay circuit comprises; a resistor and a capacitor.

4. The system of claim 1 wherein
said first electrical means further includes;
a crystal, which provides an electric pulse when impulse stressed such as by impact, electrically connected to a one-shot multivibrator;
a one-shot multivibrator connected to said crystal for providing an electric signal to said electrical signal output providing means including said quad inverter; and wherein
said electrical signal output providing means includes;
a firing circuit electrically connected to said multivibrator and triggerable by said multivibrator for providing an electric signal to said explosive charge.

5. The system of claim 1 wherein
said second electrical means includes;
an electric generator,
means for reducing the voltage output of said generator,
control means for providing an electric signal to said electrical signal output providing means when said generator voltage output is reduced; and wherein
said electrical signal output providing means includes;
a firing circuit electrically connected to said control means and triggerable by said control means for providing an electric signal to said explosive charge.

6. The system of claim 1 wherein
said electrical signal output providing means includes
a firing circuit electrically connected to said quad inverter and triggerable by said quad inverter and electrically connected to said second electrical means and triggerable by said second electrical means.

7. The system of claim 1 wherein
said quad inverter includes first, second, third, and fourth transistors and the base of said first transistor is effectively coupled to said input, the output terminal of said third transistor is coupled to the base of said second transistor, and the output terminals of said first and second transistors and the base of said third transistor are coupled to said time delay circuit.

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