(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
4 August 2011 (04.08.2011)

PCT

(10) International Publication Number
WO 2011/094059 A2

(51) International Patent Classification:
H01L 29/78 (2006.01)

(21) International Application Number:
PCT/US2011/020916

(22) International Filing Date:
12 January 2011 (12.01.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/697,235 30 January 2010 (30.01.2010) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

(54) Title: LOW LEAKAGE GAN MOSFET

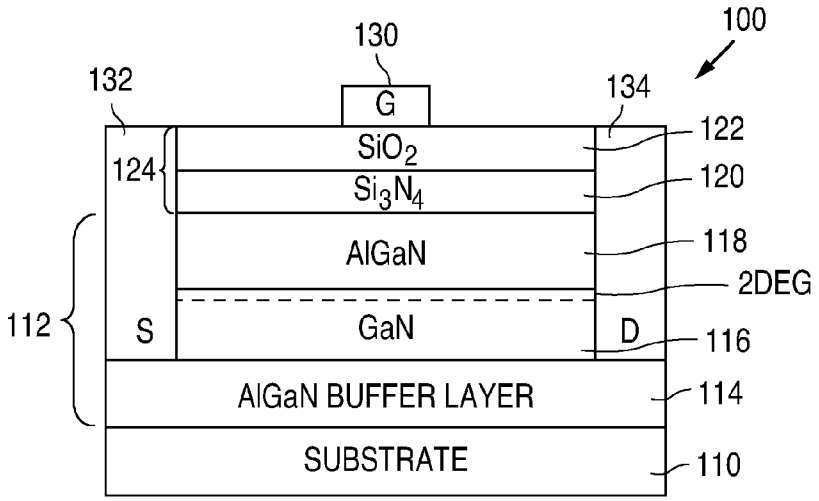

FIG. 4

(57) Abstract: An enhancement-mode GaN MOSFET (100) is formed by utilizing a $Si0_2/Si_3N_4$ gate insulation layer (124) on an AlGaN (or InAlGaN) barrier layer (118). The Si_3N_4 portion (120) of the $Si0_2/Si_3N_4$ gate insulation layer (124) reduces the formation of interface states at the junction between the gate insulation layer (124) and the barrier layer (118), while the SiO2 portion (122) of the SiO_2/Si_3N_4 gate insulation layer (124) reduces the leakage current.

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LOW LEAKAGE GAN MOSFET

TECHNICAL FIELD

The present invention relates to GaN MOSFETs and, more particularly, to an enhancement-mode GaN MOSFET with low leakage current and improved reliability.

BACKGROUND ART

GaN MOSFETS are well known in the art, and are of utilized in high power, high frequency, and high temperature applications. GaN MOSFETS are typically based on the formation of a heterojunction between a GaN region, typically known as the channel layer, and an overlying AlGaN region, typically known as a barrier layer. The GaN channel layer and the AlGaN barrier layer have different band gaps that induce the formation of a two-dimensional electron gas (2DEG) that lies at the junction between the GaN channel layer and the AlGaN barrier layer and extends down into the GaN channel layer.

The 2DEG, which functions as the "channel" of the transistor, produces a high concentration of electrons which causes a conventionally-formed GaN MOSFET to function as a depletion-mode device (nominally on when zero volts are applied to the gate of the device, and the source and drain regions of the device are differently biased).

Although there are applications for depletion-mode GaN MOSFETs, the nominally on state of a depletion-mode transistor requires the use of a control circuit during start up to ensure that source-to-drain conduction within the transistor does not begin prematurely. On the other hand, an enhancement-mode GaN MOSFET (nominally off when zero volts are applied to the gate of the device, and the source and drain regions of the device are differently biased) does not require a control circuit because the transistor is nominally off at start up when zero volts are placed on the gate.

However, to form an enhancement-mode GaN MOSFET, the AlGaN barrier layer must be made thin enough (e.g., a few nm thick) so that when zero volts are applied

to the gate of the device, (and the source and drain regions of the device are differently biased) substantially no electrons are present in the 2DEG region, and when a voltage that exceeds a threshold voltage is applied to the gate of the device, (and the source and drain regions of the device are differently biased), electrons accumulate in the 2DEG region and flow from the source region to the drain region.

One problem with reducing the thickness of the AlGaN barrier layer is that high levels of leakage current can pass through the AlGaN barrier layer to the gate, which is conventionally implemented as a Schottky contact. One solution to this problem is to add a gate insulation layer that lies between the AlGaN barrier layer and the gate.

Current-generation, enhancement-mode GaN MOSFETs use a variety of deposited oxides to form the gate insulation layer. These deposited oxides include Al_2O_3, HfO_2, MgO, Gd_2O_3, Ga_2O_3, ScO_2, and SiO_2. Of all of these oxides, SiO_2 has a bandgap Eg of 9 eV and a ΔEc to AlGaN that can be as high as 2.5 eV, thereby leading to the lowest leakage current and a threshold voltage as high as 2.5 volts.

One problem with all of these deposited oxides, including SiO_2, is that these deposited oxides have a high density of interface states (e.g., greater than $4x10^{11}/cm^2$) that results in a large number of trapping sites at the junction between the gate insulation layer and the AlGaN barrier layer. Large numbers of trapping sites lead to the breakdown of the gate insulation layer which, in turn, reduces the long-term reliability of the GaN devices. Thus, there is a need for an enhancement-mode GaN MOSFET that has a low leakage current.

DISCLOSURE OF INVENTION

An enhancement-mode GaN MOSFET of the present invention utilizes a SiO_2/Si_3N_4 gate insulation layer on an AlGaN (or InAlGaN) barrier layer. The Si_3N_4 portion of the SiO_2/Si_3N_4 gate insulation layer significantly reduces the formation of interface states at the junction between the gate insulation layer and the barrier layer, while the SiO_2 portion of the SiO_2/Si_3N_4 gate insulation layer significantly reduces the leakage current.

The GaN MOSFET of the present invention includes a barrier layer, which includes AlGaN. The GaN MOSFET of the present invention also includes a layer of

Si_3N_4 that touches the barrier layer. The GaN MOSFET of the present invention further includes a layer of SiO_2 that touches and lies over the layer of Si_3N_4, and a metal gate that touches the layer of SiO_2, and lies above the layer of SiO_2, and the layer of Si_3N_4.

A method of forming the GaN MOSFET of the present invention includes forming a barrier layer, which includes AlGaN. The method also includes forming a layer of Si_3N_4 that touches the barrier layer. The method further includes forming a layer of SiO_2 that touches the layer of Si_3N_4, and forming a metal gate that touches and lies over the layer of SiO_2.

BRIEF DESCRIPTION OF DRAWINGS

FIGS. 1-4 are a series of cross-sectional views illustrating an example of a method of forming an enhancement-mode GaN MOSFET 100 in accordance with the present invention.

FIGS. 5-9 are a series of cross-sectional views illustrating an example of a method of forming an enhancement-mode GaN MOSFET 500 in accordance with an alternate embodiment of the present invention.

FIG. 10 is a band diagram illustrating the leakage current in accordance with the present invention.

MODE(S) FOR CARRYING OUT THE INVENTION

As described in greater detail below, the present invention forms a SiO_2/Si_3N_4 gate insulation layer on an AlGaN barrier layer (or optional InAlGaN barrier layer) which significantly reduces the formation of interface states at the junction between the gate insulation layer and the barrier layer. Reducing the density of interface states significantly reduces the number of trapping sites which, in turn, improves the long-term reliability on the GaN devices.

FIGS. 1-4 show a series of cross-sectional views that illustrate an example of a method of forming an enhancement-mode GaN MOSFET 100 in accordance with the present invention. As shown in FIG. 1, the method of the present invention utilizes a

conventionally-formed semiconductor substrate 110. Substrate 110 can be implemented as an insulating substrate or with a highly resistive material such as silicon (e.g., <111>), sapphire, or silicon carbide. As further shown in FIG. 1, the method of the present invention begins by forming an epitaxial layer 112 on substrate 110. Epitaxial layer 112, which is formed in a metal organic chemical vapor deposition (MOCVD) reactor using a conventional process, includes an undoped AlGaN buffer layer 114, an undoped GaN channel layer 116, and an undoped or n-doped AlGaN barrier layer 118 (or optionally an undoped or n-doped InAlGaN barrier layer 118). The AlGaN buffer layer 114, in turn, includes a number of undoped AlGaN layers with different aluminum compositions that are used to mitigate stress.

As shown in FIG. 2, in accordance with the present invention, after epitaxial layer 112 has been formed, a Si_3N_4 layer 120 is epitaxially grown on the AlGaN barrier layer 118 directly in the same MOCVD reactor as the AlGaN barrier layer 118 using SiH_4 and NH_3. In other words, the Si_3N_4 layer 120 is epitaxially grown after the AlGaN layer 118 is grown without removing the structure with the AlGaN layer 118 from the MOCVD reactor.

The Si_3N_4 layer 120 is preferably grown to have a thickness of approximately 10-100nm, with the specific thickness being application dependent. SiN and AlGaN share the same anion and, as a result, produce a transition layer between the Si_3N_4 layer 120 and the AlGaN barrier layer 118 that has a very low density of interfacial states, e.g., expected to be less than $1x10^{11}/cm^2$.

As shown in FIG. 3, after the Si_3N_4 layer 120 has been grown, part of the Si_3N_4 layer 120 is oxidized in a steam/wet rapid thermal oxidation process to form a SiO_2 layer 122 that lies on the remaining Si_3N_4 layer 120. In the present invention, the combination of the Si_3N_4 and SiO_2 layers form a gate insulation layer 124 of the transistor which has, for example, a Si_3N_4 layer that is 64 Å thick and a SiO_2 layer that is 128Å thick. The oxidation of the Si_3N_4 layer 120 produces a transition layer between the Si_3N_4 layer 120 and the SiO_2 layer 122 that also has a very low density of interfacial states.

As shown in FIG. 4, following the formation of SiO_2 layer 122, the method completes the formation of GaN MOSFET 100 by forming a metal gate region 130, a metal source region 132, and a metal drain region 134 in a conventional fashion, e.g.,

using titanium aluminum contacts, followed by the conventional formation of an overlying passivation layer. The metal gate region 130 is formed to touch the SiO_2 layer 122 of gate insulation layer 124. The metal source 132 and metal drain regions 134 are formed to make an ohmic contact with the GaN channel layer 116 and the AlGaN barrier layer 118.

As noted above, the AlGaN of the barrier layer and the GaN of the channel layer have different band gaps, and are conventionally formed to induce a two-dimensional electron gas (2DEG) that lies at the junction between the AlGaN barrier layer and the GaN channel layer and extends down into the GaN channel layer.

As further noted above, the 2DEG, which functions as the "channel" of the transistor, produces a high concentration of electrons which causes a conventionally-formed GaN MOSFET to be a depletion mode device (nominally on when zero volts are applied to the gate of the device and the source and drain regions are differently biased).

Thus, to form GaN MOSFET 100 shown in FIG. 4 as an enhancement-mode device (nominally off when zero volts are applied to the metal gate region 130, and the metal source region 132 and the metal drain region 134 are differently biased), the AlGaN barrier layer 118 must be made thin enough (e.g., a few nm thick) so that when zero volts are applied to the metal gate region 130 (and the metal source region 132 and the metal drain region 134 are differently biased) substantially no electrons are present in the 2DEG region, and when a voltage that exceeds a threshold voltage is a applied to the metal gate region 130 (and the metal source region 132 and the metal drain region 134 are differently biased), electrons accumulate in the 2DEG region and flow from the metal source region 132 to the metal drain region 134.

FIGS. 5-9 show a series of cross-sectional views that illustrate an example of a method of forming an enhancement-mode GaN MOSFET 500 in accordance with an alternate embodiment of the present invention. As shown in FIG. 5, the alternate method of the present invention also utilizes a conventionally-formed semiconductor substrate 510. As with substrate 110, substrate 510 can also be implemented as an insulating substrate or with a highly resistive material such as silicon (e.g., <111>), sapphire, or silicon carbide.

As further shown in FIG. 5, the alternate method of the present invention begins by forming an epitaxial layer 512 on substrate 510 in the same manner that epitaxial layer 112 was formed (in a MOCVD reactor using a conventional process). As a result, epitaxial layer 512 includes an undoped AlGaN buffer layer 514, an undoped GaN channel layer 516, and an undoped or n-doped AlGaN barrier layer 518 (or optionally an undoped or n-doped InAlGaN barrier layer 518). The AlGaN buffer layer 514, in turn, includes a number of undoped AlGaN layers with different aluminum compositions that are used to mitigate stress.

However, unlike GaN MOSFET 100, the AlGaN barrier layer 518 is formed to have a conventional (depletion-mode) thickness and, as a result, induces the formation of a two-dimensional electron gas (2DEG) that lies at the junction between the AlGaN barrier layer 518 and the GaN channel layer 516 and extends down into the GaN channel layer 516. The 2DEG that lies at the junction between the AlGaN barrier layer 518 and the GaN channel layer 516 produces a high concentration of electrons.

As shown in FIG. 6, in accordance with the present invention, after epitaxial layer 512 has been formed, a mask 520, such as a layer of SiO_2, is formed and patterned on the top surface of the AlGaN barrier layer 518. Once mask 520 has been formed, the regions exposed by the mask 520 are dry etched. The dry etch can stop above, at, or below a lowest level of the 2DEG that lies at the top surface of GaN channel layer 516. (FIG. 6 illustrates the dry etch stopping just below the lowest level of the 2DEG.)

As further shown in FIG. 6, the dry etch produces an intermediate MOSFET structure 522 that has an exposed region 524. Following the dry etch, the intermediate MOSFET structure 522 is next baked in H_2 and NH_3 in the MOCVD reactor to repair damage to the lattice that was caused by the dry etch. In other words, the intermediate MOSFET structure 522 is baked after the dry etch without removing the intermediate MOSFET structure 522 from the MOCVD reactor.

As shown in FIG. 7, after the intermediate MOSFET structure 522 has been baked, a thin undoped or n-doped AlGaN barrier film 526 (or optionally a thin undoped or n-doped InAlGaN barrier film 526) is epitaxially grown on the exposed region 524. A top surface of the thin AlGaN barrier film 526 can lie above, at, or below a lowest level of the 2DEG. (FIG. 7 illustrates the top surface of the AlGaN

barrier film 526 lying at the lowest level of the 2DEG.) The thin AlGaN barrier film 526 has a thickness that is less than a largest thickness of the AlGaN barrier layer 518.

Once the thin AlGaN barrier film 526 has been grown, a Si_3N_4 layer 530 is epitaxially grown on the thin AlGaN barrier film 526 directly in the same MOCVD reactor as the thin AlGaN barrier film 526 using SiH_4 and NH_3. In other words, the Si_3N_4 layer 530 is epitaxially grown after the thin AlGaN barrier film 526 is grown without removing the structure with the thin AlGaN barrier film 526 from the MOCVD reactor. (As shown in FIG. 7, the Si_3N_4 layer 530 also grows on the side walls of the AlGaN barrier layer 518 and on the SiO_2 mask 520.)

The Si_3N_4 layer 530 is preferably grown to have a thickness of approximately 10-100nm over the thin AlGaN film 526, with the specific thickness being application dependent. As before, the process produces a transition layer between the Si_3N_4 layer 530 and the thin AlGaN barrier film 526 that has a very low density of interfacial states, e.g., expected to be less than $1x10^{11}/cm^2$.

As shown in FIG. 8, following the growth of the Si_3N_4 layer 530, a part of the Si_3N_4 layer 530 is oxidized in a steam/wet rapid thermal oxidation process to form a SiO_2 region 532 that lies on a Si_3N_4 region 534 which, in turn, lies over the thin AlGaN barrier film 526. As further shown in FIG. 8, the AlGaN barrier layer 518 lies laterally adjacent to the Si_3N_4 region 534. (The oxidation process also oxidizes the Si_3N_4 layer 530 that lies over the SiO_2 mask 520, thereby increasing the thickness of the SiO_2 mask 520.)

In the present invention, the combination of the Si_3N_4 region 534 and the SiO_2 region 532 forms a gate insulation layer 536 that lies over the thin AlGaN film 526 which has, for example, a Si_3N_4 region that is 64 Å thick and a SiO_2 region that is 128Å thick. As before, the oxidation of the Si_3N_4 layer 530 produces a transition layer between the Si_3N_4 region 534 and the SiO_2 region 532 that also has a very low density of interfacial states.

As shown in FIG. 9, following the formation of SiO_2 region 532, the method completes the formation of GaN MOSFET 500 by forming a metal gate region 540, a metal source region 542, and a metal drain region 544 in a conventional fashion, e.g., using titanium aluminum contacts, followed by the conventional formation of an overlying passivation layer. The metal gate region 540 is formed to touch SiO_2 region

532 of gate insulation layer 536. The metal source 542 and metal drain regions 544 are formed to make an ohmic contact with the GaN channel layer 516 and the AlGaN barrier layer 518.

Thus, GaN MOSFET 500 shown in FIG. 9 is formed as an enhancement-mode device (nominally off when zero volts are applied to the metal gate region 540 and the metal source region 542 and the metal drain region 544 are differently biased) by forming the AlGaN barrier film 526 to be thin enough (e.g., a few nm thick) so that when zero volts are applied to the metal gate region 540 (and the metal source region 542 and the metal drain region 544 are differently biased) substantially no electrons accumulate directly under the gate insulation layer 536 and the metal gate region 540, and when a voltage that exceeds a threshold voltage is a applied to metal gate region 540 (and the metal source region 542 and the metal drain region 544 are differently biased), electrons accumulate directly under the gate insulation layer 536 and the metal gate region 540 and flow from the metal source region 542 to the metal drain region 544.

One of the advantages of the present invention is that the Si_3N_4 portion of the SiO_2/Si_3N_4 gate insulation layer significantly reduces the formation of interface states at the junction between the gate insulation layer and the AlGaN barrier layer (or optional InAlGaN barrier layer). Significantly reducing the number of sites where electrons can be trapped significantly improves the long-term reliability of the GaN devices.

A further advantage of the present invention is that by utilizing SiO_2 as the capping layer of the SiO_2/Si_3N_4 gate insulation layer, the present invention has the lowest leakage current and a threshold voltage as high as 2.5 volts (i.e., SiO_2 has a bandgap Eg of 9 eV and a ΔEc to AlGaN that can be as high as 2.5 eV).

FIG. 10 shows a band diagram that illustrates the leakage current in accordance with the present invention. As shown in FIG. 10, the band lineup shows that there is limited tunneling in the gate oxide due to the low density of interface states and the wide band gap of SiO_2. In addition, the effective ΔEc from SiO_2 to AlGaN is greater than 2 eV with a threshold voltage Vt that is greater than 2V.

It should be understood that the above descriptions are examples of the present invention, and that various alternatives of the invention described herein may

be employed in practicing the invention. Therefore, it is intended that the following claims define the scope of the invention and that structures and methods within the scope of these claims and their equivalents be covered thereby.

WHAT IS CLAIMED IS:

1. A method of forming a transistor comprising:

forming a barrier layer, the barrier layer including AlGaN;

forming a layer of Si_3N_4 that touches the barrier layer;

forming a layer of SiO_2 that touches the layer of Si_3N_4; and

forming a metal gate that touches and lies over the layer of SiO_2.

2. The method of claim 1 wherein:

the barrier layer is epitaxially grown in a reactor; and

the layer of Si_3N_4 is epitaxially grown in the reactor after the barrier layer is grown without removing the barrier layer from the reactor.

3. The method of claim 2 wherein the layer of SiO_2 is formed to touch the layer of Si_3N_4 by oxidizing a portion of the layer of Si_3N_4.

4. The method of claim 3 and further comprising forming spaced-apart metal source and drain regions that touch the barrier layer.

5. The method of claim 4 wherein the barrier layer further includes indium.

6. The method of claim 4 and further comprising forming a channel layer before the barrier layer is formed, the channel layer including GaN, a top surface of the channel layer touching a bottom surface of the barrier layer, the channel layer including a two dimensional electron gas that touches the top surface of the channel layer.

7. The method of claim 6 and further comprising selectively etching the barrier layer to form an exposed region before the layer of Si_3N_4 is formed.

8. The method of claim 7 and further comprising forming a barrier film to touch the exposed region before the layer of Si_3N_4 is formed, the barrier film including AlGaN.

9. The method of claim 8 wherein the layer of Si_3N_4 is formed to touch and lie over the barrier film.

10. The method of claim 6 and further comprising selectively etching the barrier layer and the channel layer to form an exposed region before the layer of Si_3N_4 is formed.

11. The method of claim 10 and further comprising forming a barrier film to touch the exposed region before the layer of Si_3N_4 is formed, the barrier film including AlGaN.

12. The method of claim 11 wherein the layer of Si_3N_4 is formed to touch the barrier film.

13. The method of claim 12 wherein the barrier layer further includes indium, and the barrier film further includes indium.

14. A transistor comprising:

a barrier layer, the barrier layer including AlGaN;

a layer of Si_3N_4 that touches the barrier layer;

a layer of SiO_2 that touches and lies over the layer of Si_3N_4; and

a metal gate that touches the layer of SiO_2, and lies above the layer of SiO_2, and the layer of Si_3N_4.

15. The transistor of claim 14 and further comprising spaced-apart metal source and drain regions that touch the barrier layer.

16. The transistor of claim 15 wherein the barrier layer further includes indium.

17. The transistor of claim 15 and further comprising a channel layer that touches and lies below the barrier layer, the channel layer including GaN, the channel layer including a two dimensional electron gas that touches the top surface of the channel layer.

18. The transistor of claim 17 and further comprising a barrier film that touches and lies below the layer of Si_3N_4, the barrier film having a thickness that is less than a largest thickness of the barrier layer, the barrier film including AlGaN.

19. The transistor of claim 18 wherein the barrier layer lies laterally adjacent to the layer of Si_3N_4.

20. The transistor of claim 19 wherein the barrier layer further includes indium.

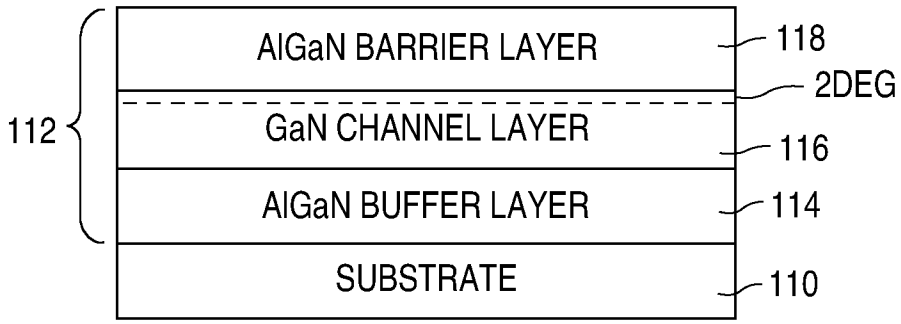


FIG. 1

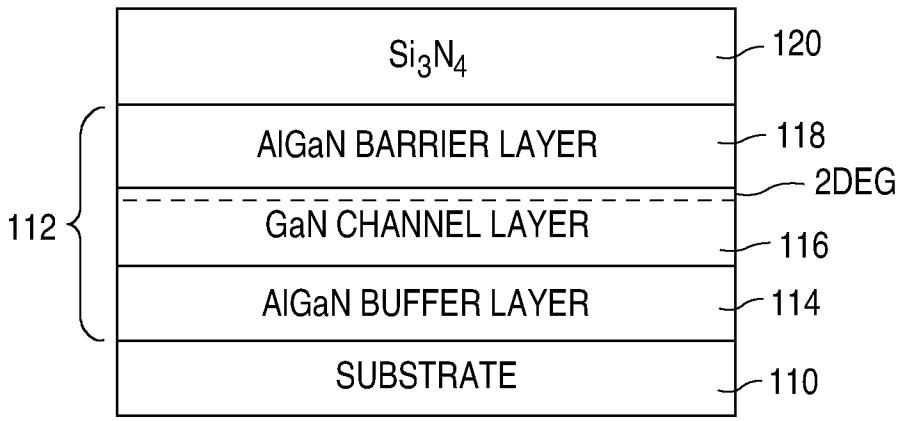


FIG. 2

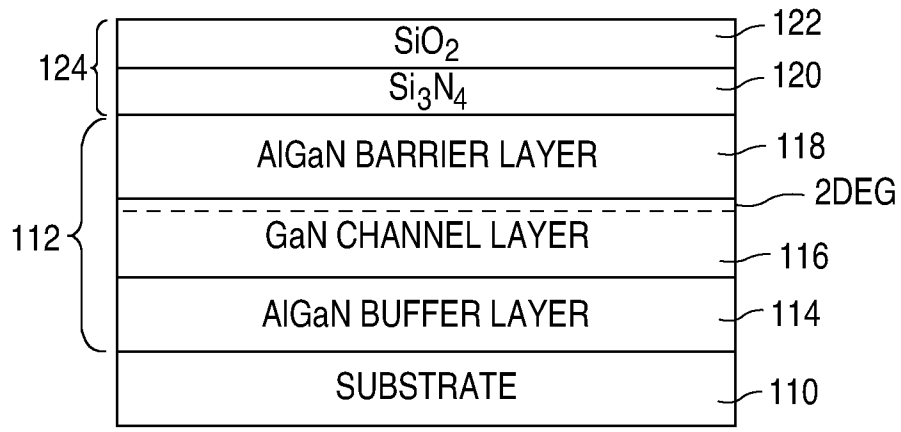


FIG. 3

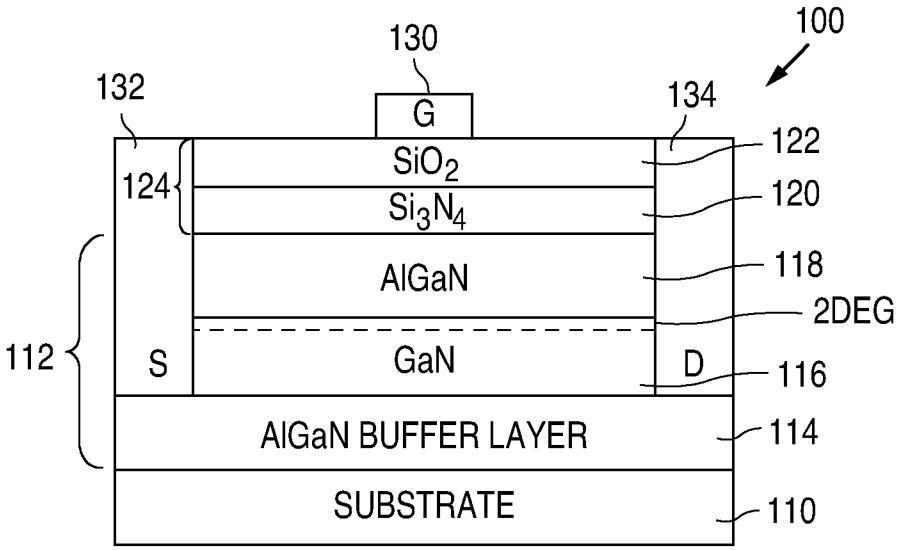


FIG. 4

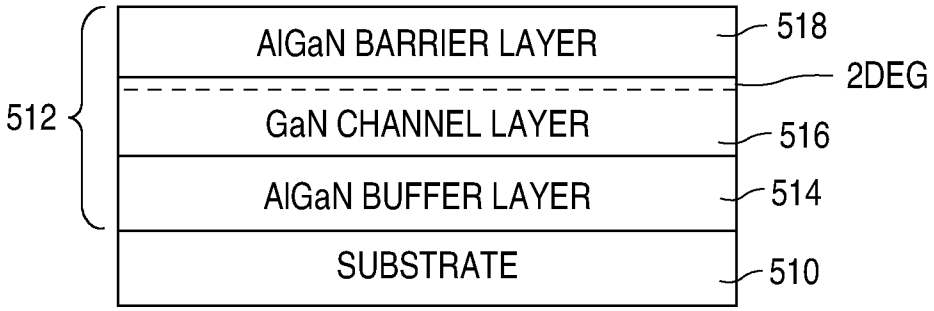


FIG. 5

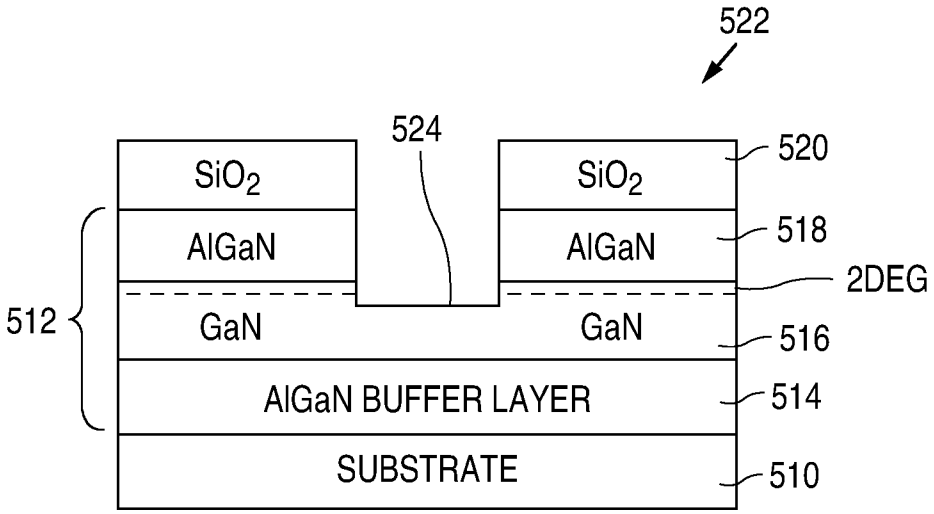
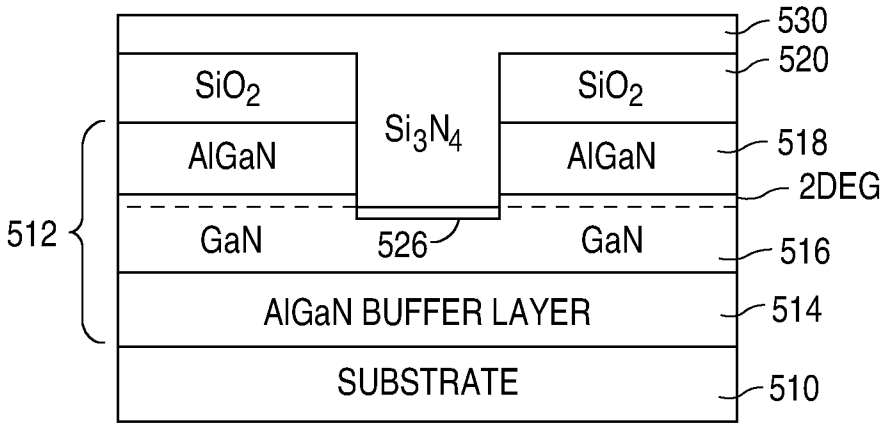


FIG. 6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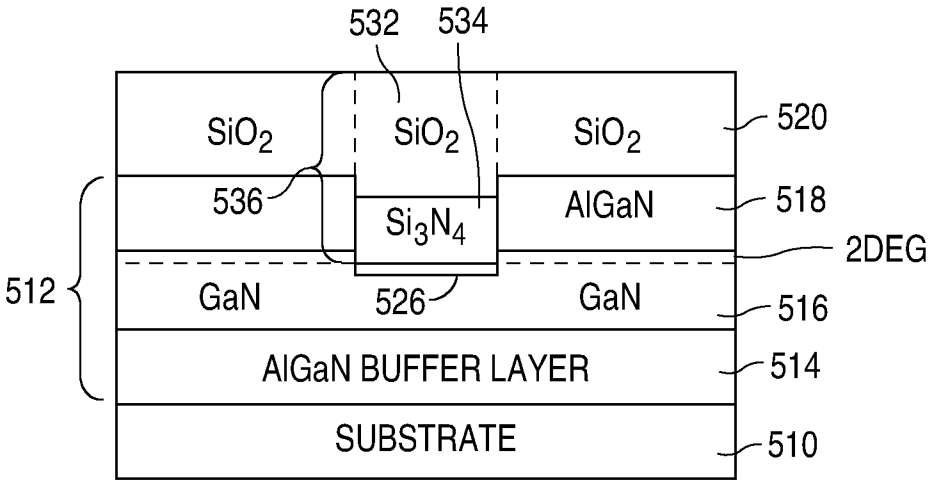
520
SiO_2
Si_3N_4
SiO_2
AlGaN
AlGaN
518
2DEG
512
GaN
526
GaN
516
AlGaN BUFFER LAYER
514
SUBSTRATE
510

FIG. 7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SiO_2
SiO_2
520
536
Si_3N_4
AlGaN
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2DEG
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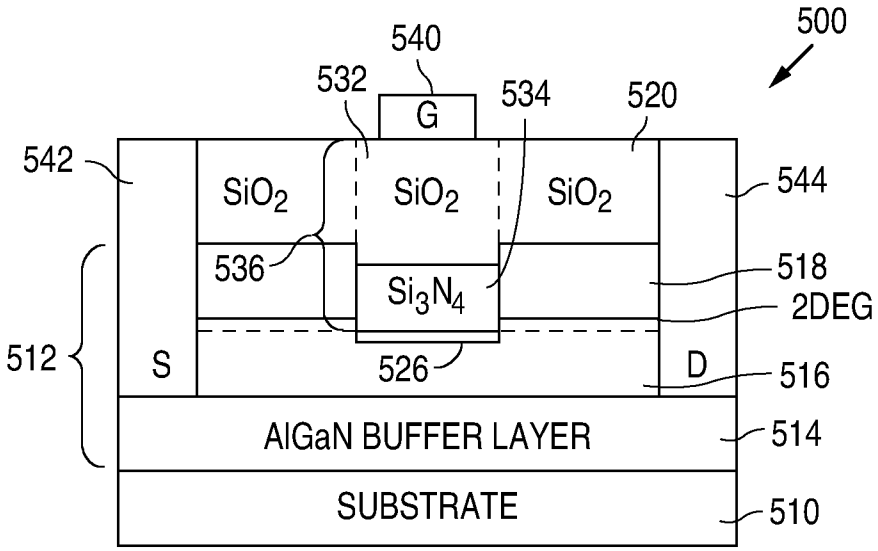
GaN
526
GaN
516
AlGaN BUFFER LAYER
514
SUBSTRATE
510

FIG. 8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SiO_2
SiO_2
544
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2DEG
512
S
526
D
516
AlGaN BUFFER LAYER
514
SUBSTRATE
510

FIG. 9

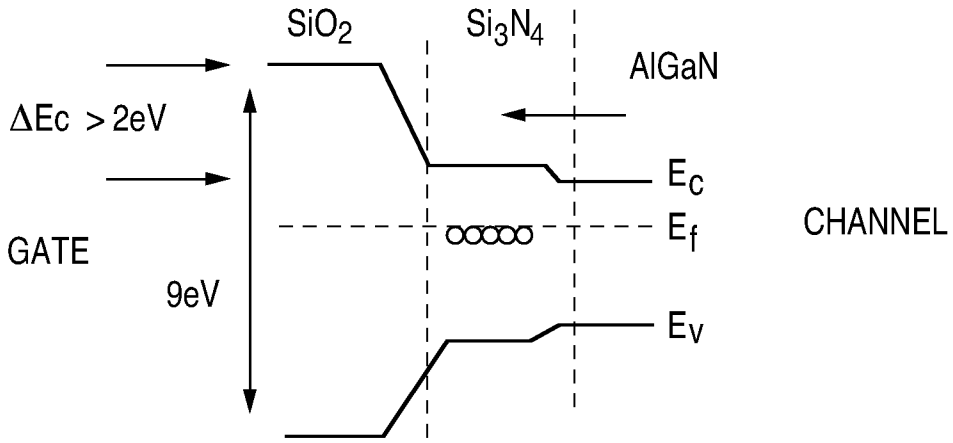
SiO_2
Si_3N_4
AlGaN
ΔEc > 2eV
E_c
E_f
CHANNEL
GATE
9eV
E_v

FIG. 10