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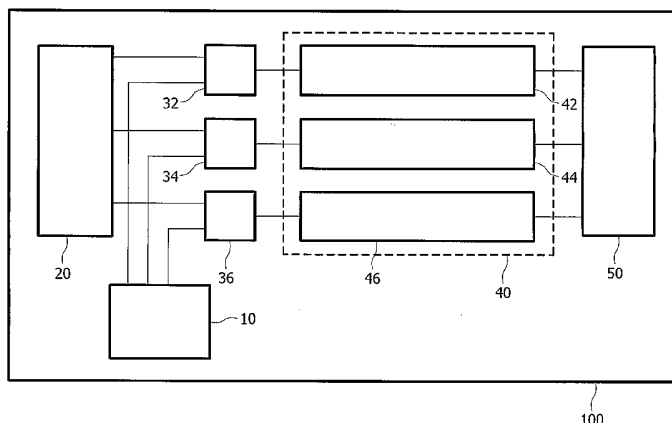
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(54) Title: CIRCUIT ARRANGEMENT AND METHOD OF TESTING AN APPLICATION CIRCUIT PROVIDED IN SAID CIRCUIT ARRANGEMENT



(57) Abstract: The object being to develop an integrated circuit arrangement (100) with at least one application circuit (40) to be tested, and with at least one self-test circuit (10, 20, 32, 34, 36, 50) provided for testing the application circuit (40) and generating at least one pseudo-random test sample, wherein said pseudo-random test sample can be converted into at least one test vector that is programmable and/or deterministic and that can be supplied to the application circuit (40) for testing purposes via at least one logic gate (32, 34, 36) and by means of at least one signal that can be applied to said logic gate (32, 34, 36), and wherein the output signal arising in dependence on the deterministic test vector can be evaluated by the application circuit (40) by means of at least one signature register (50), as well as a method of testing the application circuit (40) present in the integrated circuit arrangement (100) by means of the self-test circuit (10, 20, 32, 34, 36, 50) further such that the B[uild-I][n]S[elf-T]est hardware connected to the additional deterministic logic can be reduced, it is suggested that the signal to be supplied to the logic gate (32, 34, 36) can be made available by a B[it]F[lipping]F[unction] logic circuit (10) based on at least one

WO 2006/003596 A2



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Circuit arrangement and method of testing an application circuit provided in said circuit arrangement

Field of the invention

The invention relates to an integrated circuit arrangement with at least one application circuit to be tested, and with at least one self-test circuit provided for testing the application circuit and generating at least one pseudo-random test sample,

5 wherein said pseudo-random test sample can be converted into at least one test vector that is programmable and/or deterministic and that can be supplied to the application circuit for testing purposes

via at least one logic gate and

by means of at least one signal that can be applied to said logic gate,

10 and

wherein the output signal arising in dependence on the deterministic test vector can be evaluated by the application circuit by means of at least one signature register.

(cf. prior-art publication DE 102 01 554 A1).

15 The invention further relates to a method of testing at least one application circuit provided in such an integrated circuit arrangement by means of at least one self-test circuit.

Background of the invention

20 It is a general wish in the manufacture of integrated circuits to test these integrated circuits as to their functionality. Such tests can be carried out by means of external testing arrangements. In an external test, however, many production-related problems and high expenses occur owing to

- the very high integration density of such integrated circuits,
- 25 - the very high clock frequencies at which these integrated circuits operate, and
- the very large number of test vectors required, which lead to complicated V[ery]L[arge]S[cale]I[n]tegration testing systems with large test vector memories.

The prior-art publication US 6,061,818, US 6,671,838, US 6,684,358, and US 2003/0140293 A1 disclose possibilities for realizing such test arrangements; additionally, reference is made to the publications DE 100 38 327 A1 and DE 101 10 777 A1 from the prior art.

5 The test arrangements disclosed in these publications, however, are not suitable inter alia for solving test problems which are caused substantially by high I[n]tegrated]C[ircuit] internal clock frequencies and I[n]put]O[utput] bond pad stages that are very slow in comparison with the former. The high internal clock frequencies of the integrated circuits have indeed an unfavorable ratio to the comparatively very slow
10 input/output bond pad stages that lead to the exterior.

It is desirable for this reason to have available a kind of self-test of the integrated circuit. A self-test circuit is provided in that case within the integrated circuit, serving to test the application circuit also provided in the integrated circuit. The application circuit is that circuit that is designed for the actual practical purpose of the integrated circuit.

15 A first step in solving the above problems is the use of the so-termed B[uild-]I[n]S[elf-]T[est] method. Conventionally, the circuit is made better capable of random testing, for example by the insertion of test points, or a so-termed B[it-]F[lipping]F[unction] is used.

20 The conventional implementation based on logic gates of the additional deterministic logic BIST hardware (the so-termed DLBIST hardware) here leads to a too large additional DLBIST hardware in practice with real, large integrated circuit arrangements.

Short description of the invention: object, solution, advantages

25 Given the disadvantages and imperfections described above, and taking into account the relevant prior art, the present invention has for its object to develop an integrated circuit arrangement of the kind mentioned in the opening paragraph and a method of the kind mentioned above further such that the additional B[uild-]I[n]S[elf-]T[est] hardware can be reduced.

30 This object is achieved by means of an integrated circuit arrangement having the characterizing features of claim 1 and a method having the characterizing features of claim 6. Advantageous embodiments and useful further developments of the invention are characterized in the respective dependent claims.

The present invention is thus based on the principle of a R[ead]O[nly]M[emory] implementation which is an alternative to the conventional gate-based implementation. The B[it-]F[lipping]F[unction] used in this connection renders possible an error coverage of one hundred percent, which is not the case, for example, in a system based on waiting logic (for delimiting the present invention, for example, a so-termed waiting logic is used for improving the error coverage in the document US 6,671,838 or the document US 2003/0140293 of the prior art).

According to the teachings of the present invention, it is achieved that the additional deterministic logic BIST hardware (so-termed DLBIST hardware) can be clearly reduced, i.e. the percentage of the DLBIST hardware has a more profitable ratio to the total surface area of the integrated circuit than is the case in the gate-based implementation (an additional DLBIST hardware surface area of 50% can definitely not be regarded as profitable, whereas a small DLBIST hardware surface area of a few percents can in this respect).

The essential advantage of the present invention is that a clear saving in surface area is made owing to the implementation of the DLBIST hardware based on a R[ead]O[nly]M[emory] compared with the conventional gate-based implementation, so that the additional DLBIST hardware is reduced to an acceptable surface area. The consequence of this area reduction is a clear cost reduction for the integrated circuit with the built-in logic self-test according to the present invention.

The invention finally relates to the use of at least one integrated circuit arrangement of the kind described above and/or a method of the kind described above for testing at least one application circuit.

The present invention accordingly relates to the technical field of integrated circuits (ICs), their design for testability (DfT), their computer-aided design (CAD), and their computer-aided testing (CAT); the present invention in particular relates to integrated circuit arrangements with very high integration densities and built-in self-test logic (so-termed BIST logic) for finding production defects in the logic part of the circuit.

Short description of the drawings

As was noted above, there are various possibilities for implementing and further developing the teachings of the present invention in an advantageous manner. Reference is made in this respect to the claims dependent on claim 1 and those dependent on claim 6, while furthermore other embodiments, features, and advantages of the present

invention are explained in more detail below, inter alia with reference to two embodiments shown in Figs. 1 to 2B and given by way of example only.

In the drawing:

Fig. 1 is a block diagram of an embodiment of an integrated circuit arrangement according to the invention operating by the method according to the invention;

Fig. 2A is a block diagram of a first embodiment for a ROM-based BFF logic circuit in the circuit arrangement of Fig. 1; and

Fig. 2B is a block diagram of a second embodiment for a ROM-based BFF logic circuit in the circuit arrangement of Fig. 1.

Identical or similar embodiments, elements, or features have been given the same reference numerals in Figs. 1 to 2B.

Description of preferred embodiments

Fig. 1 is a block diagram of an integrated circuit arrangement (IC) 100 which comprises an application circuit 40. The application circuit 40 is that circuit that is designed for the practical use of the integrated circuit 100.

There is a desire to test the application circuit 40 for perfect operation after manufacture of the IC 100. For this purpose, a self-test circuit is provided on the integrated circuit 100, comprising the circuit elements 10, 20, 32, 34, 36, 50 as shown in Fig. 1.

In the integrated circuit 100 according to the invention, this self-test circuit is designed such that the associated circuit elements 10, 20, 32, 34, 36, 50 are arranged fully outside the application circuit 40, so that the behavior of the application circuit 40 during normal operation is not influenced by the self-test circuit.

It is assumed for the embodiment of Fig. 1 that the application circuit 40 comprises two circuit chains (so-termed scan chains with reference numerals 42, 44, 46), which chains are shift registers. Within the scope of the invention, however, it is alternatively possible that

- only one chain or only two chains, i.e. fewer shift registers, or
- more than three chains, i.e. further shift registers are provided. Furthermore, further circuit elements may be present.

The self-test circuit includes a linear feedback shift register (LFSR) 20 which supplies a pseudo-random sequence of test samples and that is usually fitted with an integrated or downstream-connected phase shifter. Since the shift register 20 is fed back and

has only a finite length, this test sample sequence is not genuinely random, i.e. the test sample sequence exhibits a pattern that repeats itself at certain intervals.

Since this test sample sequence does not fully comprise all test samples that are optimally designed for testing the application circuit 40, first logic gates 32, 34, 36 are provided, which are each constructed as a bit flipper block, in particular each as a XOR logic link, which gates change the output signals of the linear fed-back shift register 20 such that test samples having a programmable and deterministic structure arise at the outputs of the first logic gates 32, 34, 36 and thus at the inputs of the application circuit 40 or its circuit chains 42, 44, 46.

This is achieved in that signals are supplied to the first logic gates 32, 34, 36 by a bit flipping function (BFF) logic 10 provided within the integrated circuit 100, by means of which signals the first logic gates 32, 34, 36 modify individual bits of the test sample supplied by the linear fed-back shift register 20 such that desired deterministic test samples are created.

The test vectors are supplied to the circuit chains 42, 44, 46 within the application circuit 40 in the embodiment of Fig. 1. Owing to these test samples, the circuit chains 42, 44, 46 supply output signals within the application circuit 40 which reach a signature register 50 (a so-called multiple input signature register or MISR).

The signature register 50 is constructed such that it forms a combination of the test results over a plurality of test cycles, each comprising one test sample, and supplies a so-called signature after the test procedure, which signature has to exhibit a certain, predetermined value in the case of a zero-defect performance of the application circuit 40.

It is ensured in this manner that those bits that reach the signature register 50 during testing can definitely be evaluated. This in its turn means that the signature result present in the signature register 50 after the performance of several test cycles can be fully evaluated and supplies a reliable test result.

An essential advantage of the integrated circuit 100 according to the invention with the self-test circuit 10, 20, 32, 34, 36, 50 is that the application circuit 40 need not be modified for the test processes; this means that the application circuit 40 can be constructed in a manner which is an optimum for the use of the application circuit 40. The self-test circuit 10, 20, 32, 34, 36, 50 does not influence the normal operation of the application circuit 40 in its practical use in any way whatsoever.

Furthermore, the self-test circuit 10, 20, 32, 34, 36, 50 according to the invention renders it possible to carry out a test of the application circuit 40 on the chip, so

that comparatively slow bond pad connections do not interfere with the testing, and the operation of the application circuit 40 can take place at maximum clock speeds.

The object being to achieve a significant surface area reduction of the modified hardware, and accordingly a clear cost reduction of the integrated circuit 100 with the built-in logic self-test according to the present invention, the essential feature of the circuit 100 shown in Fig. 1 lies in the fact that the BFF logic 10 is realized by means of a ROM-based process control.

The various combinations 104o2 (cf. Figs. 2A and 2B) for the bit flipper (BF) blocks 32, 34, 36 and the information as to when these combinations 104o2 are to be created (so-called wait signals 104o1) are laid down in a special micro read-only memory (ROM) unit 102.

A counter 122 constructed as a downcounter is loaded with the number of waiting cycles 104o1 from the micro ROM 102. As long as the value of this counter is not equal to zero, the bit flip (BF) blocks 32, 34, 36 should be inactive. The counter 122 accordingly generates a signal 122o2 (for example flip = "1") which is combined with the bits of the combination 104o2 via a second logic gate 132 AND, thus preventing a flipping of the bit flip (BF) blocks 32, 34, 36.

The counter 122 counts backwards. If the counter position of this downcounter 122 is equal to zero, a "1" state is generated, and the combination 104o2 in the micro ROM 102 activates the bit flip (BF) blocks 32, 34, 36. At the same time, an address counter 112 increments the counter unit 122 by means of the first output signal (= increment or "inc" signal referenced 122o1), thus pointing to the next value of the micro ROM 102 (<--> output signal 112o of the address counter unit 112); the waiting cycles 104o1 of the micro ROM 102 are then loaded into the counter 122 again.

Fig. 2B shows how the micro ROM can be subdivided into three smaller ROMs 102', 104, 106 in a second embodiment of the ROM-based BFF logic circuit 10 in the circuit arrangement 100 of Fig. 1 that is further optimized as regards chip surface area compared with the first embodiment of Fig. 2A. The redundant information present in the micro ROM is reduced thereby for the purpose of further minimizing the chip surface area for the bit flipping logic 10.

This embodiment utilizes the circumstance that only few different combinations 104o2 occur as a rule, i.e. many combinations occur often in the micro ROM. Fifty percent or more of the total ROM surface area can be saved in practical circuits in that

these few different combinations 104o2 are encoded and the actual combination that are many bits wide are stored in a separate ROM.

The various addresses of the combinations 104o2 for the bit flipper (BF) blocks 32, 34, 36 are stored in an individual ROM, the so-termed "Comb-ROM" or
5 combination ROM 106, whose output signal 106o is fed to the second AND logic gate 132.

The interface ROM 104 comprises the addresses of the combinations 104o2 and the number of waiting cycles 104o1 until the next combination 104o2 is applied to the bit flipper 32, 34, 36.

The word width of the micro ROM 102' is given by the number of different
10 wait combinations 104o1, 104o2.

The wait signals 104o1 in the interface ROM 104 activate the downcounter 122, which counts down to zero from the wait value. As long as the value of this downcounter 122 is not equal to zero, the bit flippers 32, 34, 36 should not be active; the downcounter 122 delivers the value "1" during this time to the AND gate 132 in front of the
15 bit flippers 32, 34, 36, thus preventing the bit flipping.

When the downcounter 122 has reached the zero value, the value "1" is supplied to the AND gate 132 in front of the bit flippers 32, 34, 36; the individual bit flippers 32, 34, 36 can then flip in accordance with the value of the Comb-ROM via the output signal 132o of the second logic gate 132.

20 When the downcounter 122 has reached the zero value, the address counter 112 is incremented, and the next address of the micro ROM 102' is thus selected via the address output signal 112o of the address counter unit 112.

The present invention clearly distinguishes itself from the embodiment from the publication US 6,061,818 of the prior art, because in the embodiment of the publication
25 US 6,061,818 a bit-fixing sequence generator generates

- a fix signal for the state "0" on an OR linking logic, or
- a fix signal for the state "1" on an AND linking logic.

In the present invention, by contrast, there is always only one control signal which arises from the ROM-based BFF logic 10 and to which a XOR linking logic 32, 34, 36 is applied in
30 each case.

Furthermore, the present invention also clearly distinguishes itself from the embodiment of the publication US 6,684,358 of the prior art in that no full self-test takes place in the embodiment of US 6,684,358, because a test system is still always required for making available the test stimuli: furthermore, the linear feedback shift register (LFSR)

constructed as a decompressor in the embodiment of US 6,684,358 has a connection to chip inputs, in contrast to the present invention.

Overall, the self-test circuit 10, 20, 32, 34, 36, 50 according to the invention, and in particular the ROM-based BFF logic 10 according to the invention, enable a testing of the application circuit 40 on the chip without being subject to any restrictions. No
5 modification of the application circuit 40 is required, so that this application circuit 40 can be optimally designed for its practical function.

According to the invention, a testing at full clock speeds is also possible, because the slow, external bond pad connections need not be used for testing.

10 All test processes are also possible without restrictions for those application circuits that comprise components with a storage or analog behavior.

It is furthermore safeguarded that only those test samples reach the circuit 40 under test for which it is true that they are actually the desired deterministic or random test samples. Nevertheless, the constructional expenditure of the ROM-based BFF logic 10, and
15 thus also the space requirement on the integrated circuit, can be kept small.

List of reference numerals

100	integrated circuit arrangement, in particular integrated circuit chip
10	bit flipping function (BFF) logic circuit
20	shift register, for example linear backfed shift register, in particular with integrated and/or downstream phase shifter
5 32	logic gate associated with the first circuit chain 42, in particular bit flipper (BF) block, in particular XOR logic link
34	logic gate associated with the second circuit chain 44, in particular bit flipper (BF) block, in particular XOR logic link
36	logic gate associated with the third circuit chain 46, in particular bit flipper (BF) block, in particular XOR logic link
10 40	application circuit
42	first circuit chain
44	second circuit chain
46	third circuit chain
15 50	signature register, in particular multiple input signature register
102	read-only memory (ROM) unit, in particular micro ROM unit (first embodiment, cf. Fig. 2A)
102'	read-only memory (ROM) unit, in particular micro ROM unit (second embodiment, cf. Fig. 2B)
20 104	interface ROM unit (second embodiment, cf. Fig. 2B)
104o1	first output signal, in particular wait cycle or wait signal, of the ROM unit 102 or interface ROM unit 104
104o2	second output signal, in particular combination signal of the ROM unit 102 or interface ROM unit 104
25 106	combination ROM unit (second embodiment, cf. Fig. 2B)
106o	output signal of the combination ROM unit 106 (second embodiment, cf. Fig. 2B)
112	address counter unit

- 112o output signal, in particular address or address signal, of the address counter unit 112
- 122 counter unit, in particular downcounter
- 122o1 first output signal, in particular increment or “inc” signal, of the counter unit 122
- 5 122
- 122o2 second output signal of the counter unit 122
- 132 second logic gate, in particular AND gate
- 132o output signal of the second logic gate 132

CLAIMS

1. An integrated circuit arrangement (100)
with at least one application circuit (40) to be tested, and
with at least one self-test circuit (10, 20, 32, 34, 36, 50) provided for testing the
application circuit (40) and generating at least one pseudo-random test sample,
5 wherein said pseudo-random test sample can be converted into at least one test
vector that is programmable and/or deterministic and that can be supplied to
the application circuit (40) for testing purposes
via at least one logic gate (32, 34, 36) and
by means of at least one signal that can be applied to said logic gate
10 (32, 34, 36), and
wherein the output signal arising in dependence on the deterministic test
vector can be evaluated by the application circuit (40) by means of at least one
signature register (50),
characterized in that the signal to be supplied to the logic gate (32, 34, 36) can be made
15 available by at least one B[it]F[lipping]F[unction] logic circuit (10) based on a
R[ead]O[nly]M[emory].
2. A circuit arrangement (100) as claimed in claim 1, characterized in that the
self-test circuit (10, 20, 32, 34, 36, 50) comprises at least one linear feedback shift register
20 (20), in particular with at least one integrated and/or downstream phase shifter, for the
purpose of generating the pseudo-random test sample.
3. A circuit arrangement (100) as claimed in claim 1 or 2, characterized in that
the logic gate (32, 34, 36) is constructed as at least one B[it]F[lipper] block, in particular as at
25 least one XOR logic link.

4. A circuit arrangement (100) as claimed in at least one of the claims 1 to 3, characterized in that the B[it]F[lipping]F[unction] logic circuit (10) comprises:

- at least one R[e]a[d]O[nly]M[emory] unit (102; 102'), in particular a micro ROM unit,
- at least one address counter unit (12) whose output signal (112o) can be applied to the R[e]a[d]O[nly]M[emory] unit (102; 102'),
- at least one counter unit (122), in particular a downcounter unit, to which at least a first output signal (104o1) of the R[e]a[d]O[nly]M[emory] unit (102) can be applied, and which activates the address counter unit (112) by means of at least a first output signal (122o1), and
- at least a second logic gate (132), in particular at least an AND logic link, to which at least a second output signal (122o2) of the counter unit (122) and at least a second output signal (104o2) of the R[e]a[d]O[nly]M[emory] unit (102) can be applied.

5. A circuit arrangement (100) as claimed in claim 4, characterized in that the R[e]a[d]O[nly]M[emory] unit is subdivided into:

- at least one micro ROM unit (102') to which the output signal (112o) of the address counter unit (112) can be applied,
- at least one interface ROM unit (104) which supplies its first output signal (104o1) to the counter unit (122), and
- at least one combination ROM unit (106) to which the second output signal (104o2) of the interface ROM unit (104) can be applied.

6. A method of testing at least one application circuit (40) provided in an integrated circuit arrangement (100) by means of at least one self-test circuit (10, 20, 32, 34, 36, 50), comprising the following steps:

[i] generating at least one pseudo-random test sample by means of the self-test circuit (10, 20, 32, 34, 36, 50);

[ii] modifying the pseudo-random test sample

-by means of at least one logic gate (32, 34, 36) and

-by means of at least one signal that can be made available by a

B[it]F[lipping]F[unction] logic circuit (10) based on at least one R[e]a[d]O[nly]M[emory] and that can be applied to the logic gate (32, 34, 36),

into at least one programmable and/or deterministic test vector that can be supplied to the application circuit (40) for testing purposes;

[iii] evaluating the output signal obtained from the application circuit (40) in dependence on the deterministic test vector by means of at least one signature register (50).

5

7. A method as claimed in claim 6, characterized in that at least one R[ead]O[nly]M[emory] unit (102; 102') of the B[it]F[lipping]F[unction] logic circuit (10) has applied to it at least one output signal (112o) of at least one address counter unit (112) of the B[it]F[lipping]F[unction] logic circuit (10).

10

8. A method as claimed in claim 7, characterized in that at least one counter unit (122) of the B[it]F[lipping]F[unction] logic circuit (10)

- has applied to it at least a first output signal (104o1) of the R[ead]O[nly]M[emory] unit (102), and

15

- applies at least a first output signal (122o1) to the address counter unit (112).

9. A method as claimed in claim 8, characterized in that at least a second logic gate (132) of the B[it]F[lipping]F[unction] logic circuit (10) has applied to it

- at least a second output signal (122o2) of the counter unit (122), as well as

20

- at least a second output signal (104o2) of the R[ead]O[nly]M[emory] unit (102).

10. The use of at least one integrated circuit arrangement (100) as claimed in at least one of the claims 1 to 5 and/or of a method as claimed in at least one of the claims 6 to 9 for testing at least one application circuit (40) and/or for finding errors, in particular

25

manufacturing defects, in the logic part of the application circuit (40).

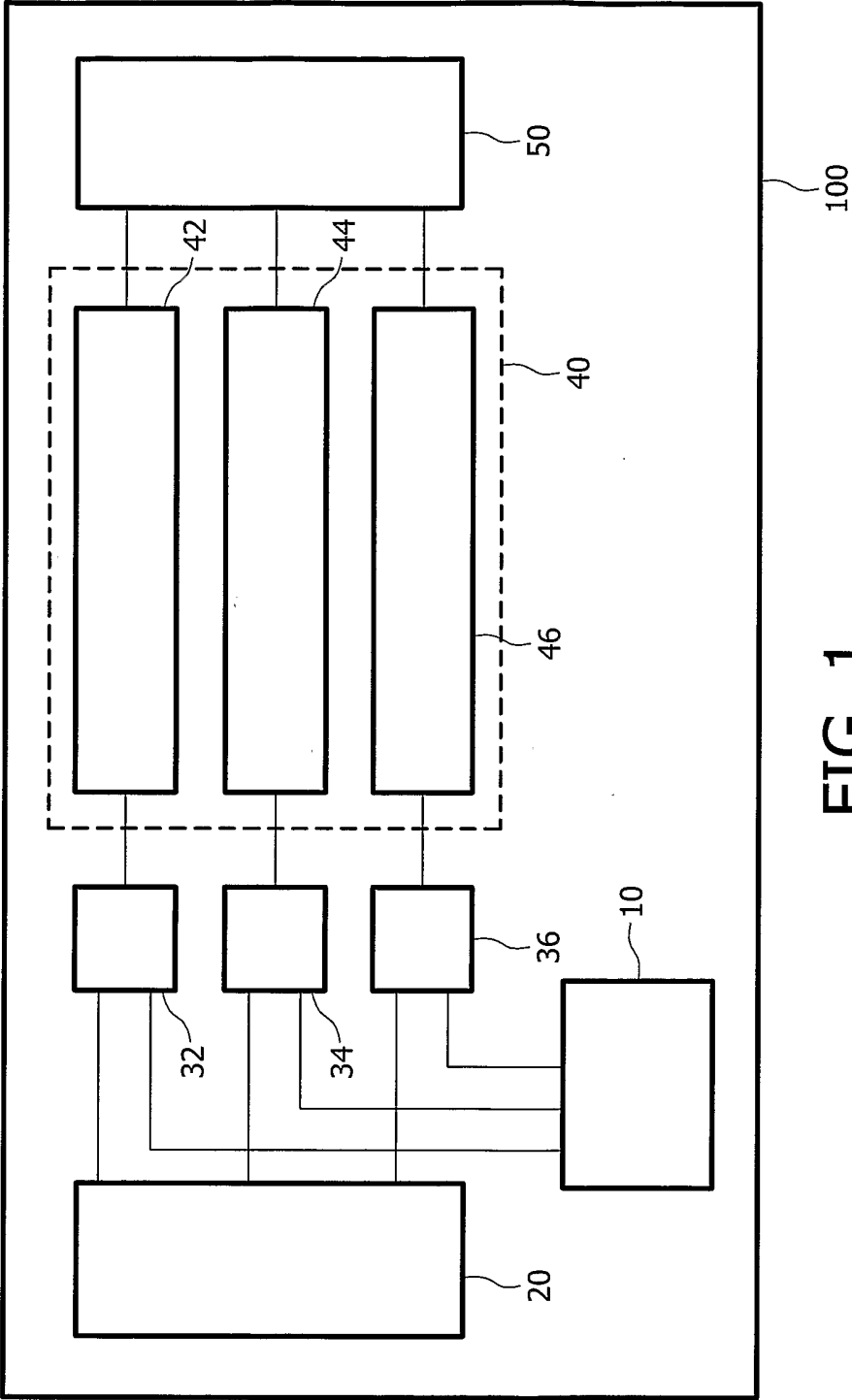


FIG. 1

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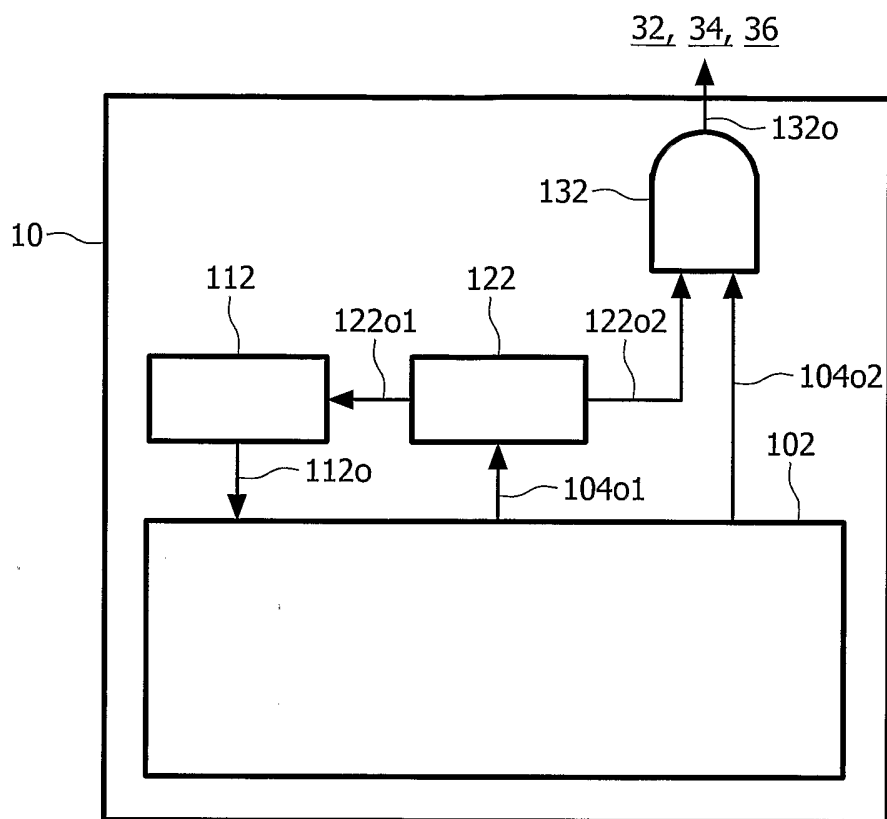


FIG. 2A

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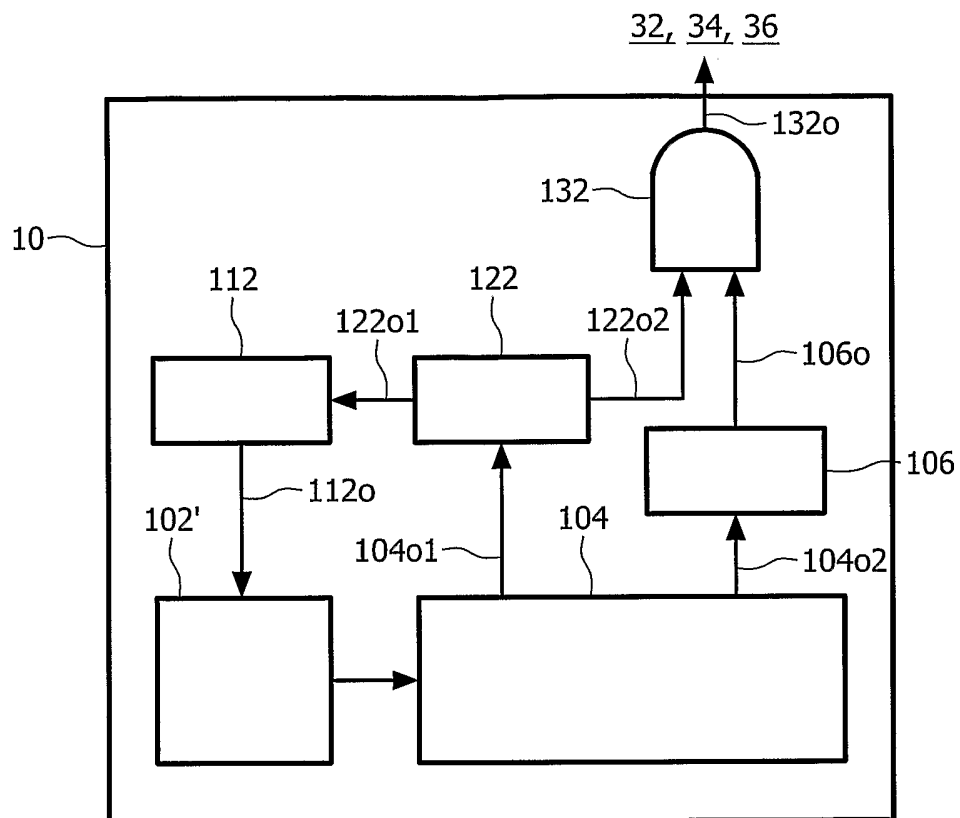


FIG. 2B