



(51) International Patent Classification:

H01L 29/10 (2006.01) *H01L 29/78* (2006.01)
H01L 29/08 (2006.01) *H01L 29/66* (2006.01)

(21) International Application Number:

PCT/US2017/031633

(22) International Filing Date:

09 May 2017 (09.05.2017)

(25) Filing Language:

English

(26) Publication Language:

English

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(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO,
DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,
HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KH, KN, KP, KR,
KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG,
MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM,
PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC,

(54) Title: TRANSISTOR ARRANGEMENTS WITH UNEVEN GATE-DRAIN SURFACES

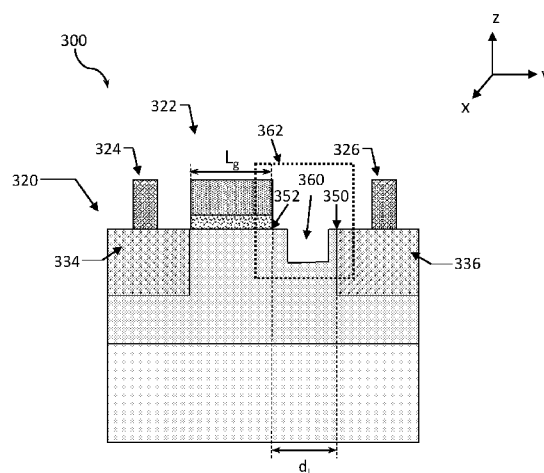


FIG. 3



(57) Abstract: Disclosed herein are transistor arrangements in which a surface between a gate stack and a drain region is uneven in that it has one or more recesses or/and protrusions. An exemplary transistor arrangement/structure includes a semiconductor material in which a channel of a transistor will be formed during operation, a gate electrode stack provided over a first portion of the semiconductor material, and a drain region that is provided at a distance to the gate stack (i.e. is not adjacent to the gate stack), in a second portion of the semiconductor material, where a surface of the semiconductor material between the gate electrode stack and the drain region includes at least one recess or/and protrusion. Ensuring that a surface of a semiconductor material in a portion of a transistor between a gate electrode stack and a drain region is not flat advantageously allows implementing transistors with relatively high breakdown voltages without having to occupy large die area.



SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR,
TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *of inventorship (Rule 4.17(iv))*

Published:

- *with international search report (Art. 21(3))*

TRANSISTOR ARRANGEMENTS WITH UNEVEN GATE-DRAIN SURFACESTechnical Field

[0001] This disclosure relates generally to the field of semiconductor devices, and more specifically, to transistor devices/arrangements where a surface between a gate stack and a drain region is uneven in that it has one or more recesses or/and protrusions.

Background

[0002] During operation of a transistor, current flows between source and drain terminals of the transistor. The source and drain terminals are connected to individual highly doped regions separated by a body region made of a channel material. The source and drain regions can have any conductivity type (e.g. can be either P-type or N-type), as long as they are of the same type and of opposite conductivity type to the body region. Performance (i.e. on-resistance) of source and drain regions affects performance of a transistor.

Brief Description of the Drawings

[0003] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0004] FIGS. 1A and 1B are different cross-sectional views of an exemplary conventional tri-gate MOS transistor.

[0005] FIG. 2 is a cross-sectional side view of an exemplary conventional extended drain (ED) MOS transistor (EDMOS).

[0006] FIG. 3 is a cross-sectional side view of an example FinFET having an uneven gate-drain surface, in accordance with various embodiments.

[0007] FIGS. 4A-4D provide enlarged views of various portions of the cross-sectional side view as shown in FIG. 3 which include different uneven profiles of a gate-drain surface, in accordance with various embodiments.

[0008] FIG. 5 is a perspective view of an example FinFET, in accordance with various embodiments.

[0009] FIG. 6 is a perspective view of an example all-around gate transistor, in accordance with various embodiments.

[0010] FIG. 7 is a flow diagram of an example method of manufacturing a transistor having an uneven gate-drain surface, in accordance with various embodiments.

[0011] FIGS. 8A and 8B are top views of a wafer and dies that include one or more transistors having uneven gate-drain surfaces in accordance with any of the embodiments disclosed herein.

[0012] FIG. 9 is a cross-sectional side view of an integrated circuit (IC) device that may include one or more transistors having uneven gate-drain surfaces in accordance with any of the embodiments disclosed herein.

[0013] FIG. 10 is a cross-sectional side view of an IC device assembly that may include one or more transistors having uneven gate-drain surfaces in accordance with any of the embodiments disclosed herein.

[0014] FIG. 11 is a block diagram of an example computing device that may include one or more transistors having uneven gate-drain surfaces in accordance with any of the embodiments disclosed herein.

Detailed Description

[0015] Disclosed herein are transistor devices/arrangements in which a surface between a gate stack and a drain region is uneven in that it has one or more recesses or/and protrusions. For example, in some embodiments, a transistor may include one or more semiconductor materials in which a channel of a transistor will be formed during operation (for simplicity, in the following, these one or more semiconductor materials are referred to as a “semiconductor material” or a “channel material”), a gate electrode stack (or, simply, a “gate stack”) that includes a gate electrode and a gate dielectric and is provided over a first portion of the semiconductor/channel material, and a drain region (also referred to in the following as a “highly doped (HD) drain region” or a “drain diffusion region”) that is provided at a distance to the gate stack (i.e. is not adjacent to the gate stack), in a second portion of the semiconductor/channel material, where a surface of the semiconductor/channel material between the gate electrode stack and the drain region includes at least one recess or/and protrusion (i.e. is uneven). As described in greater detail below, ensuring that a surface of the semiconductor/channel material in a portion of a transistor between a gate electrode stack and a drain region (said surface referred to herein as a “gate-drain surface”) is not flat advantageously allows implementing transistor devices with relatively high breakdown voltages without having to occupy large die area.

[0016] Transistors having uneven gate-drain surfaces as described herein may be implemented in one or more components associated with an integrated circuit (IC) or/and between various such components. In various embodiments, components associated with an IC include, for example, transistors, diodes, power sources, resistors, capacitors, inductors, sensors, transceivers, receivers, antennas, etc. Components associated with an IC may include those that are mounted on an IC, provided as an integral part of an IC, or those connected to an IC. The IC may be either analog or digital and may be used in a number of applications, such as microprocessors, optoelectronics, logic

blocks, audio amplifiers, etc., depending on the components associated with the IC. The IC may be employed as part of a chipset for executing one or more related functions in a computer.

[0017] For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present disclosure may be practiced without the specific details or/and that the present disclosure may be practiced with only some of the described aspects. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

[0018] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, and in which are shown, by way of illustration, embodiments that may be practiced. The accompanying drawings are not necessarily drawn to scale. For example, to clarify various layers, structures, and regions, the thickness of some layers may be enlarged. Furthermore, while drawings illustrating various structures/assemblies of exemplary devices may be drawn with precise right angles and straight lines, real world process limitations may prevent implementations of devices exactly as shown. Therefore, it is understood that such drawings revised to reflect example real world process limitations, in that the features may not have precise right angles and straight lines, are within the scope of the present disclosure. Drawings revised in this manner may be more representative of real world structure/assemblies as may be seen on images using various characterization tools, such as e.g. scanning electron microscopy (SEM) or transmission electron microscopy (TEM). In addition, the various structures/assemblies of the present drawings may further include possible processing defects, such as e.g. the rounding of corners, the drooping of the layers/lines, unintentional gaps and/or discontinuities, unintentionally uneven surfaces and volumes, etc., although these possible processing defects may not be specifically shown in the drawings. It is to be understood that other embodiments may be utilized and structural or logical changes to the drawings and descriptions may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0019] Various operations may be described as multiple discrete actions or operations in turn, in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

[0020] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C). The term "between," when used with reference to measurement ranges, is inclusive of the ends of the measurement ranges. The meaning of "a," "an," and "the" include plural references. The meaning of "in" includes "in" and "on."

[0021] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. Furthermore, stating in the present disclosure that any part (e.g. a layer, film, area, or plate) is in any way positioned on or over (e.g. positioned on/over, provided on/over, located on/over, disposed on/over, formed on/over, etc.) another part means that the referenced part is either in contact with the other part, or that the referenced part is above the other part with one or more intermediate part(s) located therebetween. On the other hand, stating that any part is in contact with another part means that there is no intermediate part between the two parts.

[0022] The terms "substantially," "close," "approximately," "near," and "about," generally refer to being within +/- 20% of a target value. Unless otherwise specified, the use of the ordinal adjectives "first," "second," and "third," etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking or in any other manner.

[0023] In the following detailed description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. In some examples, as used herein, a "high-k dielectric" refers to a material having a higher dielectric constant than silicon oxide, while the terms "oxide," "carbide," "nitride," etc. refer to compounds containing, respectively, oxygen, carbon, nitrogen, etc. In another example, the term "connected" means a direct electrical or magnetic connection between the things that are connected, without any intermediary devices, while the term "coupled" means either a direct electrical or magnetic connection between the things that are connected or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means one or more passive and/or active components that are arranged to cooperate with one another to provide a desired function.

[0024] For purposes of illustrating transistors having uneven gate-drain surfaces as proposed herein, it is important to understand the phenomena that may come into play in a typical transistor. The following foundational information may be viewed as a basis from which the present disclosure may be properly explained. Such information is offered for purposes of explanation only and, accordingly, should not be construed in any way to limit the broad scope of the present disclosure and its potential applications.

[0025] The performance of a transistor may depend on a number of factors. One factor is how a transistor of a given type and architecture behaves in terms of an early junction breakdown (also known as the “Zener’s breakdown”) caused by large electric fields at the drain or/and the gate of a transistor. Various other factors, such as e.g. Gate Induced Drain Leakage (GIDL), can make this problem worse in that the breakdown process gets triggered at lower voltages than the usual junction breakdown. This problem is particularly prominent for otherwise promising high-voltage metal-oxide-semiconductor field-effect transistors (MOSFETs), where, despite years of intensive investigations and design optimizations, building area-efficient high-voltage MOS devices still remains a challenge, hindering scaling of these devices.

[0026] Transistors can have planar or non-planar architecture. Recently, MOSFETs with non-planar architecture, such as e.g. tri-gate/FinFET and all-around gate transistors, have been extensively explored as alternatives to transistors with planar architecture.

[0027] FinFETs refer to transistors having a non-planar architecture where a fin, formed of one or more semiconductor materials, extends away from a base. FinFETs are sometimes referred to as “tri-gate transistors,” where the name “tri-gate” originates from the fact that, in use, such a transistor may form conducting channels on three “sides” of the fin. FinFETs potentially improve performance relative to single-gate transistors and double-gate transistors. An example of a basic FinFET architecture is shown in FIGs. 1A and 1B, illustrating two different cross-sectional views of an exemplary conventional FinFET 100.

[0028] FIG. 1A illustrates a side view of the FinFET 100, with a cross-section taken along the length of the fin, while FIG. 1B illustrates a front view of the FinFET 100 with a cross-section taken across the gate of the FinFET – i.e. FIG. 1B illustrates a cross-sectional view with a cross-section taken along a plane AA shown in FIG. 1A, while FIG. 1A illustrates a cross-sectional view with a cross-section taken along a plane BB shown in FIG. 1B (FIG. 1A is also a cross-sectional view with a cross-section taken along a plane such as a plane CC shown in FIG. 5 that illustrates an exemplary perspective view of a FinFET, while FIG. 1B is a cross-sectional view with a cross-section taken along a plane such as a plane DD shown in FIG. 5).

[0029] As shown in FIGS. 1A and 1B, the FinFET 100 typically includes a substrate 102 over which a channel material 104 is provided. The channel material 104 is formed as a fin 120 extending away from the substrate (the fin 120 is not specifically shown in FIG. 1A because FIG. 1 illustrates a cross-sectional view with a cross-section taken along the length of the fin 120, but can be better seen in FIG. 1B). A gate stack 122 including a gate electrode material 106 and a gate dielectric 108, typically a high-k dielectric material, wraps around the upper portion of the fin 120, as can be seen in FIG. 1B, with the active region of the channel material 104 (i.e. the region where the transistor channel is formed during operation) corresponding to the portion of the fin 120 wrapped by the gate stack. In particular, as shown in FIG. 1B, the high-k dielectric 108 may wrap around the upper portion of the fin 120 and the gate electrode material 106 may wrap around the high-k dielectric 108. As also shown in FIG. 1B, sides of a lower portion of the fin 120, i.e. a portion that is closest to the substrate 102, are enclosed by a dielectric material 112, typically an oxide, commonly referred to as a “shallow trench isolation” (STI). A portion of a fin, e.g. the fin 120, that is enclosed by an STI is typically referred to as a “sub-fin” while a portion of a fin over which a gate stack wraps around is typically referred to as a “channel” or a “channel portion.” In general, a gate stack includes a stack of one or more gate electrode metals and a stack of one or more gate dielectrics and is provided over the top and sides of the upper portion of the fin (i.e. the portion above the STI), thus wrapping around the upper portion of the fin and forming a three-sided gate of a tri-gate transistor.

[0030] FIG. 1A further illustrates source and drain electrodes 124 and 126 formed of one or more electrically conductive materials 110, electrically connected to, respectively, a source region 134 and a drain region 136. As is well-known, source/drain (S/D) regions of a transistor (also sometimes interchangeably referred to as “diffusion regions”) are regions of doped semiconductors, e.g. regions of doped channel material, so as to supply charge carriers for the transistor channel. Often, the S/D regions are highly doped, e.g. with dopant concentrations of at least above $1 \cdot 10^{21}$ dopants per cubic centimeter (cm^{-3}), in order to advantageously form Ohmic contacts with the respective S/D electrodes (e.g. electrodes 124 and 126 shown in FIG. 1A), although these regions may also have lower dopant concentrations in some implementations. Regardless of the exact doping levels, the S/D regions 134 and 136 are the regions having dopant concentration higher than in other regions between the source region 134 and the drain region 136, and, therefore, are sometimes referred to as HD drain regions. Reference numeral 128 shown in FIG. 1A illustrates a channel portion of the FinFET 100.

[0031] Junction breakdown is known to be associated with architectures where the HD drain region is adjacent to or overlaps the gate (i.e. is adjacent to or overlaps the channel material under the gate stack) where the gate work-function and high drain doping concentration enhance the electric field,

triggering the band-to-band tunneling of carriers. Therefore, a conventional FinFET device such as the one shown in FIGS. 1A and 1B, with its HD drain region being adjacent to the gate stack, is not the first choice to build a high-voltage device. Instead, the most used approach conventionally used to improve on the junction breakdown problem is a so-called extended drain (ED) MOS (EDMOS), an example of which is illustrated in FIG. 2.

[0032] FIG. 2 is a cross-sectional side view of a conventional EDMOS FinFET transistor 200, similar to the view of FIG. 1A, where the same reference numerals as those shown in FIGS. 1A-1B illustrate the same or analogous elements, description of which is not, therefore, repeated in detail. As the acronym implies, the EDMOS concept requires an extended drain field region with the HD drain region 136 being physically separated from the gate stack 122 by a dummy drain electrode 226 and a dummy gate electrode 222, as shown in FIG. 2.

[0033] FIG. 2 further illustrates a region 242 which is a region of moderate doping concentration extending from the HD drain region 136 towards, but not reaching, the source region 134. As used herein, the term “moderate doping region” refers to a region having a doping concentration, of the same type of dopants as the drain region, that is lower than the doping concentration of the HD drain region but higher than that of the channel material. For example, the moderate doping region 242 may have a doping concentration between about $5 \cdot 10^{16}$ and $2 \cdot 10^{18} \text{ cm}^{-3}$, while the HD drain region 136 may have a doping concentration higher than about $2 \cdot 10^{18} \text{ cm}^{-3}$, e.g. above $1 \cdot 10^{19} \text{ cm}^{-3}$, or $1 \cdot 10^{21} \text{ cm}^{-3}$. The moderate doping region 242 and the HD drain region 136 both have the same type of dopants – e.g. for an NMOS transistor, both are doped with N-type dopants (thus, in an NMOS transistor, the moderate doping region 242 is also referred to as an “N-well”), while the channel material is a semiconductor material of an opposite type – e.g., for an NMOS transistor, the channel material is a P-type semiconductor. The moderate doping region 242 may extend, from the edge of the gate stack 122 closest to the HD drain region 136, towards the source region 134, under the gate stack 122, by a length shown in FIG. 2 as a length “CD2.” In this manner, contrary to a conventional MOSFET as e.g. shown in FIGS. 1A-1B, the gate stack 122 is provided over a P-N junction formed where the channel material 104 interfaces the moderate doping region 242, which reduces the electric field near the gate edge directly impacting band to band tunneling and therefore improving on the early junction breakdown problem. A dimension shown in FIG. 1 as “CD1” then refers to the actual channel length, i.e. a distance between the source region 134 and the moderate doping region 242, while a dimension shown in FIG. 1 as “CD3” refers to the distance by which the HD drain region 136 of the EDMOS FinFET 200 is laterally/horizontally shifted away from the edge of the gate stack 122 that is closest to the HD drain region. Thus, the gate length L_g , also indicated in FIG. 2, is

equal to the sum of CD1 and CD2. In such an EDMOS design, CD1 may be equal to CD2 and equal to e.g. 100 nm, while CD3 is typically between about 500 and 1000 nm (one to two poly pitches).

[0034] Because the HD drain region 136 of the EDMOS FinFET transistor 200 is shifted away from the gate stack 122, forcing charge carriers to travel a longer distance between the gate and the drain terminals, junction breakdown problem is improved. However, while such EDMOS approach may be effective, it requires using substantial additional area on a die – as described above, the distance CD3 shown in FIG. 2 may be as large as between 500 and 1000 nm.

[0035] Embodiments of the present disclosure are based on a recognition that an improvement in junction breakdown issues may also be achieved by creating an asymmetric MOS device with uneven gate-drain surface. In such a device, similar to the EDMOS implementation, the HD drain region is placed not adjacent to the gate but at a distance from it. However, in stark contrast to the conventional EDMOS implementation, the path for the charge carriers is made longer not by placing the HD drain region sufficiently far away from the gate stack, but by detouring the charge carriers into a third dimension by deliberately making the surface of a semiconductor material between the gate stack and the HD drain region uneven (i.e. not flat). Having a surface of a semiconductor material between a gate stack and a HD drain region uneven by providing one or more recesses (i.e. one or more hollow spaces inside said semiconductor material), one or more protrusions (i.e. one or more regions where the semiconductor material protrudes from otherwise planar surface, e.g. as a bump or a lump), or both one or more recesses and one or more protrusions, forces the charge carriers to travel a longer distance between the gate and the drain terminals, improving on the junction breakdown problem, while allowing the lateral distance between the gate stack and the HD drain region be made smaller compared to conventional EDMOS implementation as shown in FIG. 2. Placing the HD drain region closer to the gate stack, in absence of a dummy gate electrode and a dummy drain electrode as is done in conventional EDMOS transistors, advantageously allows providing an adequate control of the early junction breakdown problems without having to occupy large die area to implement such control. The HD source region may be kept at its conventional location, i.e. adjacent to the gate stack, thus making the device “asymmetric” (i.e. the HD source and the HD drain regions are not symmetric with respect to the gate stack). One example of such an asymmetric device with uneven gate-drain surface is illustrated in FIG. 3.

[0036] FIG. 3 is a cross-sectional side view of an example FinFET 300 having an uneven gate-drain surface, in accordance with various embodiments. FIG. 3 illustrates a side view, i.e. a cross-section taken along the length of the fin, similar to that shown in FIG. 1A and FIG. 2.

[0037] Similar to the FinFETs 100 or 200, the FinFET 300 includes a substrate 302 over which a channel material 304 is provided. The substrate 302 may be any structure on which one or more

transistors having uneven gate-drain surfaces as described herein can be disposed. In some embodiments, the substrate 302 may include a semiconductor, such as silicon. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present disclosure.

[0038] In some embodiments, the substrate 302 may include an insulating layer, sometimes referred to as an “interlayer dielectric” material (ILD), such as an oxide isolation layer, e.g. to electrically isolate the semiconductor material of the substrate 302 from the S/D regions and the channel material 304, and thereby mitigate the likelihood that a conductive pathway will form between a HD source region 334 and a HD drain region 336 through the substrate 302. Examples of ILDs that may be included in/on a substrate 302 in some embodiments may include silicon oxide, silicon nitride, aluminum oxide, and/or silicon oxynitride.

[0039] Any suitable ones of the embodiments of the substrate 302 described with reference to FIG. 3 may be used for the substrate of other transistors having uneven gate-drain surfaces in accordance with any of the embodiments disclosed herein.

[0040] The channel material 304 may be composed of semiconductor material systems including, for example, N-type or P-type materials systems.

[0041] In some embodiments, the channel material 304 is an intrinsic III-V or IV semiconductor material or alloy, not intentionally doped with any electrically active impurity. In alternate embodiments, nominal impurity dopant levels may be present within the channel material 304, for example to set a threshold voltage V_t , or to provide HALO pocket implants, etc. In such impurity-doped embodiments however, impurity dopant level within the channel material 304 may be relatively low, for example below about 10^{15} cm^{-3} , and advantageously below 10^{13} cm^{-3} .

[0042] In some embodiments, the channel material 304 may be formed of a monocrystalline semiconductor. In some embodiments, the channel material 304 may be formed of a compound semiconductor with a first sub-lattice of at least one element from group III of the periodic table (e.g., Al, Ga, In), and a second sub-lattice of at least one element of group V of the periodic table (e.g., N, P, As, Sb), e.g. GaN.

[0043] In some embodiments, the channel material 304 may include multiple layers of materials – e.g. for GaN transistors (or other III-N transistors), a polarization layer of aluminum nitride (AlN),

indium aluminum nitride (InAlN), or aluminum gallium nitride (AlGaN) may be provided over the GaN (or another III-N material) layer. Due, in part, to their large bandgap and high mobility, III-N material based transistors, such as e.g. gallium nitride (GaN) based transistors, may be particularly advantageous for applications such as e.g. high voltage and/or high frequency applications. For example, because GaN has a larger band gap (~ 3.4 eV) than silicon (Si; ~ 1.1 eV), a GaN transistor should be able to withstand a larger electric field (resulting e.g. from applying a large voltage to the drain, V_{dd}) before suffering breakdown, compared to a Si transistor of similar dimensions. Furthermore, GaN transistors may advantageously employ a 2D electron gas (i.e. a group of electrons, an electron gas, free to move in two dimensions but tightly confined in the third dimension, e.g. a 2D sheet charge) as its transport channel, enabling high mobilities without using impurity dopants. For example, the 2D sheet charge may be formed at an abrupt hetero-interface formed by epitaxial deposition, on GaN, of a charge-inducing film of a material having larger spontaneous and piezoelectric polarization, compared to GaN. Such a film is generally referred to as a “polarization layer” and may include materials such as aluminum nitride (AlN), aluminum gallium nitride (AlGaN), or aluminum indium nitride (AlInN). Providing a polarization layer on a III-N material such as GaN allows forming very high charge densities, e.g. densities of about $2 \cdot 10^{13}$ charges per square centimeter (cm^2), without impurity dopants, which, in turn, enables high mobilities, e.g. mobilities greater than about $1000 \text{ cm}^2/(\text{V} \cdot \text{s})$. In various embodiments, such a polarization layer 308 may have a thickness between about 2 and 30 nm, including all values and ranges therein e.g. between about 5 and 15 nm.

[0044] In some embodiments, the channel material 304 may be a binary, ternary, or quaternary III-V compound semiconductor that is an alloy of two, three, or even four elements from groups III and V of the periodic table, including boron, aluminum, indium, gallium, nitrogen, arsenic, phosphorus, antimony, and bismuth.

[0045] For exemplary N-type transistor embodiments, the channel material 304 may advantageously be a III-V material having a high electron mobility, such as, but not limited to InGaAs, InP, InSb, and InAs. For some such embodiments, the channel material 304 may be a ternary III-V alloy, such as InGaAs or GaAsSb. For some $\text{In}_x\text{Ga}_{1-x}\text{As}$ fin embodiments, In content in the channel material 304 may be between 0.6 and 0.9, and advantageously at least 0.7 (e.g., $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$).

[0046] For exemplary P-type transistor embodiments, the channel material 304 may advantageously be a group IV material having a high hole mobility, such as, but not limited to, Ge or a Ge-rich SiGe alloy. For some exemplary embodiments, the channel material 304 may have a Ge content between 0.6 and 0.9, and advantageously is at least 0.7.

[0047] In some embodiments, the channel material 304 may include a high mobility oxide semiconductor material, such as tin oxide, antimony oxide, indium oxide, indium tin oxide, titanium oxide, zinc oxide, indium zinc oxide, gallium oxide, titanium oxynitride, ruthenium oxide, or tungsten oxide.

[0048] The channel material 304 may have a thickness (i.e. a dimension measured along the z-axis of the coordinate system shown in FIG. 3) that is e.g. between about 10 and 10000 nanometers, including all values and ranges therein. In some implementations, the channel material 304 may be viewed as a part of the substrate 302, or as a part of the crystalline semiconductor upper part of the substrate 302.

[0049] In the exemplary device shown in FIG. 3, the channel material 304 is formed as a fin 320 extending away from the substrate (a view of the FinFET 300 with the fin 320 in a cross-section across the fin would be similar to that shown in FIG. 1B). Some further considerations with respect to the fin are described below, with reference to FIG. 5.

[0050] As further shown in FIG. 3 and described above, the upper portion of the fin is wrapped by a gate stack 322 including a gate electrode material 306 and a gate dielectric 308, with the active region of the channel material 304 (i.e. the channel portion of the fin 320) corresponding to the portion of the fin wrapped by the gate stack 322. In particular, the gate dielectric 308 may wrap around the upper portion of the fin and the gate electrode material 306 may wrap around the gate dielectric 308.

[0051] The gate electrode material 306 may include at least one P-type work function metal or N-type work function metal, depending on whether the transistor 300 is a P-type metal oxide semiconductor (PMOS) transistor or an N-type metal oxide semiconductor (NMOS) transistor (P-type work function metal used as the gate electrode material 306 when the transistors 300 is a PMOS transistor and N-type work function metal used as the gate electrode material 306 when the transistor 300 is an NMOS transistor). For a PMOS transistor, metals that may be used for the gate electrode material 306 may include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides (e.g., ruthenium oxide). For an NMOS transistor, metals that may be used for the gate electrode material 306 include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals (e.g., hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide). In some embodiments, the gate electrode material 306 may include a stack of two or more metal layers, where one or more metal layers are work function metal layers and at least one metal layer is a fill metal layer. Further layers may be included next to the gate electrode material 306 for other

purposes, such as to act as a diffusion barrier layer or/and an adhesion layer, not specifically shown in FIG. 3.

[0052] In some embodiments, the gate dielectric 308 may be a high-k dielectric (i.e. a dielectric material that has a higher dielectric constant (k) than silicon dioxide) including elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric 308 may include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, tantalum oxide, tantalum silicon oxide, lead scandium tantalum oxide, and lead zinc niobate.

[0053] In some embodiments, an annealing process may be carried out on the gate dielectric 308 during manufacture of the transistor 300 to improve the quality of the gate dielectric 308. The gate dielectric 308 may have a thickness (again, a dimension measured along the z-axis of the coordinate system shown in FIG. 3), that may, in some embodiments, be between about 0.4 nanometers and 5 nanometers, including all values and ranges therein (e.g., between about 0.5 and 3 nanometers, or between 1 and 2 nanometers).

[0054] In some embodiments, the gate stack 322 of the gate dielectric material 308 and the gate electrode material 306 may be surrounded by a gate spacer, not shown in FIG. 3, configured to provide separation between the gates of different transistors. Such a gate spacer is typically made of a low-k dielectric material (i.e. a dielectric material that has a lower dielectric constant (k) than silicon dioxide). Examples of low-k materials that may be used in such a dielectric spacer may include, but are not limited to, fluorine-doped silicon dioxide, carbon-doped silicon dioxide, spin-on organic polymeric dielectrics such as e.g. polyimide, polynorbornenes, benzocyclobutene, and polytetrafluoroethylene (PTFE), or spin-on silicon based polymeric dielectric such as e.g. hydrogen silsesquioxane (HSQ) and methylsilsesquioxane (MSQ). Other examples of low-k materials that may be used in a dielectric spacer include various porous dielectric materials, such as for example porous silicon dioxide or porous carbon-doped silicon dioxide, where large voids or pores are created in a dielectric in order to reduce the overall dielectric constant of the layer, since voids can have a dielectric constant of nearly 1.

[0055] Similar to the transistor 100 shown in FIGS. 1A and 1B described above, the lower portion of the fin 320 in the transistor 300, i.e. sub-fin, is surrounded by a dielectric material, typically an oxide, e.g. the STI as shown in FIG. 1A (not specifically shown in the cross-sectional side view of FIG. 3). The dielectric material of the STI may e.g. include any of the high-k dielectric materials described herein.

[0056] The fin of the transistor 300 may further include an HD source region 334 and an HD drain region 336 on either side of the gate stack 322. The HD source and HD drain regions 334 and 336 may be formed within the channel material 304 and, in some embodiments, may include one or more highly doped crystalline semiconductor materials, compared to the channel material 304. For example, in various embodiments, dopant levels within the HD source and HD drain regions may be at least $1 \cdot 10^{19} \text{ cm}^{-3}$, e.g. between about $1 \cdot 10^{19}$ and $10 \cdot 10^{21} \text{ cm}^{-3}$. While HD source/drain regions having doping concentrations varying from about $1 \cdot 10^{19} \text{ cm}^{-3}$ to solid solubility values, i.e. above $1 \cdot 10^{21} \text{ cm}^{-3}$ would typically advantageously form Ohmic contacts with source/drain electrode metals, embodiments of the present disclosure may also be implemented for source or/and drain regions having lower doping concentrations, i.e. when the source region or/and HD drain region form Schottky contacts with their respective electrode(s), e.g. doping concentrations between about $5 \cdot 10^{16}$ and $1 \cdot 10^{19} \text{ cm}^{-3}$.

[0057] The HD source and HD drain regions 334 and 336 may be formed within the channel material 304 using either an implantation/diffusion process or a deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the channel material 304 to form the highly doped regions. An annealing process that activates the dopants and causes them to diffuse farther into the channel material 304 may follow the ion implantation process. In the latter process, an epitaxial deposition process may provide material that is used to fabricate the highly doped regions. In some implementations, the highly doped regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some embodiments, the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In some embodiments, the highly doped regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. In further embodiments, one or more layers of metal and/or metal alloys may be used to form the highly doped regions. In some embodiments, an etch process may be performed before the epitaxial deposition to create recesses in the channel material 304 in which the material for the highly doped regions is deposited.

[0058] FIG. 3 further illustrates source and drain electrodes 324 and 326 formed of one or more electrically conductive materials 310, electrically connected to, respectively, the HD source region 334 and the HD drain region 336. The S/D electrode material 310 may include any suitable electrically conductive material, alloy, or a stack of multiple electrically conductive materials. In some embodiments, the S/D electrode material 310 may include one or more metals or metal alloys, with metals such as e.g. ruthenium, palladium, platinum, cobalt, nickel, hafnium, zirconium, titanium, tantalum, and aluminum. In some embodiments, the S/D electrode material 310 may

include one or more electrically conductive alloys, oxides, or carbides of one or more metals. In various embodiments, the S/D conductive material 310 could be the same or different materials for the source electrode 324 and the drain electrode 326, and could be the same or different materials as the gate electrode material 306. In various embodiments, the S/D electrode material 310 may have a thickness between about 5 and 500 nm, including all values and ranges therein, e.g. between 5 and 100 nm.

[0059] As shown in FIG. 3, while the source region 334 may be provided adjacent to the gate stack 322 (or could be overlapping with the gate stack, i.e. a portion of the source region 334 could be below the gate stack 322), the HD drain region 336 is laterally/horizontally shifted away from the gate stack by a distance d_L (i.e. a dimension measured along the y-axis of the coordinate system shown in FIG. 3). In other words, lateral/horizontal shift by the distance d_L means that the edge of the HD drain region 336 closest to the edge of the gate stack 322 is separated from the gate stack 322 by that distance, as illustrated with showing the distance d_L in FIG. 3, or, equally, the distance d_L represents the distance between the closest two points of the HD drain region and the gate stack in a cross-section such as the one shown in FIG. 3 (these two points shown in FIG. 3 as a point 350 of the HD drain region 336 and a point 352 of the gate stack 322).

[0060] Furthermore, as also shown in FIG. 3 the surface of the channel material 304 between the gate stack 322 and the HD drain region 336 is uneven, or, in other words, has a non-linear profile with one or more features – which is illustrated in the example of FIG. 3 with a feature 360 shown as a recess in the channel material 304. While a single recess feature with a rectangular cross-section profile is illustrated in the example of FIG. 3 and described in greater detail below, in general, any number of features, where each feature may be a recess or a protrusion, in any three-dimensional (3D) shape (i.e. not necessarily with a rectangular profile as shown in FIG. 3) is within the scope of the present disclosure.

[0061] FIG. 4A illustrates an enlarged version of a window 362 of the example shown in FIG. 3, where the feature 360 implemented as a recess 402, in order to illustrate the uneven gate-drain surface more clearly. Some examples of other features 360 as shown in FIGS. 4B-4D (i.e. the window 362 shown in FIG. 3 may illustrate the features as shown in each of FIGS. 4B-4D). Namely, FIG. 4B illustrates the feature 360 implemented as a protrusion 404, FIG. 4C illustrates the feature 360 implemented as a protrusion 406, and FIG. 4D illustrates the feature 360 implemented as a recess 408. Reference numerals used to label elements of FIGS. 4A-4D which are the same as reference numerals used to label elements of FIG. 3 are intended to illustrate similar/analogous or same elements and, therefore, discussions of these elements provided with respect to FIG. 3 are applicable to FIGS. 4A-4D and, in the interests of brevity, are not repeated for FIGS. 4A-4D.

[0062] Turning to FIG. 4A, this drawing illustrates the example shown in FIG. 3 where the feature 360 is implemented as the recess 402. Measurements d_1 , d_2 , d_3 , d_4 , and d_5 , shown in FIG. 4A, illustrate various sections of the profile of the gate-drain surface in a given cross-section along the length of the fin as shown in FIG. 3 and FIGS. 4A-4D. The various sections of the profile of the surface of the channel material 304 with the feature 360 are indicated in FIGS. 4A-4D with black lines which are thicker than all of the other lines and are labeled with measurements d_1 - d_5 , where it should be noted that d_1 - d_5 shown in different ones of FIGS. 4A-4D do not necessarily refer to the same values.

[0063] A sum of the lengths of the thick black lines shown in each of FIGS. 4A-4D represents the shortest distance, along the surface of the channel material 304, between edge of the gate electrode stack 322 (represented by the point 352 shown in FIGS. 4A-4D) and the edge of the HD drain region 336 (represented by the point 350 shown in FIGS. 4A-4D) that includes one or more of the features 360. Such distance may be referred to herein as a “gate-drain feature distance” (d_{feat}) to highlight the fact that this is the distance between the gate stack and the HD drain region that includes the one or more features 360, i.e. the distance that the charge carriers have to travel between the gate and the drain terminals of a transistor. For the example of the feature 360 being the recess 402 as shown in FIG. 4A, the gate-drain feature distance d_{feat} is equal to $d_1+d_2+d_3+d_4+d_5$. For the example of the feature 360 being the protrusion 404 as shown in FIG. 4B, the gate-drain feature distance d_{feat} is also equal to $d_1+d_2+d_3+d_4+d_5$. For the example of the feature 360 being the protrusion 406 as shown in FIG. 4C, the gate-drain feature distance d_{feat} is also equal to $d_1+d_2+d_3+d_4$. For the example of the feature 360 being the recess 408 as shown in FIG. 4D, the gate-drain feature distance d_{feat} is equal to $d_1+d_2+d_3$.

[0064] It should be noted that the gate-drain feature distance d_{feat} is described above as “the shortest distance” to indicate that this is the distance measured between the gate stack and the HD drain region in a single cross-section along the fin (i.e. in a given single cross-section of a kind shown in FIG. 3 and FIGS. 4A-4D, i.e. a single cross-section along a plane y - z of the coordinate system shown in FIG. 3). On the other hand, theoretically, if a distance was measured between the gate stack of one cross-section along a first plane y - z and the HD drain region of a cross-section along a plane parallel to and different from the first plane, that distance would not be the shortest distance between the gate stack and the HD drain region because it would be longer than the distance measured in a single cross-section along a y - z plane. It should also be noted that the gate-drain feature distance d_{feat} is different from the distance d_L , which is the distance between the closest two points of the HD drain region and the gate stack in a cross-section such as the one shown in FIG. 3 (i.e. between the points 350 and 352) but measured in the direction of the y -axis of the coordinate

system shown in FIG. 3. In other words, the distance d_L is not measured along the surface of the channel material 304 and is not measured along the feature 360. To differentiate the distance d_L from the gate-drain feature distance d_{feat} , the distance d_L may be referred to herein as a “planar gate-drain distance.”

[0065] In various embodiments, a dimension of the feature 360 in a direction perpendicular to the gate stack 322 (i.e. in a direction in which the materials 308 and 306 of the gate electrode stack are stacked, which is the direction of the z-axis of the coordinate system shown in FIG. 3) may be at least 10 nm. For the example of the feature 360 being the recess 402 shown in FIG. 4A, this dimension is a depth of the recess 402 as measured by d_2 or d_4 labeled in FIG. 4A. For the example of the feature 360 being the protrusion 404 shown in FIG. 4B, this dimension is a height of the protrusion 404 as measured by d_2 or d_4 labeled in FIG. 4B. For the example of the feature 360 being the protrusion 406 shown in FIG. 4C, this dimension is a height h labeled in FIG. 4C. For the example of the feature 360 being the recess 408 shown in FIG. 4D, this dimension is a depth of the recess 408 shown as a depth d labeled in FIG. 4D.

[0066] Thus, presence of one or more of the features 360 provided between the gate stack and the HD drain region on purpose make the gate-drain surface non-flat in what goes well above as any incidental surface roughness which may be present, e.g. for the gate-drain surface of the EDMOS implementation as shown in FIG. 2. Typical for semiconductor processing, a surface may qualify as “flat” if root mean square (RMS) surface roughness of the surface is about 0.5 nm or less. Providing one or more features 360 with height or depth of at least 10 nm, or of at least 5 nm, will result in RMS surface roughness for the gate-drain surface which is well above that value. For example, in some embodiments, the RMS surface roughness for the gate-drain surface according to various embodiments of the transistor arrangements with uneven gate-drain surfaces as described herein may be at least about 5 nm. Thus, unlike conventional implementations, in all of the embodiments of the present disclosure, the surface of the channel material 304 between the gate electrode stack 322 and the HD drain region 336 is not flat.

[0067] In other words, the surface of the channel material 304 between the gate electrode stack 322 and the HD drain region 336 according to the various embodiments of the present disclosure may be viewed as having a first portion that is substantially a planar/flat surface, and a second portion that includes at least one feature 360. For the example of each of FIGS. 4A and 4B, the surfaces labeled with d_1 and d_5 together constitute such a first portion that is substantially planar/flat, while the surfaces labeled with d_2 - d_4 together constitute such a second portion that includes the feature 402/404. For the example of FIG. 4C, the surfaces labeled with d_1 and d_4 together constitute such a first portion that is substantially planar/flat, while the surfaces labeled

with d2 and d3 together constitute such a second portion that includes the feature 406. For the example of FIG. 4D, the surfaces labeled with d1 and d3 together constitute such a first portion that is substantially planar/flat, while the concave surface labeled with d2 is such a second portion that includes the feature 408. The feature 360 may then be viewed as having at least one point that is at a distance of at least about 5 nanometers, e.g. at least about 10 nm, from a plane of the first portion of the surface. For the examples of FIGS. 4A and 4B, such a distance would be the distance d2 or d4. For the example of FIG. 4C, such a distance would be the distance h. For the example of FIG. 4D, such a distance would be the distance d.

[0068] In various embodiments, the depth of the recesses and the height of the protrusions can take on any values as long as they can be supported by a manufacturing process used to form such features. For example, in case the feature 360 is a recess, considerations such as e.g. aspect ratio that is possible to achieve with a suitable manufacturing process may have influence on the exact depth of the recess.

[0069] Extending the gate-drain surface in the third dimension (i.e. in the dimension in the direction of the z-axis) allows providing sufficiently long gate-drain feature distance which the charge carriers have to traverse between the gate and the drain terminals to reduce junction breakdown effects, while reducing the planar gate-drain distance, thus occupying less area on a die for a given transistor device. In some embodiments, the planar gate-drain distance may be at least 10 nm smaller than the gate-drain feature distance, e.g. less than about 10-100 nm, including all values and ranges therein, e.g. between about 20 and 90 nm or between about 30 and 80 nm. In some embodiments, the planar gate-drain distance d_L may be less than about 90% (e.g. less than about 80%, or less than about 60%) of the gate-drain feature distance d_{feat} , including all values and ranges therein.

[0070] In various embodiments, the feature 360 may have a substantially rectangular profile (as shown with the recess 402 shown in FIG. 4A), or may have slanted sidewalls (e.g. a trapezoid profile), e.g. as a consequence of etching of the channel material 304 to form the feature, in case the feature is a recess.

[0071] In various embodiments, the gate-drain feature distance d_{feat} may be greater than about 90 nanometers, e.g. between about 90 and 1000 nm, or between about 150 and 500 nm. In some embodiments, this distance may be matched to (i.e. about equal to) CD3 of conventional EDMOS implementations shown in FIG. 2, in order to achieve similar performance and benefits in terms of improving the junction breakdown. In general, the triggering voltage for a junction breakdown increases as the distance CD3 increases. Thus, increasing the gate-drain feature distance d_{feat} may advantageously increase such a triggering voltage.

[0072] What is considered to be an appropriate triggering voltage may depend, among other things, on whether a device in which transistors are implemented is intended for high-voltage applications such as e.g. input/output (I/O) devices/drivers or low-voltage applications such as e.g. logic gates. As is known, gate lengths and, correspondingly, poly pitch distances and triggering voltages used in the low-voltage applications are smaller than those used in high-voltage applications. Therefore, the gate-drain feature distance d_{feat} and the number and the dimensions of the features 360 would depend on the type of application in which such a transistor with uneven gate-drain surface is to be used.

[0073] Each of the examples shown in FIGS. 4A-4D illustrates only one feature present between the gate stack 322 and the HD drain region 336. However, in other embodiments, more than one features 360 as described above may be present. For example, two features may be present, where, in one embodiment - both features are recesses, in another embodiment – both features are protrusions, and in a third embodiment – one feature is a recess and one feature is a protrusion. Furthermore, while each of the examples shown in FIGS. 4A-4D illustrates features which are substantially symmetrical on their own, this is illustrated only because, with typical manufacturing techniques, this is often what is easier, or possible, to manufacture. In general, one or more features 360 as described herein may be of any 3D shape.

[0074] Inspection of layout and mask data and reverse engineering of parts of a device to reconstruct the circuit using e.g. optical microscopy, Transmission Electron Microscopy (TEM), or Scanning Electron Microscopy (SEM), and/or inspection of a cross-section of a device to detect the shape and the location of various device elements described herein using e.g. Physical Failure Analysis (PFA) would allow determination of the uneven gate-drain surfaces as described herein.

[0075] While transistors having uneven gate-drain surfaces have been described above with reference to FinFETs, in various embodiments such transistors may be implemented using any suitable transistor structure, two examples of which are shown in FIGS. 5 and 6, both illustrating different non-planar architectures. In other embodiments, uneven gate-drain surfaces as proposed in the present disclosure may also be implemented with transistors having planar architectures.

[0076] FIG. 5 is a perspective view of an example FinFET 500, in accordance with various embodiments. The FinFET 500 may be seen as illustrating a perspective drawing for the FinFET 300 shown in FIG. 3 and described above, or any other FinFET with an uneven gate-drain surface as described herein.

[0077] Reference numerals used to label elements of FIG. 5 which are the same as reference numerals used to label elements of FIG. 3 are intended to illustrate similar/analogous or same elements and, therefore, discussions of these elements provided with respect to FIG. 3 are

applicable to FIG. 5 and, in the interests of brevity, are not repeated for FIG. 5. In particular, FIG. 5 illustrates the substrate 302, the channel material 304, the gate electrode 306, the gate dielectric 308, the fin 320, the gate stack 322, the source region 334, and the HD drain region 336. In addition, FIG. 5 illustrates STI 512, similar to the STI 112 described above.

[0078] Although the fin 320 illustrated in FIG. 5 is shown as having a rectangular cross section, the fin 320 may instead have a cross section that is rounded or sloped at the "top" of the fin 320, and the gate stack 322 may conform to this rounded or sloped fin 320. In use, the FinFET 500 may form conducting channels on three "sides" of the fin 320 wrapped around by the gate stack 322, potentially improving performance relative to single-gate transistors (which may form conducting channels on one "side" of a channel material or substrate) and double-gate transistors (which may form conducting channels on two "sides" of a channel material or substrate).

[0079] In some embodiments, multiple FinFETs similar to that shown in FIG. 5 may be provided along a single fin such as the fin 320, with considerations relevant to providing multiple devices on a single fin being known in the art and, therefore, in the interests of brevity, not specifically described here.

[0080] FIG. 6 is a perspective view of an example all-around gate transistor 600, in accordance with various embodiments. The transistor 600 of FIG. 6 may include one or more semiconductor materials, including a channel material 304, as described above, the one or more semiconductor materials formed as a wire 620 provided over a substrate, e.g. the substrate 302 as described above. The wire 620 may take the form of a nanowire or nanoribbon, for example. A gate stack 622 including a gate electrode material 306 and a high-k dielectric 308 may wrap entirely or almost entirely around the wire 620 as shown in FIG. 6, with the active region of the channel material 304 corresponding to the portion of the wire 620 wrapped by the gate stack. In particular, the high-k dielectric 308 may wrap around the wire 620 and the gate electrode material 306 may wrap around the high-k dielectric 308. In some embodiments, the gate stack may fully encircle the wire 620. In some embodiments, a layer of oxide material (not specifically shown in FIG. 6) may be provided between the substrate 302 and the gate electrode 306.

[0081] The wire 620 may include a source region 634 and an HD drain region 636 on either side of the gate stack, as shown. The composition of the channel material 304, the HD source region 634, and the HD drain region 636 may take the form of any of the embodiments disclosed herein, or known in the art. In particular, the HD source region 634 and the HD drain region 636 may be implemented as the source region HD 334 and the HD drain region 336 as described above, where the surface of the channel material 304 between the HD drain region 636 and the gate stack 622 is uneven.

[0082] Although the wire 620 illustrated in FIG. 6 is shown as having a rectangular cross section, the wire 620 may instead have a cross section that is rounded or otherwise irregularly shaped, and the gate stack may conform to the shape of the wire 620. In use, the all-around-gate transistor 600 may form conducting channels on more than three "sides" of the wire 620, potentially improving performance relative to FinFETs. Although FIG. 6 depicts an embodiment in which the longitudinal axis of the wire 620 runs substantially parallel to a plane of the substrate 302, this need not be the case; in other embodiments, for example, the wire 620 may be oriented "vertically" so as to be perpendicular to a plane of the substrate 302.

[0083] In some embodiments, multiple all-around-gate transistors similar to that shown in FIG. 6 may be provided along a single wire such as the wire 620, with considerations relevant to providing multiple devices on a single wire being known in the art and, therefore, in the interests of brevity, not specifically described here.

[0084] Although not specifically illustrated in the present FIGS, a dielectric spacer may be provided between the source electrode and the gate stack as well as between the transistor drain electrode and the gate stack of the transistors described herein in order to provide electrical isolation between the source, gate, and drain electrodes.

[0085] The transistors illustrated in FIGS. 3-6 do not represent an exhaustive set of transistor structures in which uneven gate-drain surfaces as described herein may be implemented, but merely provide examples of such structures. Although particular arrangements of materials are discussed with reference to FIGS. 3-6, intermediate materials may be included in the transistor devices of these FIGS. Note that FIGS. 3-6 are intended to show relative arrangements of the components therein, and that transistor devices of these FIGS may include other components that are not illustrated (e.g., gate spacers or various interfacial layers). Additionally, although various components of the transistor devices are illustrated in FIGS. 3-6 as being planar rectangles or formed of rectangular solids, this is simply for ease of illustration, and embodiments of these transistors may be curved, rounded, or otherwise irregularly shaped as dictated by, and sometimes inevitable due to, the manufacturing processes used to fabricate the transistors.

[0086] Transistors with uneven gate-drain surfaces as described herein may be manufactured using any suitable techniques. For example, FIG. 7 is a flow diagram of an example method 700 of manufacturing a transistor having an uneven gate-drain surface, in accordance with various embodiments. Although the operations of the method 700 are illustrated once each and in a particular order, the operations may be performed in any suitable order and repeated as desired. For example, one or more operations may be performed in parallel to manufacture, substantially simultaneously, multiple transistors having uneven gate-drain surfaces as described herein. In

another example, the operations may be performed in a different order to reflect the structure of a transistor in which uneven gate-drain surfaces as described herein will be included.

[0087] At 702, one or more semiconductor materials for forming a channel may be provided. The one or more semiconductor materials provided at 702 may take the form of any of the embodiments of the channel material 304 disclosed herein, for example (e.g., any of the embodiments discussed herein with reference to the transistor 300 and other transistors with uneven gate-drain surfaces described herein). The one or more semiconductor materials may be provided at 702 using any suitable deposition and patterning techniques known in the art.

[0088] At 704, the surface of the semiconductor channel material of 702 is made uneven by providing one or more features, each feature being a recess or a protrusion, in an area which will later become the region between the gate stack and the drain region. The one or more semiconductor surface features provided at 704 may take the form of any of the embodiments of the features 360 disclosed herein, for example (e.g., any of the embodiments discussed herein with reference to the transistor 300 and other transistors with uneven gate-drain surfaces described herein). The one or more surface features of the semiconductor material may be provided at 704 using any suitable deposition and patterning techniques known in the art, such as e.g. semiconductor deposition and etching, possibly using suitable masks. In some embodiments, operations of 702 and 704 may be carried out in a single step.

[0089] At 706, a gate stack may be provided over and a drain region may be provided over or in the one or more semiconductor materials 304 so that the uneven surface of the semiconductor channel material is between the gate stack and the drain region. The gate stack defined at 706 may take the form of any of the embodiments of the gate stacks 322 disclosed herein, for example (e.g., any of the embodiments discussed herein with reference to the transistor 300 and other transistors with uneven gate-drain surfaces described herein). The gate stack provided at 706 may be manufactured using any suitable deposition and patterning techniques known in the art, possibly using a suitable mask for implementing the gate stack at a desired location over the semiconductor channel material, as described above. The drain region defined at 706 may take the form of any of the embodiments of the HD drain regions 336 disclosed herein, for example (e.g., any of the embodiments discussed herein with reference to the transistor 300 and other transistors with uneven gate-drain surfaces described herein). The drain region provided at 706 may be manufactured using any suitable techniques known in the art, such as e.g. using an implantation/diffusion process or a deposition process, possibly using a suitable mask for implementing the HD drain region 336 at a desired location at a distance from the gate stack of a transistor, as described above. In some embodiments, operations of 706 may be performed after

the semiconductor channel material is provided at 702 but before the surface of the semiconductor material is made uneven by providing one or more features (i.e. 706 may be performed before 704).

[0090] Transistors having uneven gate-drain surfaces disclosed herein may be included in any suitable electronic device. FIGS. 8-11 illustrate various examples of apparatuses that may include one or more of the transistor devices having uneven gate-drain surfaces, as disclosed herein.

[0091] FIGS. 8A-B are top views of a wafer 2000 and dies 2002 that may include one or more transistors having uneven gate-drain surfaces in accordance with any of the embodiments disclosed herein. The wafer 2000 may be composed of semiconductor material and may include one or more dies 2002 having IC structures formed on a surface of the wafer 2000. Each of the dies 2002 may be a repeating unit of a semiconductor product that includes any suitable IC (e.g., ICs including one or more transistors 300, or any other transistors having uneven gate-drain surfaces as described herein). After the fabrication of the semiconductor product is complete (e.g., after manufacture of one or more transistors 300, or any other transistors having uneven gate-drain surfaces as described herein), the wafer 2000 may undergo a singulation process in which each of the dies 2002 is separated from one another to provide discrete "chips" of the semiconductor product. In particular, devices that include one or more transistors having uneven gate-drain surfaces as disclosed herein may take the form of the wafer 2000 (e.g., not singulated) or the form of the die 2002 (e.g., singulated). The die 2002 may include one or more transistors (e.g., one or more of the transistors 2140 of FIG. 9, discussed below, which may take the form of any of the transistors having uneven gate-drain surfaces as described herein) and/or supporting circuitry to route electrical signals to the transistors, as well as any other IC components. In some embodiments, the wafer 2000 or the die 2002 may include a memory device (e.g., a static random access memory (SRAM) device), a logic device (e.g., an AND, OR, NAND, or NOR gate), or any other suitable circuit element. Multiple ones of these devices may be combined on a single die 2002. For example, a memory array formed by multiple memory devices may be formed on a same die 2002 as a processing device (e.g., the processing device 2302 of FIG. 11) or other logic that is configured to store information in the memory devices or execute instructions stored in the memory array.

[0092] FIG. 9 is a cross-sectional side view of an IC device 2100 that may include one or more transistors having uneven gate-drain surfaces in accordance with any of the embodiments disclosed herein. The IC device 2100 may be formed on a substrate 2102 (e.g., the wafer 2000 of FIG. 8A) and may be included in a die (e.g., the die 2002 of FIG. 8B). The substrate 2102 may be a semiconductor substrate composed of semiconductor material systems including, for example, N-type or P-type materials systems. The substrate 2102 may include, for example, a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In some embodiments, the semiconductor

substrate 2102 may be formed using alternative materials, which may or may not be combined with silicon, that include, but are not limited to, germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. Further materials classified as group II-VI, III-V, or IV may also be used to form the substrate 2102. Although a few examples of materials from which the substrate 2102 may be formed are described here, any material that may serve as a foundation for an IC device 2100 may be used. The substrate 2102 may be part of a singulated die (e.g., the dies 2002 of FIG. 8B) or a wafer (e.g., the wafer 2000 of FIG. 8A).

[0093] The IC device 2100 may include one or more device layers 2104 disposed on the substrate 2102. The device layer 2104 may include features of one or more transistors 2140 (e.g., metal oxide semiconductor field-effect transistors (MOSFETs)) formed on the substrate 2102. The device layer 2104 may include, for example, one or more source and/or drain (S/D) regions 2120, a gate 2122 to control current flow in the transistors 2140 between the S/D regions 2120, and one or more S/D contacts 2124 to route electrical signals to/from the S/D regions 2120. Although not specifically shown in FIG. 9, the S/D regions 2120 may include the HD drain region 336 as described herein with an uneven surface between the HD drain region 2120 and the gate 2122, or any other drain and gate stack combinations where the surface of a semiconductor material between the gate stack and the drain region is uneven. The S/D regions 2120 may be formed within the substrate 2102 and asymmetric with respect to the gate 2122 of each transistor 2140, as described herein, using any suitable processes known in the art, some of which are described above. The transistors 2140 may include additional features not depicted for the sake of clarity, such as device isolation regions, gate contacts, and the like. The transistors 2140 are not limited to the type and configuration depicted in FIG. 9 and may include a wide variety of other types and configurations such as, for example, planar transistors, non-planar transistors, or a combination of both. Non-planar transistors may include FinFET transistors, such as double-gate transistors or FinFETs, and wrap-around or all-around gate transistors, such as nanoribbon and nanowire transistors. In particular, at least some of the one or more of the transistors 2140 may have an uneven gate-drain surface in accordance with any of the embodiments disclosed herein. For example, a transistor 2140 may take the form of any of the transistors 300, or other transistors with uneven gate-drain surfaces disclosed herein.

[0094] Each transistor 2140 may include a gate 2122 formed of at least two layers, a gate dielectric layer and a gate electrode layer. Generally, the gate dielectric layer of a transistor 2140 may include one layer or a stack of layers, and the one or more layers may include silicon oxide, silicon dioxide, and/or a high-k dielectric material. The high-k dielectric material included in the gate dielectric layer of the transistor 2140 may take the form of any of the embodiments of the high-k dielectric 308 disclosed herein, for example.

[0095] In some embodiments, when viewed as a cross section of the transistor 2140 along the source-channel-drain direction, the gate electrode may include a U-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate (e.g., as illustrated for a FinFET of FIGS. 1A and 1B). In other embodiments, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In other embodiments, the gate electrode may include a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may include one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers. In some embodiments, the gate electrode may include a V-shaped structure (e.g., when the fin of a FinFET does not have a "flat" upper surface, but instead has a rounded peak).

[0096] In some embodiments, a pair of sidewall spacers may be formed on opposing sides of the gate stack to bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In some embodiments, a plurality of spacer pairs may be used; for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[0097] Electrical signals, such as power and/or input/output (I/O) signals, may be routed to and/or from the transistors 2140 of the device layer 2104 through one or more interconnect layers disposed on the device layer 2104 (illustrated in FIG. 9 as interconnect layers 2106-2110). For example, electrically conductive features of the device layer 2104 (e.g., the gate 2122 and the S/D contacts 2124) may be electrically coupled with the interconnect structures 2128 of the interconnect layers 2106-2110. The one or more interconnect layers 2106-2110 may form an interlayer dielectric (ILD) stack 2119 of the IC device 2100.

[0098] The interconnect structures 2128 may be arranged within the interconnect layers 2106-2110 to route electrical signals according to a wide variety of designs (in particular, the arrangement is not limited to the particular configuration of interconnect structures 2128 depicted in FIG. 9). Although a particular number of interconnect layers 2106-2110 is depicted in FIG. 9, embodiments of the present disclosure include IC devices having more or fewer interconnect layers than depicted.

[0099] In some embodiments, the interconnect structures 2128 may include trench structures 2128a (sometimes referred to as "lines") and/or via structures 2128b (sometimes referred to as "holes") filled with an electrically conductive material such as a metal. The trench structures 2128a

may be arranged to route electrical signals in a direction of a plane that is substantially parallel with a surface of the substrate 2102 upon which the device layer 2104 is formed. For example, the trench structures 2128a may route electrical signals in a direction in and out of the page from the perspective of FIG. 9. The via structures 2128b may be arranged to route electrical signals in a direction of a plane that is substantially perpendicular to the surface of the substrate 2102 upon which the device layer 2104 is formed. In some embodiments, the via structures 2128b may electrically couple trench structures 2128a of different interconnect layers 2106-2110 together.

[0100] The interconnect layers 2106-2110 may include a dielectric material 2126 disposed between the interconnect structures 2128, as shown in FIG. 9. In some embodiments, the dielectric material 2126 disposed between the interconnect structures 2128 in different ones of the interconnect layers 2106-2110 may have different compositions; in other embodiments, the composition of the dielectric material 2126 between different interconnect layers 2106-2110 may be the same.

[0101] A first interconnect layer 2106 (referred to as Metal 1 or "M1") may be formed directly on the device layer 2104. In some embodiments, the first interconnect layer 2106 may include trench structures 2128a and/or via structures 2128b, as shown. The trench structures 2128a of the first interconnect layer 2106 may be coupled with contacts (e.g., the S/D contacts 2124) of the device layer 2104.

[0102] A second interconnect layer 2108 (referred to as Metal 2 or "M2") may be formed directly on the first interconnect layer 2106. In some embodiments, the second interconnect layer 2108 may include via structures 2128b to couple the trench structures 2128a of the second interconnect layer 2108 with the trench structures 2128a of the first interconnect layer 2106. Although the trench structures 2128a and the via structures 2128b are structurally delineated with a line within each interconnect layer (e.g., within the second interconnect layer 2108) for the sake of clarity, the trench structures 2128a and the via structures 2128b may be structurally and/or materially contiguous (e.g., simultaneously filled during a dual-damascene process) in some embodiments.

[0103] A third interconnect layer 2110 (referred to as Metal 3 or "M3") (and additional interconnect layers, as desired) may be formed in succession on the second interconnect layer 2108 according to similar techniques and configurations described in connection with the second interconnect layer 2108 or the first interconnect layer 2106.

[0104] The IC device 2100 may include a solder resist material 2134 (e.g., polyimide or similar material) and one or more bond pads 2136 formed on the interconnect layers 2106-2110. The bond pads 2136 may be electrically coupled with the interconnect structures 2128 and configured to route the electrical signals of the transistor(s) 2140 to other external devices. For example, solder bonds may be formed on the one or more bond pads 2136 to mechanically and/or electrically couple a chip

including the IC device 2100 with another component (e.g., a circuit board). The IC device 2100 may have other alternative configurations to route the electrical signals from the interconnect layers 2106-2110 than depicted in other embodiments. For example, the bond pads 2136 may be replaced by or may further include other analogous features (e.g., posts) that route the electrical signals to external components.

[0105] FIG. 10 is a cross-sectional side view of an IC device assembly 2200 that may include components having one or more transistors with uneven gate-drain surfaces in accordance with any of the embodiments disclosed herein. The IC device assembly 2200 includes a number of components disposed on a circuit board 2202 (which may be, e.g., a motherboard). The IC device assembly 2200 includes components disposed on a first face 2240 of the circuit board 2202 and an opposing second face 2242 of the circuit board 2202; generally, components may be disposed on one or both faces 2240 and 2242. In particular, any suitable ones of the components of the IC device assembly 2200 may include any of the transistors having uneven gate-drain surfaces in accordance with any of the embodiments disclosed herein.

[0106] In some embodiments, the circuit board 2202 may be a printed circuit board (PCB) including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board 2202. In other embodiments, the circuit board 2202 may be a non-PCB substrate.

[0107] The IC device assembly 2200 illustrated in FIG. 10 includes a package-on-interposer structure 2236 coupled to the first face 2240 of the circuit board 2202 by coupling components 2216. The coupling components 2216 may electrically and mechanically couple the package-on-interposer structure 2236 to the circuit board 2202, and may include solder balls (as shown in FIG. 10), male and female portions of a socket, an adhesive, an underfill material, and/or any other suitable electrical and/or mechanical coupling structure.

[0108] The package-on-interposer structure 2236 may include an IC package 2220 coupled to an interposer 2204 by coupling components 2218. The coupling components 2218 may take any suitable form for the application, such as the forms discussed above with reference to the coupling components 2216. Although a single IC package 2220 is shown in FIG. 10, multiple IC packages may be coupled to the interposer 2204; indeed, additional interposers may be coupled to the interposer 2204. The interposer 2204 may provide an intervening substrate used to bridge the circuit board 2202 and the IC package 2220. The IC package 2220 may be or include, for example, a die (the die 2002 of FIG. 8B), an IC device (e.g., the IC device 2100 of FIG. 9), or any other suitable component.

Generally, the interposer 2204 may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer 2204 may couple the IC package 2220 (e.g., a die) to a ball grid array (BGA) of the coupling components 2216 for coupling to the circuit board 2202. In the embodiment illustrated in FIG. 10, the IC package 2220 and the circuit board 2202 are attached to opposing sides of the interposer 2204; in other embodiments, the IC package 2220 and the circuit board 2202 may be attached to a same side of the interposer 2204. In some embodiments, three or more components may be interconnected by way of the interposer 2204.

[0109] The interposer 2204 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In some implementations, the interposer 2204 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer 2204 may include metal interconnects 2208 and vias 2210, including but not limited to through-silicon vias (TSVs) 2206. The interposer 2204 may further include embedded devices 2214, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer 2204. The package-on-interposer structure 2236 may take the form of any of the package-on-interposer structures known in the art.

[0110] The IC device assembly 2200 may include an IC package 2224 coupled to the first face 2240 of the circuit board 2202 by coupling components 2222. The coupling components 2222 may take the form of any of the embodiments discussed above with reference to the coupling components 2216, and the IC package 2224 may take the form of any of the embodiments discussed above with reference to the IC package 2220.

[0111] The IC device assembly 2200 illustrated in FIG. 10 includes a package-on-package structure 2234 coupled to the second face 2242 of the circuit board 2202 by coupling components 2228. The package-on-package structure 2234 may include an IC package 2226 and an IC package 2232 coupled together by coupling components 2230 such that the IC package 2226 is disposed between the circuit board 2202 and the IC package 2232. The coupling components 2228 and 2230 may take the form of any of the embodiments of the coupling components 2216 discussed above, and the IC packages 2226 and 2232 may take the form of any of the embodiments of the IC package 2220 discussed above. The package-on-package structure 2234 may be configured in accordance with any of the package-on-package structures known in the art.

[0112] FIG. 11 is a block diagram of an example computing device 2300 that may include one or more components including one or more transistor having uneven gate-drain surfaces in accordance with any of the embodiments disclosed herein. For example, any suitable ones of the components of the computing device 2300 may include a die (e.g., the die 2002 (FIG. 8B)) having one or more transistors having uneven gate-drain surfaces in accordance with any of the embodiments disclosed herein. Any one or more of the components of the computing device 2300 may include, or be included in, an IC device 2100 (FIG. 9). Any one or more of the components of the computing device 2300 may include, or be included in, an IC device assembly 2200 (FIG. 10).

[0113] A number of components are illustrated in FIG. 11 as included in the computing device 2300, but any one or more of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the components included in the computing device 2300 may be attached to one or more motherboards. In some embodiments, some or all of these components are fabricated onto a single system-on-a-chip (SoC) die.

[0114] Additionally, in various embodiments, the computing device 2300 may not include one or more of the components illustrated in FIG. 11, but the computing device 2300 may include interface circuitry for coupling to the one or more components. For example, the computing device 2300 may not include a display device 2306, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 2306 may be coupled. In another set of examples, the computing device 2300 may not include an audio input device 2318 or an audio output device 2308, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 2318 or audio output device 2308 may be coupled.

[0115] The computing device 2300 may include a processing device 2302 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 2302 may include one or more digital signal processors (DSPs), application-specific integrated circuits (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices. The computing device 2300 may include a memory 2304, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), nonvolatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive. In some embodiments, the memory 2304 may include memory that shares a die with the processing device 2302. This memory

may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random-access memory (STT-MRAM).

[0116] In some embodiments, the computing device 2300 may include a communication chip 2312 (e.g., one or more communication chips). For example, the communication chip 2312 may be configured for managing wireless communications for the transfer of data to and from the computing device 2300. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a nonsolid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0117] The communication chip 2312 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 802.11 family), IEEE 802.16 standards (e.g., IEEE 802.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultramobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 802.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. The communication chip 2312 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 2312 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 2312 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 2312 may operate in accordance with other wireless protocols in other embodiments. The computing device 2300 may include an antenna 2322 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0118] In some embodiments, the communication chip 2312 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 2312 may include multiple communication chips. For

instance, a first communication chip 2312 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 2312 may be dedicated to longer-range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 2312 may be dedicated to wireless communications, and a second communication chip 2312 may be dedicated to wired communications.

[0119] The computing device 2300 may include battery/power circuitry 2314. The battery/power circuitry 2314 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the computing device 2300 to an energy source separate from the computing device 2300 (e.g., AC line power).

[0120] The computing device 2300 may include a display device 2306 (or corresponding interface circuitry, as discussed above). The display device 2306 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[0121] The computing device 2300 may include an audio output device 2308 (or corresponding interface circuitry, as discussed above). The audio output device 2308 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0122] The computing device 2300 may include an audio input device 2318 (or corresponding interface circuitry, as discussed above). The audio input device 2318 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0123] The computing device 2300 may include a global positioning system (GPS) device 2316 (or corresponding interface circuitry, as discussed above). The GPS device 2316 may be in communication with a satellite-based system and may receive a location of the computing device 2300, as known in the art.

[0124] The computing device 2300 may include an other output device 2310 (or corresponding interface circuitry, as discussed above). Examples of the other output device 2310 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0125] The computing device 2300 may include an other input device 2320 (or corresponding interface circuitry, as discussed above). Examples of the other input device 2320 may include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0126] The computing device 2300 may have any desired form factor, such as a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultramobile personal computer, etc.), a desktop computing device, a server or other networked computing component, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device. In some embodiments, the computing device 2300 may be any other electronic device that processes data.

[0127] The following paragraphs provide various examples of the embodiments disclosed herein.

[0128] Example 1 provides a transistor structure, the transistor structure including a gate electrode stack, a drain region (also referred to herein as a “HD drain region” or a “drain diffusion region”); and a material, e.g. a semiconductor material, between the gate electrode stack and the drain region, wherein a surface of the material between the gate electrode stack and the drain region includes at least one feature, the at least one feature comprising a recess or a protrusion. Thus, unlike conventional implementations, the surface of the material between the gate electrode stack and the drain region is not flat, where, as used herein, a surface qualifies as “not flat” if root mean square (RMS) surface roughness is about 0.5 nm or more.

[0129] In all Examples described herein, each of the source and drain regions of a transistor structure are regions of doped semiconductor materials, while the channel material may include one or more semiconductor materials with doping concentrations significantly smaller than those of the source and drain regions. For example, in some embodiments, the channel material may be an intrinsic (i.e. undoped) III-V or IV semiconductor material or alloy, not intentionally doped with any electrically active impurity. In alternate embodiments, one or more a nominal impurity dopant level may be present within the channel material, for example to set a threshold voltage V_t , or to provide HALO pocket implants, etc. In such impurity-doped embodiments however, impurity dopant level within the channel material are still significantly lower than in the source and drain regions, for example below 10^{15} dopant elements per cubic centimeter (cm^{-3}), and advantageously below 10^{13} cm^{-3} . Also in all Examples described herein, the gate electrode material, as well as each of the source electrode material and the drain electrode material, may include one or more of conductor materials, e.g. one or more metals.

[0130] Example 2 provides the transistor structure according to Example 1, where a dimension of the at least one feature in a direction perpendicular to the center of the gate electrode stack (i.e. in a direction in which the materials of the gate electrode stack are stacked in the center of the gate electrode stack), or perpendicular to the substrate on which the transistor structure is provided, is at

least 10 nanometers (e.g. if the feature is a recess, then the recess may have a depth of at least 10 nanometers; or if the feature is a protrusion, then the protrusion may have a height of at least 10 nm).

[0131] Example 3 provides the transistor structure according to Examples 1 or 2, where the shortest distance between the gate electrode stack and the drain region along a surface of the material that includes the at least one feature (i.e. the gate-drain feature distance described herein) is greater than about 90 nanometers, e.g. between about 90 and 1000 nm, or between about 150 and 500 nm.

[0132] Example 4 provides the transistor structure according to any one of Examples 1-3, where a lateral distance between the gate electrode stack and the drain region (i.e. the planar gate-drain distance described herein) is at least 10 nm smaller than the shortest distance between the gate electrode stack and the drain region along the surface of the material that includes the at least one feature (i.e. the gate-drain feature distance described herein), e.g. less than about 20 nm.

[0133] Example 5 provides the transistor structure according to any one of Examples 1-3, where a lateral distance between the gate electrode stack and the drain region (i.e. the planar gate-drain distance described herein) is less than about 90% of the shortest distance between the gate electrode stack and the drain region along the surface of the material that includes the at least one feature (i.e. the gate-drain feature distance described herein). For example, the planar gate-drain distance d_L may be e.g. less than about 80%, or less than about 60% of the gate-drain feature distance d_{feat} .

[0134] Example 6 provides the transistor structure according to any one of Examples 1-5, where the at least one feature is a first feature and the surface of the material between the gate electrode stack and the drain region further includes a second feature.

[0135] Example 7 provides the transistor structure according to Example 6, where each of the first feature and the second feature is a recess.

[0136] Example 8 provides the transistor structure according to Example 6, where each of the first feature and the second feature is a protrusion.

[0137] Example 9 provides the transistor structure according to Example 6, where the first feature is a recess and the second feature is a protrusion.

[0138] Example 10 provides the transistor structure according to any one of the preceding Examples, where the drain region is a region having a dopant concentration higher than a dopant concentration between the drain region and a source region of the transistor structure.

[0139] Example 11 provides the transistor structure according to any one of the preceding Examples, where the drain region has a dopant concentration of at least $5 \cdot 10^{16}$ dopant elements per cubic centimeter.

[0140] Example 12 provides the transistor structure according to any one of Examples 1-11, where the material is shaped as a fin, and the gate electrode stack wraps around the fin.

[0141] Example 13 provides the transistor structure according to any one of Examples 1-11, where the material is shaped as a wire, and the gate electrode stack wraps around the wire.

[0142] Example 14 provides the transistor structure according to Example 13, where the gate electrode stack wraps entirely around the wire.

[0143] Example 15 provides the transistor structure according to any one of the preceding Examples, where the material includes a III-V semiconductor material.

[0144] Example 16 provides the transistor structure according to Example 15, where the material includes a stack of materials, the stack including a polarization layer (e.g. a layer of AlN, InAlN, or AlGaIn) on the III-N semiconductor material (e.g. GaN material).

[0145] Example 17 provides the transistor structure according to any one of the preceding Examples, further including a drain electrode electrically connected to the drain region.

[0146] Example 18 provides a transistor structure that includes a gate electrode stack; a drain region (also referred to as “HD drain region” or a “drain diffusion region”); and a semiconductor material (also referred to as a “channel material”) between the gate electrode stack and the drain region, where a surface of the material between the gate electrode stack and the drain region has a root mean square (RMS) surface roughness of at least about 5 nanometers.

[0147] Example 19 provides the transistor structure according to Example 18, where the surface includes a first portion that includes/is substantially a planar surface, and a second portion that includes at least one feature, the at least one feature including a recess or a protrusion, and the at least one feature has at least one point that is at a distance of at least about 5 nanometers, e.g. at least about 10 nm, from a plane of the first portion of the surface.

[0148] Example 20 provides the transistor structure according to Example 19, where the RMS surface roughness of the first portion of the surface is less than 0.5 nanometers.

[0149] In further Examples, the transistor structure according to any one of Examples 18-20 may be a transistor structure according to any one of Examples 2-17.

[0150] Example 21 provides a computing device, including a substrate; and an integrated circuit (IC) die coupled to the substrate, where the IC die includes a transistor structure having a gate electrode stack, a drain region, and a semiconductor material between the gate electrode stack and the drain region, where a surface of the material between the gate electrode stack and the drain region is not flat.

[0151] Example 22 provides the computing device according to Example 21, where the surface that is not flat includes a surface having root mean square (RMS) surface roughness of at least about 0.5 nanometers.

[0152] Example 23 provides the computing device according to Examples 21 or 22, where the computing device is a wearable or handheld computing device.

[0153] Example 24 provides the computing device according to any one of Examples 21-23, where the computing device further includes one or more communication chips and an antenna.

[0154] Example 25 provides the computing device according to any one of Examples 21-24, where the substrate is a motherboard.

[0155] Example 26 provides the computing device according to any one of Examples 21-25, where the surface includes at least one feature, the at least one feature including a recess or a protrusion.

[0156] Example 27 provides the computing device according to Example 26, where a dimension of the at least one feature in a direction perpendicular to the gate electrode stack (i.e. in a direction in which the materials of the gate electrode stack are stacked) is at least 10 nanometers (e.g. if the feature is a recess, then the recess may have a depth of at least 10 nanometers; or if the feature is a protrusion, then the protrusion may have a height of at least 10 nm).

[0157] Example 28 provides the computing device according to Examples 26 or 27, where the shortest distance between the gate electrode stack and the drain region along the surface of the material that includes the at least one feature (i.e. the gate-drain feature distance described herein) is greater than about 90 nanometers, e.g. between about 90 and 1000 nm, or between about 150 and 500 nm.

[0158] Example 29 provides the computing device according to any one of Examples 26-28, where a lateral distance between the gate electrode stack and the drain region (i.e. the planar gate-drain distance described herein) is at least 10 nm smaller than the shortest distance between the gate electrode stack and the drain region along the surface of the material that includes the at least one feature (i.e. the gate-drain feature distance described herein), e.g. less than 20 nm.

[0159] Example 30 provides the computing device according to any one of Examples 26-28, where a lateral distance between the gate electrode stack and the drain region (i.e. the planar gate-drain distance described herein) is less than about 90% of the shortest distance between the gate electrode stack and the drain region along the surface of the material that includes the at least one feature (i.e. the gate-drain feature distance described herein). For example, the planar gate-drain distance d_l may be e.g. less than about 80%, or less than about 60% of the gate-drain feature distance d_{feat} .

[0160] In further Examples, the transistor structure of the computing device according to any one of Examples 21-30 may be a transistor structure according to any one of Examples 6-17.

[0161] Example 31 provides a method of fabricating a transistor structure, the method including providing one or more semiconductor materials for forming a channel of the transistor structure, a surface of the one or more semiconductor materials having at least one recess or/and at least one protrusion; providing a drain region within a first portion of the one or more semiconductor materials, the drain region including one or more doped semiconductor materials; and providing a gate electrode stack over a second portion of the one or more semiconductor materials, where the surface of the one or more semiconductor materials having the at least one recess or/and the at least one protrusion is between the drain region and the gate electrode stack.

[0162] Example 32 provides the method according to Example 31, where providing the drain region includes doping the one or more semiconductor materials of the channel to form the drain region.

[0163] Example 33 provides the method according to Example 32, further including performing an anneal of the transistor structure to activate dopants of the drain region.

[0164] Example 34 provides the method according to Example 31, where providing the drain region includes forming an opening in the one or more semiconductor materials of the channel, and depositing the one or more doped semiconductor materials into the opening, e.g. using chemical vapor deposition (CVD), atomic layer deposition (ALD), or physical vapor deposition (PVD).

[0165] In further Examples, the method also includes providing a drain electrode material to be in electrical contact with the drain region. In various Examples, providing transistor structure electrode materials (i.e. gate, source, and drain electrode materials) includes depositing titanium, aluminum, titanium nitride, erbium, gadolinium, or ytterbium, using any suitable deposition and patterning techniques.

[0166] The above description of illustrated implementations of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

[0167] These modifications may be made to the disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit the disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope of the disclosure is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

CLAIMS:

1. A transistor structure, comprising:
a gate electrode stack;
a drain region; and
a semiconductor material between the gate electrode stack and the drain region, wherein the semiconductor material includes at least one feature between the gate electrode stack and the drain region, the at least one feature comprising a recess or a protrusion.
2. The transistor structure according to claim 1, wherein the semiconductor material is over a substrate, and a dimension of the at least one feature in a direction perpendicular to the substrate is at least 10 nanometers.
3. The transistor structure according to claim 1, wherein the shortest distance between the gate electrode stack and the drain region along a surface of the semiconductor material that includes the at least one feature is greater than 90 nanometers.
4. The transistor structure according to any one of claims 1-3, wherein a lateral distance between the gate electrode stack and the drain region is at least 10 nm smaller than the shortest distance between the gate electrode stack and the drain region along a surface of the semiconductor material that includes the at least one feature.
5. The transistor structure according to any one of claims 1-3, wherein a lateral distance between the gate electrode stack and the drain region is less than 90% of the shortest distance between the gate electrode stack and the drain region along a surface of the semiconductor material that includes the at least one feature.
6. The transistor structure according to any one of claims 1-3, wherein the at least one feature is a first feature and a surface of the semiconductor material between the gate electrode stack and the drain region further includes a second feature.
7. The transistor structure according to claim 6, wherein each of the first feature and the second feature is a recess.

8. The transistor structure according to claim 6, wherein each of the first feature and the second feature is a protrusion.
9. The transistor structure according to claim 6, wherein the first feature is a recess and the second feature is a protrusion.
10. A transistor structure, comprising:
 - a gate electrode stack;
 - a drain region; and
 - a material between the gate electrode stack and the drain region, wherein a surface of the material between the gate electrode stack and the drain region has a root mean square (RMS) surface roughness of at least 5 nanometers.
11. The transistor structure according to claim 10, wherein:
 - the surface includes a first portion that includes a planar surface, and a second portion that includes at least one feature, the at least one feature comprising a recess or a protrusion, and
 - the at least one feature has at least one point that is at a distance of at least 5 nanometers from a plane of the first portion of the surface.
12. The transistor structure according to claim 11, wherein the RMS surface roughness of the first portion of the surface is less than 0.5 nanometers.
13. A computing device, comprising:
 - a substrate; and
 - an integrated circuit (IC) die coupled to the substrate, wherein the IC die includes a transistor structure having:
 - a gate electrode stack;
 - a drain region; and
 - a material between the gate electrode stack and the drain region, wherein a surface of the material between the gate electrode stack and the drain region is not flat.
14. The computing device according to claim 13, wherein the surface that is not flat comprises a surface having root mean square (RMS) surface roughness of at least 0.5 nanometers.

15. The computing device according to claims 13 or 14, wherein the computing device is a wearable or handheld computing device.
16. The computing device according to claims 13 or 14, wherein the computing device further includes one or more communication chips and an antenna.
17. The computing device according to claims 13 or 14, wherein the surface includes at least one feature, the at least one feature comprising a recess or a protrusion.
18. The computing device according to claim 17, wherein a dimension of the at least one feature in a direction perpendicular to the gate electrode stack is at least 10 nanometers.
19. The computing device according to claim 17, wherein the shortest distance between the gate electrode stack and the drain region along the surface of the material that includes the at least one feature is greater than 90 nanometers.
20. The computing device according to claim 17, wherein a lateral distance between the gate electrode stack and the drain region is at least 10 nm smaller than the shortest distance between the gate electrode stack and the drain region along the surface of the material that includes the at least one feature.
21. The computing device according to claim 17, wherein a lateral distance between the gate electrode stack and the drain region is less than 90% of the shortest distance between the gate electrode stack and the drain region along the surface of the material that includes the at least one feature.
22. A method of fabricating a transistor structure, the method comprising:
providing one or more semiconductor materials for forming a channel of the transistor structure, a surface of the one or more semiconductor materials having at least one recess or/and at least one protrusion;
providing a drain region within a first portion of the one or more semiconductor materials, the drain region comprising one or more doped semiconductor materials; and
providing a gate electrode stack over a second portion of the one or more semiconductor materials,

wherein the surface of the one or more semiconductor materials having the at least one recess or/and the at least one protrusion is between the drain region and the gate electrode stack.

23. The method according to claim 22, wherein providing the drain region comprises doping the one or more semiconductor materials of the channel to form the drain region.

24. The method according to claim 23, further comprising performing an anneal of the transistor structure to activate dopants of the drain region.

25. The method according to claim 22, wherein providing the drain region comprises:
forming an opening in the one or more semiconductor materials of the channel, and
depositing the one or more doped semiconductor materials into the opening.

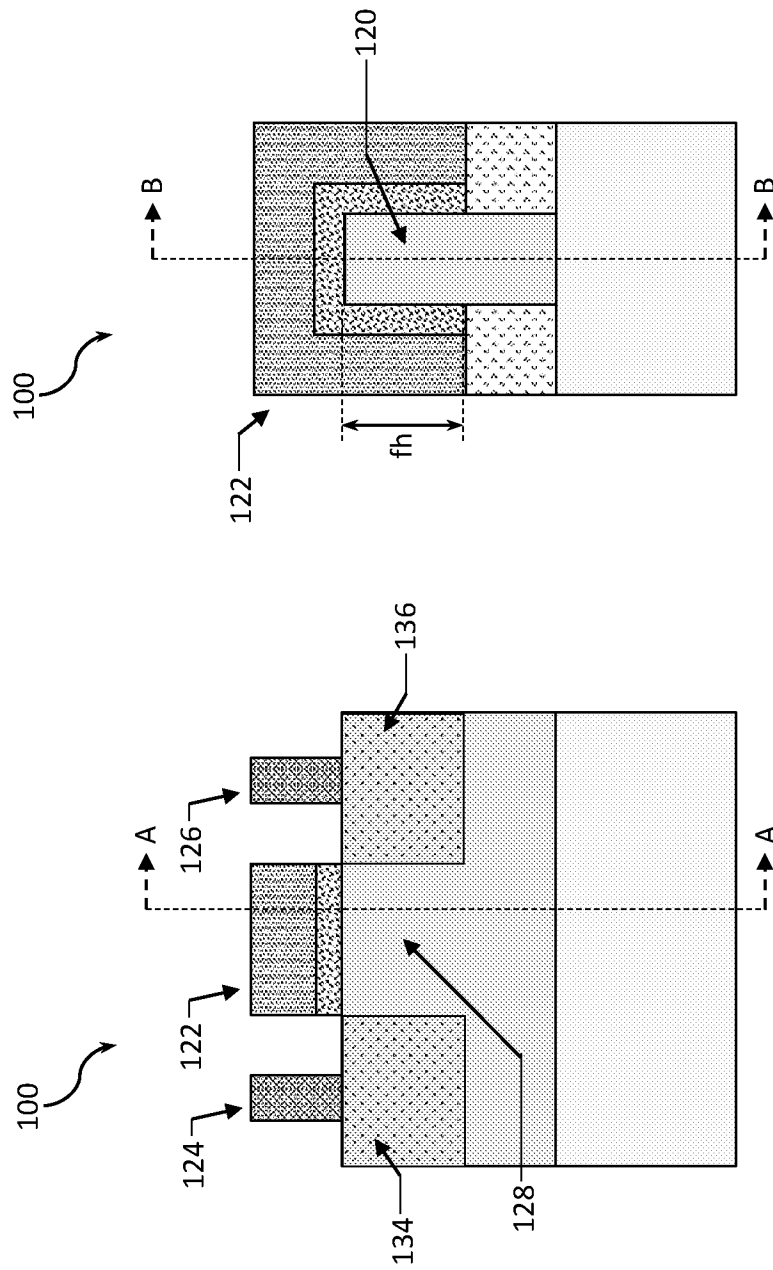


FIG. 1B

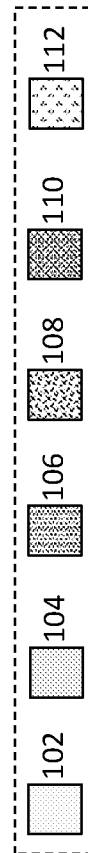
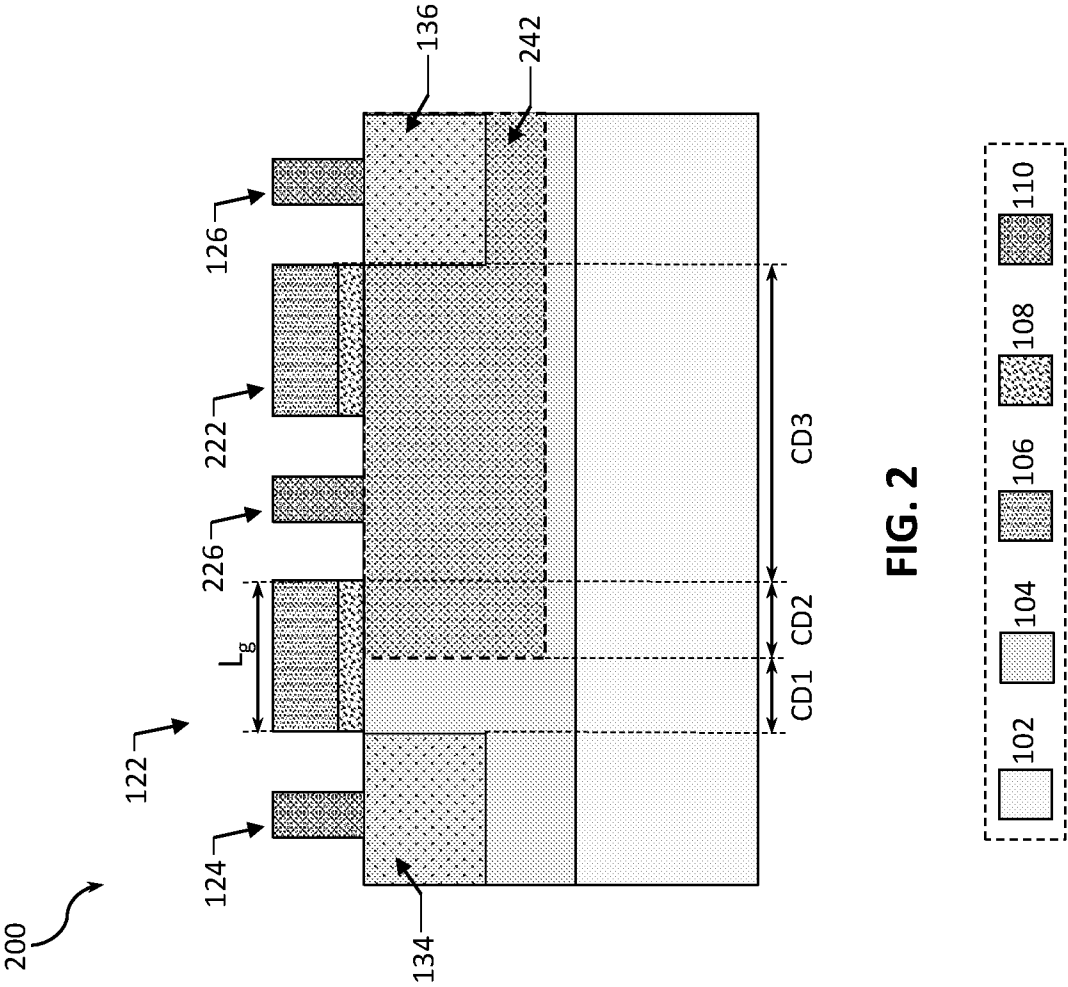
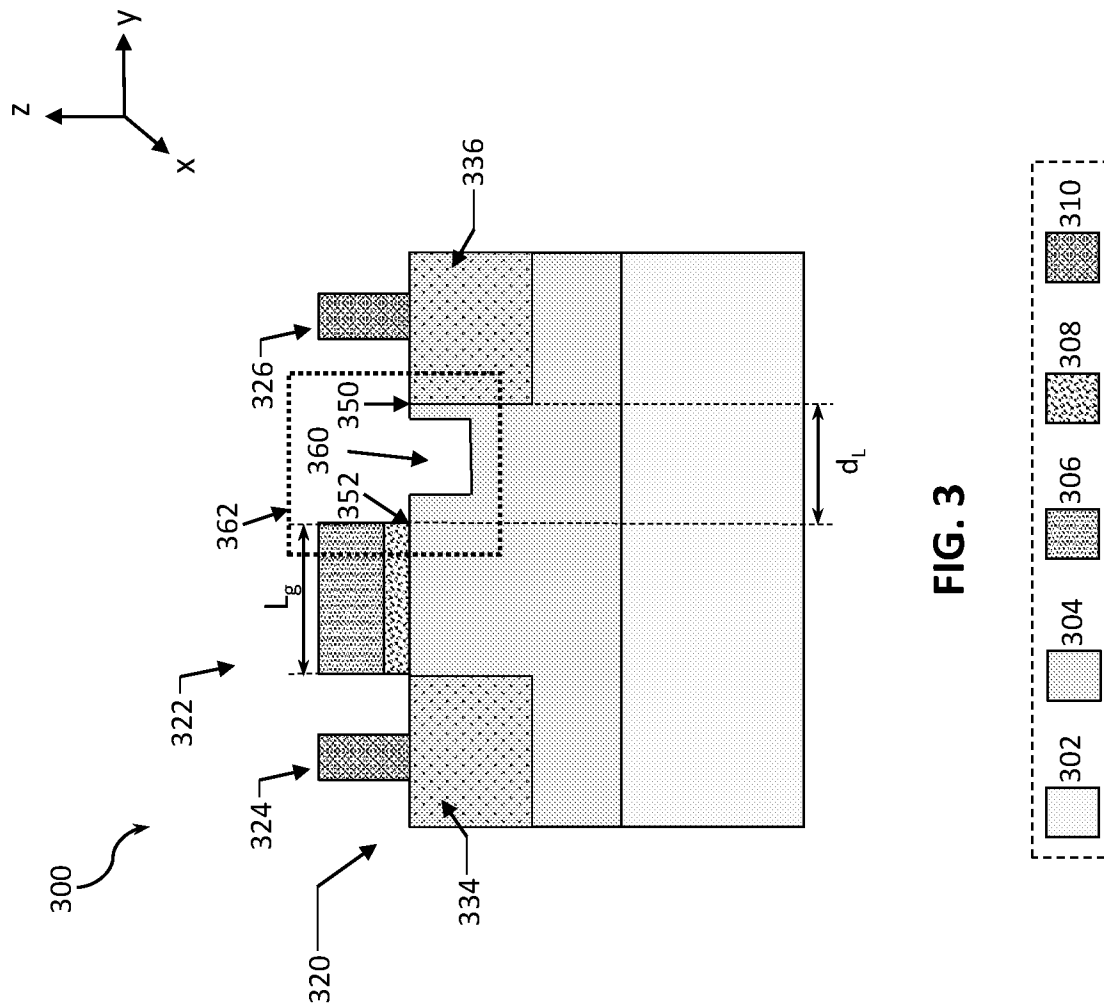


FIG. 1A





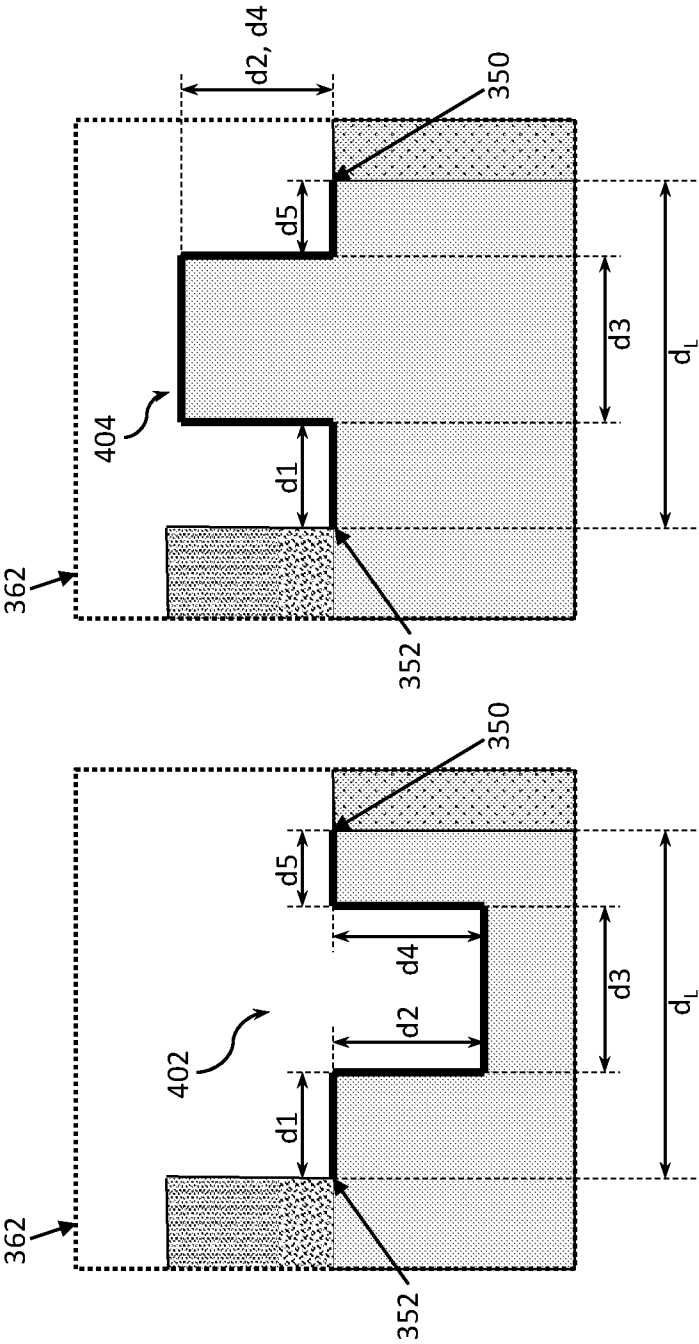


FIG. 4B

FIG. 4A

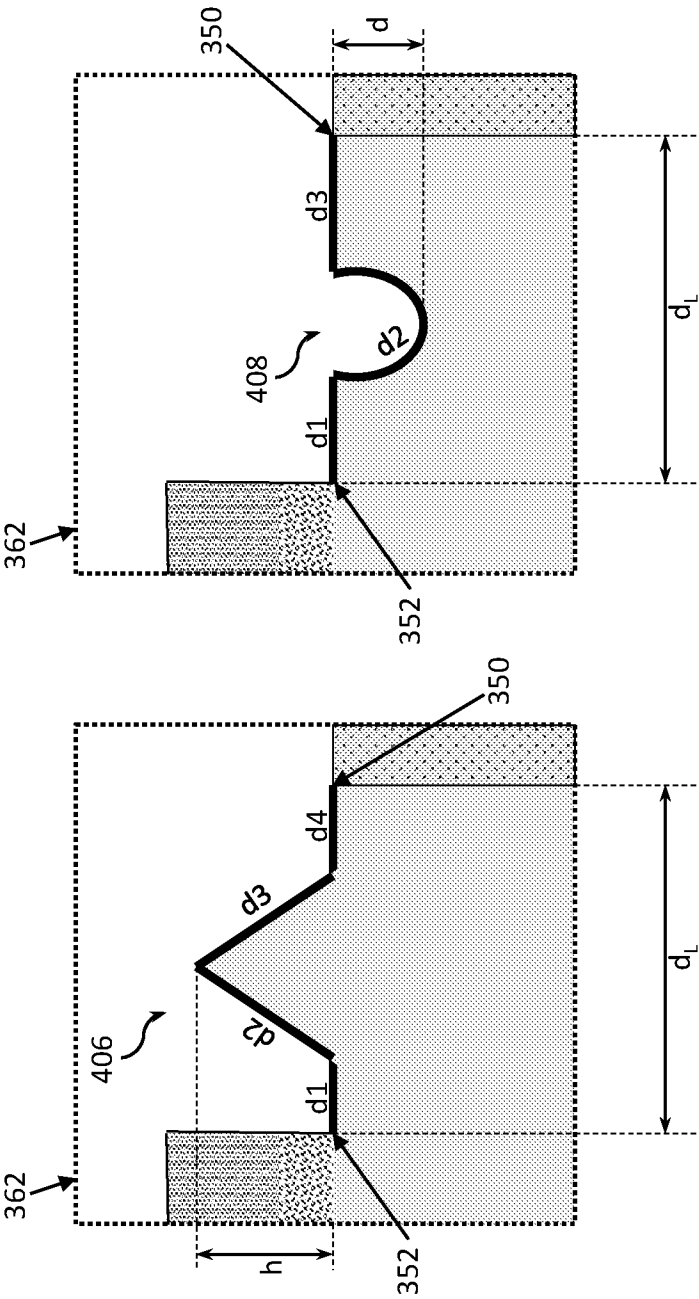


FIG. 4D

FIG. 4C

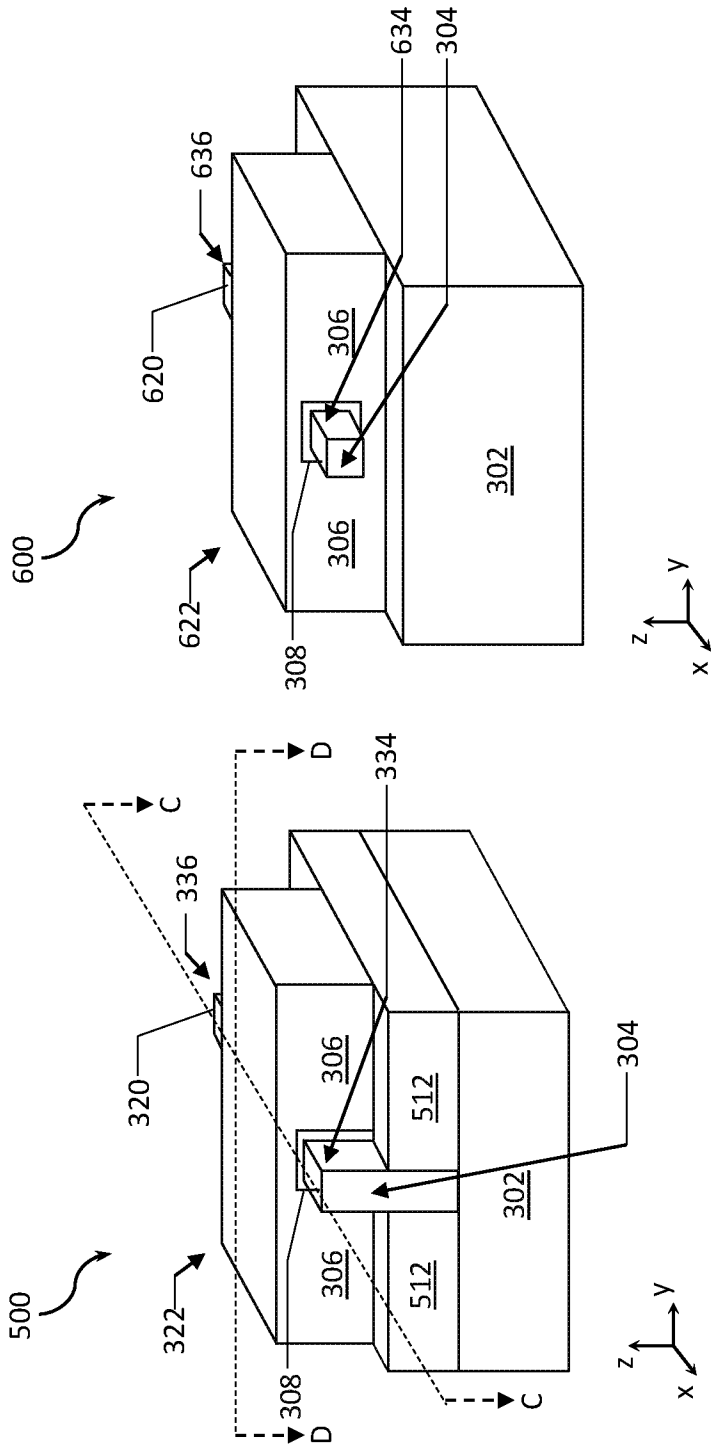


FIG. 5

FIG. 6

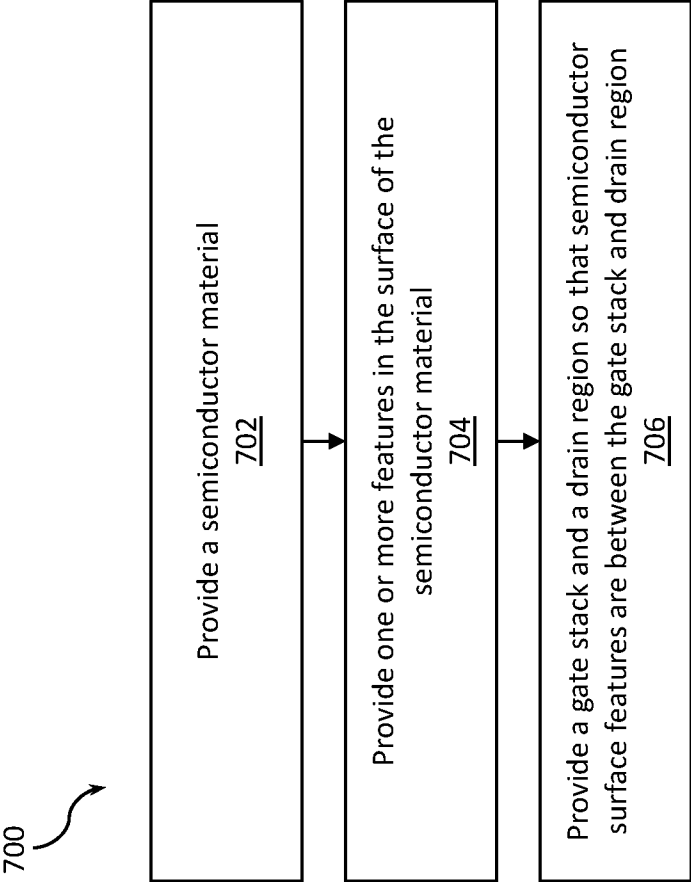


FIG. 7

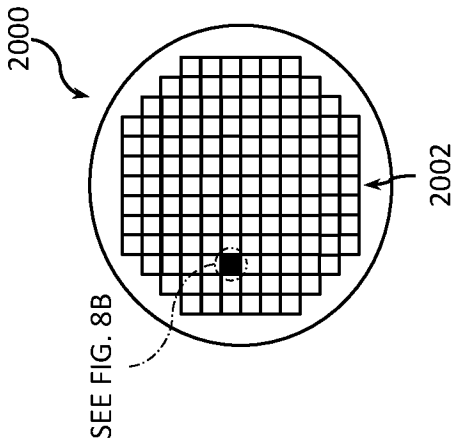


FIG. 8A

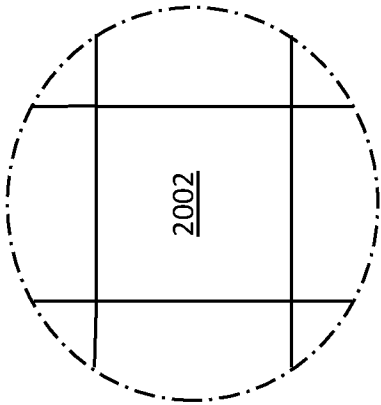


FIG. 8B

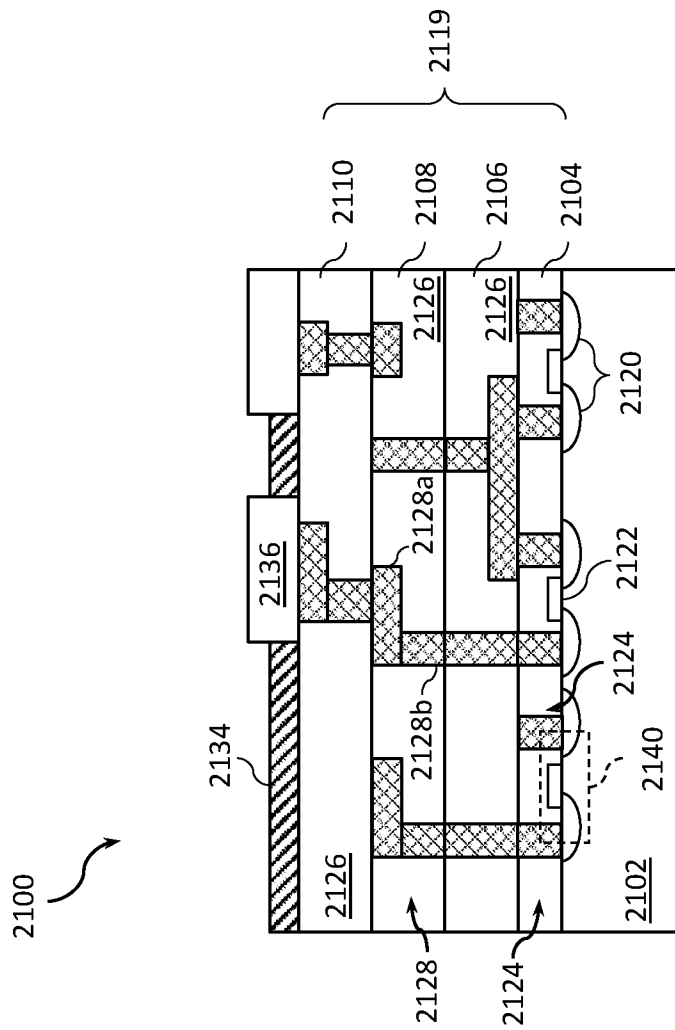


FIG. 9

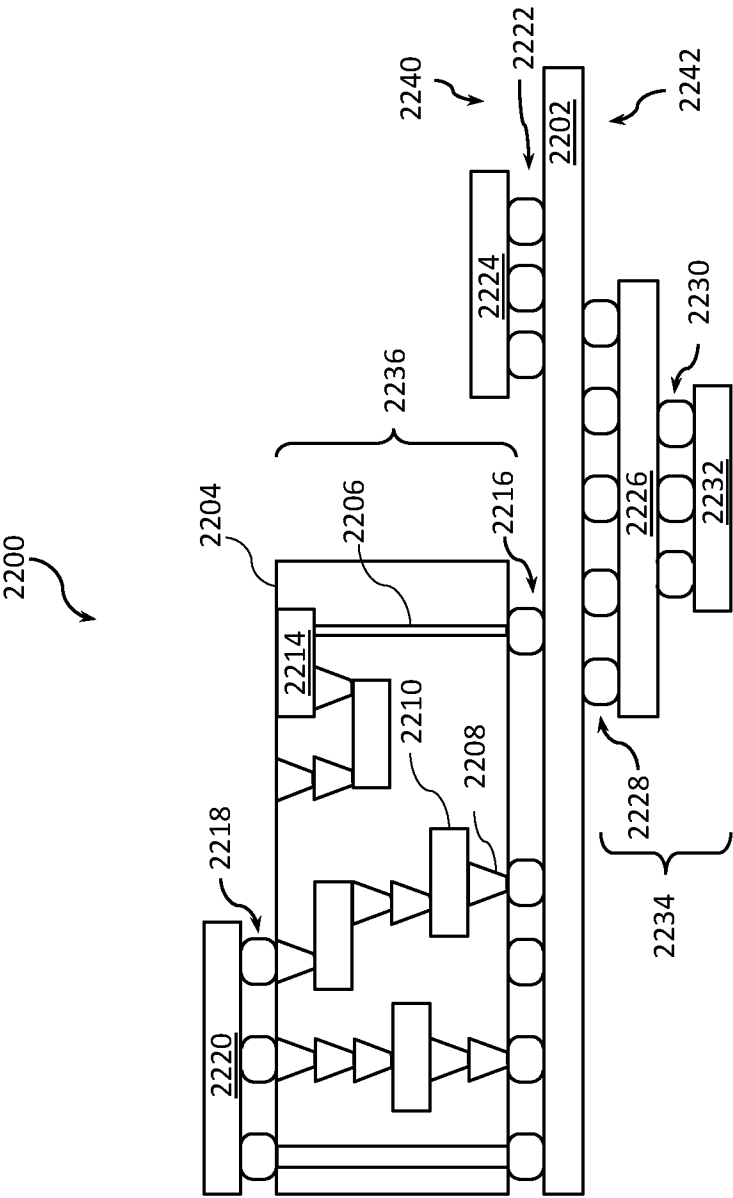


FIG. 10

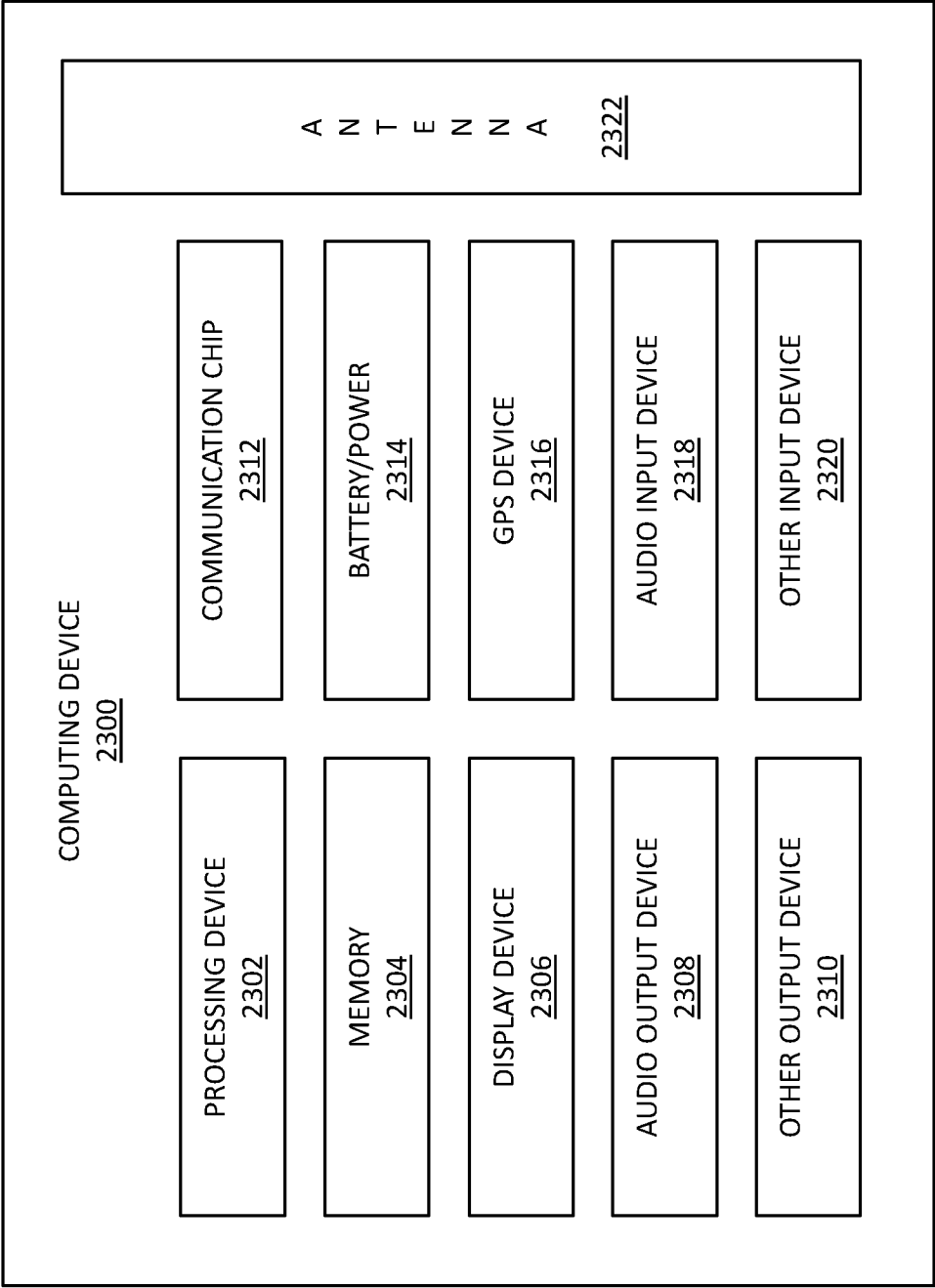


FIG.11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/031633**A. CLASSIFICATION OF SUBJECT MATTER****H01L 29/10(2006.01)i, H01L 29/08(2006.01)i, H01L 29/78(2006.01)i, H01L 29/66(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/10; H01L 29/165; H01L 21/84; H01L 31/0328; H01L 21/336; H01L 29/78; H01L 29/417; H01L 27/092; H01L 29/08; H01L 29/66

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: transistor, source, drain, channel, surface, uneven, recess, protrusion, dimension, distance, root mean square, roughness

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2016-0087053 A1 (JIN-BUM KIM et al.) 24 March 2016 See paragraphs 46-196, claims 19, 33 and figures 1A-12.	1, 6-9, 13, 15-17 , 22-25
A		2-5, 10-12, 14, 18-21
A	US 2015-0380553 A1 (SAMSUNG ELECTRONICS CO., LTD.) 31 December 2015 See paragraphs 39-81 and figures 1A-11B.	1-25
A	US 2004-0201038 A1 (TOKUHARU KIMURA et al.) 14 October 2004 See paragraphs 37-85 and figures 1A-7B.	1-25
A	US 7476898 B2 (MITSUMA OISHI et al.) 13 January 2009 See column 6, line 19-column 7, line 30 and figures 4A-4C.	1-25
A	US 2006-0046407 A1 (WERNER JUENGLING) 02 March 2006 See paragraphs 63-95 and figures 1-13.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search

30 January 2018 (30.01.2018)

Date of mailing of the international search report

30 January 2018 (30.01.2018)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/031633

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