



(51) International Patent Classification:

H01G 11/00 (2013.01) *H01G 9/00* (2006.01)
H01G 11/04 (2013.01) *H01M 16/00* (2006.01)

(21) International Application Number:

PCT/US2015/060530

(22) International Filing Date:

13 November 2015 (13.11.2015)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

14/593,230 9 January 2015 (09.01.2015) US

(71) Applicant: **ANALOG DEVICES, INC.** [US/US]; One Technology Way, Norwood, Massachusetts 02062-9106 (US).

(72) Inventors: **JIANG, Yingqi**; 18 Alaska Avenue, Bedford, Massachusetts 01730 (US). **YANG, Kuang L.**; 40 Van Roosen Road, Newton, Massachusetts 02459 (US).

(74) Agents: **SAUNDERS, Steven G.** et al.; Sunstein Kann Murphy & Timbers LLP, 125 Summer Street, Boston, Massachusetts 02110-1618 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: INTEGRATED CIRCUIT WITH SHARED ELECTRODE ENERGY STORAGE DEVICES

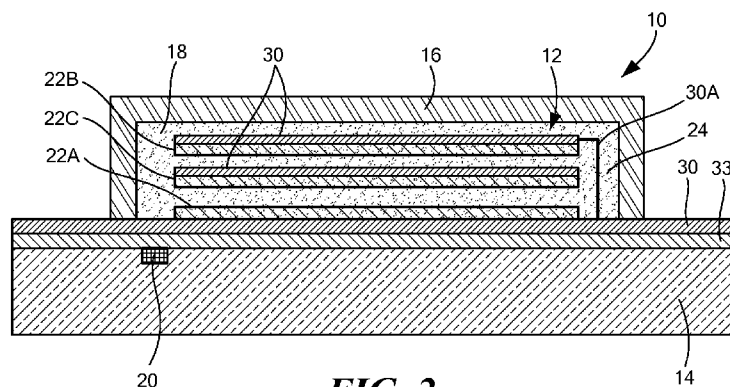


FIG. 2

(57) Abstract: An integrated circuit has a substrate, a super-capacitor supported by the substrate, and a battery supported by the substrate. The super-capacitor includes a super-capacitor electrode and a shared electrode, and the battery has a battery electrode and the prior noted shared electrode. The super-capacitor and battery form at least a part of a monolithic integrated circuit.

INTEGRATED CIRCUIT WITH SHARED ELECTRODE ENERGY STORAGE DEVICES

5

REFERENCE TO RELATED PATENT APPLICATIONS

This patent application is related to the following patent application, each of which is incorporated herein, in its entirety, by reference:

10

- United States patent application number 14/469,004, filed August 26, 2014, entitled, "**METHOD OF PRODUCING A SUPER-CAPACITOR**," assigned attorney docket number 2550/E73, and naming Yingqi Jiang and Kuang L. Yang as inventors,

15

- United States patent application number 14/492,376, filed September 22, 2014, entitled, "**SUPER-CAPACITOR WITH SEPARATOR AND METHOD OF PRODUCIGN THE SAME**," assigned attorney docket number 2550/E75, and naming Yingqi Jiang and Kuang L. Yang as inventors,

20

- United States patent application number 14/509,950, filed October 8, 2014, entitled, "**INTEGRATED SUPER-CAPACITOR**," assigned attorney docket number 2550/E76, and naming Yingqi Jiang and Kuang L. Yang as inventors,

25

FIELD OF THE INVENTION

The invention generally relates to integrated circuits and, more particularly, the invention relates to energy storage devices on integrated circuits.

BACKGROUND OF THE INVENTION

Although the size of portable electronic devices continues to shrink, their energy requirements often do not comparably decrease. For example, a next-
5 generation MEMS accelerometer may have a volume that is 10 percent smaller and yet, require are only 5 percent less power than the prior generation MEMS accelerometer. In that case, more of the MEMS die may be used for energy storage. Undesirably, this trend can limit miniaturization and applicability of such electronic devices.

10 The art has responded to this problem by developing chip-level super-capacitors (also known as “micro super-capacitors”), which have much greater capacitances than conventional capacitors. In a manner similar to conventional capacitors, super-capacitors generally have higher power densities than batteries. Undesirably, however, super-capacitors generally have lower storage capabilities
15 than batteries.

SUMMARY OF VARIOUS EMBODIMENTS

20 In accordance with one embodiment of the invention, an integrated circuit has a substrate, a super-capacitor supported by the substrate, and a battery supported by the substrate. The super-capacitor includes a super-capacitor electrode and a shared electrode, and the battery has a battery electrode and the prior noted shared electrode. The super-capacitor and battery form at least a
25 part of a monolithic integrated circuit.

The battery and super-capacitor may be electrically connected in parallel. Moreover, the shared electrode may be formed at least in part from a material so

that it has surface energy storage capability (i.e., an electrode of this type is used for a super-capacitor, such as graphene) and substantially no volumetric storage capability (i.e., an electrode of this type is for a battery, such as graphite). The shared electrode in that case may form a shared anode for both the super-
5 capacitor and the battery. In that case, among other cases, the super-capacitor electrode and shared electrode can have about the same capacitance. As another example, the shared anode embodiment may have three respective electrodes comprising graphene (super-capacitor), graphene (shared anode), and lithium cobalt oxide (battery cathode).

10 In contrast, the shared electrode may include a material having both surface energy storage capability and volumetric energy storage capability. In that case, the super-capacitor may form an asymmetric super-capacitor with the shared electrode, thus forming a shared cathode for the super-capacitor and the battery. For example, the shared cathode embodiment may have three respective
15 electrodes comprising graphene (super-capacitor), and lithium cobalt oxide (shared cathode), and metal lithium (battery anode).

In some embodiments, at least one of active circuitry and MEMS structure also is/are supported by the substrate and in electrical communication with the battery and the super-capacitor. For example, the integrated circuit may include
20 switching circuitry to switch between at least a) a first state using the battery only, and b) a second state using the super-capacitor only. Moreover, the integrated circuit may include a plurality of layers, and at least one of the layers may include two of the electrodes. Accordingly, both of these same-layer electrodes may be formed by the same processing/microfabrication step.

25 The electrodes may be shaped and oriented in a wide variety of geometries. For example, the super-capacitor electrode may have a portion that is interdigitated with a portion of the battery electrode.

In accordance with another embodiment of the invention, a micro-level energy storage device has a substrate, a first electrode formed from a material having surface energy storage capability (but no volumetric energy storage capability), and a second electrode formed from a material having volumetric energy storage capability. The device also has a third electrode formed from a material having one or both surface energy storage capability and volumetric energy storage capability, and an electrolyte in communication with the first electrode, the second electrode, and the third electrode. The first electrode is configured to interact with the third electrode to form first energy storage device and, in a similar manner, the second electrode is configured to interact with the third electrode to form a second energy storage device. The substrate, first electrode, second electrode, and third electrode form at least a part of a monolithic integrated circuit.

In accordance with other embodiments, a method of forming an integrated circuit having an energy storage device forms first, second, and third electrodes on a substrate, and adds an electrolyte to the substrate so that the electrolyte at least partly encapsulates the first and second electrodes. The third electrode is spaced from the first and second electrodes. The electrolyte is between the first electrode and the third electrode, and between the second electrode and the third electrode. The method also separates (e.g., through cutting, dicing, breaking, or other conventional technique) the substrate into a plurality of individual monolithic integrated circuit dice/dies. A plurality of the dice have the first electrode, the second electrode, and the third electrode. Moreover, that plurality of dice each are configured so that the first electrode interacts with the third electrode to form first energy storage device, and so that the second electrode interacts with the third electrode to form a second energy storage device.

BRIEF DESCRIPTION OF THE DRAWINGS

Those skilled in the art should more fully appreciate advantages of various embodiments of the invention from the following "Description of Illustrative Embodiments," discussed with reference to the drawings summarized immediately below.

Figure 1 schematically shows a perspective view of an integrated circuit having a shared energy device that may be configured in accordance with illustrative embodiments of the invention.

Figure 2 schematically shows a cross-sectional view of the integrated circuit shown in Figure 1 across line 2-2.

Figure 3 schematically shows a diagram of the electrical connections of an internal battery and super-capacitor within the integrated circuit of Figure 1.

Figure 4A schematically shows a first interdigitated arrangement of electrodes configured in accordance with illustrative embodiments of the invention.

Figure 4B schematically shows a second interdigitated arrangement of electrodes configured in accordance with illustrative embodiments of the invention.

Figure 4C schematically shows a cross-sectional view of the electrode implementations of Figures 4A and 4B.

Figure 5A schematically shows a perspective, exploded view of another electrode arrangement configured in accordance with illustrative embodiments of the invention.

Figure 5B schematically shows a cross-sectional view of the electrode arrangement of Figure 5A.

Figure 6 shows a process of forming a monolithic integrated circuit having a shared energy device configured in accordance with illustrative embodiments of the invention.

Figure 7A schematically shows a cross-sectional view of the process of Figure 6 through step 600.

Figure 7B schematically shows a cross-sectional view of the process of Figure 6 through step 602.

Figure 7C schematically shows a cross-sectional view of the process of Figure 6 through step 604.

Figure 7D schematically shows a cross-sectional view of the process of Figure 6 through step 606.

Figure 7E schematically shows a cross-sectional view of the process of Figure 6 through step 608.

DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

In illustrative embodiments, an integrated circuit has a shared energy device with a super-capacitor and battery that together share a common electrode. Depending on the design, the common electrode can form either a common anode or a common cathode. Such a shared energy device therefore can respond to high-power spikes from an underlying device or circuit while still delivering effective long-term energy storage needs. Details of illustrative embodiments are discussed below.

Figure 1 schematically shows a perspective view of an integrated circuit 10 having a shared energy device 12 configured in accordance with illustrative embodiments of the invention. Figure 2 schematically shows one embodiment of

a cross-sectional view of the integrated circuit 10 along line 2-2 of Figure 1. As shown, the integrated circuit 10 may be considered to be a monolithic, unitary chip-level device having a multilayer substrate 14 supporting a cap 16 that together form an interior chamber 18. Among other things, the interior chamber
5 18 has a plurality of electrodes 22A-22C and electrolyte material(s) 24 that together form a super-capacitor 26 and a battery 28. In other words, the electrodes 22A-22C and electrolyte material 24 cooperate to have the capacity to store a prescribed electrical charge.

The interior chamber 18 also may have internal circuitry 20, which may
10 include any of a wide variety of different devices commonly formed on an integrated circuit. Among other things, the circuitry 20 can contain active circuit devices (e.g., diodes and transistors) and/or passive circuit devices (resistors, and inductors, and standard capacitors) that together provide the desired functionality. For example, the circuitry 20 can form one or more of a digital
15 signal processor, a controller, a microprocessor, and adder, a digital-to-analog converter, and/or memory. In addition or alternatively, the integrated circuit 10 also may have movable microstructure and thus, form a microelectromechanical system (i.e., a MEMS device).

In some embodiments, the circuitry 20 may include one or more
20 additional batteries and/or super-capacitors that do not share an electrode. Further embodiments may have more shared energy devices 12 similar to those discussed above and below. Accordingly, illustrative embodiments are not limited to integrated circuits 10 having one shared energy device 12 only. For simplicity, Figure 2 generically identifies both the circuitry (e.g., additional
25 batteries, super-capacitors, converters, etc.) and microstructure schematically by reference number 20.

The electrode used only for the super-capacitor 26 is referred to herein as a "super-capacitor electrode 22A" (Figure 2), while the electrode used only for the battery 28 only is referred to herein as a "battery electrode 22B" (Figure 2). The electrode shared by both the super-capacitor 26 and the battery 28 simply is referred to herein as a "shared electrode 22C" (Figure 2). As discussed below, these electrodes 22A-22C are formed on the substrate 14, which has an insulation layer 33.

In the embodiment shown in Figure 2, the shared electrode 22C is sandwiched between the battery electrode 22B and the super-capacitor electrode 22A—essentially a "stacked" electrode arrangement. Thus, the battery electrode 22B and shared electrode 22C interact to form the battery 28, while the super-capacitor electrode 22A and shared electrode 22C interact to form the super-capacitor 26. In some embodiments, the shared electrode 22C and super-capacitor electrode 22A interact to form what is known in the art as an "asymmetric super-capacitor." As discussed in greater detail below, a stacked configuration like that shown in Figure 2 is but one of a wide variety of different electrode configurations.

To improve conductivity and provide exterior access to the electrodes 22A-22C, illustrative embodiments form current collector layers 30. Each current collector layer 30 is in electrical contact with one of the electrodes 22A-22C. In addition, the current collector layers 30 are in electrical communication with conductive contacts 31 on the exterior of the integrated circuit 10. Some embodiments form the conductive contacts 31 by elongating the current collector layers 30 to the outside of the interior chamber 18. Among other things, the current collector layer 30 may be formed from a highly conductive metal, such as gold, or a highly doped semiconductor, such as polysilicon. Those skilled in the art can select other materials for this purpose.

In preferred embodiments, the battery electrode 22B and the super-capacitor electrode 22A are maintained at substantially the same potential through a connection represented schematically by reference number 30A. Although this connection 30A is shown schematically as a simple line, those skilled in the art can use any of a number of different techniques for making that connection. Some embodiments, however, may not maintain the battery electrode 22B and super-capacitor electrode 22A at the same potential.

The electrodes 22A and 22B respectively used for the super-capacitor 26 and battery 28 may be formed from conventional materials known in the art.

More specifically, to improve surface charge storage capacity, the super-capacitor electrode 22A preferably is formed from a porous material. For example, the super-capacitor electrode 22A may be formed from graphene, which is known to be a porous material with tortuous interior and exterior surfaces. Virtually every surface of the super-capacitor electrode 22A exposed to the electrolyte 24 therefore may be considered part of the surface area of the capacitor plates represented in the well-known equation:

$$C = \epsilon^*(A/D) \text{ (Equation 1),}$$

where:

C is capacitance,

ϵ is a constant,

A is the area, and

D is distance.

Indeed, those skilled in the art can use other materials to form the super-capacitor electrode 22A, such as activated carbon, carbon aerogel, or carbon

nanotubes, to name but a few. Some embodiments may form the super-capacitor electrode 22A from a plurality of graphene monolayers. Accordingly, discussion of a layer of graphene is by example only and not intended to limit various other embodiments of the invention.

5 As known by those skilled in the art, the super-capacitor electrode 22A has surface energy storage capability. In particular, this electrode has the quality of being capable of storing charge at its surface. In contrast, however, the super-capacitor electrode 22A does not have the effective ability to store charge/power an appreciable distance beneath its surface; i.e., at the molecular level within the
10 larger volume of material forming the super-capacitor electrode 22A.

 Super-capacitors therefore typically are considered to have a negligible “volumetric energy storage capacity.” As such, when compared to batteries, super-capacitors are known to have a lower capability for storing energy/charge. Despite this shortcoming, super-capacitors also are known to have the capability
15 of generally providing higher power densities than those of comparably sized batteries. The super-capacitor 26 thus should be useful when a circuit powered by the battery 28 demands a very high current/power for a short time (a power “spike”). As discussed in more detail below, the shared energy device 12 has the capability to provide both adequate power during spikes, and substantial energy
20 storage capability during steady state operation.

 The battery electrode 22B may be formed from any conventional material having a non-negligible volumetric energy storage capability. For example, among other things, the battery electrode 22B may be formed at least in part from graphite or lithium. Moreover, although it has substantial volumetric
25 energy storage capacity, the battery electrode 22B also may store some of its energy/charge at or near its surface.

Those skilled in the art can select any of a variety of materials for the shared electrode 22C. Some embodiments may form the shared electrode 22C from a material better suited for a super-capacitor application. For example, the shared electrode 22C may act as an anode formed from graphene. In that case, illustrative embodiments may form the shared electrode 22C to have about the same capacitance as that of the super-capacitor electrode 22A.

Other embodiments, however, may form the shared electrode 22C from a material better suited for a battery application. For example, the shared electrode 22C may act as a cathode formed from lithium cobalt oxide (LiCoO₂).

In the latter case, the super-capacitor electrode 22A and shared electrode 22C may be considered to form an asymmetric super-capacitor (suggested above). Accordingly, the shared electrode 22C may have both surface energy storage capacity and volumetric energy storage capacity, or surface energy storage capacity only. Indeed, as noted above, those skilled in the art can select an appropriate material for the shared electrode 22C and thus, the materials discussed above are mentioned for illustrative purposes only.

The electrolyte 24 can be formed from any of a wide variety of other corresponding materials typically used in powering applications. For example, electrolyte 24 can be formed from an aqueous salt, such as sodium chloride, or a gel, such as a polyvinyl alcohol polymer soaked in a salt. Additional examples include lithium tetrafluoroborate (LiBF₄) or lithium hexafluorophosphate (LiPF₆) plus polypyrrole). Some embodiments may use an ionic liquid, in which ions are in the liquid state at room temperature. Although not necessarily aqueous, such electrolytes are known to be extremely conductive due to the relatively free movement of their ions. The inventors believe that such an electrolyte 24 should cause the super-capacitor 26 to have a relatively high energy storage capacity

because, as known by those skilled in the art, the energy storage of a capacitor is a function of the square of the voltage.

As noted, the electrolyte 24 preferably is generally integrated with both the internal and external surfaces of one or more of the electrodes 22A-22C.

5 Among other things, the internal surfaces may be formed by tortuous internal channels and pores within the electrodes 22A-22C. The external surfaces simply may be those surfaces visible from the electrode exteriors. The electrolyte 24 and noted electrode surfaces thus are considered to form an electrode/electrolyte interface that stores energy.

10 Depending upon the electrode material, electrons can flow somewhat freely within the electrodes 22-22C. For example, electrons can flow within graphene of the super-capacitor electrode 22A. The electrolyte 24, however, acts as an insulator and thus, does not conduct the electrons from the super-capacitor electrode 22A. In a corresponding manner, the electrolyte 24 has ions that can
15 migrate somewhat freely up to the noted interface with the super-capacitor electrodes 22A. Like electrons in the super-capacitor electrode 22A, ions in the electrolyte 24 do not migrate through the interface.

Continuing with the super-capacitor electrode example, when subjected to an electric field, ions within the electrolyte 24 migrate to align with the electric
20 field. This causes electrons and holes in the super-capacitor electrode 22A to migrate in a corresponding manner, effectively storing charge. For example, in a prescribed electric field, positive ions in the electrolyte 24 may migrate toward a first super-capacitor electrode surface, and the negative ions in the electrolyte 24 may migrate toward a second super-capacitor electrode surface. In that case, the
25 positive ions near the first super-capacitor electrode surface attract electrons (in the electrode 22A) toward that interface, while the negative ions near the second super-capacitor electrode surface attract holes (in the electrode 22A) for that

interface. The distance of the ions to the interface plus the distance of the electrons to the same interface (on the opposite side of the interface) represent distance “d” of Equation 1 above.

As noted above, the battery electrode and the super-capacitor electrode
5 22B and 22A preferably are fixed at the same potential. Accordingly, as parallel-connected devices, the shared energy device 12 (i.e., the super-capacitor 26 and battery 28) effectively may meet both short-term power spike/surge needs and long-term power needs. Other embodiments, however, may include switching circuitry to selectively connect and disconnect the battery 28 and/or super-
10 capacitor 26 from an underlying circuit.

To those ends, Figure 3 schematically shows a diagram of the electrical connections of the battery 28 and super-capacitor 26 within the integrated circuit 10 of Figure 1 – a power circuit 37. More specifically, the power circuit 37 has circuit interfaces 32 that together receive power from the combined shared
15 energy device 12. Other circuits thus may connect to the two interfaces 32 for receiving the power. The power circuit 37 also has one or more switches 34, along with a switch controller 36, for selectively connecting the battery 28 and the super-capacitor 26 between four different states. Those four states include:

20 1) Parallel State: both the battery 28 and super-capacitor 26 are in the power circuit 37 – both switches 34 are closed,

2) Battery State: only the battery 28 is in the power circuit 37 – only the switch 34 for the battery 28 is closed,

3) Super-capacitor state: only the super-capacitor 26 is the power circuit
25 37 – only the switch 34 for the super-capacitor 26 is closed, and

4) Disconnected State: neither the battery 28 nor the super-capacitor 26 is in the power circuit 37 – both switches 34 are open.

The switch controller 36 may control the switches 34 for any of a wide variety of power management functions. Among other ways, the switch controller 36 can receive switch control input from other circuit components, or have preprogrammed instructions to make the appropriate switching connections in the power circuit 37. The switch controller 36 thus can be formed from a wide variety of conventional switching designs, such as those using passive or active circuitry.

As noted above, the stacked electrode configuration of Figure 2 is but one of a wide variety of potentially viable electrode configurations for the shared energy device 12. Figures 4A and 4B schematically show the electrode arrangements of two related but different embodiments having overlapping shapes. This overlapping is often referred to in the art as "interdigitating," in a manner similar to the interlacing one's fingers. More specifically, the battery and super-capacitor electrodes 22B and 22A in Figures 4A and 4B are formed in the noted overlapping configuration within same plane of the integrated circuit 10.

In the embodiment of Figure 4A, the battery electrode 22B is a single, unitary electrode. In a similar manner, the super-capacitor electrode 22A of Figure 4A also has a single, unitary electrode. This is in contrast to the embodiment of Figure 4B, in which the battery electrode 22B is formed by three separate and physically unconnected battery electrodes 22B (they may be electrically connected). In a corresponding manner, the super-capacitor electrode 22A of Figure 4B also is formed by three separate and physically unconnected super-capacitor electrodes 22A. Like the separate electrodes forming the battery electrode 22B, the electrodes of the super-capacitor electrode 22A may be electrically connected. For convenience, each of these electrodes 22A and 22B is referred to as a "finger." Figure 4C schematically shows a cross-section of the

electrodes 22A-22C across a plane that is substantially perpendicular to the plane of the substrate 14.

The embodiment of Figure 4B thus permits power management circuitry (not shown) to selectively connect the various fingers as needed. For example, during system startup, to quickly boost system voltage from zero to usable level for a given application, controlling circuitry may charge and connect only a few super-capacitor fingers to the system. As the voltage increases, controlling circuitry may gradually charge and introduce more super-capacitor fingers to the system. After the super-capacitor 26 fully charges and provides the initial power, the battery 28 may act as the primary power source. Moreover, if the battery and/or super-capacitor fingers has a defect or otherwise malfunctions, then controlling circuitry may remove that finger from the system. While this solution may reduce power delivery capacity, it still may provide enough power for the given application.

Figures 5A and 5B schematically show another electrode configuration in which the super-capacitor electrode 22A and the battery electrode 22B also are formed in the same plane of the integrated circuit 10. In this case, the super-capacitor electrode 22A circumscribes the battery electrode 22B, while the shared electrode 22C is formed in a different layer/plane of the integrated circuit 10.

Indeed, this embodiment alternatively can circumscribe the battery electrode 22B about the super-capacitor electrode 22A, or circumscribe one of the battery or super-capacitor electrodes 22B or 22A about the shared electrode 22C. In the latter case, the other electrode 22A or 22B is in another plane. It should be noted that discussion of the specific electrode configurations, such as those in Figures 2, 4A-4C and 5A-5B, are but a few of a wide variety of different electrode configurations that may prove effective. Accordingly, those skilled in the art can

apply principles of illustrative embodiments to form different electrode configurations that incorporate the spirit of those embodiments.

Figure 6 shows a process of fabricating the integrated circuit 10 in accordance with illustrative embodiments of the invention. In this example, the integrated circuit 10 has an electrode configuration like that of Figures 5A and 5B. It should be noted that this process is substantially simplified from a longer process that normally would be used to form the integrated circuit 10 and its shared energy device 12. Accordingly, the process of forming the integrated circuit 10 has many steps, such as adding the noted current collector layers 30, testing the individual dice, or additional passivation steps that those skilled in the art may use. In addition, some of the steps may be performed in a different order than that shown, or at the same time. Those skilled in the art therefore can modify the process as appropriate.

It also should be noted that the process of Figure 6 is a bulk process, which forms a plurality of integrated circuits 10 on the same wafer/base at the same time. Although typically less efficient, those skilled in the art can apply these principles to a process that forms only one integrated circuit 10.

The process begins at step 600, which deposits and patterns the battery electrode 22B on the insulated wafer/substrate 14. For simplicity, the wafer/substrate 14 is not shown in Figures 7A-7E. Among other ways, this step may use conventional sputtering or other well-known deposition techniques, as well as conventional patterning techniques, to deposit and pattern the battery electrode 22B. Figure 7A schematically shows relevant portions of the integrated circuit 10 at the conclusion of this step.

Next, the process coats the battery electrode 22B with a masking material 38, such as photoresist (step 602). Once the masking material 38 cures, step 602 also patterns the masking material 38 into the negative of the intended shape of

the super-capacitor electrode 22A. Figure 7B schematically shows relevant portions of the integrated circuit 10 at the conclusion of this step.

Step 604 then deposits the super-capacitor electrode material onto the masking material 38, and then removes the mask, leaving the two electrodes 22A and 22B in place on the substrate 14. Accordingly, in this embodiment, both electrodes 22A and 22B form anodes of their respective devices and are positioned on the same layer of the integrated circuit 10. Figure 7C schematically shows the relevant portions of the integrated circuit 10 at the conclusion of this step.

The process continues to step 606, which deposits the electrolyte 24 over both electrodes 22A and 22B. To that end, illustrative embodiments may pour or otherwise deposit a liquid electrolyte onto the exposed top surface, and then apply a vacuum infiltration process to the substrate 14, including to the electrodes 22A and 22B, which draws the liquid electrolyte 24 into the porous electrode material forming the electrodes 22A and 22B.

Illustrative vacuum infiltration processes preferably substantially uniformly distribute the electrolyte 24 within the porous material without damaging the morphology of the electrodes 22A and 22B. Since the electrolyte 24 is in liquid form, heating is not generally necessary at this stage. Some embodiments, however, may omit the vacuum infiltration processes. The step may conclude by permitting the electrolyte 24 to cure.

Rather than using a liquid electrolyte 24, some embodiments spin coat or otherwise deposit a solid/gel electrolyte to the substrate 14. Other embodiments may use other electrolytes. Figure 7D schematically shows the relevant portions of the integrated circuit 10 at the conclusion of this step.

At this point the process, the solid/gel electrolyte 24 is capable of supporting the shared electrode 22C. Accordingly, using conventional

techniques such as sputtering, step 608 deposits the shared electrode 22C onto the surface of the solid electrolyte 24. In this case, the shared electrode 22C acts as a cathode for both the super-capacitor 26 and the battery 28. This step also may pattern the shared electrode 22C if necessary. Figure 7E schematically shows the relevant portions of the integrated circuit 10 at the conclusion of this step.

After capping (e.g., using the cap 16) or otherwise encapsulating the integrated circuit 10 (e.g., using an in-situ cap), the process concludes at step 610, which separates/singulates the noted integrated circuit dice formed on the substrate 14. Indeed, those skilled in the art can use any of a wide variety of techniques for separating the dice, such as conventional saw or dicing processes along scribe streets or prescribed regions. Other embodiments can use a perforated wafer, or other techniques known in the art. Regardless of the technique, this final step of the process concludes with a plurality of die-level integrated circuit 10 having shared energy devices 12 ready for testing, further processing, or commercial use.

These resulting dice/integrated circuits 10 deliver a number of benefits. For example, as noted above, repeated power spikes can damage the battery 28 under normal operating conditions. Illustrative embodiments can mitigate that battery damage on a micro-chip level by having the super-capacitor 26 respond to spikes—effectively removing the battery 28 from the circuit for the short duration of the spike. The battery 28 thus likely will provide the majority of the power to the circuit in the steady state, while the capacitor primarily handles the power spikes.

Illustrative embodiments therefore can deliver both high energy density and high power functionality on a single, robust integrated circuit 10. By sharing the electrode 22C, such embodiments further can provide both functionalities

with a smaller footprint – using less die real estate. This should increase cost effectiveness and permit more devices to be formed on a single substrate 14. In addition, the shared electrode 22C reduces the necessary interconnections between the super-capacitor 26 and the battery 28, correspondingly reducing internal die resistances, favorably reducing internal die power consumption.

Illustrative embodiments therefore provide the combined functionality of the super-capacitor 26 and battery 28 on the micro-level semiconductor scale; namely on a monolithic integrated circuit 10. This new design consequently opens up a wide variety of new applications, enhancing circuit design flexibility and functionality.

Although the above discussion discloses various exemplary embodiments of the invention, it should be apparent that those skilled in the art can make various modifications that will achieve some of the advantages of the invention without departing from the true scope of the invention.

What is claimed is:

1. An integrated circuit comprising:
a substrate;

5 a super-capacitor supported by the substrate, the super-capacitor
comprising a super-capacitor electrode and a shared electrode; and
a battery supported by the substrate, the battery comprising a battery
electrode and the shared electrode,

10 the super-capacitor and battery forming at least a part of a monolithic
integrated circuit.

2. The integrated circuit as defined by claim 1 wherein the battery and
super-capacitor are electrically connected in parallel.

15 3. The integrated circuit as defined by claim 1 wherein the shared electrode
is formed at least in part from a material so that it has surface energy storage
capability and substantially no volumetric storage capability, the shared
electrode comprising a shared anode for both the super-capacitor and the
battery.

20

4. The integrated circuit as defined by claim 3 wherein the super-capacitor
electrode and shared electrode have about the same capacitance.

25 5. The integrated circuit as defined by claim 1 wherein the shared electrode
comprises a material having both surface energy storage capability and
volumetric energy storage capability, the super-capacitor forming an asymmetric

super-capacitor, the shared electrode forming a shared cathode for the super-capacitor and the battery.

6. The integrated circuit as defined by claim 1 further comprising at least one
5 of active circuitry and MEMS structure supported by the substrate and in electrical communication with the battery and the super-capacitor.

7. The integrated circuit as defined by claim 1 wherein the integrated circuit
10 comprises a plurality of layers, at least one of the layers including two of the electrodes.

8. The integrated circuit as defined by claim 1 further comprising switching
circuitry to switch between at least a) a first state using the battery only, and b) a
second state using the super-capacitor only, and c) a third state connecting the
15 super-capacitor and battery.

9. The integrated circuit as defined by claim 1 wherein the super-capacitor
electrode has a portion that is interdigitated with a portion of the battery
electrode.

10. The integrated circuit as defined by claim 1 wherein the super-capacitor
electrode comprises graphene and the battery electrode comprises graphite.

11. A micro-level energy storage device comprising:
25 a substrate;
a first electrode formed from a material having surface energy storage capability and substantially no volumetric energy storage capability;

a second electrode formed from a material having volumetric energy storage capability;

a third electrode formed from a material having one or both surface energy storage capability and volumetric energy storage capability;

5 electrolyte in communication with the first electrode, the second electrode, and the third electrode;

the first electrode configured to interact with the third electrode to form a first energy storage device,

10 the second electrode configured to interact with the third electrode to form a second energy storage device,

the substrate, first electrode, second electrode, and third electrode forming at least a part of a monolithic integrated circuit.

12. The micro-level energy storage device as defined by claim 11 wherein the
15 first energy storage device comprises a super-capacitor.

13. The micro-level energy storage device as defined by claim 11 wherein the second energy storage device comprises a battery.

20 14. The micro-level energy storage device as defined by claim 11 wherein the first energy storage device is electrically connected in parallel with the second energy storage device.

15. The micro-level energy storage device as defined by claim 11 wherein the
25 third electrode is configured to form an anode with both the first energy storage device and the second energy storage device.

16. A method of forming an integrated circuit having an energy storage device, the method comprising:

forming a first electrode on a substrate;

forming a second electrode on the substrate;

5 adding an electrolyte to the substrate, the electrolyte at least partly encapsulating the first and second electrodes;

forming a third electrode on the substrate, the third electrode being spaced from the first and second electrodes, the electrolyte being between the first electrode and the third electrode, the electrolyte being between the second
10 electrode and the third electrode;

separating the substrate into a plurality of individual monolithic integrated circuit dice, a plurality of the dice having the first electrode, the second electrode, and the third electrode,

the plurality of dice each being configured so that the first electrode
15 interacts with the third electrode to form first energy storage device, each of the plurality of dice also being configured so that the second electrode interacts with the third electrode to form a second energy storage device.

17. The method as defined by claim 16 wherein the first energy storage device
20 comprises a super-capacitor and the second energy storage device comprises a battery.

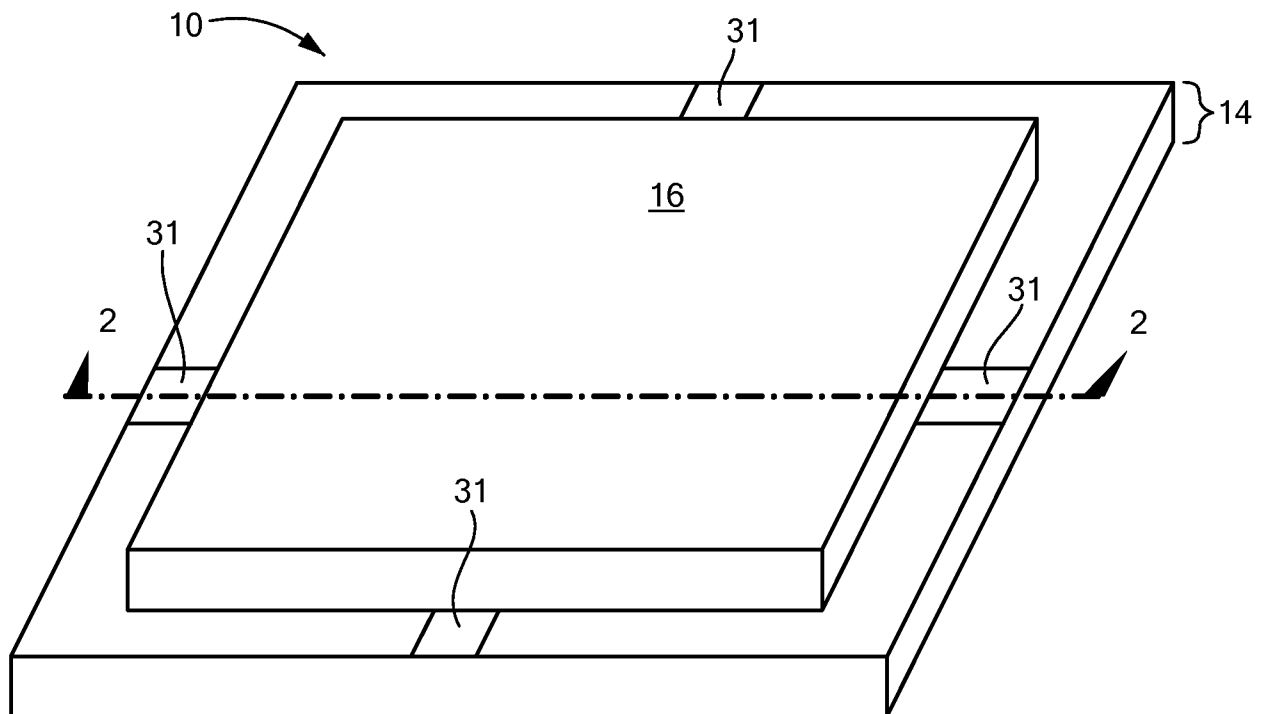
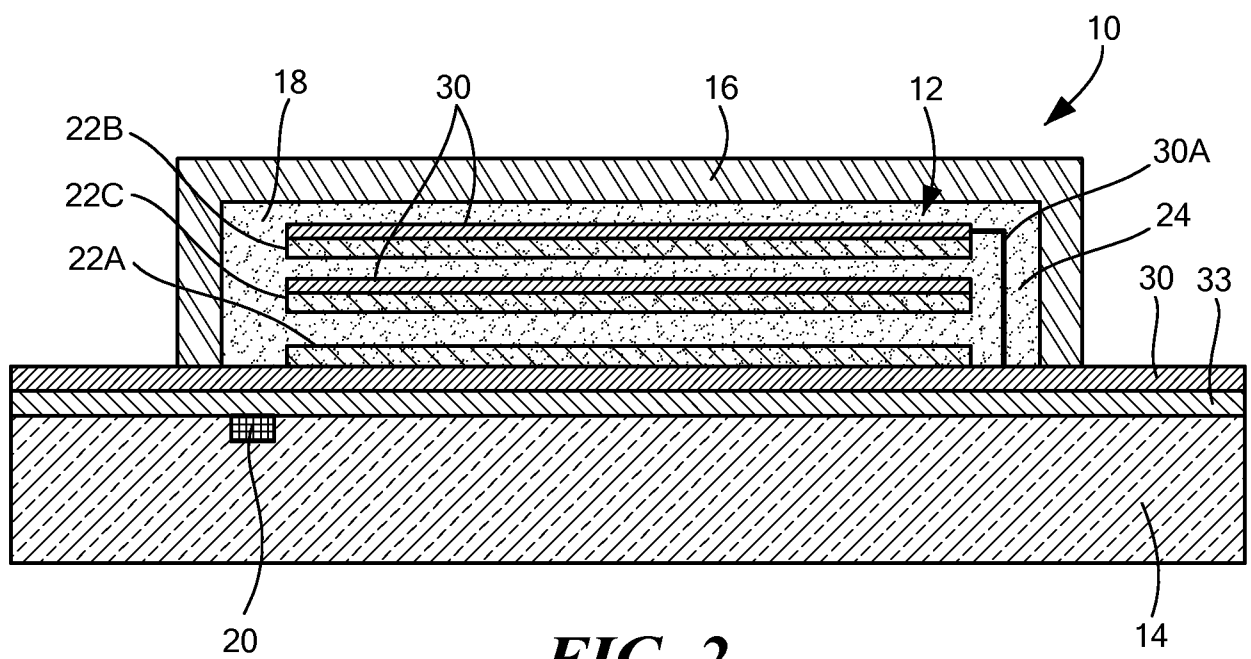
18. The method as defined by claim 17 wherein the super-capacitor is electrically connected in parallel with the battery.

25

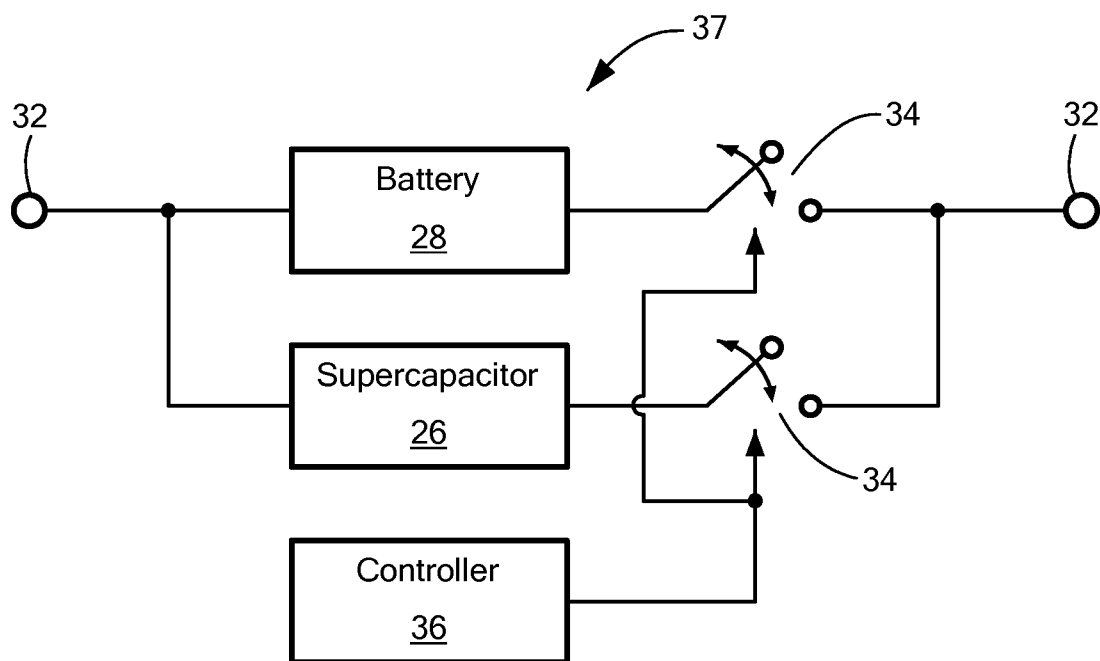
19. The method as defined by claim 16 wherein the electrolyte comprises a solid electrolyte material.

20. The method as defined by claim 16 wherein the third electrode comprises a material having one or both surface energy storage capability and volumetric energy storage capability.

1/6

**FIG. 1****FIG. 2**

2/6

**FIG. 3**

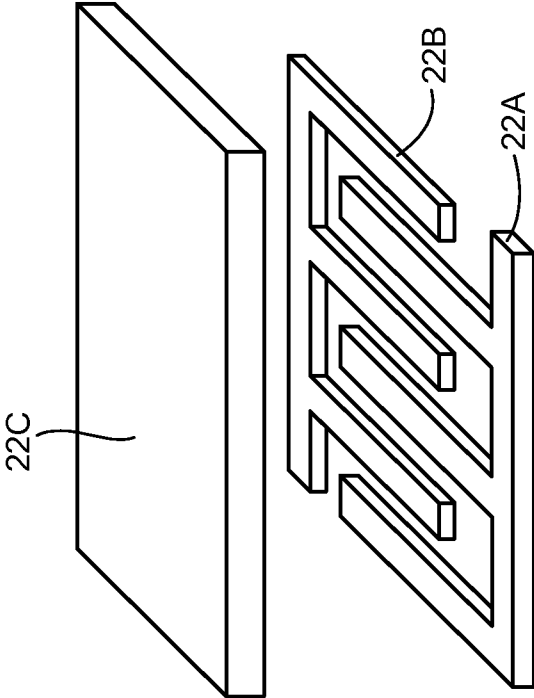
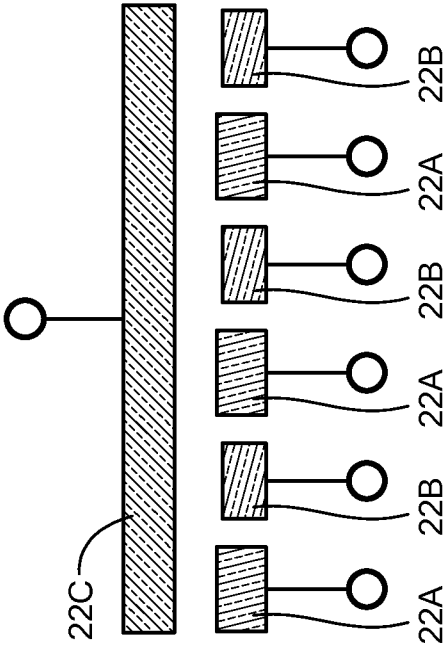
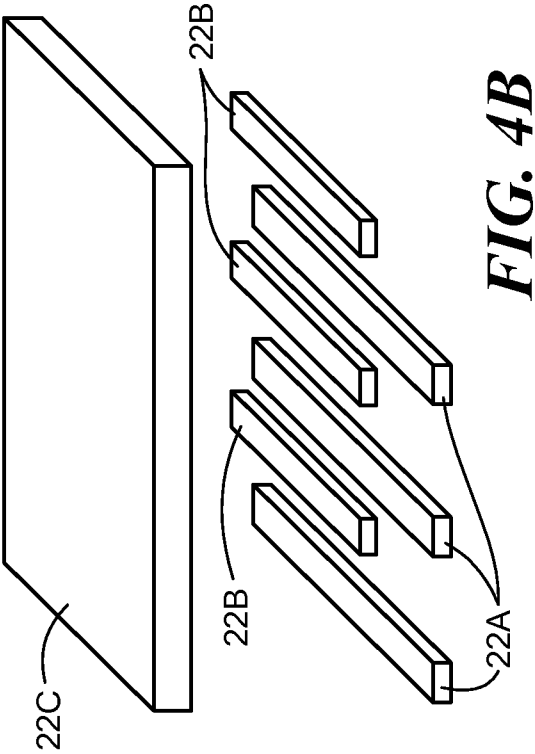
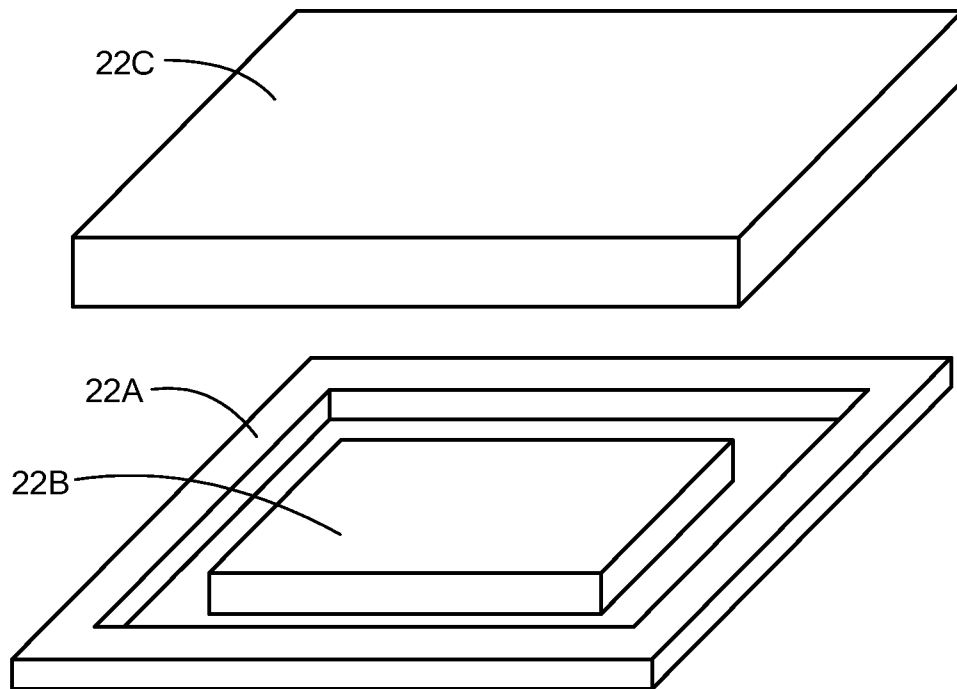
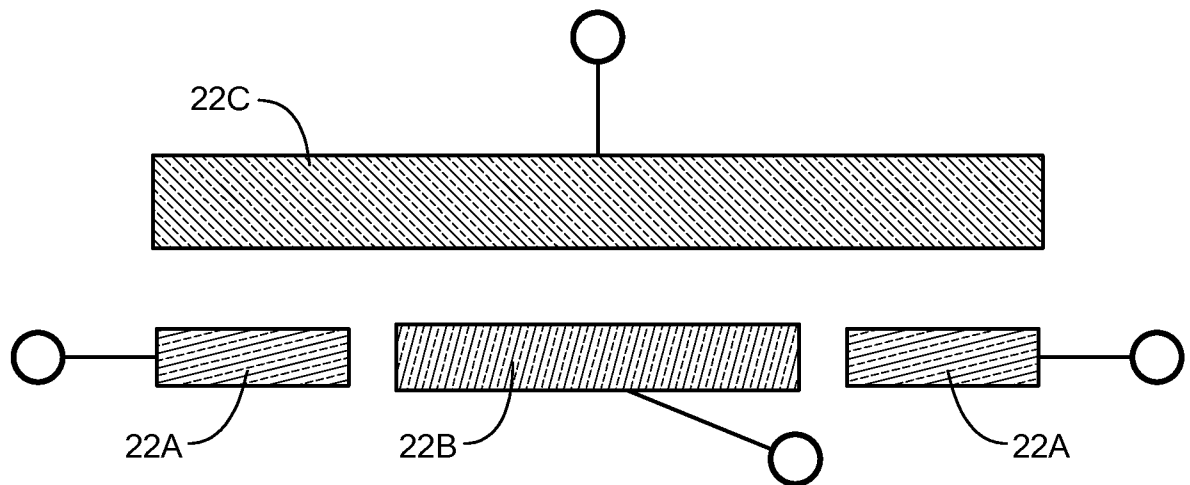


FIG. 4A

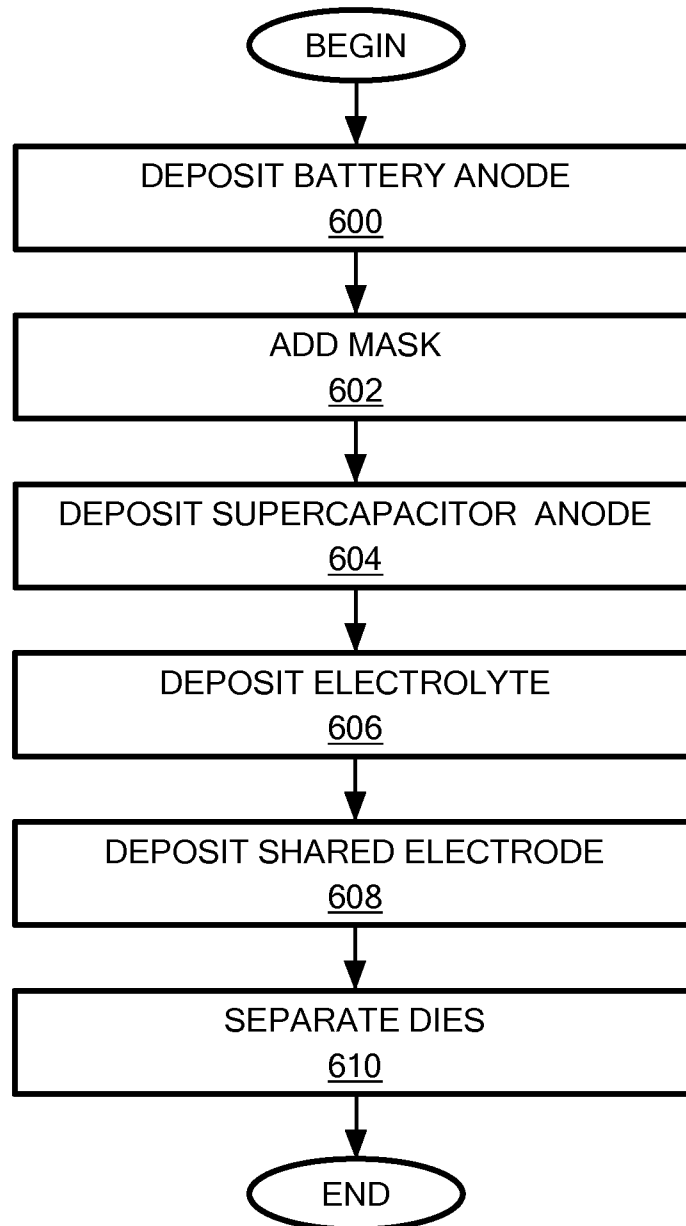
FIG. 4C

FIG. 4B

4/6

**FIG. 5A****FIG. 5B**

5/6

**FIG. 6**

6/6

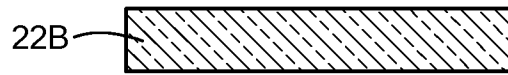


FIG. 7A

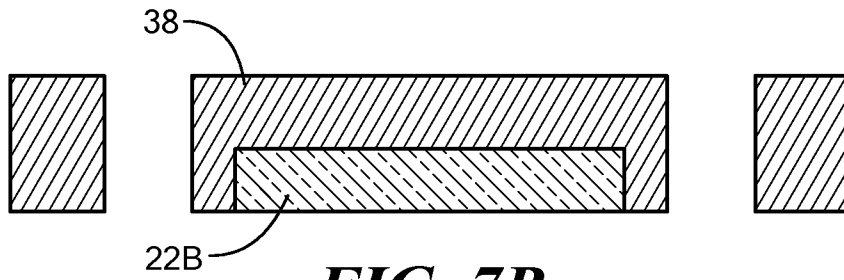


FIG. 7B

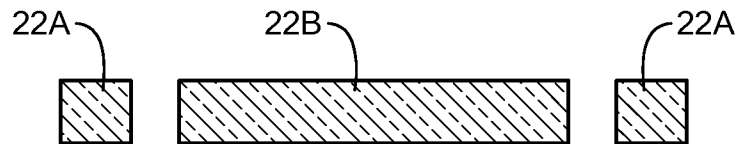


FIG. 7C

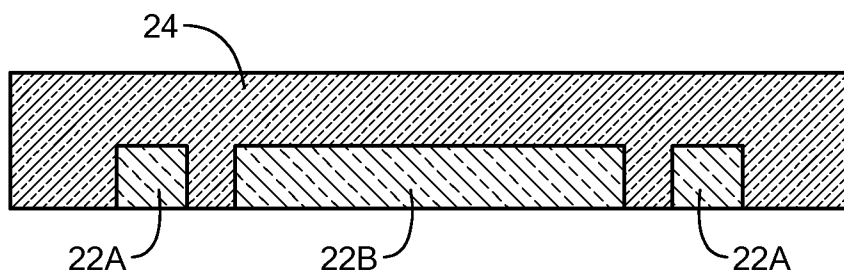


FIG. 7D

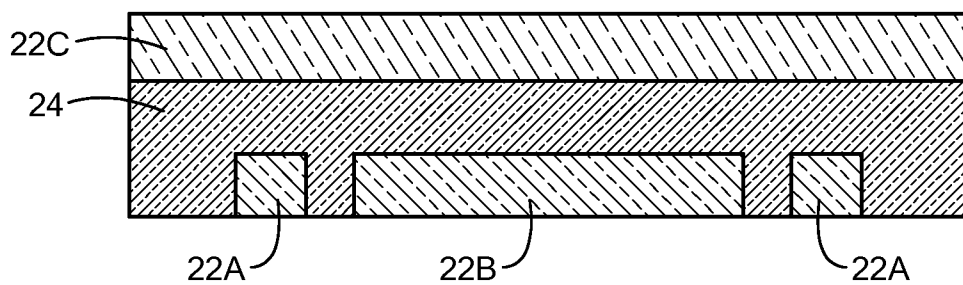


FIG. 7E

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2015/060530

A. CLASSIFICATION OF SUBJECT MATTER IPC (2016.01) H01G 11/00, H01G 11/04, H01G 9/00, H01M 16/00 According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) IPC (2016.01) H01M, H01G Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) Databases consulted: Esp@cenet, Google Patents, FamPat database, PatBase		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6117585 A MOTOROLA INC [US] 12 Sep 2000 (2000/09/12) Entire document	1-20
X	US 2003035982 A1 RYU KWANG-SUN et al [KR] 20 Feb 2003 (2003/02/20) Entire document	1-20
X	US 5439756 A MOTOROLA INC [US] 08 Aug 1995 (1995/08/08) Entire document	1-20
A	US 2004161640 A1 SALOT RAPHAEL [FR] 19 Aug 2004 (2004/08/19) Entire document	1-20
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 22 Feb 2016		Date of mailing of the international search report 25 Feb 2016
Name and mailing address of the ISA: Israel Patent Office Technology Park, Bldg.5, Malcha, Jerusalem, 9695101, Israel Facsimile No. 972-2-5651616		Authorized officer ORGAD Yaniv Telephone No. 972-2-5651787

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2015/060530

Patent document cited search report			Publication date	Patent family member(s)			Publication Date
US	6117585	A	12 Sep 2000	US	6117585	A	12 Sep 2000
US	2003035982	A1	20 Feb 2003	US	2003035982	A1	20 Feb 2003
				JP	2003100353	A	04 Apr 2003
				KR	20030014988	A	20 Feb 2003
US	5439756	A	08 Aug 1995	US	5439756	A	08 Aug 1995
				CA	2156638	A1	29 Aug 1995
				EP	0700583	A1	13 Mar 1996
				EP	0700583	A4	11 Sep 1996
				JP	H08510088	A	22 Oct 1996
				KR	0169015	B1	15 Jan 1999
				MX	9504546	A	31 Jan 1997
				WO	9523437	A1	31 Aug 1995
US	2004161640	A1	19 Aug 2004	US	2004161640	A1	19 Aug 2004
				AU	2002358840	A1	06 May 2003
				CN	1639816	A	13 Jul 2005
				EP	1543533	A2	22 Jun 2005
				FR	2831318	A1	25 Apr 2003
				FR	2831318	B1	09 Jun 2006
				JP	2005507544	A	17 Mar 2005
				WO	03036670	A2	01 May 2003
				WO	03036670	A3	28 Apr 2005