Abstract: Computer modules with small thicknesses and associated methods of manufacturing are disclosed. In one embodiment, the computer modules can include a module substrate having a module material and an aperture extending at least partially into the module material. The computer modules can also include a microelectronic package carried by the module substrate. The microelectronic package includes a semiconductor die carried by a package substrate. At least a portion of the semiconductor die extends into the module material via the aperture.
COMPUTER MODULES WITH PRINTED CIRCUIT BOARD HAVING AN APERTURE IN WHICH A SEMICONDUCTOR DIE IS INSERTED AND ASSOCIATED METHODS OF MANUFACTURING

TECHNICAL FIELD

[0001] The present disclosure is related to computer modules carrying microelectronic packages with a plurality of semiconductor dies and associated methods of manufacturing.

BACKGROUND

[0002] Today’s computer systems typically include a motherboard with a plurality of sockets spaced apart from one another for receiving memory modules, network interface cards, video cards, and/or other suitable computer modules. Such computer modules can include a printed circuit board that carries one or more microelectronic packages on a surface of the printed circuit board. The microelectronic packages typically include a substrate carrying one or more semiconductor dies encapsulated in a protective covering.

[0003] Stacking a plurality of dies in the microelectronic packages is a technique for increasing the processing power of the computer modules. However, stacking the dies also increases the thickness of the computer modules by increasing the extension of the microelectronic packages from the surface of the printed circuit board. As a result, the limited spacing between adjacent sockets may be insufficient for accommodating a large number of stacked dies in the microelectronic packages.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figure 1 is an exploded perspective view of a computer module in accordance with embodiments of the disclosure.

[0005] Figure 2 is a cross-sectional view of the computer module in Figure 1 as assembled in accordance with an embodiment of the disclosure.

[0006] Figure 3 is a cross-sectional view of the computer module in Figure 1 as assembled in accordance with another embodiment of the disclosure.
Figure 4 is a cross-sectional view of the computer module in Figure 1 as assembled in accordance with yet another embodiment of the disclosure.

Figure 5 is a cross-sectional view of the computer module in Figure 1 as assembled in accordance with a further embodiment of the disclosure.

5 DETAILED DESCRIPTION

Specific details of several embodiments of the disclosure are described below with reference to computer modules with small thicknesses and associated methods of manufacturing. The computer modules can carry at least one microelectronic package having a plurality of stacked dies. Typical microelectronic packages include microelectronic circuits or components, thin-film recording heads, data storage elements, microfluidic devices, and other components manufactured on microelectronic substrates. Micromachines and micromechanical devices are included within this definition because they are manufactured using technology similar to that used in the fabrication of integrated circuits. Microelectronic substrates can include semiconductor pieces (e.g., doped silicon wafers or gallium arsenide wafers), non-conductive pieces (e.g., various ceramic substrates), or conductive pieces. A person skilled in the relevant art will also understand that the disclosure may have additional embodiments, and that the disclosure may be practiced without several of the details of the embodiments described below with reference to Figures 1-5.

Figure 1 is an exploded perspective view of a computer module 100 in accordance with embodiments of the disclosure. As shown in Figure 1, the computer module 100 can include a module substrate 102 carrying a first microelectronic package 104a and a second microelectronic package 104b (collectively referred to as microelectronic packages 104). As shown in Figure 1, the module substrate 102 can include a substrate material 103 having an aperture 110, a plurality of bond sites 112 proximate to the aperture 110, a plurality of contact pads 114 for electrically coupling with a computer socket (not shown), and a plurality of optional supporting electronic components 116 (e.g., resistors, capacitors, diodes, etc.).

In certain embodiments, the substrate material 103 can include a printed circuit board that has a first surface 106a opposite a second surface 106b and a first edge 108a opposite a second edge 108b. The first and second edges 108a and 108b extend between the first and second surfaces 106a and 106b. In the illustrated embodiment, the substrate material 103 includes a sheet-like structure with a generally rectangular shape. In other embodiments, the...
substrate material 103 can include other types of structure with other desired shapes. Even though the substrate material 103 is shown in Figure 1 as a single layer of material, in certain embodiments, the substrate material 103 can also include a plurality of conductive and/or non-conductive layers laminated and/or otherwise combined with one another.

[0012] The aperture 110 can be shaped and sized to accommodate at least a portion of the microelectronic packages 104. In the illustrated embodiment, the aperture 110 has a generally rectangular cross-section and extends between the first and second surfaces 106a and 106b of the substrate material 103 at a depth D. As a result, the depth D of the aperture 110 generally equals to the thickness of the module substrate 102. In other embodiments, the aperture 110 can have a stepped cross-section, a curved cross-section, a partially curved cross-section, and/or other suitable cross-sectional geometries corresponding to the geometry of the microelectronic packages 104. In yet further embodiments, the aperture 110 may extend only partially between the first and second surfaces 106a and 106b with a depth that is less than D. The aperture 110 may be formed by cutting, punching, etching, and/or other suitable techniques for removing a portion of the substrate material 103.

[0013] The microelectronic packages 104 can include a package substrate 118 carrying one or more semiconductor dies 130 (not shown in Figure 1) encapsulated in an encapsulant 120. As shown in Figure 1, the package substrate 118 can include a first surface 119a generally facing the module substrate 102 and a second surface 119b opposite the first surface 119a. The first surface 119a includes a peripheral portion 118b that extends laterally from a central portion 118a. The central portion 118a can generally correspond to the semiconductor dies 130 encapsulated in the encapsulant 120. The encapsulant 120 with the encapsulated semiconductor dies 130 can extend from the first surface 119a for a height d. The peripheral portion 118b can carry a plurality of contact pads 122 in electrical communication with the semiconductor dies 130. In the illustrated embodiment, the microelectronic packages 104 are generally similar in structure and in function. In other embodiments, the microelectronic packages 104 can have different structure and/or function. In further embodiments, one of the microelectronic packages 104 may be omitted, as described in more detail below with reference to Figures 4 and 5.

[0014] In certain embodiments, the depth D of the aperture 110 can be larger than twice the height d of the encapsulant 120 with the encapsulated semiconductor dies 130 as follows:

\[
D \geq 2d
\]
As a result, the encapsulated semiconductor dies 130 of both the microelectronic packages 104 can be completely inside the aperture 110 of the substrate module 102. In other embodiments, the depth \( D \) of the aperture 110 can be larger than the height \( d \) of the encapsulant 120 with the encapsulated semiconductor dies 130 but less than twice the height \( d \) as follows:

\[
2d > D \geq d
\]

As a result, in certain embodiments, the encapsulated semiconductor dies 130 of both the microelectronic packages 104 can be partially inside the aperture 110. In other embodiments, the encapsulated semiconductor dies 130 of one microelectronic package 104 may be substantially inside the aperture 110, and those of the other microelectronic package 104 may be only partially inside the aperture 110. In further embodiments, the depth \( D \) of the aperture 110 can be less than the height \( d \) of the encapsulant 120 with the encapsulated semiconductor dies 130 as follows:

\[
D < d
\]

As a result, the encapsulated semiconductor dies 130 of the microelectronic packages 104 may be partially inside the aperture 110.

[0015] During assembly, a plurality of electric couplers 124 (e.g., solder bumps, gold bumps, etc., not shown in Figure 1) can be disposed onto the individual bond sites 112 and/or the contact pads 122. The microelectronic packages 104 can then be positioned relative to the module substrate 102 by (1) at least partially inserting the encapsulated semiconductor dies 130 into the aperture 110; and (2) aligning the individual contact pads 122 with the corresponding bond sites 112 on the module substrate 102. Subsequently, the electric couplers 124 may be reflowed and/or otherwise processed to electrically couple the bond sites 112 of the module substrate 102 with the corresponding contact pads 122.

[0016] Several embodiments of the computer module 100 can have a reduced thickness when compared to conventional computer modules. By at least partially inserting the microelectronic packages 104 into the aperture 110 of the module substrate 102, the microelectronic packages 104 can have a reduced height from the first and/or second surfaces 106a and 106b of the module substrate 102. Accordingly, the microelectronic packages 104 may incorporate a larger number of stacked semiconductor dies 130 with a reduced impact on the thickness of the computer module 100 when compared to conventional computer modules.
[0017] Even though the computer module 100 is shown in Figure 1 as having one aperture 110, in other embodiments, the computer module 100 can have two, three, four, or any other desired number of apertures 110 to accommodate corresponding microelectronic packages 104. In certain embodiments, some of the apertures 110 may have different shape, size, and/or other characteristics than the other apertures 110. In other embodiments, all of the apertures 110 may be generally identical to one another. In further embodiments, the microelectronic packages 104 may be electrically coupled to the module substrate 102 using wirebonds, leadframes, and/or other suitable techniques.

[0018] Figures 2-5 are cross-sectional views of the computer module 100 in Figure 1 as assembled in accordance with several embodiments of the disclosure. As shown in Figure 2, the computer module 100 includes the microelectronic packages 104 coupled to a first side 102a and a second side 102b of the substrate module 102 with a plurality of electric couplers 124. The electric couplers 124 can include solder balls, solder bumps, gold bumps, and/or other suitable conductive couplers. The microelectronic packages 104 can include a plurality of semiconductor dies 130 attached to the package substrate 118 and to one another with an adhesive layer 132 in a stacked arrangement. A plurality of wirebonds 134 electrically couple bond sites 136 of the individual semiconductor dies 130 to corresponding terminals 137 on the package substrate 118. The semiconductor dies 130 can include DRAM, VRAM, FPRAM, and/or other suitable types of semiconductor dies. Even though four semiconductor dies 130 are shown for illustration purposes, the microelectronic packages 104 may include one, two, three, five, or any other desired number of semiconductor dies 130. In other embodiments, the plurality of semiconductor dies 130 may be coupled to the package substrate 118 and/or to one another in a flip-chip arrangement and/or other suitable arrangements.

[0019] In certain embodiments, the microelectronic packages 104 individually include a processor die 138 encapsulated in the encapsulant 120. In the illustrated embodiment, the processor die 138 is electrically coupled to one of the semiconductor dies 130 with a plurality of conductive couplers 142 (e.g., solder balls). In other embodiments, the processor die 138 may be coupled to the second surface 119b of the package substrate 118 as shown in Figure 3. In further embodiments, the processor die 138 may be omitted.

[0020] In the embodiment shown in Figure 2, the depth D of the aperture 110 is greater than twice the distance d of the encapsulant 120 and the encapsulated semiconductor dies 130. The semiconductor dies 130, the processor dies 138, and the encapsulant 120 of the
microelectronic packages 104 are substantially disposed inside the aperture 110 in a face-to-face configuration. Even though a gap 146 is shown in Figures 2 and 3 between the microelectronic packages 104, in certain embodiments, top surfaces 105 of the microelectronic packages 104 may abut each other.

[0021] In another embodiment, as shown in Figure 4, the computer module 100 may include only one microelectronic package 404 that substantially occupies the entire space in the aperture 110. The microelectronic package 404 can be generally similar to the microelectronic packages 104 of Figure 2 except that the microelectronic package 404 can include more semiconductor dies 130 than the microelectronic packages 104 of Figure 2. In the illustrated embodiment, the top surface 105 of the microelectronic package 404 is generally flush with the second side 102b of the substrate module 102. In other embodiments, the top surface 105 of the microelectronic package 404 can be recessed from the second side 102b of the module substrate 102. In further embodiments, the top surface 105 can extend beyond the second side 102b of the substrate module 102. Even though the microelectronic package 404 is shown to include eight semiconductor dies 130, in other embodiments, the microelectronic package 404 can include any desired number of semiconductor dies 130. In further embodiments, the microelectronic package 404 can include the processor die 138 electrically coupled to the second surface 119b of the package substrate 118 generally similar to that shown in Figure 3.

[0022] In further embodiments, as shown in Figure 5, the computer module 100 can include a microelectronic package 504 electrically coupled to a module substrate 502. The module substrate 502 can be generally similar in structure and in function as the module substrate 102 shown in Figures 1-4. However, the module substrate 504 can include a recess 103 at the first side 102a and the bond sites 112 disposed in the recess 103. In the illustrated embodiment, the recess 103 is sized and shaped to receive the package substrate 118 such that the second surface 119b of the package substrate 118 is generally flush with the first side 102a of the module substrate 504. In other embodiments, the recess 103 may be sized and shaped such that the package substrate 118 is recessed from or extending beyond the first side 102a.

[0023] As shown in Figure 5, the microelectronic package 504 can include a plurality of semiconductor dies 130 encapsulated in an encapsulant 520 having an opening 521. The microelectronic package 504 can also include a plurality of electronic components 516 electrically coupled to the semiconductor die 130 through the opening 521 with conductive couplers 517 (e.g., solder balls). The electronic components 516 can include resistors,
capacitors, and/or other suitable electronic components configured for signal/power filtering, power rectifying, and/or other signal or power processing functions. Without being bound by theory, it is believed that the short distance between the semiconductor dies 130 and the electronic components 516 can improve the quality of signal and/or power processing by at least partially reducing transmission interference.

Even though the module substrate 502 is shown to have the recess 103 on the first side 102a, in other embodiments, the module substrate 502 may include the recess 103 on the second side 102b. In further embodiments, the module substrate 502 may include the recess 103 on the first side 102a and another recess (not shown) on the second side 102b. In yet further embodiments, the recess 103 may be omitted.

From the foregoing, it will be appreciated that specific embodiments of the disclosure have been described herein for purposes of illustration, but that various modifications may be made without deviating from the disclosure. In addition, many of the elements of one embodiment may be combined with other embodiments in addition to or in lieu of the elements of the other embodiments. Accordingly, the disclosure is not limited except as by the appended claims.
CLAIMS

I/We claim:

1. A computer module, comprising:
   a printed circuit board having a first surface, a second surface opposite the first surface, and an aperture extending between the first and second surfaces, the printed circuit board including a plurality of bond sites proximate to the aperture; and a microelectronic package having a semiconductor die and a package substrate carrying the semiconductor die, the package substrate having a plurality of contact pads individually aligned with the bond sites of the printed circuit board, wherein at least a portion of the semiconductor die is inside the aperture of the printed circuit board.

2. The computer module of claim 1 wherein
   the bond sites are a first plurality of bond sites on the first surface;
   the printed circuit board further includes a second plurality of bond sites on the second surface;
   the microelectronic package is a first microelectronic package having a first plurality semiconductor dies encapsulated in a first encapsulant and carried by a first package substrate, the plurality of contact pads being a first plurality of contact pads;
   the computer module also includes a second microelectronic package proximate to the second surface of the printed circuit board, the second microelectronic package having a second plurality of semiconductor dies encapsulated in a second encapsulant, a second package substrate carrying the second semiconductor dies, and a second plurality of contact pads;
   the first contact pads are individually generally aligned with the first plurality of bond sites on the printed circuit board and the second contact pads are individually generally aligned with the second plurality of bond sites on the printed circuit board; and
   the first and second plurality of semiconductor dies and the first and second encapsulants are substantially completely inside the aperture of the printed circuit board.
3. The computer module of claim 1 wherein
the bond sites are a first plurality of bond sites on the first surface;
the printed circuit board further includes a second plurality of bond sites on the second surface;
the microelectronic package is a first microelectronic package having a first plurality of semiconductor dies encapsulated in a first encapsulant and carried by a first package substrate, the plurality of contact pads being a first plurality of contact pads;
the computer module also includes a second microelectronic package proximate to the second surface of the printed circuit board, the second microelectronic package having a second plurality of semiconductor dies encapsulated in a second encapsulant, a second package substrate carrying the second semiconductor dies, and a second plurality of contact pads;
the first contact pads are individually generally aligned with the first plurality of bond sites on the printed circuit board and the second contact pads are individually generally aligned with the second plurality of bond sites on the printed circuit board; and
the first and second plurality of semiconductor dies and the first and second encapsulants are substantially completely inside the aperture of the printed circuit board with the first and second encapsulants abutting each other.

4. The computer module of claim 1 wherein the microelectronic package includes an encapsulant encapsulating the semiconductor die, and wherein the aperture has a cross-sectional dimension larger than that of the encapsulated semiconductor die.

5. The computer module of claim 1 wherein the microelectronic package includes an encapsulant encapsulating the semiconductor die, and wherein the aperture has a cross-sectional dimension larger than that of the encapsulated semiconductor die but smaller than that of the package substrate.

6. The computer module of claim 1 wherein the microelectronic package includes an encapsulant encapsulating the semiconductor die, the encapsulated semiconductor die having a surface facing away from the package substrate, and wherein the package substrate is attached
to the first surface of the printed circuit board, and further wherein the surface of the
encapsulated semiconductor die is generally flush with the second surface of the printed circuit
board.

7. The computer module of claim 1 wherein the microelectronic package includes
an encapsulant encapsulating the semiconductor die, the encapsulated semiconductor die having
a surface facing away from the package substrate, and wherein the package substrate is attached
to the first surface of the printed circuit board, and further wherein the surface of the
encapsulated semiconductor die is recessed from the second surface of the printed circuit board.

8. The computer module of claim 1 wherein the microelectronic package includes
an encapsulant encapsulating the semiconductor die, the encapsulated semiconductor die having
a surface facing away from the package substrate, and wherein the package substrate is attached
to the first surface of the printed circuit board, and further wherein the surface of the
encapsulated semiconductor die is extending beyond the second surface of the printed circuit board.

9. The computer module of claim 1 wherein the microelectronic package further
includes a processor die and an encapsulant encapsulating the semiconductor die and the
processor die, the encapsulated semiconductor die having a surface facing away from the
package substrate, and wherein the package substrate is attached to the first surface of the
printed circuit board, and further wherein the surface of the encapsulated semiconductor die is
generally flush with the second surface of the printed circuit board.

10. The computer module of claim 1 wherein the microelectronic package includes
an encapsulant encapsulating the semiconductor die, the encapsulant having an opening facing
away from the package substrate, and wherein the microelectronic package further includes a
plurality of electronic components electrically coupled to the semiconductor die via the opening.

11. The computer module of claim 1 wherein the module substrate includes a recess
proximate to the aperture, and wherein the bond sites of the printed circuit board are located in
the recess.
12. A computer module, comprising:
   a module substrate having a module material and an aperture extending at least partially into the module material; and
   a microelectronic package carried by the module substrate, the microelectronic package having a semiconductor die carried by a package substrate, wherein at least a portion of the semiconductor die extends into the substrate material via the aperture.

13. The computer module of claim 12 wherein the module substrate includes a plurality of bond sites on a surface of the module substrate and adjacent to the aperture, and wherein the microelectronic package includes a plurality of contact pads generally aligned with the individual bond sites.

14. The computer module of claim 12 wherein the module substrate includes a plurality of bond sites on a surface of the module substrate and adjacent to the aperture, and wherein the microelectronic package includes a plurality of contact pads generally aligned with the individual bond sites, and further wherein the computer module includes a plurality of electric couplers between individual bond sites and corresponding contact pads while the semiconductor die extends into the substrate material via the aperture.

15. The computer module of claim 12 wherein the aperture has a depth generally equal to a thickness of the module substrate.

16. The computer module of claim 12 wherein the aperture has a depth less than a thickness of the module substrate.

17. The computer module of claim 12 wherein the aperture has a depth generally equal to a thickness of the module substrate, and wherein the semiconductor die extends from the package substrate for a distance less than the depth of the aperture.

18. The computer module of claim 12 wherein the aperture has a depth generally equal to a thickness of the module substrate, and wherein the semiconductor die extends from the package substrate for a distance less than half of the depth of the aperture.
19. The computer module of claim 12 wherein the aperture has a depth generally equal to a thickness of the module substrate, and wherein the semiconductor die extends from the package substrate for a distance generally equal to the depth of the aperture.

20. The computer module of claim 12 wherein the aperture has a depth generally equal to a thickness of the module substrate, and wherein the semiconductor die extends from the package substrate for a distance longer than the depth of the aperture.

21. A method for assembling a computer module, comprising:
positioning a microelectronic package proximate to a module substrate having a module material and an aperture extending at least partially into the module material, the microelectronic package having a semiconductor die carried by a package substrate;
generally aligning the semiconductor die of the microelectronic package with the aperture of the module substrate; and
extending at least a portion of the semiconductor die into the substrate material via the aperture.

22. The method of claim 21 wherein the module substrate includes a bond site on a surface of the module substrate and adjacent to the aperture, and wherein the microelectronic package includes a contact pad electrically coupled to the semiconductor die, and further wherein the method includes generally aligning the contact pad with the bond site.

23. The method of claim 21 wherein the module substrate includes a bond site on a surface of the module substrate and adjacent to the aperture, and wherein the microelectronic package includes a contact pad electrically coupled to the semiconductor die, and further wherein the method includes:
generally aligning the contact pad with the bond site;
disposing an electric coupler between the contact pad and the bond site; and
electrically coupling the contact pad and the bond site with the electric coupler.
24. A printed circuit board for carrying a microelectronic package, comprising:
   a substrate having a first surface, a second surface opposite the first surface, a first side
   and a second side opposite the first side, both the first and second sides extending
   between the first and second surfaces;
   an aperture located between the first and second sides of the substrate and extending
   between the first and second surfaces, wherein the aperture is configured to
   receive at least a portion of the microelectronic package;
   a plurality of bond sites proximate to the aperture; and
   a plurality of contact pads proximate to the first side, the contact pads being configured
   to interface with a socket of a motherboard.

25. The printed circuit board of claim 24 wherein the aperture extends completely
    between the first and second surfaces.

26. The printed circuit board of claim 24 wherein the aperture extends completely
    between the first and second surfaces, the aperture having a generally rectangular uniform cross-
    section between the first and second surfaces.

27. The printed circuit board of claim 24 wherein the aperture extends partially
    between the first and second surfaces.
**A. CLASSIFICATION OF SUBJECT MATTER**

INV. H01L25/10      H05K1/14      H05K1/18      H01L25/065

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

HOIL        H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

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Date of the actual completion of the international search

12 March 2010

Date of mailing of the international search report

26/03/2010

Name and mailing address of the ISA/

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Fax (+31-70) 340-3016

Authorized officer

Le Gallo, Thomas
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