

Nov. 29, 1966

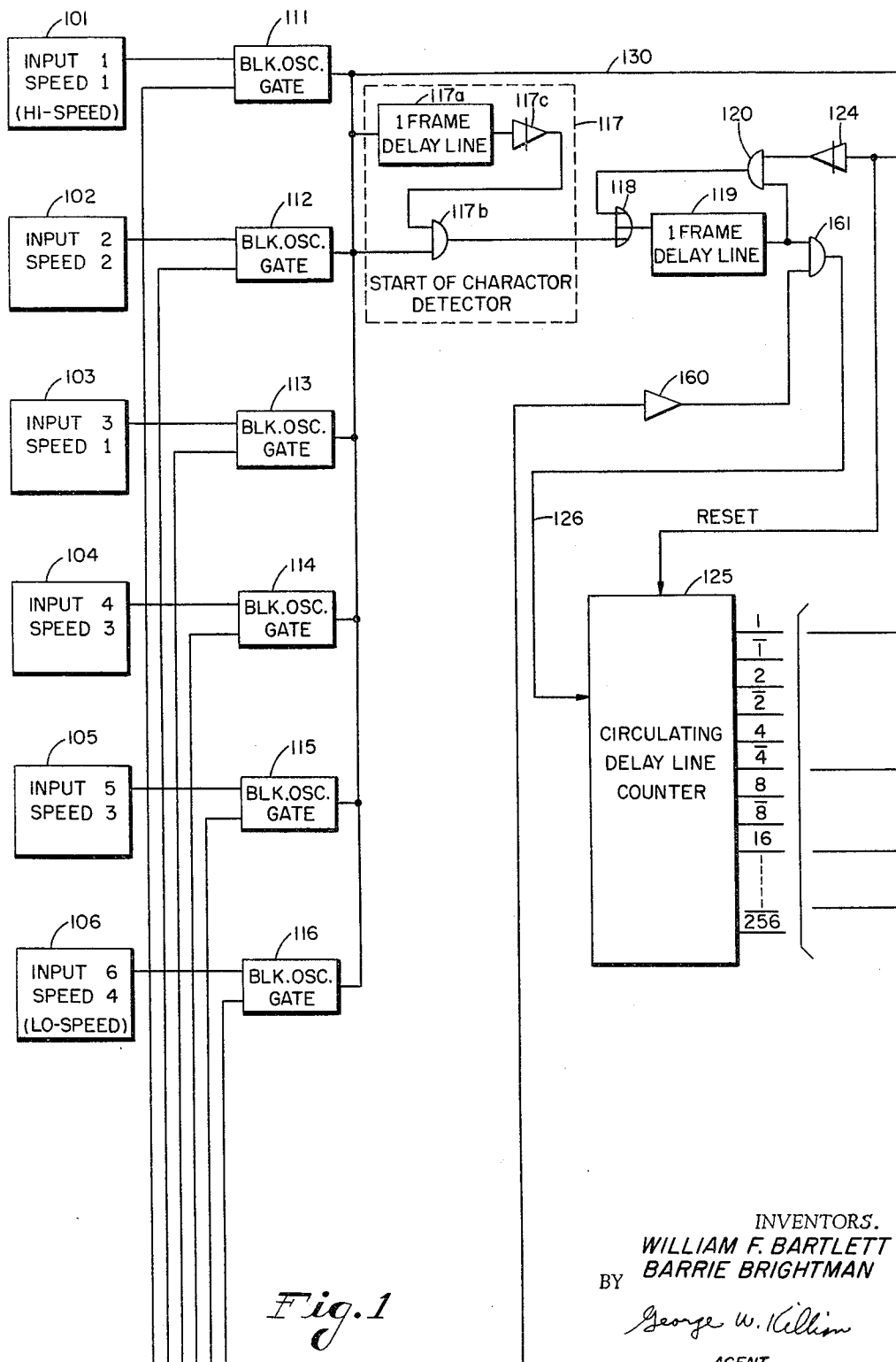
W. F. BARTLETT ETAL

3,288,928

SAMPLING DETECTOR

Filed Aug. 21, 1963

4 Sheets-Sheet 1



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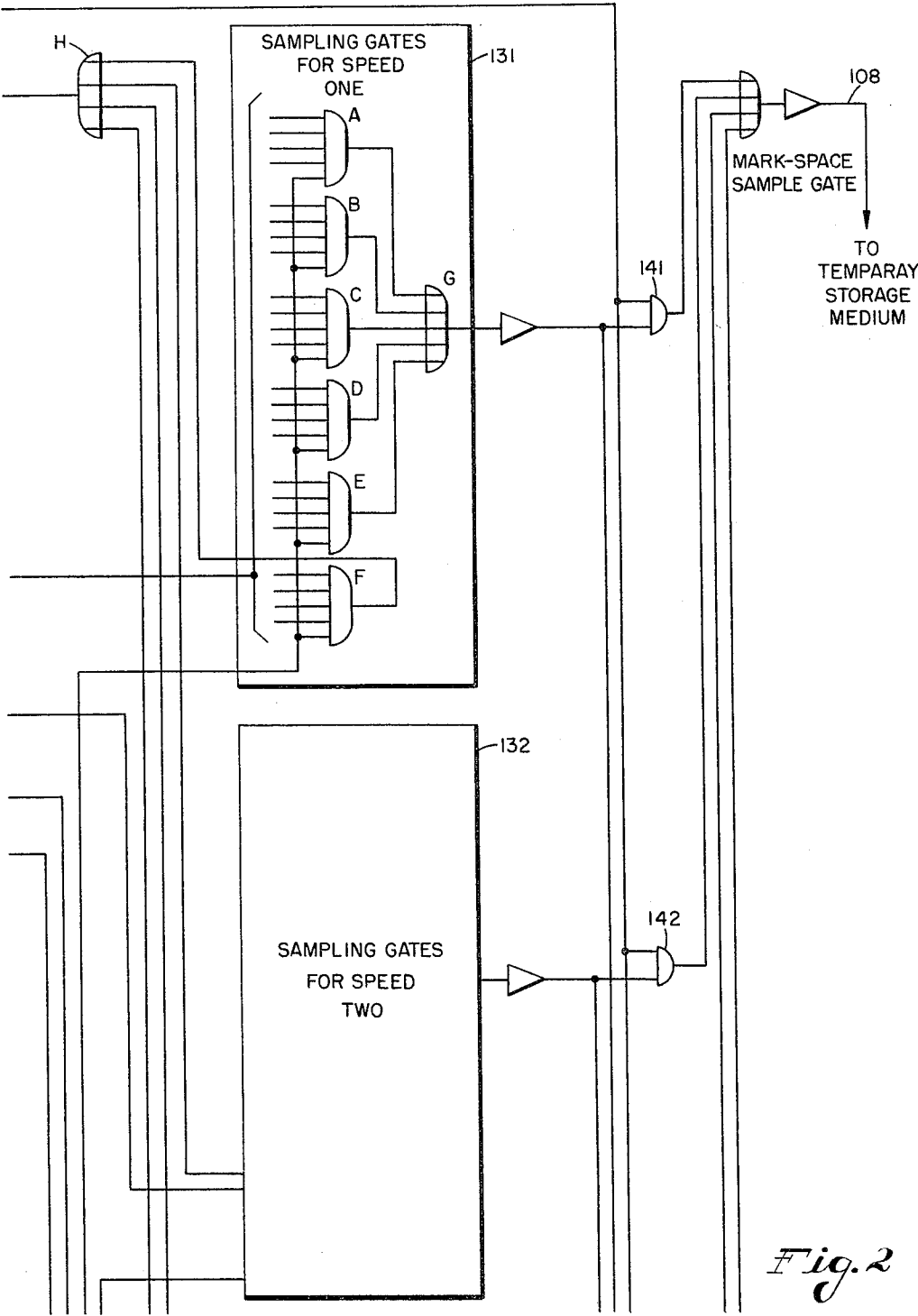
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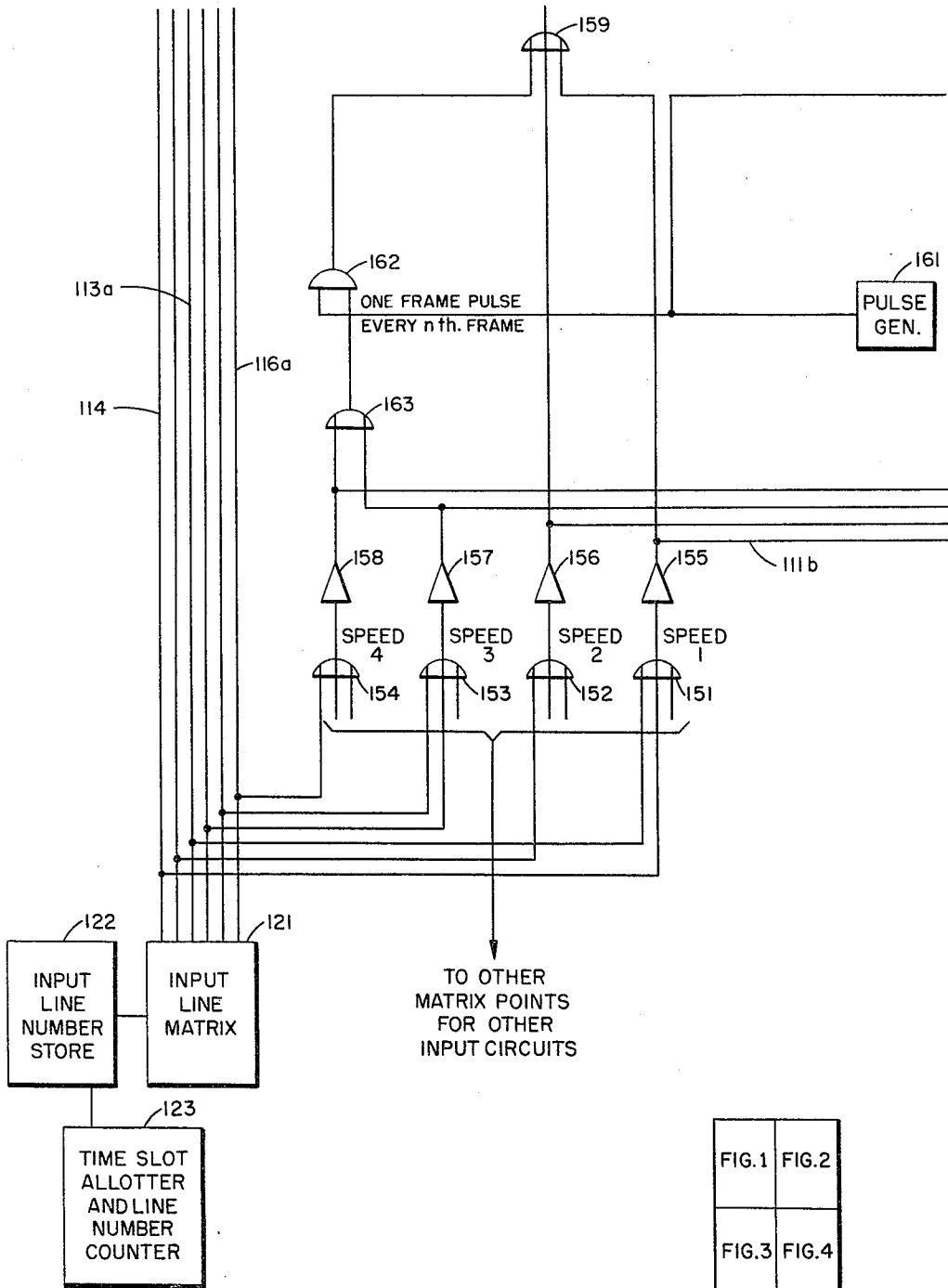


Fig. 3

Fig. 5

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SAMPLING DETECTOR

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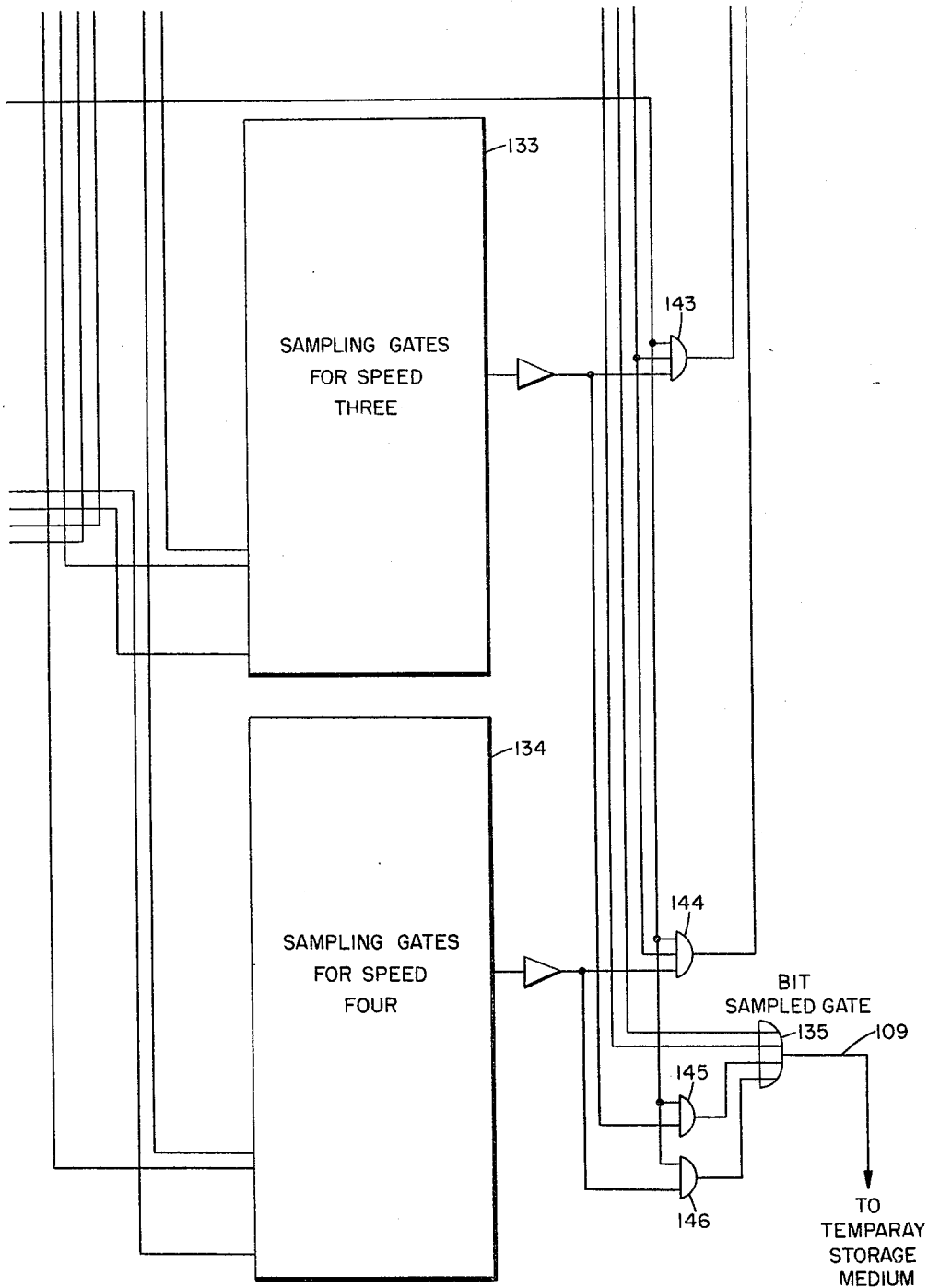


Fig. 4

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3,288,928

SAMPLING DETECTOR

William F. Bartlett, Rochester, and Barrie Brightman, Webster, N.Y., assignors to General Dynamics Corporation, Rochester, N.Y., a corporation of Delaware
Filed Aug. 21, 1963, Ser. No. 303,519
12 Claims. (Cl. 178-50)

This invention relates in general to data processing equipment and, more particularly, to a common control means for accepting input signals from a plurality of sources operating at a plurality of speeds with a plurality of code formats.

The invention herein disclosed may find utility in a wide variety of devices; however, it is particularly adapted for use in teletype systems which are required to receive messages from a plurality of sources which may be working at different speeds and with different code formats. In such systems, it is frequently necessary to temporarily store a message and subsequently forward the message to one or more locations and/or to retransmit them at a different speed and/or with a different code format. It is known in prior art systems to receive a plurality of messages from a plurality of sources at various speeds and with various code formats. However, in such systems, it is customary to provide individual detectors and temporary storage means for each message source.

It is the general object of this invention to provide a new and improved means for receiving signals from a plurality of sources operating at different speeds and for directing the signals to a common temporary storage medium.

It is a more particular object of this invention to provide a new and improved means for sampling signals received from a plurality of signal sources operating at a plurality of speeds.

It is another object of this invention to provide a common means for sampling signals received from a plurality of signal sources and operating at a plurality of speeds.

It is another object of this invention to provide a common means for sampling signals received from a plurality of signal sources operating at a plurality of speeds and for gating selected ones of said samples to a succeeding circuit.

In accordance with the illustrated embodiment of the present invention, it is assumed that each of the plurality of signal sources will operate at a known bit-per-second rate. That is, a given source is designed to function and operate at a predetermined speed, but the speed of a particular source may be substantially different from that of another source. Of course, two or more of the plurality of sources may be operating at the same bit-per-second rate. However, if desired, the operating speed of a given unit may be altered; but, if the speed is altered it will be necessary to change certain connections. That is, for a given set of connections a given source may be operated at one speed only. The normal range of source speeds is from approximately 40 or 50 bits-per-second to about 2500 bits-per-second. The system of the present invention employs time division multiplex techniques similar to those used in modern telephone systems such as that disclosed in the copending patent application of Barrie Brightman, Serial No. 45,342, filed on July 26, 1960. Such systems employ a repetitive time frame having a fixed number of time slots per frame. For convenience, it will be assumed that the system of the present invention employs a 60-microsecond time frame and that there are twelve time slots of 5 microseconds each per time frame. A blocking oscillator gate is associated with each of the sources to gate signals from the associated source to a common signaling chan-

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nel in a time slot assigned to the associated source. In response to a start-of-message signal from a given source, an idle time slot is assigned to that source and thereafter the associated blocking oscillator gate admits signals indicative of the instantaneous signal from that source to the common signaling channel for one time slot each time frame. Since the identity of the source is known, the bit-per-second transmission rate is known and marking is provided indicative of the bit rate in the assigned time slot.

In conventional code systems, each character is indicated by a plurality of bits and the start of the group of bits indicative of an individual character is indicated by a predetermined start-of-character signal. Accordingly, when a start-of-character signal is transmitted from a known source, the speed of the source, the code format, the number of frames that will elapse for each bit, and the number of frames required for the transmission of all the bits forming the character are known. With this information, the number of frames from the start-of-character signal are counted and at appropriate times sampling gates are enabled to pass a single time slot pulse per bit to the succeeding circuits.

Individual groups of sampling gates are required for each source speed; but if two or more sources operate at the same speed and with the same code format, the same sampling gates may be used even if both sources are transmitting simultaneously. A common frame counter is used to count time frame periods for all sources and to control all sampling gates.

At the very low bit-per-second rates, the number of 60-microsecond frames from the start-of-character signal to the last bit for that character may be so great that the counter would have to have a very large capacity if required to count all the frames. Therefore, for the low speeds, the required capacity of the counter is minimized by providing an arrangement for counting only every n th frame where n may be any integer. For the usual range of bit-per-second rates n will usually be of the order of 5 to 10.

When a predetermined count has been attained, it is an indication that sufficient time has elapsed for the transmission and sampling of all the bits comprising a character and therefore the counter will be reset in that time slot.

The one sample per bit that is gated through the sampling gates is selected from the available samples to be the one which is most likely to be free of noise or distortion. In general, this means that a sample from approximately the middle time frame of the bit is employed.

In addition to gating a sample indicative of the bit, another signal is generated simultaneously to indicate that a bit was, in fact, sampled.

Further objects and advantages of the invention will become apparent as the following description proceeds and features of novelty which characterize the invention will be pointed out with particularity in the claims annexed to and forming a part of this specification.

For a better understanding of the invention, reference may be had to the accompanying drawings in which FIGS. 1 to 4, when arranged as shown in FIG. 5, illustrate the invention in logic diagram form.

For convenience, the invention described herein is illustrated in block and logic diagram form as it is believed that the inclusion of well-known and unnecessary circuit detail would only tend to mask or obscure the inventive concept disclosed herein.

As already mentioned, some of the techniques employed in the illustrated embodiment of the invention are similar to those disclosed in the cited Brightman application. For example, the drawings illustrate at 101 a signal source which provides input signals at a speed

arbitrarily designated speed 1. This source is coupled to the system in much the same manner that a telephone line is coupled to the time division multiplex system in the cited application. Thus, 101 and its associated blocking oscillator gate 111 are similar to item 100 in the cited application. The pairs 102 and 112, etc., are also similar. The input line matrix 121 is similar to the matrix 124 in the cited application, the input line number store 122 is similar to the calling line store 122, and the time slot allotter and line number counter 123 is similar to the time allotter 120 of the cited application.

Each of the signal sources 101 to 106 is presumed to operate at an individual and known bit-per-second rate. For illustrative purposes, the pairs 101 and 102 as well as 104 and 105 are presumed to operate at speeds 1 and 3, respectively. Speeds 1, 2, 3 and 4 are presumed to have declining bit-per-second speed rates which speeds 1 and 4 representing approximately the maximum and minimum bit-per-second rates that may be encountered.

When one of the signal sources 101 to 106 starts to provide input signals, or is called upon to provide input signals, the input line matrix 121, the input line number store 122 and the time slot allotter and line number counter 123 operate in a manner similar to that of their counterparts in the cited application to gate signals once per time frame in an individual time slot for each source, to the common signaling channel 130. Since these operations do not form a part of this invention and since the summarized operations are well known to those skilled in the time division multiplex art, they will not be described herein in detail. However, it must be understood that once per repetitive time frame each of the sources may apply a time slot pulse, in their respective individually assigned time slots, to the common signaling channel 130.

For the present discussion, it will be assumed that each time frame is 60 microseconds long and that there are twelve 5-microsecond time slots per 60-microsecond time frame.

Devices, such as AND gates, OR gates, amplifiers and inverters, are illustrated in logic diagram form to facilitate understanding of the invention. AND gates are represented in the drawings by a symbol which has the general shape of a D. The inputs to an AND gate are drawn to the straight line part of the D, while the output is drawn from the arcuate portion of the D. All the AND gates illustrated in the drawings are of the type that will provide a negative output potential only when all the inputs are negative. When any one or more of the inputs to an AND gate are positive, the output potential will rise to a more positive potential.

OR gates are similar in appearance to AND gates but are distinguished therefrom by having the input leads extend beyond the straight line portion of the D and to the arcuate portion. All the OR gates illustrated in the drawings are of the type that will provide a negative output potential when one or more of the inputs are negative. When all of the inputs to an OR gate are positive, the output potential will rise to a more positive potential.

Amplifiers are represented by an isosceles triangle with the input at the base and the output at the apex. The amplifiers used in the illustrated embodiment of the invention provide a ground or positive output signal at all times except when a negative input signal is applied to the input of the amplifier. Accordingly, the application of a negative signal to the input of the amplifier causes the amplifier to remove an inhibiting ground potential.

Inverters are similar in appearance to the amplifiers but have an additional line which is equal in length to the base of the triangle and is drawn parallel to the base and bisected by an imaginary altitude of the triangle. The inverter used in the illustrated embodiment of the invention provides a negative output signal at all times except when a negative input signal is applied to the input of the inverter. Accordingly, the application of a negative input

signal to the input of the inverter causes the inverter to produce an inhibiting or ground output signal.

Typical circuits for these well known devices may be seen in the cited Brightman application.

The circulating delay line counter 125 may be quite similar to the calling line store 122 or the terminating line store 128 disclosed in detail in the cited application. For the purpose of understanding this invention, it should be understood that the circulating delay line counter 125 includes a plurality of delay lines which are interconnected to form a counter such that on selected ones of a plurality of output leads the counter can provide a coded indication, in each time slot, of the total number of input pulses applied during that time slot. The counter could be of the binary decimal counter type described in the cited application. However, more efficient use can be made of the delay lines, in this application, if a binary arrangement is used. Accordingly, the drawings illustrate a binary counter having the output leads designated $\bar{1}, \bar{2}, \bar{4}, \bar{8}, \bar{16}, \bar{32}$, etc. The number of stages in the counter and the number of output leads will be a function of the maximum capacity that the counter would be required to have. It will be noted that the output leads are designated in such a manner that the designated numbers are all 2 to successive powers of 2, starting with 2^0 . The output leads with the bars over the designation are frequently referred to as the "not" numbers. With this system it is possible to arrange the counter so that the decimal equivalent of a binary output may be determined by adding together the numbers of all unbarred leads on which an output signal is placed. If a given unbarred output is not used in a particular coded output signal, the corresponding barred lead will have a signal applied thereto. For example, the output 11 may be represented by a signal on leads $\bar{1}, \bar{2}$, and $\bar{8}$ as well as on $\bar{4}$ and all barred leads having designations greater than 8. In the illustrated case the counter may be required to count to numbers of the order of 300 and, therefore, the illustrated counter has output leads numbered up to and including $\bar{256}$, which provides a capacity for counting to 512.

The sampling gates 131 to 134 each comprise a plurality of AND gates A to F and OR gate G. Each of the sampling gates is designed to provide an enabling signal to the associated AND gates 141 to 144, respectively, only when the counter 125 provides output signals indicative of predetermined settings. More specifically, each of the AND gates A to F is selectively enabled by being connected to a selected group of the output leads from counter 125 thereby allowing a signal to be passed through an enabled one of the AND gates only when the counter has been advanced to a predetermined setting.

As already stated, the present invention provides a common means for sampling signals, as received from a plurality of signal sources, each of which may be operating at different bit-per-second rates, and for gating selected ones of the samples forward to a succeeding circuit. It is desired to gate forward only one sample per bit and, therefore, it is essential that the forward gated sample be truly representative of the bit. Although the system of this invention may be used with various code formats currently in use, it will be described herein in connection with a standard teletype code in which each letter or signal is made up of five units of equal length in the manner illustrated on page 100 of "Principles of Electricity Applied to Telephone and Telegraph Work," as prepared by the American Telephone and Telegraph Company. In addition to the five units, there are also start and stop units which are spaces and marks, respectively. Each of the five units and the start unit have the same time duration, while the stop unit has a time duration of approximately 1.42 of the other units. In general, the sample for each unit, or bit, that is to be gated forward should be selected from approximately the midpoint of the bit in the order to minimize the possibility of gating forward incorrect in-

formation resulting from distortion of the bit pulse. Samples from any other portion of each bit may be gated forward if there is any reason to believe that they are more representative of the bit.

In general, each bit will be transmitted from its source at a known bit-per-second rate and once each time frame a representative portion of the bit will be gated to a common signaling channel at a rate which permits the gating of several portions of each bit to the common signaling channel. Therefore, by counting the portions applied to the common signaling channel, in a given time slot, it is possible to select a sample which is obtained from any desired portion of each bit.

The usual range for the receipt of bits is from 40 or 50 bits-per-second to about 2500 bits-per-second, which means that with a 60-microsecond frame period that there are about 3000 and 50 frame periods per seven-bit-character, respectively. To eliminate the need for a counter having a capacity to count to 3000, the counter is arranged to count only every tenth frame of the low speed sources. The speeds of 500 and more bits-per-second are considered high speeds, while speeds below 500 bits-per-second are considered low speeds. The following table illustrates the number of microseconds per bit, the number of 60 μ s. frame periods per bit and the total number of available samples in a seven-bit-character for various high and low speed sources.

Bit-per-second rate	Micro-seconds per bit	No of 60 μ s. frames per bit	Samples per bit at 60 μ s. sample speed (Hi-speed)	Samples per bit at 600 μ s. sample speed (Lo-speed)	Available samples per seven-bit-character
2,500.....	400	6.66	6.66	-----	46.7
2,400.....	416	6.95	6.95	-----	48.6
1,500.....	667	11.12	11.12	-----	78.0
1,000.....	1,000	16.66	16.66	-----	117
500.....	2,000	33.33	33.33	-----	233
400.....	2,500	41.6	-----	3.33	29.2
200.....	5,000	83.4	-----	4.10	58.5
100.....	10,000	166.66	-----	8.34	117
50.....	20,000	333.33	-----	16.66	233
40.....	25,000	400.00	-----	33.33	280
				40.00	

As may be seen from the table, the sampling rates have been selected to allow at least three samples per bit and so that the total number of samples per seven-bit-character does not exceed 300. This choice permits a selection of a sample from a desired portion of the bit without requiring that the counter have an excessive capacity. If desired, more sampling rates could be provided to further reduce the capacity of the counter. If information is received from a 40 bit-per-second source and a counter is caused to start to count one stage each 600 μ s. upon the start of the first bit, it will be known that the start pulse will be over at approximately the time the counter has counted to 40. Therefore, if a gate, similar to the gate A in the group 131, is arranged to gate a sample therethrough when counter 125 has advanced to count 60, the midpoint of the first information bit will have been sampled and gated to the next circuit. In a similar manner, gates B, C, D and E may be arranged to gate samples at counts 100, 140, 180 and 220, respectively. At any count after 240, it will be known that all five information bits have been completed and, therefore, gate F may be set to pass a pulse therethrough at any convenient higher count to reset the counter and prepare to count the samples in the next character.

It is believed that the interaction of the components of the system can best be understood by, figuratively speaking, following the pulses received from one of the machines, such as 101, and observing the output pulses on leads 108 and 109. For this purpose, it will be assumed that machine 101 provides bits at the rate of 2400 per second, and that a character comprises seven bits, including the start and stop bits. In response to a start-of-message signal or a roll call operation, the source 101 will be as-

signed any available one of the twelve time slots in a repetitive 60 μ s. time frame and frame then to the end of the message the blocking oscillator gate 111, which is associated with source 101, will be gated open once per time frame in the assigned time slot by the time slot allotter and line number counter 123, the input line number store 122, and the input line matrix 121 operating together, as explained for their counterparts in the cited application. Accordingly, in the assigned time slot of the time frame, a 5 μ s. pulse representative of the instantaneous mark or space intelligence from source 101 will be gated through blocking oscillator gate 111 to the common signal channel 130. Before a character is transmitted, a continuous stop or mark signal will be transmitted, but upon the start of a character a one bit space signal will be transmitted. The first mark pulse this is gated through blocking oscillator gate 111 will enter the start of character detector 117 and be applied as an input to the delay line 117A and the AND gate 117B. No signal will be passed through the AND gate 117B as the output of the inverter 117C and the applied signals are of opposite potentials. A pulse is, however, entered into the delay line 117A and one time frame later will be applied to inverter 117C. One time frame later, if a mark pulse is still being provided from source 101, a 5 μ s. sample thereof will be passed through blocking oscillator gate 111 to the common signaling channel 130 to be applied to the delay line 117A and AND gate 117B. At the same time, the inverse of the first mark pulse will be applied to inverter 117C to inhibit the AND gate 117B. However, when the first space signal, which has a polarity opposite to that of the mark signal, is transmitted from source 101 to indicate a start of character, a 5 μ s. sample thereof will be gated through blocking oscillator gate 111. The last mark pulse will be passed through inverter 117C. Under these conditions, a time slot pulse will be passed through AND gate 117B and applied as an input to OR gate 118 and thereby to delay line 119. Once each time frame, the pulse entered in delay line 119 will be recirculated by means of gates 120 and 118. The AND gate 120 will normally be held enabled by inverter 124.

The time slot pulses that are applied to lead 111A to enable blocking oscillator gate 111 will also be applied to OR gate 151. Other inputs to OR gate 151 will be from other points in the matrix 121 that are assigned to machines operating at the same speed, for example machine 103. Accordingly, once each time frame, a pulse will be passed through OR gate 151, amplifier 155, OR gate 159 and amplifier 160 to be applied as an input to AND gate 161. When the next time slot pulse is applied to lead 111A, the pulse entered in delay line 119 will have circulated therethrough and will be applied to AND gate 161 and, therefore, AND gate 161 will be enabled to pass a time slot pulse to the counter 125 over lead 126 to advance the counter one step from its reset condition in the assigned time slot. It will be shown later how the counter had been reset. In a similar manner, the counter will be advanced one step each time frame in the assigned time slot.

As previously mentioned, the counter 125 provides in each time slot an indication on its output leads of the number of elapsed time periods which, in the illustrated case, equals the number of time frames. Selected output leads of the counter are wired to the sampling gate 131 for speed 1. It is to be noted that the sampling gate 131 is common to all sources having the same speed. Gate A of the group 131 will be connected in such a manner that it will be enabled when a count of eleven has been attained in the assigned time slot. That is, since each bit of the 2400 bit-per-second source is 6.95 frames long, the approximate midpoint of the first information bit will occur during the eleventh frame. In a similar manner, the approximate midpoint of the successive information bits will occur during the eighteenth, twenty-fourth, thirty-second and thirty-ninth frames. Therefore, the gates B to

E of the group 131 will be wired to the counter 125 in a manner so that they will be enabled on the eighteenth, twenty-fourth, thirty-second and thirty-ninth counts, respectively. In addition, it will be noted that each of the gates A to E is enabled by the application of the time slot pulse passed through OR gate 151 and amplifier 155 to lead 111B. Therefore, a predetermined number of time frames after the start of a character, a pulse will be passed through the AND gates A to E and thence through OR gate G.

The selected time slot pulses that are gated through OR gate G will enable AND gate 141 to pass a pulse indicative of the instantaneous pulse on the common signaling channel 130, which, in turn, is indicative of the pulse being received from source 101. Thus a sample from the approximate midpoint of each bit is passed through AND gate 141 in the assigned time slot of the time frame.

As already pointed out, AND gate E is enabled when counter 125 has counted to the thirty-ninth time frame after the start of the character. The gate F may be enabled at any count that is convenient during the stop period of the character, for example at count 44. Thus, when the forty-fourth frame period is reached, a time slot pulse will be passed through gates F and H to reset the counter in the assigned time slot. In addition, the pulse through gate H causes inverter 124 to inhibit the recirculation of the pulse in the assigned time slot in delay line 119. Therefore, AND gate 161 will not be fully enabled in the assigned time slot and no further counts will be made until the start-of-character detector 117 detects another start-of-the-character, whereupon the described process will be repeated. Since the counting starts over for each character there is character-by-character synchronization, thereby minimizing any speed variation problems.

If two sources, such as sources 101 and 103, are producing input signals at the same time, there will be no interference even though both are using the same counter 125 and the same sampling gate 131, since each is operating in a different time slot. That is, when the assigned time slot is applied to lead 111A, a pulse will simultaneously appear on leads 130, 111B and possibly on lead 108 which all relate to the same message. At some other time in another time slot, a pulse may be applied to lead 113A to do the same thing for another message source. The sampling gates are individually enabled during the required time slots and pulses will be passed therethrough only if the counter is at the right setting in that time slot.

In the event that two different sources operate at the same bit-per-second rate but with different code formats such that a character is represented by one number of bits from one of the sources and a different number of bits from the other source, it will be necessary to use either a separate group of sampling gates for each source or else a modified sampling gate. When separate groups of sampling gates are used, the sources may be treated as if they were not of the same speed. If a single sampling gate is used, it is necessary to provide special signals so that the group of sampling gates will appear to have different characteristics for each of the sources.

If the message source 106 is operating, and it is assumed to be a low speed source such as fifty bits-per-second, it will be evident that so many 60 μ s. time frame periods will elapse between the start of the character and the end of the character that a very large capacity counter would have to be provided to count them all. Accordingly, an arrangement is provided to count only every n th frame. The example assumes that $n=10$, but any other integer value of n could be used that is compatible with the capacity of the counter 125 and the speed of the source. A pulse source 161 is provided which produces a pulse of one time frame every tenth time frame. That is, with n assumed to be 10, pulse source 161 will provide a 60 μ s. pulse every 600 μ s. Thus the AND gate 162 is enabled for only one time frame in every ten

time frames. Therefore, the counter 125 is allowed to count only every tenth time frame. Since the counter 125 will remain at the same setting for ten time frames, the pulses from source 161 are also used to enable gates 142, 144, 145 and 146 to permit only one pulse per counter setting therethrough. Thus, by counting only every tenth time frame for the low speed signal source, the capacity of the counter can be kept within a reasonable range without interfering with the accuracy of the selection of the sample from the middle of the bit since each slow speed bit is so much longer than the high speed bit.

Each time that a bit is sampled and a mark or space indicating pulse is applied to lead 108, a time slot pulse is also applied to lead 109. That is, since no information and the space signal are represented by the same signal on lead 108, it is necessary to provide a signal on lead 109 to indicate that a bit has, in fact, been sampled and that the signal on lead 108 indicates a space. Thus, no signal on lead 108, together with a signal on lead 109, indicates a space, while a simultaneous signal on both leads 108 and 109 is indicative of a mark signal.

If more than four distinct speeds are used, it will be necessary to provide additional sets of sampling gates and another gate, such as gate 151, will be added.

While there has been shown and described what is considered at present to be preferred embodiment of the invention, modifications thereto will readily occur to those skilled in the art. It is not desired, therefore, that the invention be limited to the embodiment shown and described, and it is intended to cover in the appended claims all such modifications as fall within the true spirit and scope of the invention.

What is claimed is:

1. In a data handling system, a common signaling channel, first and second signal sources for providing groups of signals at first and second predetermined bit-per-second rates, respectively, time division multiplex means coupled to said sources for applying signal samples from said first and second signal sources to said common signaling channel once per repetitive time frame in first and second time slots, respectively, common detecting means coupled to said common signaling channel for providing first and second start signals in said first and second time slots in response to the start of a group of signals from said first and second source, respectively, common counting means coupled to said detecting means and responsive to said first and second start signals for producing a first and second series of indications in said first and second time slots, respectively, which are indicative of the duration of the elapsed time, as measured in time periods comprising a predetermined number of frame periods, subsequent to the generation of said first and second start signals, respectively, a common signal output channel, a first group of sampling gates coupling said common signaling channel and said common signal output channel and associated with said first signal source for gating a first signal sampled from said first source to said common signal output channel in said first time slot only when said common counting means produces a signal in said first time slot indicating that a first predetermined time has elapsed subsequent to the generation of said first start signal, and a second group of sampling gates coupling said common signaling channel and said common signal output channel and associated with said second signal source for gating a first signal sampled from said second source to said common signal output channel in said second time slot only when said common counting means produces a signal in said second time slot indicating that a second predetermined time has elapsed subsequent to the generation of said second start signal.

2. The combination as set forth in claim 1 wherein said first and second predetermined times are so selected that the samples which are gated to said common signal output

channel are selected from a first predetermined bit within said first and second groups of signals.

3. The combination as set forth in claim 2 wherein said first and second groups of sampling gates will gate a second signal sampled from said first and second sources, respectively, to said common signal output channel in said first and second time slots, respectively, at another predetermined time which is so selected that said second signal samples are selected from a second predetermined bit within said first and second groups of signals.

4. The combination as set forth in claim 3 and including means in said first and second groups of sampling gates for gating a third signal sample from their respective sources to said counter in said first and second time slots, respectively, at a specific predetermined time which is so selected for each sample that said third signal samples are selected from the last bit within their respective groups of signals.

5. The combination as set forth in claim 4 wherein said counter is reset to a predetermined setting in said first and second time slots in response to the application of said third signal samples thereto in said first and second time slots, respectively.

6. In a data handling system, first and second sources of data signals operating at first and second known bit-per-second rates for providing intelligence character by character, a common signaling channel, time division multiplex means including first and second gate means coupled to said first and second sources, respectively, for gating a sample of the signal from said first and second sources to said common signaling channel once each repetitive time frame in first and second time slots, respectively, and for providing periodic signals in said first and second time slots, a start-of-character detector coupled to said common signaling channel for providing first and second time slot output signals in said first and second time slots, respectively, which are coincident with that sample from said first and second sources which is indicative of the start of a group of samples representing on individual character, a dynamic counter having a plurality of output leads and coupled to said time division multiplex means and said detector, said counter being responsive to said first and second time slot output signals from said detector and to said periodic signals from said time division multiplex means for providing on said output leads in said first and second time slots of each time frame a series of coded signals indicative of the number of time periods which have elapsed since the generation of said first and second time slot output signals, respectively, first and second groups of individual sampling gates for said first and second known bit-per-second rates, respectively, each of said individual gates within said first and second groups of gates coupled to said common signaling channel and to selected output leads of said counter for enabling said individual gates to pass therethrough only those samples emanating from said first and second sources, respectively, which occur in predetermined time periods.

7. The combination as set forth in claim 6 wherein said predetermined time periods are so selected that one sam-

ple per bit of each character is gated through said individual gates.

8. The combination as set forth in claim 7 wherein the last sample per character that is gated through said individual gates is applied to said counter for resetting said counter to a predetermined setting in the time slot of the applied sample.

9. In a data handling system, a plurality of sources of data signals each operating at an individual and known bit-per-second rate for providing intelligence character by character with each character from a given source represented by a predetermined number of said bits, a common signal channel, time division multiplex means including individual gate means coupled to their respective sources for gating a sample of the signal from their respective sources to said common signal channel once each repetitive time frame in the individual time slot assigned to the respective sources, a start-of-character detector coupled to said common signal channel for providing a time slot signal coincident with that sample from each of said sources which is indicative of the start of a group of samples representing an individual character, a dynamic counter coupled to said time division multiplex means and said detector for providing on output leads therefrom a time slot output signal, in each of the time slots in which said detector provides an output signal, which is indicative of the number of elapsed time periods of a predetermined interval which have elapsed since the production of the output signal of the detector in the respective time slots, a plurality of groups of sample gates with one group for each of said first and second rates, and with each gate within any one of said groups coupled to said common signal channel and to selected output leads of said counter for gating therethrough only those samples from the source operating at the bit-per-second rate associated with said one group which occur in predetermined time periods following the start of each character.

10. The combination as set forth in claim 9 wherein said predetermined time periods are so selected that one sample from a selected portion of each bit of each character is gated through one of said gates within said group of sampling gates.

11. The combination as set forth in claim 10 wherein each of said groups of sampling gates includes means for coupling the last sample of each character which is gated through one of said gates within said groups of sampling gates to said counter.

12. The combination as set forth in claim 11 wherein said counter is reset to a predetermined setting in the time slot of said last sample in response to the coupling of said last sample to said counter.

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