United States Patent

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[54] **CHARACTER GENERATOR**
8 Claims, 3 Drawing Figs.

[52] **U.S. Cl.** **340/324,**
315/18, 340/347
[51] **Int. Cl.** **G06f 3/14**
[50] **Field of Search** 315/18, 22,
19; 340/324.1, 347 DD, 347 DA

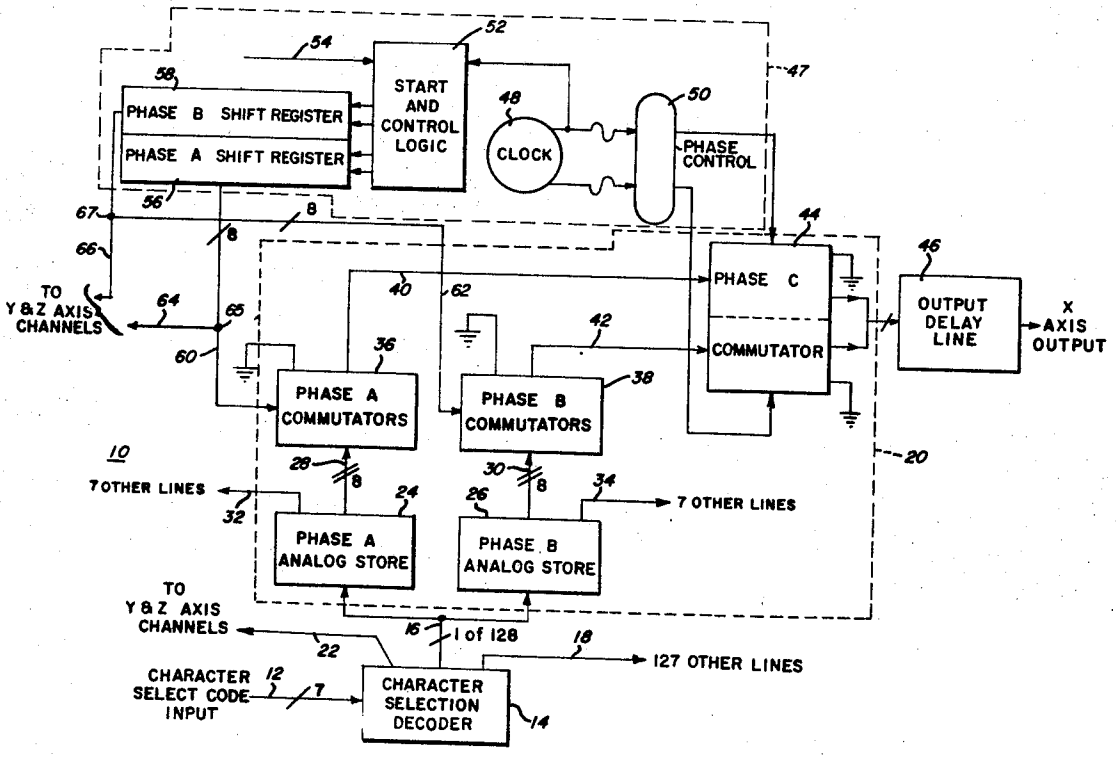
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ABSTRACT: A high-speed character generator which employs single resistors for storing character stroke information and which employs alternating low-speed current mode commutators to alternately drive a two-phase, high-speed current mode commutator.



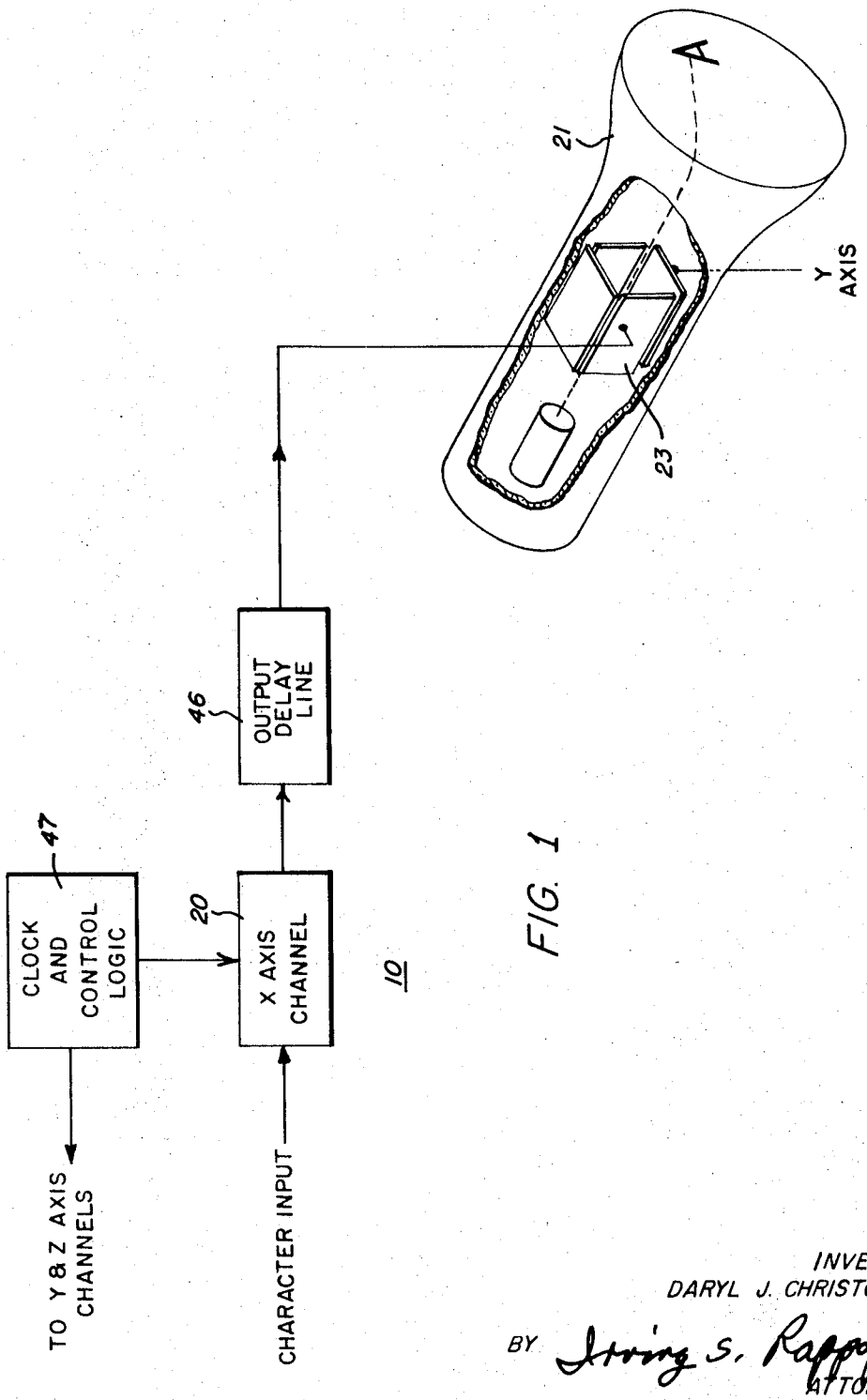


FIG. 1

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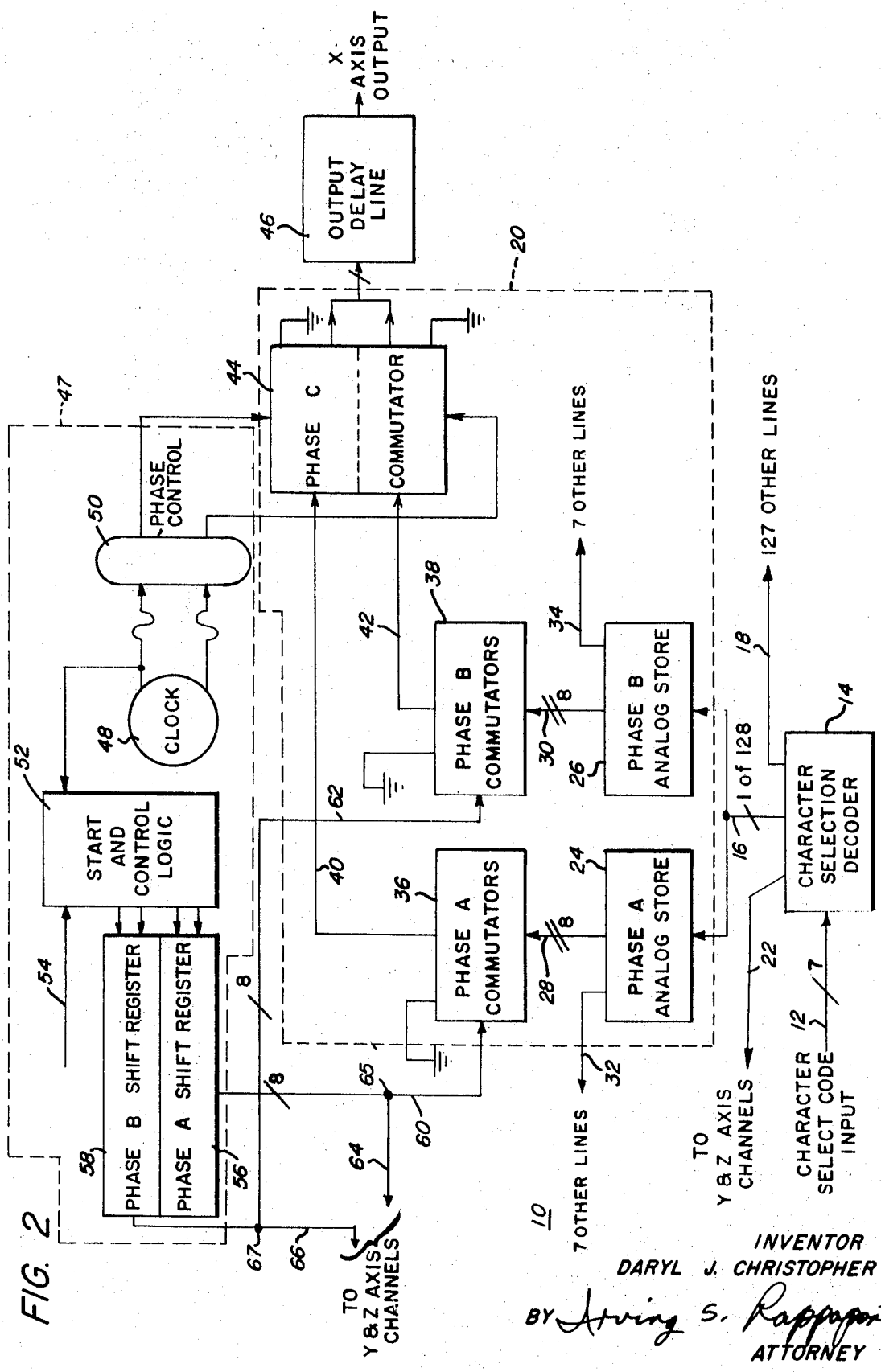


FIG. 2

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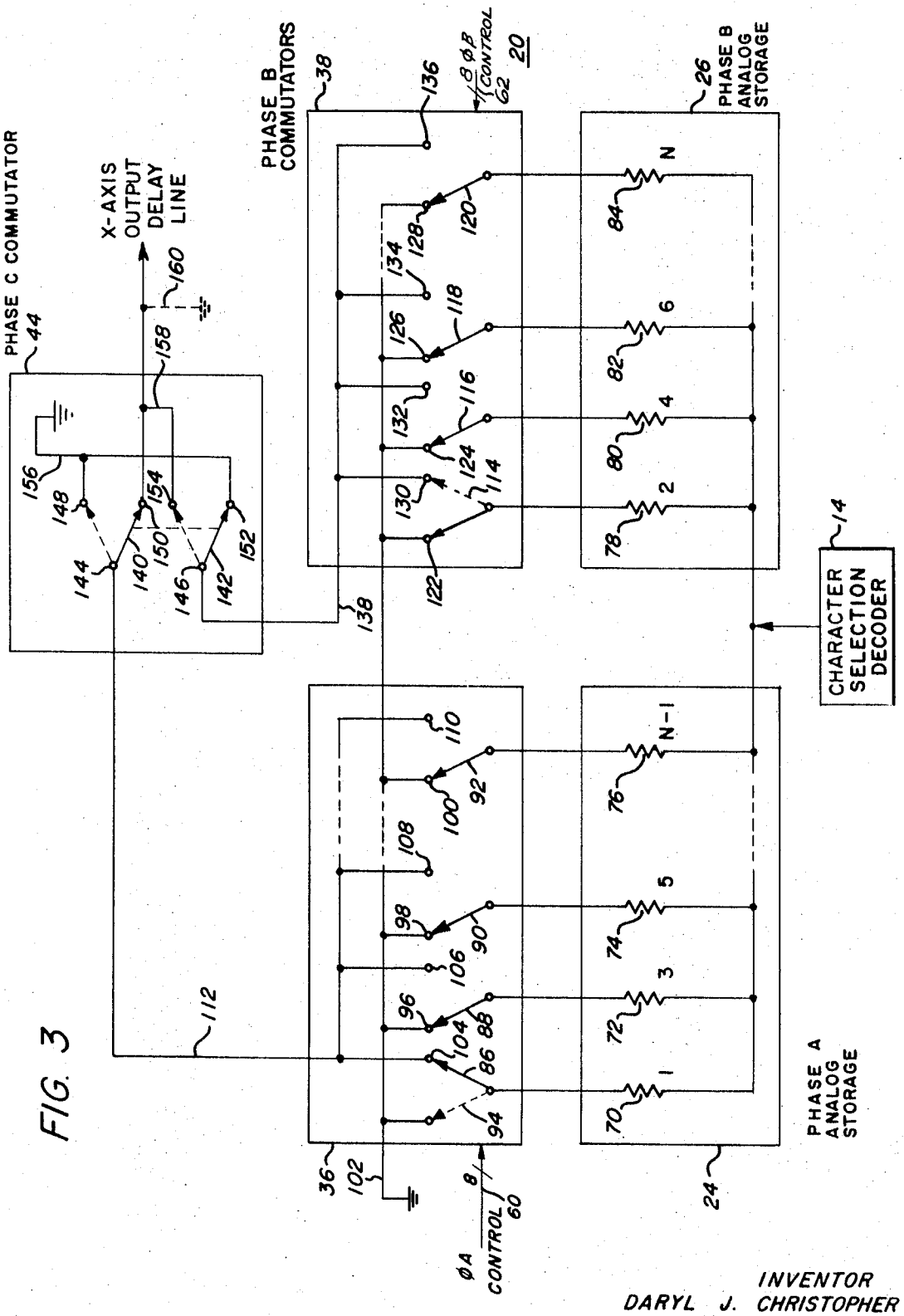


FIG. 3

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CHARACTER GENERATOR

BACKGROUND OF THE INVENTION

One type of character generator is a real time function generator using the slope approximation technique rather than truly cursive character generation. The slope approximation technique uses straight line segments or strokes of predetermined lengths to generate the characters or symbols. In such prior art types of character generators the points representing the straight line segments or strokes are stored as binary quantities using diodes. The memory of the generator is sequentially interrogated to obtain the information from the storage. Each point is called up one at a time and the writing takes place one point at a time. Thus, these prior art generators operate in a serial sequence. A great disadvantage of serial machines is that they tend to be very noisy in interrogating the memory, extracting data for each point, etc.

The uniqueness of the present invention lies in the methods of generating the strokes, storing the stroke data and other features. The approach of the present invention utilizes inexpensive resistors to store the individual stroke data in the form of resistance values. In addition, the data stored has been expanded to include brightness coding of the Z-axis as well as X- and Y-axis coding for each stroke in the character deflection waveform function. Thus, three resistors of appropriate value are required for each segment of the character (one resistor for each of the X-, Y- and Z-axes). Each character contains 16 strokes or less, depending on the complexity or number of strokes required for a particular character. In the prior art the character generators have utilized all time intervals allotted for the most complex characters for even the very simple characters, therefore consuming unnecessary time in the generation of the characters. The generator of the present invention is uniquely coded in the Z-axis with a particular resistive value which automatically terminates the character generator timing cycle and provides system reset capability. This feature may be extremely important when large amounts of data must be presented on the cathode-ray tube displays per unit time. This feature alone may enable doubling of data rates. Alternatively, by increasing data rates, two displays could be serviced with one character generator, thus decreasing overall system cost. The addition of the Z-axis coding adds another important characteristic over prior art generators. Heretofore, no intensity compensation was provided for each character stroke segment. Therefore, it was necessary to confine or restrict the coding such that the writing rate of the electron beam was maintained within certain limits. If these limits were not maintained very undesirable visible effects, such as adjacent high and low intensity segments within a character, occur. Furthermore, prior art generators require more time per character in order to stay within the segment length variability in order to satisfy the intracharacter brightness requirements. The character generator of the present invention allows a very accurate intra- and inter-character brightness control.

Another important aspect of the generator of the present invention lies in the manner in which data is stored. This stored data is necessary in order to provide the generator with all the information required to generate the complete set of characters. In prior art generators this storage has been provided by using a multiplicity of diodes in the character matrix cards. Each stroke of a character required upward of **11** diodes which energize the digital-to-analog converters and provided a blank or unblank function in the axis. The generator of the present invention utilizes just three resistors for each segment of a character and in so doing provides the following advantages:

(1) Z-axis brightness control: (2) character termination; (2) increased data presentation rates; (4) greater flexibility in character coding; (5) parallel operation of stroke value selection on a whole character basis; (6) greatly enhanced reliability due to the reduction in both the number and cost of the component part; (7) compatability with integrated circuit packaging techniques; (8) better character quality through improved signal-to-noise ratios obtained through parallel data organization techniques.

Operationally, all the stroke date for the selected character is brought up in parallel prior to the start of character writing through low-speed current mode switches. The individual character strokes are then generated sequentially by simply switching the path of the store current to the output delay line averager through a high-speed current mode commutator. Since this high-speed commutator is a two-phase, two pole-two throw switch, the speed requirements on the low-speed current mode switches are reduced. This arrangement allows for increased output bandwidth without increasing the total internal bandwidth. The generator approach of the present invention allows reduction of the internal bandwidth requirements by more than an order of magnitude below prior art sequential data character generators. By so doing, the high-speed circuits are confined to a smaller area, which is extremely desirable when improved signal-to-noise ratios are desired at the output. Because of the parallel data presentation mode, the prospects for generating submicrosecond characters are extremely good.

SUMMARY OF THE INVENTION

A high-speed character generator comprising three resistors for each character stroke providing X- and Y-axis coding storage and Z-axis brightness coding storage and low-speed current mode commutators for alternately supplying all the stroke data for the selected character to a two-phase, high-speed, current mode commutator.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1** and **2** are block diagrams of the X-axis channel of the generator of the present invention; and

FIG. **3** is a circuit diagram of the X-axis channel shown in the dotted block in FIG. **2**.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **1** shows a character generator **10**. The generator **10** includes an X-axis channel **20** to which the character input its applied. Clocking and control logic circuitry **47** control the X-axis channel **20** as well as the Y- and Z-axis channels. The output from the channel **20** is applied to X-axis deflection plates **23** of a cathode ray tube **21** via an output delay line **46**.

In FIG. **2** the generator **10** includes seven character select code input lines symbolically represented by the input line **12** and carrying the number seven adjacent the line. The particular character generator **10** shown has a repertoire of **128** characters and requires a seven bit input in order to generate the **128** characters. The seven input lines **12** are connected to a character selection decoder **14** which operates to select the bus containing the character information which the generator has been instructed to generate. The output line **16** from the decoder **14** represents one character of the **128** capable of being generated by the generator **10** and is labeled **1** of **128**. A line **18** from decoder **14** symbolically represents the other **127** possible characters which may be generated by the system. The output from the decoder **14** which is contained on line **16** is fed to the X-axis channel which is represented by the dotted block **20**. A line **22** from decoder **14** indicates that the decoder also selects the appropriate character input code for the Y- and Z-axis channels.

The output signal which is contained on line **16** is fed in parallel to a phase A analog store **24** and a phase B analog store **26** which are included in the X-axis channel **20**. The phase A and B analog stores **24** and **26** serve to alternately store the stroke information relating to the character to be generated. The phase A and B analog stores **24** and **26** each have **8** output lines as symbolically represented by lines **28** and **30**. Lines **32** and **34** from phase A and B analog stores **24** and **26** respectively represent the connections to the other charac-

ters. The output lines 28 and 30 from the phase A and B analog stores 24 and 26 respectively are applied to the phase A and B commutators 36 and 38 respectively, each of which includes 8 current mode commutators (shown in FIG. 3). The phase A and B current mode commutators 36 and 38 are low-speed commutators which are relatively inexpensive. The outputs from the phase A and phase B commutators 36 and 38 are fed via lines 40 and 42 to a phase C current mode commutator 44. The phase C current mode commutator 44 is a high-speed, two-phase, two pole-two throw switch. The resulting signal from the phase C commutator 44 is applied to an output delay line 46 whose output represents the X-axis character stroke. The phase A and B commutators 36 and 38 operated alternately, such that when the phase B commutator 38 diverts current from the phase B analog store 26 the phase A commutator 36 is applying analog current through the high-speed phase C commutator 44. The switches of the high-speed commutator 44 are linked together in time as shown in FIG. 3 in order to provide two-phase operation. Thus, one of the low-speed commutators 36 and 38 is receiving information from its corresponding analog store 24 or 26 while the other low-speed commutator 36 or 38 is supplying the high-speed commutator 44 with the already stored stroke. During the next stroke the operation of the low-speed commutators 36 and 38 is reversed. This alternating action provides a continuous output to the output delay line 46.

Connected to the phase C commutator 44 is a crystal controlled clock 48 and a phase control circuit 50. The clock 48 generates clocking signals such as the sine and inverted sine functions shown. A start and control logic circuit 52 is connected to one side of the clock 48 and provides internal timing for converting asynchronous start information such as may be provided on line 54 into synchronous clock information. A pair of phase A and phase B shift registers 56 and 58 respectively are also connected to the start and control logic circuit 52. The phase A shift register 56 is an eight-bit shift register and has eight connecting lines symbolically shown by line 60 to couple synchronization and control signals to the corresponding eight lines of the phase A commutator 36. Correspondingly, the phase B shift register 58 is an eight-bit shift register having eight lines connected to the eight commutators of the phase B commutator 38, which connection is made symbolically via line 62 to couple synchronization and control signals to phase B commutator 38. Lines 64 and 66 which are connected to lines 60 and 62 at connection points 65 and 67 respectively are provided to indicate that the phase A and B shift registers 56 and 58 are also connected to the Y- and Z-axis channels. The start and control logic circuitry 52 acts to tie the shift registers 56 and 58 and the clock 48 together into synchronous operation. It should be noted that analog data current flow once established before the start of the character generation is never interrupted. The shift registers 56 and 58 serve only to transfer the analog character current from the phase A and B commutators 36 and 38 to the phase C current mode commutator 44 in preparation for transfer to the output delay line 46. Therefore, the character generator speed is limited only by the shift registers and current mode switching capabilities. The complementary functions generated by the clock 48 control the operation of the two-phase commutator 44 to give a 180° phase change. The clock 48 controls the effective switch transfers of the high-speed commutator 44 while the shift registers 56 and 58 control the switching of the low-speed commutators 36 and 38.

FIG. 3 is a circuit diagram of the X-axis channel shown in the dotted block 20 in FIG. 2. Included in the X-axis channel are the phase A and B analog stores 24 and 26, the phase A and B low-speed commutators 36 and 38 and the high-speed phase C commutator 44. The phase A analog store 24 includes parallel-connected resistors 70, 72, 74 and 76 which are labeled 1, 3, 5 and N-1, where in the described embodiment N is 16, corresponding to the order of the stroke information stored on each of these resistors. The phase B analog store 26 includes parallel-connected resistors 78, 80, 82 and 84 which are labeled with the numbers 2, 4, 6 and N respectively to denote the order of the stroke information carried by each of these resistors. Although the present embodiment has been described when N, the number of resistors in the phase A and B analog stores, is 16, the stores may be constructed to include any desired number of character-stroke-storing resistors. These resistors in the analog stores 24 and 26 are ± 1percent precision deposited carbon resistors. Although the resistors shown are carbon resistors, any other resistor having the required accuracy may be employed. Each of the resistors 70, 72, 74 and 76 of the analog store 24 is connected to a two-position switch 86, 88, 90 and 92 respectively of the phase A low-speed commutators 36. These switches are two-position switches, each having a terminal 94, 96, 98 and 100 respectively connected to a common line 102 which is connected to ground. Each of the switches 86, 88, 90 and 92 also has another terminal 104, 106, 108 and 110, respectively, each of which is connected to a common line 112.

Each of the resistors 78, 80, 82 and 84 of the analog store 26 are connected to a switch 114, 116, 118 and 120, respectively, of the phase B low-speed commutator 38. The switches 114, 116, 118 and 120 are two position switches, each having one terminal, 122, 124, 126 and 128, respectively, all of which are connected to the line 102. These switches also have another terminal 130, 132, 134 and 136, respectively, each of which is connected to a common line 138.

The lines 112 and 138 are connected to the phase C high-speed commutator 44 which includes a pair of switches 140 and 142. The line 112 is connected to the switch 140 at terminal 144 while the line 138 is connected to the switch 142 at terminal 146. Each of the switches 140 and 142 of the high-speed commutator 44 have two positions indicated by the terminals 148 and 150 of switch 140 and terminals 152 and 154 of switch 142. The terminals 148 and 152 of the switches 140 and 142 respectively are both connected to a common line 156 which is connected to ground. The terminals 150 and 154 of the switches 140 and 142 respectively are connected to a common line 158 which leads to the output delay line shown in FIG. 1. The dotted ground symbol 160 indicates that the line 158 is effectively equivalent to ground.

During operation of the generator when the decoder 14 selects the appropriate character bus, the selected character stroke information has been established for the analog stores 24 and 26. During the transfer of the stroke current from resistor 70, which resistance value is determinative of the first bit of stroke information in current form, the switch 86 is connected to terminal 104. This connection allows the stroke current from resistor 70 to pass via line 112 to the terminal 144 and the switch 140 which is connected to the terminal 150, thereby allowing the current to be passed on line 158 to the output delay line. During this same time the switches 88, 90 and 92 of the low-speed commutator 36 are connected to their respective terminals 96, 98 and 100 which are grounded via line 102. While the information stored on resistor 70 is passed in current form from the phase A low-speed commutator 36 to the high-speed commutator 44, the next bit of stroke information which is stored in resistor 78 of the phase B analog store 26 is passed in current form from the commutator 38 to the commutator 44. During the passage in current form of the first bit of stroke information from resistor 70 through the high-speed commutator 44, all of the switches 114, 116, 118 and 120 of the phase B low-speed commutator 38 are connected to ground by their respective terminals 122, 124, 126 and 128 respectively. However, before the completion of the passage of the information stored on resistor 70, the switch 114 moves from its connection to its corresponding terminal 122 to its terminal 130 and shortly thereafter the switch 86, which was connected to its corresponding terminal 104 is switched to its terminal 94, thereby connecting it to ground. The switch 114 when connected to its terminal 130 will pass in current form the information contained on resistor 78 by line 138 to terminal 146 of the switch 142 of the high-speed commutator 44. At the completion of the sampling of phase A the switch 140

which was connected to terminal **150** will be switched to terminal **148** leading to ground via line **156** and the switch **142** will switch from its terminal **152** to terminal **154** thereby allowing the information passing through the switch **114** from the resistor **78** to be passed to the output delay line via line **158**. The X-axis channel **20** will continue to operate in this alternating manner until all of the bits of stroke information have been passed to the output delay line. Therefore, through this alternating action between the phase A and phase B low-speed commutators **36** and **38** the system of the present invention requires only one high-speed commutator **44** for each axis. It should be pointed out that the decoder **14** and the timing circuits including the phase control circuit **50**, the clock **48**, the start and control logic circuitry **52** and the shift registers **56** and **58** are common to the X-, Y- and Z-axis channels.

I claim:

1. A high-speed character generator comprising:
character selection code input means for receiving character stroke selection information;
character selection decoding means connected to said input means for selecting the desired character strokes;
analog storage means for storing the resistance value corresponding to the character stroke selected by said decoding means;
alternating first and second commutating means for alternately receiving character stroke generation currents derived from said storage means;
third commutating means for alternately receiving and switching character stroke currents derived from said first and second commutating means; and
synchronizing means including means for controlling the operation of said first, second and third commutating means.

2. A character generator as set forth in claim **1** wherein:
said analog storage means includes a plurality of parallel-connected resistors for storing character stroke information.

3. A character generator comprising:
a plurality of character selection code input lines for receiving character stroke selection information;
character selection decoding means connected to said input lines for selecting the desired character strokes;
analog storage means including a plurality of resistors each of which, when connected to a constant voltage by said decoding means, conducts a current, the value of which current is uniquely determined by the particular resistor to which said decoding means is connected;
a plurality of commutators connected to said analog storage means for alternately receiving character stroke generation currents derived from said analog storage means;
an additional commutator for alternately receiving and switching information derived from said plurality of commutators; and
clocking and control logic circuitry for synchronizing and controlling the operation of said plurality of commutators with said additional commutator.

4. A character generator as set forth in claim **3** including display means coupled to the output of said additional commutator for displaying the generated characters.

5. A character generator comprising:
a plurality of character selection code input lines for receiving character stroke selection information;
a character selection decoder connected to said input lines for selecting the desired character stroke selection information;
phase A and B analog means each including a plurality of parallel-connected resistors for conversion of the character stroke selection information selected by said decoder into a plurality of character stroke generation currents;
phase A and phase B commutators operable at a first speed each including a plurality of switches, each switch being connected to a corresponding resistor of said analog means, said commutators alternately receiving character stroke generation currents derived from said analog means;
an additional commutator operable at a second speed connected to each of said phase A and phase B commutators for alternately receiving and switching character stroke generation currents derived from said phase A and phase B commutators, wherein said second speed is greater than said first speed;
synchronizing means including means for controlling the operation of said commutators said synchronizing means and said controlling means including clocking and control logic circuitry respectively; and
display means coupled to the output of said additional commutator for displaying the generated character.

6. A character generator comprising:
character selection code input means for receiving character stroke selection information;
switchable analog conversion means for converting the character selection code to a plurality of stroke generation signals;
alternating first and second commutation means for alternately receiving stroke generation signals derived from the switchable analog conversion means;
third commutating means for alternately receiving and switching signals derived from said first and second commutating means; and
synchronizing means including means for controlling the operation of said first, second and third commutating means.

7. A character generator in accordance with claim **6**, wherein said switchable analog conversion means includes a plurality of parallel-connected resistors for converting stroke selection information into analog currents.

8. An alphanumeric display comprising:
input means for receiving visual informational pattern selection information;
decoding means connected to said input means for selecting the desired information pattern;
storage means for storing data selected by said decoding means;
means for alternately receiving visual informational pattern data derived from said storage means, including at least first and second commutating means;
means for alternately receiving and switching the output derived from said means for alternately receiving visual informational pattern data, including at least third commutating means; and
synchronizing means including means for controlling the operation of each of said commutating means.