Abstract: A composite analog-to-digital converter, ADC, comprising a plurality of successive approximation registers, SAR, ADCs, each of which comprises one or more significant conversion capacitors, each of which is dynamically connectable by one or more first reference switches to a first plurality of reference voltages, wherein the first plurality of reference voltages has a common first nominal voltage.
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The present invention relates to a composite analog-to-digital converter.

Composite analog-to-digital converters (ADC) comprise one or more sub-ADCs that are used for sampling the signal of the composite ADC. For example, time interleaved (TI) Analog to Digital Converters (ADCs) can comprise two or more successive approximation register (SAR) ADCs. A Time-Interleaved ADC with SAR ADCs is comprised of an analogue signal demultiplexer or de-interleaver that converts a high-bandwidth analog input signal into a number of lower bandwidth analog signals, which are then converted into digital signals in multiple low sample rate SAR ADCs working in parallel. The resulting digital signals may optionally be multiplexed or interleaved back to a single full sample rate digital signal.

Time Interleaved ADCs, and especially Time Interleaved ADCs with SAR ADCs are a preferred type of ADCs for converting wide-band signals of moderate signal-to-noise ratio, in applications that can tolerate interleaving spurs, moderate latency and extra system complexity. They benefit from high performance efficiency of SAR ADCs and significantly increase their moderate conversion rates by de-interleaving the input analog signal. De-interleaving ratios of 2x to 256x have been demonstrated and are limited by the overhead of time-interleaving implementation, size, and frequency spurs location. As the power consumption of a TI ADC scales proportionally to the number of SAR ADCs, interleaving is often a more power efficient method of increasing the ADC sample rate than boosting the sample rate of a single ADC.

TI ADCs suffer from a number of issues not present in non-interleaved ADCs that reduce the effectiveness of this technique. They are primarily related to sampling and distribution of input signals, and distribution of reference signals.
A typical TI SAR ADC comprises an analog de-multiplexer followed by an array of SAR sub-ADCs, where all SAR ADCs operate with the same reference signals, usually reference voltages. Low resolution ADCs typically use a low-impedance passive reference voltage distribution network driven by a low output impedance reference voltage buffer. Another commonly used solution uses dedicated reference voltage buffers for each sub ADC.

A SAR ADC of a composite ADC may be implemented in a number of ways, with one or more reference signals, with different numbers of bits resolved per conversion step, with or without redundancy, with a capacitive or resistive DAC, with top or bottom plate capacitor sampling, with an input voltage or an input current as input signal.

In TI ADCs with SAR (sub-)ADCs, static reference errors directly translate into ADC gain errors. Different SAR ADC signal gains produce a repetitive amplitude modulation pattern that causes a portion of the input signal to be mirrored around interleaving spurs. When multiple reference signals are used in SAR sub-ADCs, reference errors may also produce nonlinear distortion components and degrade total harmonic distortion (THD). An amplitude of reference errors should never exceed the redundancy embed in the SAR ADC, if it does the performance drops sharply because of large INL/DNL errors that are not corrected by the redundant step(s).

Dynamic reference errors, originating from either noise or interference between SAR sub-ADCs, cause similar issues to the ones described above. However, due to the stochastic nature of these errors the performance impairments are better approximated as a higher noise floor rather than discrete frequency spurs.

The most important source of reference voltage errors is the DAC itself, which produces significant disturbances when switching MSB bits.

In a SAR ADC, in the MSB extraction step, the switching capacitance is larger than MSB-1 stage and so on. Hence, the disturbance on the reference starts with big steps and goes down as the conversion proceeds to an end. In a single SAR ADC MSB steps are the most important phase of the conversion where decisions can go wrong. In high resolution SAR ADCs this issue is resolved by inserting one or more redundant steps to the conversion procedure. In low
resolution SAR ADCs it may be sufficient to lower the impedance of the reference voltage buffer.

In addition to the above self-interference issue, TI SAR ADCs also suffer from reference errors caused by other Sub-ADCs in the array. Redundancy alone cannot resolve them because these errors may occur at any phase of conversion. Large reference errors produced by SAR ADCs converting MSB bits may affect SAR ADCs converting LSB bits, which cannot be protected by redundancy.

State of the art TI ADC designs usually cope with this issue by using one of the following techniques:

1. Making sure that the output impedance of the reference generator is low enough (both resistive and reactive) that the biggest error caused by the disturbance on the reference is smaller than the LSB of the ADC. This requires a huge power and area consumption sacrifice.

2. Duplicating reference buffers and therefore blocking interference propagation between sub-ADCs. As a result, each sub-ADC operates independently like a stand-alone SAR ADC. This requires extra power and die area for multiple reference buffers and decoupling capacitors, and more importantly, it results in static and dynamic reference voltage mismatches between Sub-ADCs that require precise calibration of reference voltages.

3. Making SAR steps synchronous and slow enough so that reference voltages can recover before the end of each conversion step. The main drawback is that the speed of this solution is very low, effectively removing any performance gains obtained by time interleaving.
SUMMARY OF THE INVENTION

The objective of the present invention is to provide a composite analog-to-digital converter, wherein the composite analog-to-digital converter overcomes one or more of the above-mentioned problems of the prior art. In particular, an objective of the present invention can include improving a conversion accuracy of a composite ADC.

A first aspect of the invention provides a composite analog-to-digital converter, comprising a plurality of successive approximation register, SAR, ADCs, each of which comprises one or more significant conversion capacitors, each of which is dynamically connectable by one or more first reference switches to a first plurality of reference voltages, wherein the first plurality of reference voltages has a common first nominal voltage.

It is understood that in addition to the above-mentioned SAR ADCs that comprise one or more significant conversion capacitors, the composite ADC may comprise further SAR ADCs that are configured differently and e.g. do not comprise significant conversion capacitors.

Also, it is understood that some of the capacitors of some of the SAR ADCs may not be dynamically connectable.

A composite ADC is an ADC that comprises more than one internal ADCs, e.g. successive approximation register, SAR, ADCs.

The composite ADC of the first aspect comprises one or more significant conversion capacitors. In embodiments of the invention, the composite ADC further comprises least-significant conversion capacitors. Preferably, the least-significant conversion capacitors are arranged differently than the significant conversion capacitors. For example, the least-significant conversion capacitors can be dynamically connectable to only one of the reference voltages of the first plurality of reference voltages.

In embodiments of the invention, a conversion capacitor can be any component that has a capacitive characteristic.

Dynamically connectable refers to a connection that is dynamically changed during an operation of the composite ADC. For example, dynamical connection can be implemented by
changing a state of the one or more reference switches based on a phase of conversion of a SARADC.

The composite ADC of the first aspect makes it possible that conversion capacitors are dynamically connected to different reference voltages such that noise from switching a first conversion capacitor does not affect the reference voltage of another conversion capacitor. In particular, the dynamic connections can be performed such that conversion capacitors performing higher-significance conversions do not affect conversion capacitors performing lower-significance conversions.

In a first implementation of the composite analog-to-digital converter according to the first aspect, each of the significant conversion capacitors is dynamically connectable by one or more second reference switches to a second plurality of reference voltages, wherein the second plurality of reference voltages has a common second nominal voltage.

The first and second reference switches can be the same physical switches. For example, a reference switch can be configured to connect a conversion capacitor to one of the first plurality of reference voltages or one of the second plurality of reference voltages. In other embodiments, first and second reference switches can be separate switches.

In a preferred embodiment, the first plurality of reference voltages are positive voltages compared to a ground level of the composite ADC and the second plurality of reference voltages are negative compared to a ground level of the composite ADC. Ground can also be referred to as zero reference voltage. In some embodiments of the invention, the first and/or second plurality of reference voltages have a zero reference voltage, i.e. are at ground level.

In a further embodiment, the conversion capacitors comprise also a third plurality of reference voltages and/or further pluralities of reference voltages. These third and further pluralities of reference voltages can have different nominal voltages.

In a second implementation of the composite analog-to-digital converter according to the first aspect, at least one of the plurality of SAR ADCs further comprises one or more least-significant conversion capacitors which are dynamically connectable to only one from the first plurality of reference voltages and/or to only one from the second plurality of reference voltages.
Since the least-significant conversion capacitors are dynamically connectable to only one from the first plurality of reference voltages and/or to only one from the second plurality of reference voltages, these switches can be simpler than the switches that dynamically connect the significant conversion capacitors. Therefore, the composite ADC of the second implementation has the advantage that an overall complexity of the SAR ADC and the composite ADC can be reduced.

The least-significant conversion capacitors may include one or more least significant redundant step conversion capacitors.

In a third implementation of the composite analog-to-digital converter according to the first aspect, the first and/or the second plurality of reference voltages comprises \( m \) reference voltages and the one or more significant and one or more least-significant conversion capacitors comprise \( m \) groups of conversion capacitors, wherein the \( m \) groups of conversion capacitors are sorted in order of increasing significance and wherein an \( n \)-th group of conversion capacitors is dynamically connectable to the first \( n \) of the \( m \) reference voltages, wherein preferably the \( m \) reference voltages are sorted in order of increasing fluctuation levels.

Having the conversion capacitors in groups grouped in order of increasing conversion significance has the advantage and assigning corresponding reference voltages to the groups of conversion capacitors has the advantage that noise from high-significance conversion capacitors (which may have a very high capacitance) of other SAR ADCs does not propagate to low-significance conversion capacitors of the SAR ADCs performing its LSB conversion (which may have a very low capacitance and thus a high sensitivity to noise propagated through the reference voltage).

In a fourth implementation of the composite analog-to-digital converter according to the first aspect, the composite analog-to-digital converter further comprises a controller which is configured to switch the first and/or the second reference switches of at least one of the SAR ADCs such that during a phase of conversion corresponding to a \( p \)-th group of the conversion capacitors, one or more switched conversion capacitors that are switched to one of the reference voltages of the first or the second plurality of reference voltages are connected to a \( p \)-th reference voltage of the first or the second plurality of reference voltages.
This has the advantage that the \( p \)-th group of conversion capacitors is only dynamically connected to the \( p \)-th reference voltage, which corresponds to the significance level of the \( p \)-th group. Thus, a voltage fluctuation caused by the conversion of a high-significance conversion capacitor of other SAR ADCs does not propagate to a low-significance conversion capacitor of the SAR ADCs performing its LSB conversion.

Furthermore, the controller can be configured to switch the first and/or the second reference switches of at least one of the SAR ADCs such that at any phase of conversion all reference-connected conversion capacitors that are dynamically connected to one of the reference voltages of the first or second plurality of reference voltages are dynamically connected to the same reference voltage of the first or second plurality of reference voltages.

This has the advantage that there is no noise propagation between different reference voltages.

In a fifth implementation of the composite analog-to-digital converter according to the first aspect, a subset of the conversion capacitors of at least one SAR ADC are dynamically connectable to a first voltage reference line which is switchable by a first line switch between the first plurality of reference voltages and/or a second voltage reference line which is switchable by a second line switch between the second plurality of reference voltages.

Having a reference line which is switchable between the first or second plurality of reference voltages has the advantage that a reference switch can be dynamically connectable only to the reference line instead of the plurality of reference switches. Thus, a further switch further for switching the reference line is required, but an overall complexity of the circuitry can still be reduced.

In a sixth implementation of the composite analog-to-digital converter according to the first aspect, at least one SAR ADC comprises at least one one-to-many switch which is configured to dynamically connect a terminal of at least one of the conversion capacitors to:

- an input signal, ground, and the first and/or second voltage reference line; or
- ground and the first and/or second voltage reference line.
In a seventh implementation of the composite analog-to-digital converter according to the first aspect further comprises at least one one-to-many switch which is configured to dynamically connect a terminal of one of the conversion capacitors to:

- an input signal, ground and the first plurality of reference voltages and/or the second plurality of reference voltages, or

- ground and the first plurality of reference voltages and/or the second plurality of reference voltages.

Having one-to-many switches which can connect a terminal of the conversion capacitor to the plurality of reference voltages has - compared e.g. to an implementation with a switchable voltage reference line - the advantage that there is only one switch between a conversion capacitor and its reference line. This reduces a series resistance of the reference switches and thus reduces the settling time.

In an eighth implementation of the composite analog-to-digital converter according to the first aspect, the composite ADC further comprises a composite controller configured to set the first and/or the second reference switches to a different one of the plurality of reference voltages based on a phase of conversion.

In a ninth implementation of the composite analog-to-digital converter according to the first aspect, at least one of the plurality of SAR ADCs further comprises a SAR controller which is configured to connect an active one of the plurality of conversion capacitors to a selected reference voltage, which is selected from the plurality of reference voltages based on a significance of the active conversion capacitor and/or based on a phase of the conversion.

An active conversion capacitor is a capacitor that is being switched in the current conversion phase.

In a tenth implementation of the composite analog-to-digital converter according to the first aspect, the reference voltages of the first and/or second plurality of reference voltages are sorted in order of increasing fluctuation levels, wherein the conversion capacitors include one or more redundant conversion capacitors and wherein the SAR controller is configured to select a quieter one of the first and/or second plurality of reference voltages for a redundant step conversion corresponding to the one or more redundant conversion capacitors.
The different fluctuation levels of the different reference voltages are a result of the different connections to different conversion capacitors, which typically have different capacitances and therefore cause different levels of voltage fluctuation. Assigning the different reference voltages based on their fluctuation levels has the advantage that e.g. lower-significance conversion capacitors, which may be more sensitive to voltage fluctuations are not connected to reference voltages with higher fluctuation levels.

**BRIEF DESCRIPTION OF THE DRAWINGS**

To illustrate the technical features of embodiments of the present invention more clearly, the accompanying drawings provided for describing the embodiments are introduced briefly in the following. The accompanying drawings in the following description are merely some embodiments of the present invention, but modifications on these embodiments are possible without departing from the scope of the present invention as defined in the claims.

FIG. 1 is a simplified diagram illustrating a conventional time-interleaved composite ADC,

FIG. 2 is a simplified diagram illustrating a composite ADC in accordance with an embodiment of the present invention,

FIG. 3 is a circuit diagram of a SAR ADC for use in a composite ADC with a first and second voltage reference line in accordance with a further embodiment of the present invention,

FIG. 4 is a circuit diagram of a SAR ADC for use in a composite ADC in accordance with a further embodiment of the present invention, wherein the SAR ADC comprises one-to-many reference switches,

FIG. 5 is a circuit diagram of a SAR ADC for use in a composite ADC in accordance with a further embodiment of the present invention, wherein the SAR ADC uses a first and second plurality of reference voltages,
is a circuit diagram of a SAR ADC for use in a composite ADC in accordance with a further embodiment of the present invention, wherein the SAR ADC uses a first and second plurality of reference voltages and a reduced number of reference switches,

is a circuit diagram of a SAR ADC for use in a composite ADC in accordance with a further embodiment of the present invention, wherein the SAR ADC uses a first and second plurality of reference voltages and one-to-many reference switches,

is a circuit diagram of a SAR ADC for use in a composite ADC in accordance with a further embodiment of the present invention, wherein the SAR ADC is configured to use a first and second plurality of reference voltages, which each comprise three reference voltages,

is a circuit diagram of a SAR ADC for use in a composite ADC in accordance with a further embodiment of the present invention, wherein the SAR ADC is configured to use a first and second plurality of reference voltages, which each comprise three reference voltages and wherein reference switches are connected to a plurality of voltage reference lines,

is a circuit diagram of a SAR ADC for use in a composite ADC in accordance with a further embodiment of the present invention, wherein the SAR ADC is configured to use a first and second plurality of reference voltages, wherein the reference switches are designed as one-to-many switches,

is a timing diagram of a SAR ADC for use in a composite ADC in accordance with a further embodiment of the present invention,

is a circuit diagram of a SAR ADC for use in a composite ADC in accordance with a further embodiment of the present invention, wherein the SAR ADC is configured to use a first and a second plurality of reference voltages and top-plate sampling,
FIG. 13 is a circuit diagram of a SAR ADC for use in a composite ADC in accordance with a further embodiment of the present invention, wherein the SAR ADC uses a first and a second plurality of reference voltages and top-plate sampling and wherein the composite ADC is configured to convert 2 bits per conversion step.

Detailed Description of the Embodiments

The foregoing descriptions are only implementation manners of the present invention, the scope of the present invention is not limited to this. Any variations or replacements can be easily made through person skilled in the art. Therefore, the protection scope of the present invention should be subject to the protection scope of the attached claims.

FIG. 1 illustrates a conventional time-interleaved composite ADC 100 which comprises a T/H circuit 102, an analog de-multiplexer 106 that is driven by a clocking unit 104 and followed by an array of SAR sub-ADCs 108a to 108e, where all sub-ADCs operate with the same reference voltages Vref. The signals output by the sub-ADCs 108a to 108e are multiplexed by the multiplexer 110 to obtain an output signal D_{out}.

As indicated in FIG. 1, the switching of the SAR ADCs 106a, 106b that are currently performing a most significant bits (MSBs) conversion causes an interference on the voltage reference Vref. This interference passes to the SAR ADCs 106d, 106e that are currently performing a least-significant bits (LSBs) conversion. The accuracy of the LSB conversions is adversely affected by the interference from the SAR ADCs 106a, 106b performing the MSB conversions.

FIG. 2 illustrates a SAR ADC 200 for use in a composite ADC in accordance with an embodiment of the invention. The SAR ADC 200 comprises a T/H circuit 202, a clocking unit 204, a demultiplexer 206 and a multiplexer 210 that can be configured similar to the corresponding units from the composite ADC shown in FIG. 1. Instead of one reference voltage Vref, the composite ADC 200 of FIG. 2 comprises a plurality of reference voltages, namely a first reference voltage V_{ref_quiet} and a second reference voltage V_{ref_noisy}.
FIG. 2 illustrates a snapshot of the conversion process - a moment where a first group of SAR ADCs 208a, 208b are currently performing a conversion of the most-significant bit (MSB) and the second-most significant bit (MSB-1). A further SAR ADC 208c is the last SAR ADC in the row of SAR ADC before the SAR ADC 208d that is currently performing a redundant step conversion. A second group of SAR ADCs 208e, 208f is currently performing a second-least significant bit (LSB+1) and a least-significant bit (LSB) conversion.

The reference switches are controlled such that the active conversion capacitors of the SAR ADCs 208a, 208b and 208c are dynamically connected to \( V_{\text{ref noisy}} \) and the active conversion capacitors of SAR ADCs 208d, 208e, 208f are dynamically connected to \( V_{\text{ref quiet}} \). Thus, no interference from the SAR ADCs currently performing more significant conversions is passed to the SAR ADCs currently performing the less significant conversions.

In general, the controller can be configured such that \( V_{\text{ref noisy}} \) is only used during MSB conversion steps before the first redundant step. \( V_{\text{ref quiet}} \) is only used during LSB conversion steps starting from the last redundant step. The switching between references also updates the output of the DAC for previously converted bits.

FIG. 3 is a circuit diagram of a SAR ADC for use in a composite ADC according to a further embodiment of the present invention. The composite ADC 300 comprises a MSB conversion section 302, a redundant step conversion section 304, a LSB conversion section 306, a comparator 310, a SAR Digital Logic 310. \( C_p \) represents the parasitic capacitance between a positive input 310a of the comparator 310 and ground, and between a negative input 310b and ground.

Furthermore, the SAR ADC 300 comprises input lines for a plurality of reference voltages which consists of a first reference voltage \( V_{\text{ref quiet}} \) and a second reference voltage \( V_{\text{ref noisy}} \). The SAR ADC 300 also comprises input lines for a control signal \( SEL_{\text{f noisy}} \), for ground, a positive and a negative input signal \( V_{i_{\text{in+}}} \) and \( V_{i_{\text{in-}}} \) and a common voltage \( VC_{\text{MM}} \). The composite ADC 300 comprises an upper line switch LS and a lower line switch LS’. The upper line switch LS is configured to switch an upper reference line 320a between \( V_{\text{ref noisy}} \) and \( V_{\text{ref quiet}} \) and the lower line switch LS’ is configured to switch a lower reference line 320b between \( V_{\text{ref noisy}} \) and \( V_{\text{ref quiet}} \). Both line switches are controlled by the same control signal \( SEL_{\text{Ref noisy}} \).
In other embodiments of the invention, the upper line switch LS and the lower line switch LS’ can be replaced by one common line switch.

Each of the sections 302, 304, 306 comprises an upper conversion part, which is connected to the positive input 310a of the comparator 310, and a lower conversion part, which is connected to the negative input 310b of the comparator 310.

The MSB conversion section 302 comprises in its upper conversion part conversion capacitors C_{n-i} to C_{r+i} which are connected with their upper terminal to upper reference switches S_{n-i} to S_{r+i} and to the positive input 310a of the comparator 310 with their lower terminals. In its lower conversion part, the MSB conversion section 302 comprises conversion capacitors C’_{n-i} to C’_{r+i} which are connected with their lower terminal to lower reference switches S’_{n-i} to S’_{r+i} and to the negative input 310b of the comparator 310 with their upper terminals.

The first reference voltage Vref_{qs,quiet} and the second reference voltage Vref_{n,isy} are isolated references but with the same nominal value. Averaged over time they have the same voltage or almost the same voltage, however their level of fluctuation over the common nominal voltage is different. Vref_{n,isy} will have a higher fluctuation than Vref_{qs,quiet} because it is used (only) during MSB comparison steps which involve the conversion capacitors with higher capacitance values. Due to the switching of bigger capacitance, the MSBs reference will have high disturbance and ripple, hence called Vrefnoisy. The second reference voltage Vrefquiet is used during the LSB conversion steps. The reference voltage Vrefquiet will be quieter due to smaller size capacitance switching, hence the name Vrefquiet. Note that in an ideal situation where there is no switching, \( Vref_{noisy} = Vref_{quiet} \).

The conversion capacitors \( C_0 \) to \( C_r \) can be seen as forming a first group of conversion capacitors and the conversion capacitors \( C_{r+i} \) to \( C_{n-i} \) can be seen as forming a second group of conversion capacitors. As outlined above, the first group of conversion capacitors is dynamically connectable only to the first reference voltage Vrefquiet. The second group of conversion capacitors is dynamically connectable to the first reference voltage Vrefquiet and the second reference voltage Vrefnoisy.

A composite ADC can comprise several SAR ADCs as shown in FIG. 3. Although all SAR ADCs share the same Vrefnoisy reference, they are less sensitive to the noise injected into it.
MSB conversion steps that use this reference are followed by a redundant step that removes any DAC errors smaller than the redundancy margin, including ones that originated from reference disturbance. At the redundant step, the second group of conversion capacitors are switched to the quiet reference \( V_{\text{ref quiet}} \) and disconnected from \( V_{\text{ref noisy}} \). In general, there may be more \( V_{\text{ref}} \) references with intermediate noise specifications used, each followed by a redundant step and switch to progressively quieter references, each with lower noise but also lower redundancy margin. The final reference \( V_{\text{ref quiet}} \) has no redundancy and therefore the ADC is exposed to interference from other SAR ADCs. However, at this stage, the worst-case noise injected into the reference is many times smaller than the one originating from MSB conversion capacitors switching, so it is much easier to maintain it at sub-LSB level. For example, if the redundant step and thus switch from \( V_{\text{ref noisy}} \) to \( V_{\text{ref quiet}} \) occurs after six binary conversion steps, the amount of charge injected into \( V_{\text{ref quiet}} \) is 64x lower than the charge injected into \( V_{\text{ref noisy}} \), corresponding to proportionally lower voltage fluctuation.

The redundant step also covers any static and dynamic mismatches between \( V_{\text{ref noisy}} \) and \( V_{\text{ref quiet}} \), so in most cases, unless the designer chooses to further optimize the design, reference calibration is not necessary.

FIG. 4 is a simplified circuit diagram illustrating a SAR ADC 400 for use in a composite ADC in accordance with a further embodiment of the invention, wherein the SAR ADC 400 uses parallel bottom plate switches \( S_{n-1} \) to \( S_0 \) and \( S'_{n-1} \) to \( S'_0 \) to select the reference voltage instead of an extra series switch used in the SAR ADC of FIG. 3. This approach reduces a series resistance of the reference switches and thus reduces the settling time. This technique can involve a higher complexity of the composite ADC and digital circuits driving it.

FIG. 5 is a circuit diagram of a SAR ADC 500 for use in a composite ADC, wherein the SAR ADC uses a first and a second plurality of reference voltages. The setup of the SAR ADC of FIG. 5 is similar to the setup of the SAR ADC shown in FIG. 3, however, it uses a first plurality of reference voltages, \( V_{\text{ref noisy}} \) and \( V_{\text{ref quiet}} \), and a second plurality of reference voltages, \( V_{\text{ref noisy}} \) and \( V_{\text{ref quiet}} \). \( V_{\text{ref noisy}} \) and \( V_{\text{ref quiet}} \) have a same first nominal voltage and \( V_{\text{ref noisy}} \) and \( V_{\text{ref quiet}} \) have a same second nominal voltage. In the embodiment shown in FIG. 5, first and second nominal voltage have the same absolute value, but the first nominal voltage is positive and the second nominal voltage is negative.
The upper conversion part comprises a first upper line switch LSi and a second upper line switch LS2. The first upper line switch LSi is configured to dynamically switch a first reference line Vref+ mux between Vrefnoisy and Vrefquiet. The second upper line switch LS2 is configured to dynamically switch a second reference line Vref+ mux between Vref+qisy and Vrefnoisy.

The upper reference switches S'n;i to S'o are configured such that the conversion capacitors C'n;i to C'o are dynamically connectable to Vm+. Vref+ mux, Vref+ mux or ground. Similarly, the lower reference switches S'n;i to S'o are configured such that the conversion capacitors C'n;i to C'o are dynamically connectable to Vm-, Vref+ mux, Vref+ mux or ground.

Thus, ground can be seen as serving as a third reference with zero differential voltage and it can use any DC voltage. There may be embodiments wherein ground is removed and only first and second plurality of reference voltages are used. There can also be further reference lines. Isolation between the different reference voltage domains should be maintained.

Reference switching should be followed or performed together with a redundant step(s) to correct any errors caused by differences between Vrefnoisy and Vrefquiet.

FIG. 6 is a circuit diagram of a SAR ADC 600 for use in a composite ADC, wherein the SAR ADC uses a first and a second plurality of reference voltages and a reduced number of reference switches. The SAR ADC 600 of FIG. 6 is configured similar to the SAR ADC 500 shown in FIG. 5, however, the LSB switches S'r;i to S'o and S'r;i to S'o are connected directly to Vrefquiet and Vref+quiet. This has the advantage that simpler switches with few connections can be used for the LSB conversion part.

FIG. 7 is a circuit diagram of a SAR ADC 700 for use in a composite ADC, wherein the SAR ADC uses a first and a second plurality of reference voltages and one-to-many reference switches. The one-to-many switches are directly connected to the different reference voltages of the first and the second plurality of reference voltages. Thus, no line switches as shown in FIG. 5 and FIG. 6 are required. The reference switches S'r;i to S'o and S'r;i to S'o are "flattened" so that each switch directly selects a required reference line. Single series switch results in faster settling times at the cost of extra decoding in SAR Digital Logic.
FIG. 8 is a circuit diagram of a SAR ADC 800 for use in a composite ADC, wherein the SAR ADC is configured to use a first and second plurality of reference voltages. The setup is similar to the SAR ADC 500 shown in FIG. 5, however each plurality of reference voltages comprises three reference voltages. During switching of the MSB conversion capacitors $S_{n-1}$ to $S_{n+i}$, the MSB conversion capacitors are dynamically connected to the third reference voltage $V_{ref+noisy}$ of the first plurality of reference voltages and to the third reference voltage $V_{ref+noisy}$ of the second plurality of reference voltages. During switching of the intermediate significant bit, ISB, switches $S_{1}$ to $S_{2+i}$, the ISB conversion capacitors $C_{1}$ to $C_{2+i}$ are dynamically connected to the second reference voltage $V_{ref+middle}$ of the first plurality of reference voltages or to the second reference voltage $V_{ref+middle}$ of the second plurality of reference voltages. During switching of the LSB conversion capacitors $C_{2}$ to $C_{0}$, the LSB conversion capacitors are dynamically connected to the first reference voltage $V_{ref+q_{i}}$ of the first plurality of reference voltages or the first reference voltage $V_{ref+q_{i}}$ of the second plurality of reference voltages.

Preferably, the first redundant step conversion capacitor $C_{1}$ is dynamically connected to the second reference voltage and the second redundant conversion capacitor $C_{2}$ is dynamically connected to the first reference voltage. This allows having a lower fluctuation level and thus higher accuracy during the redundant step conversion.

The lower switches $S'_{n-1}$ to $S'_{0}$ and the lower conversion capacitors $C'_{n-1}$ to $C'_{0}$ are switched correspondingly to the upper switches and conversion capacitors.

FIG. 9 is a circuit diagram of a SAR ADC 900 for use in a composite ADC, wherein the SAR ADC is configured to use a first and second plurality of reference voltages, which each comprise three reference voltages and wherein the reference switches are connected to a plurality of voltage reference lines. The setup of the SAR ADC 900 essentially corresponds to the SAR ADC 600 shown in FIG. 6, however, the first and second plurality of reference voltages now comprise three reference voltages instead of two.

The MSB conversion capacitors $C_{n-1}$ to $G_{i}$ are connected to switches $S_{n-1}$ to $S_{i}$. $S_{n-1}$ to $S_{i}$ have wired connections to a first voltage reference line $V_{max+MSB}$ which has a wired connection to a first line switch $LS_{1}$. The first line switch $LS_{1}$ can switch the first voltage reference line $V_{max+MSB}$ between the first plurality of reference voltages, i.e. between $V_{ref+noisy}$, $V_{ref+middle}$ and $V_{ref+q_{i}}$. Similarly, $S_{n-1}$ to $S_{i}$ have wired connections to a second voltage
reference line \( V_{\text{ref}+\text{MSB}} \) which has a wired connection to a second line switch \( \text{LS}_2 \). The second line switch can switch the second voltage reference line between the second plurality of reference voltages.

5 The first redundant step conversion capacitor \( C_{r1} \) and the ISB conversion capacitors \( \text{Gi-i} \) to \( C_{r2+i} \) are connected to switches \( S_{r1} \) to \( S_{r2+i} \). \( S_{r1} \) to \( S_{r2+i} \) have wired connections to a further first voltage reference line \( V_{\text{ref}-\text{MSB}} \) which is connected to a further first line switch \( \text{LS}_1 \). The further first line switch \( \text{LS}_1 \) can switch the further first voltage reference line \( V_{\text{ref}-\text{MSB}} \) between the second and the first plurality of reference voltages, i.e. between \( \text{Vref middle} \) and \( \text{Vref LSB} \). Similarly, \( S_{r1} \) to \( S_{r2+i} \) are connected to a further second voltage reference line \( V_{\text{ref}-\text{MSB}} \) which is connected to a further second line switch \( \text{LS}_2 \). The second line switch can switch the further second voltage reference line \( V_{\text{ref}-\text{MSB}} \) between the second and the first reference voltage of the second plurality of reference voltages, i.e. between \( \text{Vref+middle} \) and \( \text{Vref+LSB} \).

10 As shown in FIG. 9, a corresponding setup exists for the conversion capacitors connected to the negative input of the comparator.

FIG. 10 is a circuit diagram of a SAR ADC 1000 for use in a composite ADC, wherein the SAR ADC is configured to use a first and second plurality of reference voltages, wherein the reference switches are designed as one-to-many switches. The setup of the SAR ADC 1000 of FIG. 10 essential corresponds to the SAR ADC 700 of FIG. 7, however with the first and second plurality of reference voltages comprising three reference voltages instead of two. As can be seen in FIG. 10, the MSB conversion capacitors are dynamically connectable to the first, second and third reference voltage of the first and second plurality of reference voltages. The first redundant step conversion capacitor and the ISB conversion capacitors are dynamically connectable to the first and second reference voltage of the first and second plurality of reference voltages. The second redundant step conversion capacitor and the LSB conversion capacitors are dynamically connectable only to the first reference voltage of the plurality of reference voltages.

25 FIG. 11 is a timing diagram of a SAR ADC for use in a composite ADC. The timing diagram shows the switch states during a single conversion cycle of a SAR ADC. The diagram corresponds to bottom-plate sampling in a setup with two pluralities of reference voltages.
The switching is performed in three conversion stages:

1) In MSB conversion steps only ground and \( V_{\text{ref+ noisy}} \) and \( V_{\text{ref-noisy}} \) references are used. Fluctuations from the switching of conversion capacitors are therefore injected only into \( V_{\text{ref+ noisy}} \) and \( V_{\text{ref-noisy}} \).

2) In ISB conversion steps only ground and \( V_{\text{ref+ middle}} \) \( V_{\text{ref-middle}} \) reference voltage are used. Reference switches previously connected to \( V_{\text{ref+ noisy}} \) and \( V_{\text{ref-noisy}} \) are dynamically re-routed to \( V_{\text{ref+ middle}} \) \( V_{\text{ref-middle}} \) Noise (of comparatively lower amplitude) is injected only into \( V_{\text{ref+ middle}} \) \( V_{\text{ref-middle}} \).

3) In LSB conversion steps only ground and \( V_{\text{ref+ quiet}} \) \( V_{\text{ref-quiet}} \) references are used. Reference switches that were previously connected to \( V_{\text{ref+ middle}} \) \( V_{\text{ref-middle}} \) are dynamically re-routed to \( V_{\text{ref+ quiet}} \) \( V_{\text{ref-quiet}} \) Noise (of even lower amplitude) is injected only into \( V_{\text{ref+ quiet}} \) \( V_{\text{ref-quiet}} \).

This implies that MSB reference switches have to select one of \( V_{\text{ref+ noisy}} \) \( V_{\text{ref-noisy}} \) \( V_{\text{ref+ middle}} \) \( V_{\text{ref-middle}} \) \( V_{\text{ref+ quiet}} \) \( V_{\text{ref-quiet}} \) \( V_{\text{ref+ quiet}} \) \( V_{\text{ref-quiet}} \) ground and optionally \( V_{m} \) while ISB switches need \( V_{\text{ref+ middle}} \) \( V_{\text{ref-middle}} \) \( V_{\text{ref+ quiet}} \) \( V_{\text{ref-quiet}} \) \( V_{\text{ref+ quiet}} \) \( V_{\text{ref-quiet}} \) ground and optionally \( V_{m} \) and LSB switches only need \( V_{\text{ref+ quiet}} \) \( V_{\text{ref-quiet}} \) \( V_{\text{ref+ quiet}} \) \( V_{\text{ref-quiet}} \) \( V_{\text{ref+ quiet}} \) \( V_{\text{ref-quiet}} \) ground and optionally \( V_{m} \).

The reference voltage fluctuations shown are not to scale. In practical implementations \( V_{\text{ref+ noisy}} \) \( V_{\text{ref-noisy}} \) ripple is at around 1% of \( V_{\text{ref+ noisy}} \) \( V_{\text{ref-noisy}} \) nominal value. Each consecutive domain can reduce the noise by a factor of 10–100x.

FIG. 11 is shown with a variant of a monotonic conversion algorithm (preferred for high speed, high resolution ADCs) but many other algorithms, including classic binary successive approximation algorithm, can be used as well.

One or more redundant steps should be performed after switching the references to correct any errors caused by reference voltage mismatches. Redundancy can be spread across conversion steps.
The ground DC voltage may vary. For example $V(\text{Ground}) = V(\text{Vref-noisy})$ is a valid solution.

A ground voltage equal to $(V(\text{Vref+ noisy}) + V(\text{Vref-noisy}))/2$ is preferred because the common-voltage is maintained at a constant level during conversion.

FIG. 12 is a circuit diagram of a SAR ADC 1200 for use in a composite ADC, wherein the SAR ADC is configured to use a first and a second plurality of reference voltages and top-plate sampling. In top-plate sampling, the conversion capacitors $C_0$ to $C_n$ are connected with one terminal to $\text{Vin}+$ and with another terminal to the reference switches $S_0$ to $S_n$. Correspondingly, the conversion capacitors $C'_0$ to $C'_n$ are connected with one terminal to $\text{Vin}-$ and with another terminal to the switches $S_0$ to $S_n$.

FIG. 13 is a circuit diagram of a SAR ADC 1300 for use in a composite ADC, wherein the SAR ADC uses a first and a second plurality of reference voltages and top-plate sampling and wherein the composite ADC is configured to convert 2 bits per conversion step. For two bit per step conversion, the comparator outputs have to indicate one of four ($2^2$) signal levels. This means the three threshold voltages, and therefore three DACs and three comparators are needed. The SAR ADC 1300 thus comprises three DACs 1310, 1312, 1314, which are connected to three comparators 1320, 1322, 1324, which provide their outputs to the SAR Digital Logic 1330.

The three DACs 1310, 1312, 1314 can be implemented with multiple reference voltage domains using one of the previously shown techniques. To produce three different offsets, an offset signal of two out of three DACs or comparators has to be dynamically varied by SAR Digital Logic. Different methods of adding the offset can be used.
CLAIMS

1. A composite analog-to-digital converter, ADC, (200) comprising a plurality of successive approximation registers, SAR ADCs, (300, 400, 500, 600, 700, 800, 900, 1000, 1200, 1300) each of which comprises one or more significant conversion capacitors (Co, ... , Cn-i, C’0, ... , C’n-i), each of which is dynamically connectable by one or more first reference switches (So, ... , Sn+i, S’0, ... , S’n-i) to a first plurality of reference voltages (Vrefnoisy, Vref+noisy, Vref+middle, Vref+quiet), wherein the first plurality of reference voltages has a common first nominal voltage.

2. The composite ADC of claim 1, wherein each of the significant conversion capacitors (Co, ... , Cn-i, C’0, ... , C’n-i) is dynamically connectable by one or more second reference switches (So, ... , Sn+i, S’0, ... , S’n-i) to a second plurality of reference voltages (Vrefnoisy, Vref middle, Vrefquiet), wherein the second plurality of reference voltages has a common second nominal voltage.

3. The composite ADC of one of the previous claims, wherein at least one of the plurality of SAR ADCs further comprises one or more least-significant conversion capacitors (Co, ... , C) which are dynamically connectable to only one from the first plurality of reference voltages (Vrefquiet, Vref+quiet) and/or to only one from the second plurality of reference voltages (Vrefquiet).

4. The composite ADC of claim 3, wherein the first and/or the second plurality of reference voltages comprises m reference voltages and the one or more significant and one or more least-significant conversion capacitors comprise m groups of conversion capacitors, wherein the m groups of conversion capacitors are sorted in order of increasing significance and wherein an n-th group of conversion capacitors is dynamically connectable to the first n of the m reference voltages, wherein preferably the m reference voltages are sorted in order of increasing fluctuation levels.

5. The composite ADC of one of the previous claims, further comprising a controller which is configured to switch the first and/or the second reference switches (So, ... , Sn+i, S’0, ... , S vi) of at least one of the SAR ADCs such that:
- during a phase of conversion corresponding to a \( p \)-th group of the conversion capacitors, one or more switched conversion capacitors that are switched to one of the reference voltages of the first or second plurality of reference voltages are connected to a \( p \)-th reference voltage of the first or second plurality of reference voltages, and/or

- at any phase of conversion all reference-connected conversion capacitors that are dynamically connected to one of the reference voltages of the first or second plurality of reference voltages are dynamically connected to the same reference voltage of the first or second plurality of reference voltages.

6. The composite ADC of one of the previous claims, wherein a subset of the conversion capacitors of at least one SAR ADC are dynamically connectable to a first voltage reference line (320a, \( V_{ref+mux} \)) which is switchable by a first line switch (LSi) between the first plurality of reference voltages (\( V_{ref_{noisy}}, V_{ref+isy}, V_{ref+middle}, V_{ref+quiet} \)) and/or a second voltage reference line (320b, \( V_{ref_{mux}} \)) which is switchable by a second line switch (LS2) between the second plurality of reference voltages (\( V_{refnoisy}, V_{ref_{middle}}, V_{refquiet} \)).

7. The composite ADC of claim 6, wherein at least one SAR ADC comprises at least one one-to-many switch which is configured to dynamically connect a terminal of at least one of the conversion capacitors to:
   - an input signal (\( V_{in+}, V_{in-} \)), ground, and the first and/or second voltage reference line (320a, 320b, \( V_{ref_{mux}}, V_{ref_{mux}} \)); or
   - ground and the first and/or second voltage reference line (320a, 320b, \( V_{ref+mux}, V_{refimux} \)).

8. The composite ADC of one of the previous claims, comprising at least one one-to-many switch which is configured to dynamically connect a terminal of at least one of the conversion capacitors to:
   - an input signal, ground and the first plurality of reference voltages (\( V_{refnoisy}, V_{ref+noisy}, V_{ref+middle}, V_{ref+quiet} \)), and/or the second plurality of reference voltages (\( V_{refnoisy}, V_{refimiddle}, V_{refquiet} \)), or
ground and the first plurality of reference voltages \((V_{\text{ref} \_\text{isy}}, V_{\text{ref} \_\text{isy}+}, V_{\text{ref} \_\text{middle}}, V_{\text{ref} \_\text{quiet}})\) and/or the second plurality of reference voltages \((V_{\text{ref} \_\text{noisy}}, V_{\text{ref} \_\text{middle}}, V_{\text{ref} \_\text{quiet}})\).

9. The composite ADC of one of the previous claims, further comprising a composite controller configured to set the first and/or the second reference switches to a different one of the plurality of reference voltages based on a phase of conversion.

10. The composite ADC of one of the previous claims, wherein at least one of the plurality of SAR ADCs further comprises a SAR controller which is configured to connect an active one of the plurality of conversion capacitors \((C_0, \ldots C_{n-1}, C'_0, \ldots C'_{n-i})\) to a selected reference voltage, which is selected from the plurality of reference voltages based on a significance of the active conversion capacitor \((C_0, \ldots C_{n-1}, C'_0, \ldots C_{Yi})\) and/or based on a phase of the conversion.

11. The composite ADC of claim 10, wherein the reference voltages of the first and/or second plurality of reference voltages are sorted in order of increasing fluctuation levels, wherein the conversion capacitors include one or more redundant conversion capacitors \((C_r, C_{ri}, C_{r2}, C'r, C'r_i, C'r_2)\) and wherein the SAR controller is configured to select a quieter one of the first and/or second plurality of reference voltages for a redundant step conversion corresponding to the one or more redundant conversion capacitors \((C_r, C_{rl}, C_{r2}, C'r, C'r_{rl}, C'r_{r2})\).
FIG. 1
FIG. 2
FIG. 3
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

INV. H03M1/08
ADD. H03M1/46

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data, COMPENDEX, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
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<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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<tr>
<td>X</td>
<td>US 6 958 722 B1 (JANAKI RAMAN SEETHARAMAN [IN ET AL]) 25 October 2005 (2005-10-25) column 1, line 62 - column 2, line 4; figures 3, 5 column 1, line 9/29 column 9, line 38 - column 10, line 12</td>
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Further documents are listed in the continuation of Box C. See patent family annex.

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