Abstract: A multilevel inverter circuit comprising a positive generator terminal (21) and a negative generator terminal (22) for connecting a generator (1) with a generator voltage, and also comprising an inverter bridge (10) for converting the generator voltage into an AC voltage at a bridge output (19), which can be connected to a power supply grid (9), wherein the inverter bridge (10) is connected to the generator terminals (21, 22) via five terminals (11-15), of which - a first terminal (11) is connected via a step-up converter (2) to the generator terminals (21, 22) for generating a stepped-up positive generator voltage, - a second terminal (12) is connected directly to the positive generator terminal (21), and a fourth terminal (14) is connected directly to the negative generator terminal (22), - a fifth terminal (15) is connected via a step-up converter (3) to the generator terminals (21, 22) for generating a stepped-up negative generator voltage, and - a third terminal (13) is connected to the generator terminals (21, 22) via a capacitive voltage divider (C1/C2, C3/C4), wherein the bridge output (19) is connected - to the fifth terminal (15) via a first series circuit comprising at least two semiconductor switches (S1, S2), - to the second terminal (12) via a second series circuit comprising a diode (D2) and at least two semiconductor switches (S21, S22), - to the third terminal (13) via two parallel series circuits, each consisting of a semiconductor switch (S31, S32) and a diode (D31, D32), - to the fourth terminal (14) via a fourth series circuit comprising a diode (D4) and at least two semiconductor switches (S41, S42), and - to the fifth terminal (15) via a fifth series circuit comprising at least two semiconductor switches (S51, S52).
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MULTILEVEL INVERTER CIRCUIT

The invention relates to a multilevel inverter circuit for feeding electrical energy generated by a generator into a power supply grid.

The term multilevel inverter circuits refers to systems in which a stepping-up DC-DC actuator (also called step-up converter) generates an additional voltage level.

Said additional voltage level is used when the voltage of a voltage source supplying the inverter with DC voltage (for example a photovoltaic generator, a fuel cell or a wind generator) is less than an instantaneous voltage value of a power supply grid voltage of a power supply grid (for example of the public supply grid) into which the inverter circuit feeds its voltage.

A multilevel inverter circuit of this type is known from the document DE 10020537 A1.

Document DE 102006010694 B4 likewise discloses a multilevel inverter circuit, embodied in a BS-NPC (Bipolar Switched Neutral Point Clamped) topology. A circuit topology having five voltage levels is thereby realized, which, moreover, can be embodied in single- and also three-phase fashion. The relatively high voltage stress of the semiconductors used appears to be problematic with regard to this circuit topology.

Against this background, the object of the invention is to improve the known circuit topology by reducing the voltage stress of the semiconductors.

The invention achieves this object by means of the circuit in claim 1. Embodiments of the invention are described in the dependent claims.
According to the invention, a multilevel inverter circuit comprises a positive generator terminal and a negative generator terminal for connecting a generator with a generator voltage. The inverter circuit further comprises an inverter bridge for converting the generator voltage into an AC voltage at a bridge output, which can be connected to a power supply grid. The inverter bridge is connected to the generator terminals via five terminals. A first terminal is connected via a step-up converter to the generator terminals for generating a stepped-up positive generator voltage, a second terminal is connected directly to the positive generator terminal, and a fourth terminal is connected directly to the negative generator terminal, a fifth terminal is connected via a step-up converter to the generator terminals for generating a stepped-up negative generator voltage, and a third terminal is connected to the generator terminals via a capacitive voltage divider. The inverter is characterized in that the bridge output is connected to the first terminal via a first series circuit comprising at least two semiconductor switches, to the second terminal via a second series circuit comprising a diode and at least two semiconductor switches, to the third terminal via two parallel series circuits, each comprising a semiconductor switch and a diode, to the fourth terminal via a fourth series circuit comprising a diode and at least two semiconductor switches, and to the fifth terminal via a fifth series circuit comprising at least two semiconductor switches.

An according multilevel inverter circuit has the advantage that it is possible to use semiconductors of a lower voltage rating, which results in cost savings.

In advantageous embodiments of the multilevel inverter circuit, a first semiconductor switch is a common part.
of the first series circuit, of the second series circuit and of one of the two parallel series circuits, and/or a second semiconductor switch is a common part of the fourth series circuit, of the fifth series circuit and of one of the two parallel series circuits.

In a further advantageous embodiment of the multilevel inverter circuit, the switches of the second series circuit form a common part with the first series circuit, and the switches of the fourth series circuit form a common part with the fifth series circuit. These ways, semiconductor switches are present that are used in more than one series circuits. Accordingly, the total number of semiconductor switches can be kept as small as possible.

In a further advantageous embodiment of the multilevel inverter circuit, the diodes of the two parallel series circuits are respectively assigned further semiconductor switches, arranged in such a way that, in the on state, they bridge the respective diodes in the reverse direction thereof. In yet a further advantageous embodiment, the diodes of the second series circuit and of the fourth series circuit are respectively assigned further semiconductor switches arranged in such a way that, in the on state, they bridge the respective diodes in the reverse direction thereof. The additional bridging switches enable reactive power operation of the inverter, and simultaneously have a protection function, because they allow to limit the maximum voltage across the switches to half the intermediate circuit voltage.

In further advantageous embodiments of the multilevel inverter circuit, the capacitive voltage divider has a series circuit formed by two capacitors between the generator terminals, and/or the capacitive voltage divider has a series circuit formed by two capacitors between the first terminal and the fifth terminal. In
both cases the series circuits formed by the respective capacitors provides a reference potential at a midpoint of the series connection. The reference potential can be directly provided to the third terminal.

In a further advantageous embodiment of the multilevel inverter circuit, the third terminal is connected to a neutral conductor of the power supply grid. This way, feeding into a single-phase power supply grid or feeding into a single phase of a multi-phase power supply grid is possible.

In a further advantageous embodiment of the multilevel inverter circuit, the power supply grid is a three-phase power supply grid, and the bridge output is connected to one of the phases of the power supply grid.

In a further advantageous embodiment of the multilevel inverter circuit, a control device for operating the inverter bridge is configured to alternately switch the bridge output between two of the terminals, the two terminals being selected depending on a present power supply grid voltage. This way, efficient operation of the inverter circuit using modulation methods is possible.

The invention is described in greater detail below with reference to the accompanying drawings, in which:

figure 1 shows by way of example a block diagram for illustrating a multilevel inverter principle,

figure 2 shows by way of example a voltage profile for illustrating a multilevel inverter principle,
Figure 3a shows by way of example a block diagram of an embodiment of a circuit according to the invention with elucidation of a function,

Figure 3b shows by way of example the block diagram from figure 3a with illustration of a further function,

Figure 4a shows by way of example the block diagram from figure 3a with illustration of a further function in another operating phase,

Figure 4b shows by way of example the block diagram from figure 3a with illustration of a further function in the other operating phase,

Figure 5 shows by way of example a schematic illustration of a further embodiment of a circuit according to the invention, and

Figure 6 shows by way of example a schematic illustration of a further embodiment of a circuit according to the invention.

Figure 7 shows by way of example a schematic illustration of a further embodiment of a circuit according to the invention.

Figure 1 shows by way of example a block diagram for illustrating a multilevel inverter circuit. The circuit comprises a generator 1, in particular a photovoltaic generator or a fuel cell, having a positive generator output 21 and a negative generator output 22, at which the generator voltage is present. The positive generator output 21 is directly connected to a second terminal 12, and the negative generator output 22 is directly connected to a fourth terminal 14. Furthermore, the positive generator output 21 is
connected to a first terminal 11 via a first step-up converter 2, and the negative generator output 22 is connected to a fifth terminal 15 via a second step-up converter 3.

Between the positive generator output 21 and the negative generator output 22, figure 1 shows a capacitive voltage divider, formed by a series circuit comprising a first capacitor C1 and a second capacitor C2. The midpoint 23 of the capacitive voltage divider defines a reference potential 7, and is directly connected to the third terminal 13.

The step-up converter 2 has the task of converting the positive generator potential present at the positive generator output 21 into a stepped-up positive generator voltage, i.e. a voltage higher than the positive generator potential. The step-up converter 3 has the task of converting the negative generator potential present at the negative generator output 22 into a stepped-up negative generator voltage, i.e. a voltage lower than the negative generator potential, respectively. For reasons of clarity, figure 1 does not show that the two step-up converters 2, 3 are likewise connected to the respective other generator potential, or alternatively to the reference potential 7, in order to generate the corresponding stepped-up generator voltage therefrom. Any circuit arrangement known in the literature for this purpose and also step-up/step-down converters, for example Cuk, Sepic, Zeta or other converter circuits, are suitable as step-up converters 2, 3.

A second capacitive voltage divider, formed by a third capacitor C3 and a fourth capacitor C4, is arranged between the first terminal 11 and the fifth terminal 15, which are connected to the respective outputs of the assigned step-up converters 2, 3. The midpoint of
said voltage divider is likewise connected to the reference potential 7. The second capacitive voltage divider can be provided both in addition to the first capacitive voltage divider and as a replacement thereof. Preferably, the capacitive voltage divider splits the generator voltage into equal parts, such that the reference potential 7 is located symmetrically between the positive and the negative generator potential. This interconnection is also referred to as NPC inverter (Neutral Point Clamped).

With the aid of the circuit arrangement shown in figure 1, five different voltage levels can be provided at the five terminals 11 to 15, said voltage levels being generated from the positive generator potential and the negative generator potential of the generator 1. These five voltage levels can be connected to an inverter output 19 via an inverter bridge 10 in a controlled sequence of switching operations by means of a number of switches in such a way that a DC voltage power generated by the generator 1 is converted and fed as AC voltage power into a connected power supply grid 9. An inductor L for smoothing the current into the power supply grid 9 is arranged between the inverter bridge 10 and the inverter output 19. The power supply grid 9 may likewise be connected to the reference potential 7 as shown.

In this case, the first terminal 11 is connected to the inverter output 19 via a series circuit formed by at least two switches S11, S12 and the inductor L. The second terminal 12 is connected to the inverter output 19 via a series circuit comprising a diode D1 and at least two switches S21, S22, and the inductor L. The fourth terminal 14 is likewise connected to the inverter output 19 via a series circuit comprising a diode D2 and at least two switches S41, S42, and the inductor L. The fifth terminal 15 is connected to the
inverter output 19 by a series circuit comprising at least two switches S51, S52 and the inductor L. Finally, the third terminal 13 is connected to the inverter output 19 via two parallel connection paths, wherein each of the two connection paths has a series circuit comprising a diode D3 and D4, respectively, and at least one switch S31 and S32, respectively. In this way, the two parallel connection paths jointly form a bidirectional switch between the third terminal 13 and the inverter output 19.

The switches S11 to S52 can be any type of semiconductor switch, for example JFETs, MOSFETs, IGBTs or thyristors, wherein it is also contemplated to use different types of switch alongside one another within the inverter bridge 10. Thus, by way of example, the switches S21 and S41 may be MOSFETs, while the remaining switches are IGBTs.

Through the series circuit comprising at least two switches in the connection paths between the voltage-carrying terminals 11, 12, 14 and 15, on the one hand, and the inverter output 19, on the other hand, the voltage stress of the switches used is advantageously reduced, such that, if appropriate, switches with a voltage rating of 1200 V can be used, although the peak voltage of the connected power supply grid 9 in conventional multilevel inverters already necessitates the use of considerably more expensive and more lossy switches with a voltage rating of approximately 1700 V. This is the case, for example, if the multilevel inverter is connected to an AC power supply grid having a root-mean-square voltage of more than 600 V.

Figure 2 shows by way of example a clocking scheme with the aid of which the inverter bridge 10 converts the generator DC voltage into an AC voltage at the power supply grid frequency. One half-cycle of the power
supply grid voltage 100 is shown. Depending on the present value of the power supply grid voltage 100, the inverter bridge 10 switches alternately between two adjacent voltage levels of the terminals 11-15. Thus, by way of example, in the phase A, in which the power supply grid voltage 100 has a value between a third voltage value 130 present at the third terminal 13 of the inverter bridge 10, and a second voltage value 120 present at a second terminal 12 of the inverter bridge 10, the inverter bridge alternately switches between these voltage values. The length of the time segments in which the third voltage value 130 is output to the inverter output 19 in relation to the length of the time segments in which the second voltage value 120 is output to the inverter output 19 is chosen depending on the present value of the power supply grid voltage 100. Analogously, in a phase B, switching is effected alternately between the second voltage value 120 and a first voltage value 110, which is present at the first terminal 11 of the inverter bridge 10. In the phase C, the inverter bridge 10 is again switched alternately between the second voltage value 120 and in the third voltage value 130. Analogously, in a negative half-cycle of the power supply grid voltage 100, clocking is effected between the third voltage value 130, a fourth voltage value, which is present at the fourth terminal 14, and a fifth voltage value, which is present at the fifth terminal 15.

In one advantageous variant of the inverter bridge 10 from figure 1, a plurality of the switches of different connection paths between the terminals 11-15 and the inverter output 19 can be combined to form a common switch. By way of example, it is possible to combine the switch S22 and the switch S31 to form a common switch S3, or to combine the switches S32 and S42 to form a common switch S3'. This results in a multilevel inverter circuit as shown in figure 6 and discussed in
It is likewise possible to combine the switches S12, S22 and S31 to form a common switch S2, or the switches S32, S42 and S52 to form a common switch S2'. This results in a multilevel inverter circuit in accordance with figures 3a to 4b, the function of which is discussed in greater detail below.

The current flow (dashed line) illustrated in figure 3a corresponds to the state of the circuit in the region A of the time axis t (cf. figure 2). The semiconductor valve S21 and S2 are switched on. The remaining switches are switched off. Switch S21 is clocked at high frequency for pure active power operation. As a result, the current flow changes between the path shown in figure 3a and that shown in figure 3b. This clocking is typically maintained as long as the present power supply grid voltage lies between the reference potential 7 and the positive generator potential.

The current flow (dashed line) illustrated in figure 4a corresponds to the state of the circuit in the region B of the time axis t (cf. figure 2). The semiconductor switches S11 and S2 are switched on. S11 is clocked at high frequency for pure active power operation. The feeding is effected with the voltage stepped up by the step-up converter 2. As a result of the clocking of the switch S11, the current flow changes, in the phases in which the switch S11 is open, to the path shown in figure 4b. This clocking is typically maintained as long as the present power supply voltage lies above the positive generator potential.

The function of the circuit for a negative half-cycle is achieved accordingly.

Figure 5 shows a further embodiment of a multilevel inverter circuit according to the invention. In this case, an additional third switch S21 is integrated into
the connection path from the first terminal 11 to the
power supply grid 9, said third switch simultaneously
also being part of the connection path from the second
terminal 12 to the power supply grid 9. Analogously,
the connection path from the fifth terminal 15 to the
power supply grid 9 comprises an additional third
switch S41 that is simultaneously also part of the
connection path from the fourth terminal 14 to the
power supply grid 9. As already shown in the circuit in
figures 3a to 4b, common switches S2 and S2' each forms
part of the connection paths between the power supply
grid 9 and a plurality of the terminals 11 to 15.

As a result of this embodiment, the voltage stress for
the semiconductor valves S11, S21, S2, and S41, S51 and
S2' can advantageously be reduced since the stepped-up
voltage values can now be split between three switches.
This makes it possible to use more cost-effective
semiconductor switches.

Furthermore, it is shown as an alternative embodiment
that the diode D2 in the connection path between the
second terminal 12 and the power supply grid 9 can be
bridged via an additional bridging switch 30 in the
reverse direction of the diode D2. Likewise, the diode
D4 in the connection path between the fourth terminal
14 and the power supply grid 9 can be bridged by a
bridging switch 31 in the reverse direction of the
diode D4. These additional bridging switches 30 and 31
enable reactive power operation of the inverter, and
simultaneously have a protection function, because they
allow to limit the maximum voltage across the switches
S2 and S2' to half the intermediate circuit voltage. In
one advantageous form of operation of the inverter
circuit, the switch 30 is closed if the switches S11 and
S21 are open, and, analogously, the switch 31 is
closed if switch S41 and switch S51 are open.
A further embodiment of the multilevel inverter circuit according to the invention is shown in figure 6. The circuit substantially corresponds to the circuit from figures 3a to 4b with the difference that the diodes D31, D32 can respectively be bridged by a bridging switch 32 and a bridging switch 33 in the reverse direction of the corresponding diode, which likewise serves the purpose described above. Here, the switch 32 may be operated to be closed if the switches S11 and S2 are open, and, accordingly, the switch 33 is closed if switch S41 and switch S2' are open.

The bridging switches 30 to 33 can be used individually or in combination in each of the circuit arrangements described above.

As shown in figure 7, the concept according to the invention can also be used for three-phase inverters. In this case, three isolated inverter bridges 10a, 10b, 10c are used via the inverter outputs 19a, 19b, 19c, respectively, for feeding into a phase of the three-phase power supply grid 9 which is assigned to them. In this case, it is not necessary to connect the midpoint of the capacitive voltage divider as reference potential 7 to a neutral conductor of the power supply grid 9. As a result, in particular the modulation methods described in the literature, such as space vector modulation, flat top modulation, etc., become possible.

It is likewise easily possible, by means of only two of the inverter bridges 10a, 10b as a full bridge, to realize feeding into a single-phase power supply grid without connection to a neutral conductor, by connecting the inverter outputs 19a, 19b to the two terminals of the power supply grid. In this case, too, the midpoint of the capacitive voltage divider can
remain isolated from a neutral conductor of the power supply grid.

The different possibilities for operating the semiconductor switches are known to the person skilled in the art and need no further explanation in the context of the present invention.

The invention is not limited to the embodiments described, which can be modified in many different ways. In particular, it is possible for the features mentioned to be embodied in combinations other than those mentioned.
Claims:

1. A multilevel inverter circuit comprising a positive generator terminal (21) and a negative generator terminal (22) for connecting a generator (1) with a generator voltage, and also comprising an inverter bridge (10) for converting the generator voltage into an AC voltage at a bridge output (19), which can be connected to a power supply grid (9), wherein the inverter bridge (10) is connected to the generator terminals (21, 22) via five terminals (11-15), of which
   - a first terminal (11) is connected via a step-up converter (2) to the generator terminals (21, 22) for generating a stepped-up positive generator voltage,
   - a second terminal (12) is connected directly to the positive generator terminal (21), and a fourth terminal (14) is connected directly to the negative generator terminal (22),
   - a fifth terminal (15) is connected via a step-up converter (3) to the generator terminals (21, 22) for generating a stepped-up negative generator voltage, and
   - a third terminal (13) is connected to the generator terminals (21, 22) via a capacitive voltage divider (C1/C2, C3/C4)
characterized in that the bridge output (19) is connected
   - to the first terminal (11) via a first series circuit comprising at least two semiconductor switches (S11, S12),
   - to the second terminal (12) via a second series circuit comprising a diode (D2) and at least two semiconductor switches (S21, S22),
   - to the third terminal (13) via two parallel series circuits, each comprising a semiconductor switch (S31, S32) and a diode (D31, D32),
- to the fourth terminal (14) via a fourth series circuit comprising a diode (D4) and at least two semiconductor switches (S41, S42), and
- to the fifth terminal (15) via a fifth series circuit comprising at least two semiconductor switches (S51, S52).

2. The multilevel inverter circuit as claimed in claim 1, characterized in that a first semiconductor switch (S2) is a common part of the first series circuit, of the second series circuit and of one of the two parallel series circuits.

3. The multilevel inverter circuit as claimed in claim 1 or 2, characterized in that a second semiconductor switch (S2') is a common part of the fourth series circuit, of the fifth series circuit and of one of the two parallel series circuits.

4. The multilevel inverter circuit as claimed in any of the preceding claims, characterized in that the switches (S21, S22) of the second series circuit form a common part with the first series circuit, and that the switches (S41, S42) of the fourth series circuit form a common part with the fifth series circuit.

5. The multilevel inverter circuit as claimed in any of the preceding claims, characterized in that the diodes (D31, D32) of the two parallel series circuits are respectively assigned further semiconductor switches (S2, S3) arranged in such a way that, in the on state, they bridge the respective diodes in the reverse direction thereof.

6. The multilevel inverter circuit as claimed in any of the preceding claims, characterized in that the diodes (D2, D4) of the second series circuit and of the fourth series circuit are respectively assigned further
semiconductor switches (30, 31) arranged in such a way that, in the on state, they bridge the respective diodes in the reverse direction thereof.

5 7. The multilevel inverter circuit as claimed in any of the preceding claims, characterized in that the capacitive voltage divider has a series circuit formed by two capacitors (C1, C2) between the generator terminals (21, 22).

10 8. The multilevel inverter circuit as claimed in any of the preceding claims, characterized in that the capacitive voltage divider has a series circuit formed by two capacitors (C3, C4) between the first terminal (11) and the fifth terminal (15).

15 9. The multilevel inverter circuit as claimed in any of the preceding claims, characterized in that the third terminal (13) is connected to a neutral conductor of the power supply grid (9).

20 10. The multilevel inverter circuit as claimed in any of the preceding claims, characterized in that the power supply grid (9) is a three-phase power supply grid, and the bridge output (19) is connected to one of the phases of the power supply grid (9).

25 11. The multilevel inverter circuit as claimed in any of the preceding claims, characterized in that a control device for operating the inverter bridge is configured to alternately switch the bridge output (19) between two of the terminals, the two terminals being selected depending on a present power supply grid voltage.
Fig. 2
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

INV. H02M7/483 H02M7/487

ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02M H02J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal , INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
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C) Further documents are listed in the continuation of Box C.

X) See patent family annex.

* Special categories of cited documents:

"A": document defining the general state of the art which is not considered to be of particular relevance

"E": earlier document but published on or after the international filing date

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"X": document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y": document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"A": document member of the same patent family

Date of the actual completion of the international search

6 February 2012

Date of mailing of the international search report

13/02/2012

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk
Tel: (+31-70) 340-2040, Fax: (+31-70) 340-3016

Authorized officer

Gotzig, Bernhard
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