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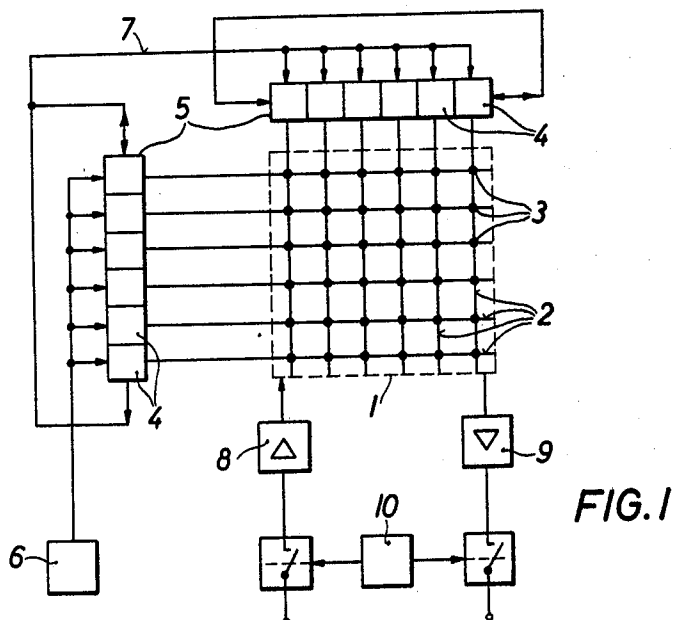
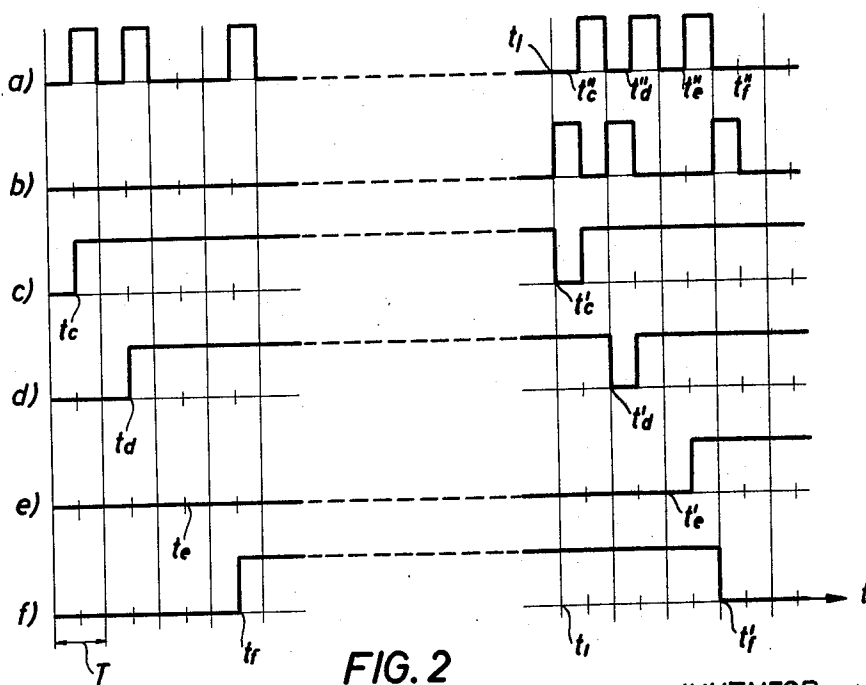
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3,478,332

APPARATUS FOR THE RETARDATION OF IMPULSE SEQUENCES

Filed March 30, 1964

2 Sheets-Sheet 1



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2 Sheets-Sheet 2

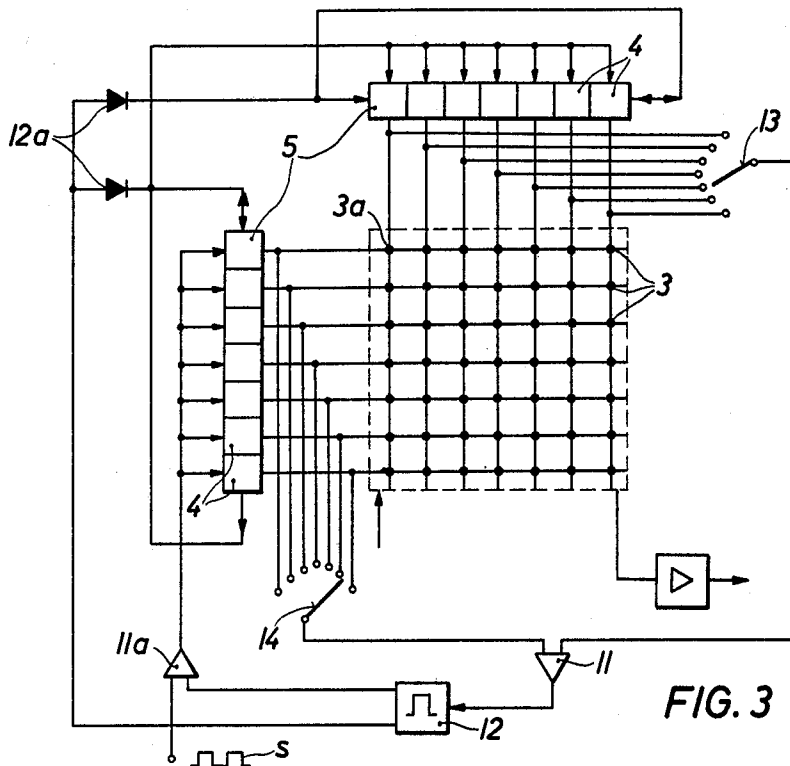


FIG. 3

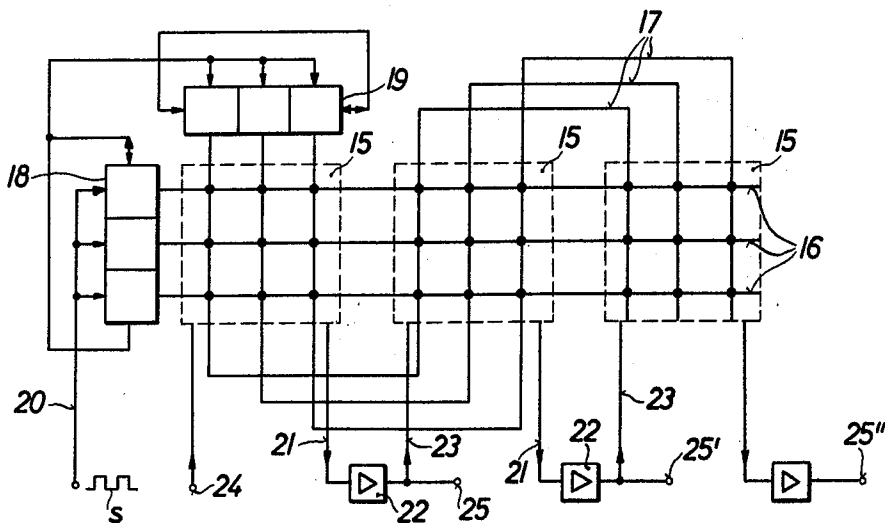


FIG. 4

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APPARATUS FOR THE RETARDATION OF IMPULSE SEQUENCES

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4 Claims

ABSTRACT OF THE DISCLOSURE

Apparatus for retarding impulse sequences, in which the individual storage segments of a matrix have coincidence signals applied to them in such a way that all or some of the segments are selected successively and cyclically, with each such segment being read out during the first part of a selection period and being thereafter written into during the last part of the select period.

The present invention deals with a method and apparatus for the retardation of impulse sequences of a constant amplitude in which the presence or the absence of individual impulses, respectively, represents information in a binary code.

The retardation of such sequences of impulses might be required, for example, for the purpose of smoothing out phase differences in the performance of several collaborating switch groups in data processing installations.

For retardation times of the various orders of magnitudes which might occur, there is used, as a rule, different kinds of devices. Simple retardation members and transit time chains are well suited for short retardation times, up till several microseconds, but such devices have the disadvantage of changing the course of the stored impulse with respect to time.

For greater time periods, switch members of double stability must be used, linked so as to form pusher chains. However, as soon as retardation times of a certain magnitude are reached, the complicated nature of the connections for setting up switches of this type becomes very great, because there must be present just as many chain steps of double stability, with their control elements, as there are retardation cadences.

For very long retardation times permanent storage devices, like magnetic cores, magnetic drums, magnetic tapes, are used, and, in extreme cases, even punched tapes.

With the last mentioned devices the sequence of impulses which shall be retarded in its totality is stored, is then read out at the desired moment of time. From this it may be derived that the storage capacity must correspond to the total number of impulse cadences present in the impulse sequence, which means that a limit must be put on the duration of the impulse sequences to be handled, or the unit storage must be so very big that an inconvenience is created especially with respect to cost.

It is the object of the present invention to provide a method and apparatus in which commonly known matrix storage units are used, especially ones with magnetic cores, which operate according to the coincidence method, which method allows retardation of impulse sequences of any arbitrary length, and the number of individual storage segments is determined only by the desired number of retarding cadences.

The problem is solved by the invention by providing an arrangement whereby storage occurs in storage segments from which the information is read out in a continuous, cyclic sequence. An important characteristic is

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the provision of a number of storage segments corresponding to the number of retarding cadences, and there will occur in the selected storage segment, within one cadence, first a read out of one impulse of the retarded sequence of impulses; which impulse at the preceding cycle had become stored in said storage segment; and that thereafter will occur the writing in or storage of the newly arriving impulse of the sequence of impulses which shall be retarded, in the same storage segment which just had become emptied due to read-out.

There is achieved in this way, in comparison to the known retardation circuits with pushing chains, a great decrease of the complexity and cost of the device because, as a matrix storage unit is used which performs in coincidence operation, for each row and each column one selector switch only is needed. On the other hand, in comparison to the retardation procedures commonly used at matrix storage units, there is a saving, with respect to individual storage segments, which, in turn, leads to the possibility of handling a limitless sequence of impulses.

Part of the subject matter of the present invention is, furthermore, an advantageous switch arrangement or circuit for the practice of the retardation method. By the use of annularly through-connected chain-switches for the selecting of the rows and the columns of the matrix storage unit, an adjustability of the retardation time such that the steps of the chain-switches may be connected selectively to switches which are controlled by the impulses of the individual storage segments, which switches shorten the cycle through which the impulses must pass, by calling-out again from the first storage segment.

Furthermore, the retardation may be channeled stepwise by subdividing the storage matrix into approximately square submatrices, the rows and columns of which are connected always to the same switch, and the read-outs of which, with the exception of the one of the last submatrix, are always connected to the recording input of the next partial submatrix.

The change of the retardation time occurs simply by a selective withdrawal of the read-out impulses at the output side of one of the submatrices. This circuit, in comparison to arrangements with closed storage matrix, furthermore saves a great number of steps of the selector switches, because the rows and columns of the submatrices which correspond to each other, are contacted only by one step of the switches. There is required for this a somewhat more bulky and expensive amplifier for recording and read-out at the submatrices, but this drawback, as a rule, is overcompensated by the advantages just outlined.

The greatest possible saving with respect to steps of the selector switches is, according to a preferred embodiment of the invention, brought about by such a subdividing of the storage unit into submatrices, that the number of such submatrices which are switched in series, is equal approximately to the number of rows or columns, respectively of each submatrix.

Other advantages of the invention may be derived from the following specification with reference to typical examples which are shown in the accompanying drawings, in which:

FIGURE 1 is the circuit diagram of a matrix storage unit known per se to prior art, with which the method of the present invention can be practiced;

FIGURE 2 shows the transit time of impulses according to the method of the present invention;

FIGURE 3 shows the construction of a special selector switch for matrix storage units for the practice of the method of the present invention; and

FIGURE 4 shows a storage unit which consists of square submatrices for a retardation time which is adjustable in steps.

In FIGURE 1 there is a commonly known matrix storage unit 1, the leads 2 of the rows and columns of which at their crossover prints are linked to the annular cores which are coordinated to the individual storage segments 3. These storage segments are selected in a coincidence operation by the steps 4 of the switches 5 which are constructed e.g. as pushing chains. These switches show a continuous, annular connection between their input and output steps, so that always the impulses, which are ready for use in one of the switch steps, will flow in a circular path under the action of the pushing impulses which are fed into each switch. To the row-switch the pushing impulses are fed from a beat-generator 6, whereas the pushing lead 7 of the column switch is connected to the connection lead between the first and the last step of the row-switch and thus it will obtain upon each revolution of this switch one pushing impulse. In this way the storage segments are selected, column by column, one after the other, continuously, in a cyclic sequence.

The binary information to be deposited or written in the storage segment, is forwarded to the amplifier 8 of a recording device, of the usual type (not shown) which might operate, for example, according to the inhibition method. Such forwarding occurs synchronously with the rhythm imparted to switches 5, whereas the read-out information is read out by the aid of a read-out device (not shown) and a reading amplifier 9. The input of the recording amplifier 8 and the output of the reading amplifier 9 are conveyed across the corresponding switches by a cadence tapper switch 10 which operates essentially synchronously with the beat generator 6, according to a retardation program which is described in its principle by the impulse chart shown in FIGURE 2. The construction of the cadence tapper switch 10 may be accomplished by use of suitable means in manners which will easily come into the mind of any party versed in the art, and which thus does not fall under the purview of the appended claims.

FIGURE 2 shows in the rows *a* to *f*, the course of the impulse at the various points of the circuit according to FIGURE 1, during the time *t*. In the row *a*, there is indicated an arbitrarily chosen, binary sequence of impulses with the period *T*, which is fed into the input of the recording amplifier 8 under the action of the cadence tapper switch 10, with a scanning ratio of 1:1, whereby one impulse period *T* coincides with respect to time with one cadence of the storage unit 1.

The impulses of the impulse sequence according to row *a*, are fed into the storage segments 3 of the storage unit 1. Thereby during the first half of each impulse period the cadence tapper switch 10 switches-in first the read-out amplifier 9, while the recording amplifier 8 remains out of action, and then, in each second half of the impulse periods, occurs the recording process proper, whereby the read-out amplifier 9 becomes switched off, and the recording amplifier 8 becomes switched on.

The result of the first cycle of the storage unit which extends till the time *t*₁, i.e. until the very last storage segment has been reached, therefore is one transmitting of one binary information each into each storage segment. For the first four storage segments one can recognize this transmitting in the drawing in the rows *c*, to *f*, at the times *t*₀ to *t*₁. On the other hand, during the first halves of the impulse periods according to row *b*, no information is read-out till the time *t*₁, as storage unit was empty when the operation was started.

After the beginning of the second cycle, at the time *t*₁, there is read-out always the information which was stored in the first half of an impulse period according to row *b*, during the preceding cycle into the corresponding storage segment, and this now brings about that at the

output of the read-out amplifier 9 will appear the originally deposited sequence of impulses with the retardation time which corresponds to the number of storage segments which were passed-through in the cycle.

By the reading-out of the information from the storage segments, the segments are returned to their starting state, and become ready for the registering of new information. This return into the starting position may be recognized from FIGURE 2 for the first four storage segments in the rows *c* to *f* at the times *t*₀' to *t*₁'. Thereafter occurs always in the second half of the impulse period the registering of the newly arriving impulse of the impulse sequence which shall become delayed, according to row *a*, at the time *t*₀' to *t*₁', whereby the lacking of the newly registered impulse in a manner known *per se* is equivalent to the registration of one of the two possible binary information.

FIGURE 3 shows a circuit arrangement for a matrix storage unit in which the retardation time is variable. Here the output of the steps of the row and column switches are led to the stationary contacts of one multiple commutator or sweep switch 13 or 14, respectively each, these outputs then in any combination corresponding on one storage segment each, may be connected to the inputs of an AND gate 11.

When calling-out from the storage segment which was preset by aid of the switch 13, 14, a monostable sweep circuit 12 is tripped which has been introduced so as to act as a time switch, and which sweep circuit, in the state of rest, will feed across an AND-gate 11a, the pusher impulses *s* to the push inputs of the row-switch, but which when tripped, not being in the state of rest, will block the pushing impulses *s* for the duration of the next beat or cadence. In this way the further progressing of the unshortened call-out cycle is stopped. Simultaneously, from a second output of the monostable sweep circuit 12 an impulse is passed on across the decoupling diodes 12a into the combination of call-out switch steps 4 which are coordinated in the first storage segment 3a, and this way is started a new call-out cycle which is correspondingly shortened.

FIGURE 4 shows the subdividing of a matrix storage setup with 27 storage segments, into 3 square submatrices. The row-wires 16 and the column-wires 17 of all submatrices are connected in series, and are connected to only the step each of the row switch 18 or of the column-switch 19 respectively. The push-impulses *s*, as this is usually done are fed into the row-switch, across a pushing lead 20 which is common to all the steps. Furthermore the read-out outputs 21 of the first and of the second submatrix are connected, across a read-out amplifier 22, to the recording input 23 of the one submatrix which always is the next one in sequence. The feeding of the sequence of impulses which shall be retarded, occurs at the input 24 of the first submatrix.

At the switches which are in operation, simultaneously in all submatrices the corresponding storage segments are selected, one after the other, in cyclic succession. Across the read-out amplifiers 22, however, into the last two submatrices always this sequence of impulses is fed, which is read-out from the one submatrix which was switched ahead. In this way, it becomes possible to tap from the outputs 25, 25' or 25'', respectively, this sequence of impulses, which was fed into the input 24, selectively with a retardation of 9, 18 or 27 impulse cadences, respectively.

By connecting a complete set of storage segments of all submatrices which segments correspond to each other, to one step only of the switches 18 or 19 respectively the number of steps thereof is considerably lowered. On the other hand, due to the subdividing of the submatrices, the number of read-out or recording amplifiers required, will increase correspondingly. If it is assumed that the expenditures for material and work for one of the last named types of amplifiers is roughly the same as that for one call-out switch step, then, as can be found, on the basis of a mathematical analysis, the optimum economical perform-

ance is obtained for a given total retarding time, if a subdividing is made into square submatrices, the number of which should be equal to the number of rows or columns, respectively of each submatrix.

Such a construction combines the advantage of the least amount of operations to be done when switching, with the advantage that the retarding time may be changed in steps.

What is claimed is:

1. In a circuit arrangement for retarding impulse sequences; a storage matrix comprising a plurality of storage segments, switch means comprising
 - two chain switches pertaining respectively to the rows and columns of the storage matrix and
 - operable for selecting at least some of said segments successfully and cyclically and for applying coincidence signals to each of the selected segments, means operable during the first part of the period of selection of each segment for reading out from each respective segment and impulse of the impulse sequence previously deposited therein, means operable during the last part of the period of selection of each segment for writing into each respective segment a newly received impulse of the impulse sequence in consequence of which each of the selected segments is, during each period, first read out and thereafter written into,
 - means for effecting the selection of the storage segments at the same cadence as that of the impulses in said impulse sequence, and
 - further switch means adapted for selective connection to the individual steps of said chain switches and under the control of the impulses pertaining to the storage segments and operable to shorten the cycle during which impulses are fed to each storage segment.
2. In a circuit arrangement for retarding impulse sequences; a storage matrix comprising a plurality of storage segments, switch means comprising
 - two chain switches pertaining respectively, to the rows and columns of the storage matrix and
 - operable for selecting at least some of said segments

successfully and cyclically and for applying coincidence signals to each of the selected segments, means operable during the first part of the period of selection of each segment for reading out from each respective segment and impulse of the impulse sequence previously deposited therein, means operable during the last part of the period of selection of each segment for writing into each respective segment a newly received impulse of the impulse sequence in consequence of which each of the selected segments is, during each period, first read out and thereafter written into,

means for effecting the selection of the storage segments at the same cadence as that of the impulses in said impulse sequence,

said storage matrix being in the form of a plurality of substantially square submatrices having the respective rows and columns thereof connected to the same chain switches, a read out output from each submatrix, a writing in input to each submatrix, and each read out output being connected to the writing in input of the next following submatrix.

3. The circuit arrangement according to claim 1 in which said further switch means comprise an AND gate having two inputs connected to a selected step combination of said chain switches and a time delay switch connected to the output side of the gate and itself having output means connected to said chain switches in controlling relation thereto.

4. The circuit arrangement according to claim 2 in which the number of submatrices is substantially equal to the number of rows or columns of each submatrix.

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