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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 :		(11) International Publication Number:
H03K 19/086, 19/21, 17/62	A1	WO 93/17500
		(43) International Publication Date: 2 September 1993 (02.09.93)

(21) International Application Number: PCT/CA92/00494

(22) International Filing Date: 12 November 1992 (12.11.92)

(30) Priority data:
838,171 20 February 1992 (20.02.92) US

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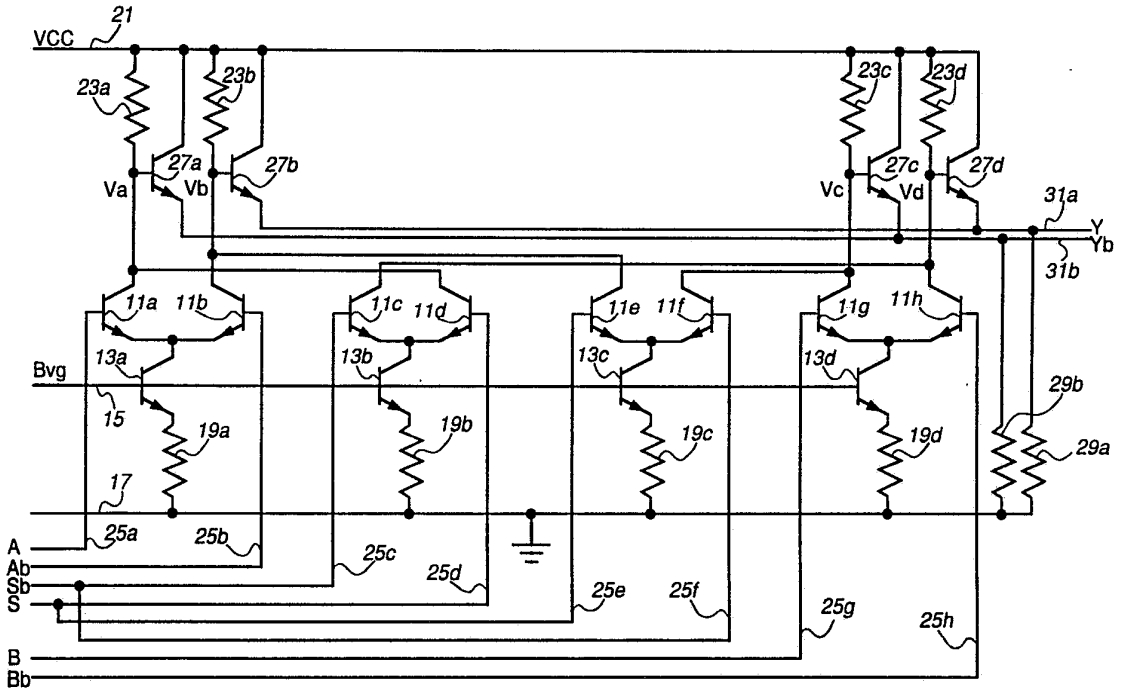
(81) Designated States: CA, JP, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, SE).

Published
With international search report.

(54) Title: DIFFERENTIAL ECL CIRCUIT



(57) Abstract

A differential ECL (emitter coupled logic) circuit, with differential inputs and output and no series gates, comprises a plurality of transistor pairs (11A-11H). The differential ECL circuit can operate at high speed as there are no series gates and its noise margin is large because of differential operation. The differential circuit can be implemented into a multiplexer or various logic circuits such as XOR (exclusive OR)/NXOR, OR/NOR, AND/NAND.

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DIFFERENTIAL ECL CIRCUIT

FIELD OF THE INVENTION

The present invention relates generally to emitter coupled logic (ECL) circuits with differential inputs and output, and more particularly to a multiplexer and logic function circuits.

BACKGROUND OF THE INVENTION

A multiplexer or logic function circuit such as an exclusive OR (XOR), non-exclusive (NXOR), OR, NOR, AND or NAND circuit is usually formed on a semiconductor integrated circuit chip. For example, United States Patent No. 4,963,767 dated October 16, 1990 by Nguyen X. Sinh discloses an ECL (emitter coupled logic) multiplexer of non-differential type. United States Patent No. 4,866,306 dated September 12, 1989 by Daniel F. Hopta discloses an ECL multiplexer, which has series gates with differential outputs and non-differential inputs. United States Patent No. 4,628,216 dated December 9, 1986 by Nikhil C. Mazumder discloses multiplexers and XOR and other logic circuits. Also, ELECTRONICS LETTERS, 29th March 1990, Vol.26, No.7, pp.430-431, shows a high speed XOR and ELECTRONICS LETTERS, 12th October 1989, Vol. 25, No. 21, pp. 1422-1423, discloses a high speed multiplexer.

However, these prior art circuits have disadvantages - low speed, a small noise margin and/or a large power consumption - due to the use of series gates or non-differential type circuits.

SUMMARY OF THE INVENTION

The present invention provides differential ECL circuits (e.g. a multiplexer and logic function circuits), which overcome such disadvantages.

According to the most general aspect of the present invention, a differential ECL circuit comprises: a plurality of transistor pairs, each respectively comprising first and second transistors whose emitters are connected to each other; a plurality of constant current sources, each being connected between the connected emitters of each transistor pair and a first potential terminal; four load resistors connected between the first and second transistors' collectors of two transistor pairs and a second potential terminal; an emitter follower circuit comprising four emitter follower transistors and two emitter resistors; and means for providing a plurality of differential input signals to the transistor pairs. In the differential ECL circuit, at least some of the first and second transistors' collectors of each of the transistor pairs to which the four load resistors are connected, are connected to the counterparts of the other transistor pairs. The bases of the four emitter follower transistors are connected to the first and second transistors' collectors of the transistor pairs to which the four load resistors are connected. The emitters of the two emitter follower transistors are connected to the first potential terminal through the one emitter resistor. The emitters of the other two emitter follower transistors are connected to the first potential terminal through the other emitter resistor. A differential output signal is provided across the emitter resistors, depending upon logic states of the differential input signals.

Preferably in any one differential ECL circuit, all of the transistors are of the same NPN (PNP) type and the first and second potential terminals are low and high (high and low) potential terminals, respectively.

In response to the differential input and select signals, the transistor pairs function as a multiplexer. Also, in response to the differential input signals, the transistor pairs function as logic circuits (e.g. XOR, OR, AND).

The differential ECL circuit has no series gates. Therefore, its speed is high and propagation times from any input to the output are the same and the circuit is symmetrical. Also, due to the differential input and outputs, it has very good noise margin characteristics.

BRIEF DESCRIPTION OF THE DRAWINGS

An embodiment of the present invention will now be described by way of example only with reference to the accompanying drawings in which:

Figure 1 is a schematic diagram of a multiplexer according to the present invention;

Figure 2 is a schematic diagram of an XOR circuit according to the present invention;

Figure 3 is a schematic diagram of an OR circuit according to the present invention; and

Figure 4 is a schematic diagram of an AND circuit according to the present invention.

OBJECT OF THE INVENTION

1. MULTIPLEXER

First, an embodiment multiplexer according to the present invention is described.

I. Structure of the Multiplexer

Referring to Figure 1, the multiplexer comprises four differential transistor pairs and four constant current sources, which are connected to the transistor pairs. In each transistor pair, the emitters of two transistors 11a, 11b; 11c, 11d; 11e, 11f; and 11g, 11h are mutually coupled. The constant current sources comprise transistors 13a - 13d, the collectors of which are connected to the coupled emitters of transistor pairs, the bases of which are connected to a common bias voltage line 15, and the emitters of which are connected to a ground

line 17 through resistors 19a - 19d. The ground line 17 is the reference potential line in this circuit (a low potential line). A positive DC voltage Bvg (typically 2.0 volts) is fed to the common bias voltage line 15.

The collectors of the transistors 11c, 11d, 11e and 11f are connected to the collectors of the transistors 11h, 11a, 11b and 11g, respectively. The collectors of the transistors 11a, 11b, 11g and 11h are connected to a voltage supply line 21 through resistors 23a - 23d, respectively. Another positive DC voltage VCC (typically 4.5 volts) is fed to the voltage supply line 21.

Input lines 25a - 25h are connected to the bases of the transistors 11a - 11h so as to feed first and second differential input signals and a differential select signal to the transistor pairs. The input lines 25c and 25f, or the bases of the transistors 11c and 11f, are connected to each other. The input lines 25d and 25e, or the bases of the transistors 11d and 11e, are connected to each other.

The multiplexer also comprises an emitter follower circuit including four transistors 27a - 27d, the bases of which are connected to the collectors of the transistors 11a, 11b, 11g and 11h, respectively. Both emitters of the transistors 27b and 27d are connected to the ground line 17 through a resistor 29a. Similarly, both emitters of the transistors 27a and 27c are connected to the ground line 17 through a resistor 29b. Output lines 31a and 31b are connected to the emitters of transistors 27b, 27d and 27a, 27c, respectively, so as to provide a differential output signal across both resistors 29a and 29b.

II. Operation of the Multiplexer

Each of the first and second differential input signals and the differential select signal consists of non-inverted and inverted phase components. The non-inverted and inverted phase components A and Ab of the first differential input signal are fed to the input lines 25a and 25b, respectively. The non-inverted and inverted phase

components B and Bb of the second differential input signal are fed to the input lines 25g and 25h, respectively. The non-inverted and inverted phase components S and Sb of the differential select signal are fed to the input lines 25d, 25e and 25c, 25f, respectively.

When a select signal voltage Vss, which is the potential difference between the non-inverted and inverted phase components S and Sb, is negative or positive, the logic level of the differential select signal is "0" or "1", respectively. Also, when each of voltages Vsa and Vsb of the first and second differential input signals is negative or positive, its logic level is "0" or "1", respectively.

With the voltage Bvg being fed to the bases of the transistors 13a - 13d, a constant current flows in the connected emitters of each transistor pair, so that the total current Io flowing in the collectors of each transistor pair is constant. In the following description, when a differential signal is fed to the bases of the transistor pair, the current Io flows in either one or the other transistor of that pair. Voltage drops between bases and emitters of the transistors are ignored. The four resistors 23a, 23b, 23c and 23d have the same resistance R. Base potentials of the transistors 27a, 27b, 27c and 27d are referred to as Va, Vb, Vc and Vd, respectively.

In response to the input and select signals, the transistors of the four transistor pairs function as a differential ECL circuit. Table I shows the relationship between the input signal voltages, the base potentials of the transistor pairs and the output voltage for both negative and positive select signal voltages.

Under the negative select signal voltage Vss, when both first and second input signal voltages Vsa and Vsb are negative, the current Io flows in each of the transistors 11b, 11c, 11f and 11h. Since the base-emitters of the transistors 27c and 27d are reverse-biased, they are non-conductive. Output potentials V(Y) and V(Yb) at the output

lines 31a and 31b are nearly equal to the base potentials Vb and Va, respectively, so that the output signal voltage, V(Y)-V(Yb), is negative (or logic "0"). Likewise, when the first and second input signal voltages Vsa and Vsb are negative and positive, respectively, the transistors 11b, 11c, 11f and 11g are conductive. When the first and second input signal voltages Vsa and Vsb are positive and negative, respectively, the transistors 11a, 11c, 11f and 11h are conductive. When both first and second input signal voltages Vsa and Vsb are positive, the transistors 11a, 11c, 11f and 11g are conductive.

Under the positive select signal voltage Vss, when both first and second input signal voltages Vsa and Vsb are negative, the current Io flows in each of the transistors 11b, 11d, 11e and 11h. When the first and second input signal voltages Vsa and Vsb are negative and positive, respectively, the transistors 11b, 11d, 11e and 11g are conductive. When the first and second input signal voltages Vsa and Vsb are positive and negative, respectively, the transistors 11a, 11d, 11e and 11h are conductive. When both first and second input signal voltages Vsa and Vsb are positive, the transistors 11a, 11d, 11e and 11g are conductive.

As a result, the logic output signals which correspond to the first or second input signals selected by the select signal, are provided from the output lines 31a and 31b.

2. XOR CIRCUIT

Second, an embodiment XOR circuit according to the present invention is described.

I. Structure of the XOR circuit

As shown in Figure 2, the collectors of the transistors 11c and 11d are connected to the collectors of the transistors 11b and 11a, respectively. The collectors of the transistors 11e and 11f are connected to the

collectors of the transistors 11h and 11g, respectively. The input lines 25a and 25g, or the bases of the transistors 11a and 11g, are connected to each other. The input lines 25b and 25h, or the bases of the transistors 11b and 11h, are connected to each other. The input lines 25c and 25f, or the bases of the transistors 11c and 11f, are connected to each other. The input lines 25d and 25e, or the bases of the transistors 11d and 11e, are connected to each other. The output lines 31a and 31b are connected to the emitters of transistors 27c, 27d and 27a, 27b, respectively. The other connections are the same as those of the circuit shown in Figure 1.

II. Operation of the XOR circuit

In the XOR circuit shown in Figure 2, compared to the multiplexer shown in Figure 1, the non-inverted and inverted phase components B and Bb of the second differential input signal, instead of the non-inverted and inverted phase components S and Sb of the differential select signal, are fed to the bases of the transistors 11d, 11e and 11c, 11f, respectively. The non-inverted and inverted phase components A and Ab of the first differential input signal, instead of the non-inverted and inverted B and Bb of the second differential input signal, are fed to the bases of the transistors 11g and 11h, respectively.

In response to the differential input signals, the transistors of the four transistor pairs function as a logic circuit. Table II shows the relationship between the input signal voltages, the base potentials of the transistor pairs and the output voltage.

When both first and second input signal voltages Vsa and Vsb are negative, the current Io flows in each of the transistors 11b, 11c, 11f and 11h. Similarly, when the first and second input signal voltages Vsa and Vsb are negative and positive, respectively, the transistors 11b, 11d, 11e and 11h are conductive. When the first and second

input signal voltages Vsa and Vsb are positive and negative, respectively, the transistors 11a, 11c, 11f and 11g are conductive. When both first and second input signal voltages Vsa and Vsb are positive, the transistors 11a, 11d, 11e and 11g are conductive.

As a result, the output signals from the output lines 31a and 31b are of the XOR logic on the basis of the first and second input signals.

3. OR CIRCUIT

Third, an embodiment OR circuit according to the present invention is described.

I. Structure of the OR circuit

As shown in Figure 3, the OR circuit has a similar circuit structure as the multiplexer shown in Figure 1. The transistors 11e and 11f and their related circuits and connections are deleted. The input lines 25c and 25g, or the bases of the transistors 11c and 11g, are connected to each other. The input lines 25d and 25h, or the bases of the transistors 11d and 11h, are connected to each other. The output lines 31a and 31b are connected to the emitters of transistors 27b, 27c and 27a, 27d, respectively.

II. Operation of the OR circuit

In the OR circuit shown in Figure 3, compared to the multiplexer shown in Figure 1, the non-inverted and inverted phase components B and Bb of the second differential input signal, instead of the non-inverted and inverted phase components S and Sb of the differential select signal, are fed to the bases of the transistors 11d, 11h and 11c, 11g, respectively. Table III shows the relationship between the input signal voltages, the base potentials of the transistor pairs and the output voltage.

When both first and second input signal voltages Vsa and Vsb are negative, the current Io flows in each of the transistors 11b, 11c, and 11g. Similarly, when the

first and second input signal voltages Vsa and Vsb are negative and positive, respectively, the transistors 11b, 11d, and 11h are conductive. When the first and second input signal voltages Vsa and Vsb are positive and negative, respectively, the transistors 11a, 11c, and 11g are conductive. When both first and second input signal voltages Vsa and Vsb are positive, the transistors 11a, 11d and 11h are conductive.

As a result, the output signals from the output lines 31a and 31b are of the OR logic on the basis of the first and second input signals.

4. AND CIRCUIT

Fourth, an embodiment AND circuit according to the present invention is described.

I. Structure of the AND circuit

As shown in Figure 4, the AND circuit has a similar circuit structure as the multiplexer shown in Figure 1. The transistors 11e and 11f and their related circuits and connections are deleted. The input lines 25c and 25g, or the bases of the transistors 11c and 11g, are connected to each other. The input lines 25d and 25h, or the bases of the transistors 11d and 11h, are connected to each other. The output lines 31a and 31b are connected to the emitters of transistors 27a, 27d and 27b, 27c, respectively.

II. Operation of the AND circuit

In the AND circuit shown in Figure 4, compared to the multiplexer shown in Figure 1, the non-inverted and inverted phase components B and Bb of the second differential input signal, instead of the non-inverted and inverted phase components S and Sb of the differential select signal, are fed to the bases of the transistors 11c, 11g and 11d, 11h, respectively. To the bases of the transistors 11a and 11b, the inverted and non-inverted

phase components Ab and A, respectively, instead of the non-inverted and inverted phase components A and Ab of the first differential input signal, are fed. Table IV shows the relationship between the input signal voltages, the base potentials of the transistor pairs and the output voltage.

When both first and second input signal voltages Vsa and Vsb are negative, the current Io flows in each of the transistors 11a, 11d, and 11h. When the first and second input signal voltages Vsa and Vsb are negative and positive, respectively, the transistors 11a, 11c, and 11g are conductive. When the first and second input signal voltages Vsa and Vsb are positive and negative, respectively, the transistors 11b, 11d, and 11h are conductive. When both first and second input signal voltages Vsa and Vsb are positive, the transistors 11b, 11c and 11g are conductive.

As a result, the output signals from the output lines 31a and 31b are of the AND logic on the basis of the first and second input signals.

5. OTHER CIRCUITS

The line 21 may be connected to the ground terminal (the reference potential terminal) and negative voltages may be fed to the lines 15 and 17. The circuit's function is the same as described above.

By replacing all NPN transistors to PNP transistors and altering the high and low potentials, the same function circuits as those described above are provided.

Other logic NOR, NAND and NXOR circuits are formed where the output signals are inverted.

TABLE I (MULTIPLEXER)

Input Signals 1st Vsa	Input Signals 2nd Vsb	Select Signal Vss	Base Potentials Va	Vb	Vc	Vd	Output Potentials V(Y)	V(Yb)	Output Voltage V(Y)-V(Yb)
-	-	-	VCC	VCC-RIo	VCC-RIo	VCC-2RIo	VCC-RIo	VCC	-RIo
-	+	-	VCC	VCC-RIo	VCC-2RIo	VCC-RIo	VCC-RIo	VCC	-RIo
+	-	-	VCC-RIo	VCC	VCC-RIo	VCC-2RIo	VCC	VCC-RIo	RIo
+	+	-	VCC-RIo	VCC	VCC-2RIo	VCC-RIo	VCC	VCC-RIO	RIo
-	-	+	VCC-RIo	VCC-2RIo	VCC	VCC-RIo	VCC-RIo	VCC	-RIo
-	+	+	VCC-RIo	VCC-2RIo	VCC-RIo	VCC	VCC	VCC-RIo	RIo
+	-	+	VCC-2RIo	VCC-RIo	VCC	VCC-RIo	VCC-RIo	VCC	-RIo
+	+	+	VCC-2RIo	VCC-RIo	VCC-RIo	VCC	VCC	VCC-RIO	RIo

TABLE II (XOR)

Input Signals 1st Vsa	Input Signals 2nd Vsb	Base Potentials Va	Vb	Vc	Vd	Output Potentials V(Y)	V(Yb)	Output Voltage V(Y)-V(Yb)
-	-	VCC	VCC-2RIo	VCC-RIo	VCC-RIo	VCC-RIo	VCC	-RIo
-	+	VCC-RIo	VCC-RIo	VCC	VCC-2RIo	VCC	VCC-RIo	RIo
+	-	VCC-RIo	VCC-RIo	VCC-2RIo	VCC	VCC	VCC-RIo	RIo
+	+	VCC-2RIo	VCC	VCC-RIo	VCC-RIo	VCC-RIo	VCC	-RIo

TABLE III (OR)

Input Signals 1st Vsa	2nd Vsb	Base Potentials Va	Vb	Vc	Vd	Output Potentials V(Y)	V(Yb)	Output Voltage V(Y)-V(Yb)
-	-	VCC	VCC-RIo	VCC-RIo	VCC-RIo	VCC-RIo	VCC	-RIo
-	+	VCC-RIo	VCC-RIo	VCC	VCC-RIo	VCC	VC-RIo	RIo
+	-	VCC-RIo	VCC	VCC-RIo	VCC-RIo	VCC	VCC-RIo	RIo
+	+	VCC-2RIo	VCC	VCC	VCC-RIo	VCC	VCC-RIo	RIo

TABLE IV (AND)

Input Signals 1st Vsa	2nd Vsb	Base Potentials Va	Vb	Vc	Vd	Output Potentials V(Y)	V(Yb)	Output Voltage V(Y)-V(Yb)
-	-	VCC-2RIo	VCC	VCC	VCC-RIo	VCC-RIo	VCC	-RIo
	+	VCC-RIo	VCC	VCC-RIo	VCC-RIo	VCC-RIo	VCC	RIo
+	-	VCC-RIo	VCC-RIo	VCC	VCC-RIo	VCC-RIo	VCC	-RIo
+	+	VCC	VCC-RIo	VCC-RIo	VCC-RIo	VCC	VCC-RIo	RIo

WHAT IS CLAIMED IS:

1. A differential ECL circuit comprising:

a plurality of transistor pairs, each comprising first and second transistors whose emitters are connected to each other;

a plurality of constant current sources, each being connected between the connected emitters of each transistor pair and a first potential terminal;

four load resistors connected between the first and second transistors' collectors of two transistor pairs and a second potential terminal;

an emitter follower circuit comprising four emitter follower transistors and two emitter resistors; and

means for providing a plurality of differential input signals to the transistor pairs,

in which:

the first and second transistors' collectors of each of the transistor pairs to which the four load resistors are connected, are connected to the counterparts of the other transistor pairs;

the bases of the four emitter follower transistors are connected to the first and second transistors' collectors of the transistor pairs to which the four load resistors are connected;

the emitters of the two emitter follower transistors are connected to the first potential terminal through the one emitter resistor; and

the emitters of the other two emitter follower transistors are connected to the first potential terminal through the other emitter resistor,

so that a differential output signal is provided across the emitter resistors, depending upon logic states of the differential input signals.

2. A differential ECL circuit according to claim 1, wherein:

the transistor pairs are first, second and third ones;

the first and second transistors' collectors of the second transistor pair are connected to the second transistor's collector of the third transistor pair and to the first transistor's collector of the first transistor pair, respectively;

the four load resistors are connected between the first and second transistors' collectors of the first and third transistor pairs and the second potential terminal;

the four emitter follower transistors are first, second, third and fourth ones;

the two emitter resistors are first and second ones;

the emitters of the first and fourth emitter follower transistors are connected to the first potential terminal through the second emitter resistor;

the emitters of the second and third emitter follower transistors are connected to the first potential terminal through the first emitter resistor;

the differential input signals are first and second ones;

the first differential input signal is provided between the bases of the first and second transistors of the first transistor pair; and

the second differential input signal is provided between the bases of the second and first transistors of the second transistor pair and between the bases of the second and first transistors of the third transistor pair,

so that a differential output signal of an OR or NOR logic based on the first and second differential input signals is provided across the emitter resistors.

3. A differential ECL circuit according to claim 1, wherein:

the transistor pairs are first, second and third ones;

the first and second transistors' collectors of the second transistor pair are connected to the second transistor's collector of the third transistor pair and to the first transistor's collector of the first transistor pair, respectively;

the four load resistors are connected between the first and second transistors' collectors of the first and third transistor pairs and the second potential terminal;

the four emitter follower transistors are first, second, third and fourth ones;

the two emitter resistors are first and second ones;

the emitters of the first and fourth emitter follower transistors are connected to the first potential terminal through the first emitter resistor;

the emitters of the second and third emitter follower transistors are connected to the first potential terminal through the second emitter resistor;

the differential input signals are first and second ones;

the first differential input signal is provided between the bases of the second and first transistors of the first transistor pair; and

the second differential input signal is provided between the bases of the first and second transistors of the second transistor pair and between the bases of the first and second transistors of the third transistor pair,

so that a differential output signal of an AND or NAND logic based on the first and second differential input signals is provided across the emitter resistors.

4. A differential ECL circuit according to claim 1, wherein:

the transistor pairs are first, second, third and fourth ones;

the first and second transistors' collectors of the second transistor pair are connected to the second

transistor's collector of the third transistor pair and to the first transistor's collector of the first transistor pair, respectively;

the first transistor's collector of the second transistor pair is connected to the second transistor's collector of the fourth transistor pair;

the second transistor's collector of the second transistor pair is connected to the first transistor's collector of the first transistor pair;

the first transistor's collector of the third transistor pair is connected to the second transistor's collector of the first transistor pair;

the second transistor's collector of the third transistor pair is connected to the first transistor's collector of the fourth transistor pair;

the four load resistors are connected between the first and second transistors' collectors of the first and third transistor pairs and the second potential terminal;

the four emitter follower transistors are first, second, third and fourth ones;

the two emitter resistors are first and second ones;

the emitters of the first and third emitter follower transistors are connected to the first potential terminal through the second emitter resistor;

the emitters of the second and fourth emitter follower transistors are connected to the first potential terminal through the first emitter resistor;

the differential input signals are first, second and third ones;

the first differential input signal is provided between the bases of the first and second transistors of the first transistor pair;

the second differential input signal is provided between the bases of the first and second transistors of the second transistor pair; and

the third differential input signal is provided between the bases of the second and first transistors of the second transistor pair and between the bases of the first and second transistors of the third transistor pair, so that the first or second differential input signal is selected depending upon the logic state of the third differential signal and is provided across the emitter resistors.

5. A differential ECL circuit according to claim 1, wherein:

the transistor pairs are first, second, third and fourth ones;

the first and second transistors' collectors of the second transistor pair are connected to the second and first transistors' collectors of the first transistor pair, respectively;

the first and second transistors' collectors of the third transistor pair are connected to the second and first transistors' collectors of the fourth transistor pair, respectively;

the four load resistors are connected between the first and second transistors' collectors of the first and fourth transistor pairs and the second potential terminal;

the four emitter follower transistors are first, second, third and fourth ones;

the two emitter resistors are first and second ones;

the emitters of the first and second emitter follower transistors are connected to the first potential terminal through the second emitter resistor;

the emitters of the third and fourth emitter follower transistors are connected to the first potential terminal through the first emitter resistor;

the differential input signals are first and second ones;

the first differential input signal is provided between the bases of the first and second transistors of the first transistor pair and between the bases of the first and second transistors of the fourth transistor pair; and

the second differential input signal is provided between the bases of the second and first transistors of the second transistor pair and between the bases of the first and second transistors of the third transistor pair,

so that a differential output signal of an XOR non-XOR logic based on the first and second differential input signals is provided across the emitter resistors.

6. A differential ECL circuit comprising:

first, second, third and fourth transistor pairs, each comprising first and second transistors whose emitters are connected to each other;

four constant current sources, each being connected between the connected emitters of each transistor pair and a first potential terminal;

four load resistors connected between the first and second transistors' collectors of the first and fourth transistor pairs and a second potential terminal;

first, second, third and fourth emitter follower transistors whose bases are connected to the first and second transistors' collectors of the first and fourth transistor pairs;

first and second emitter resistors, each being connected between the emitters of the two emitter follower transistors and the first potential terminal; and

means for providing a plurality of differential input signals to the transistor pairs,

in which the first and second transistors' collectors of the second and third transistor pairs being connected to the counterparts of the first and fourth transistor pairs,

whereby a differential output signal based on the differential input signals is provided across the emitter resistors.

7. A differential ECL circuit according to claim 6, wherein:

the first and second transistors' collectors of the second transistor pair is connected to the second and first transistors' collectors of the first transistor pair, respectively;

the first and second transistors' collectors of the third transistor pair is connected to the second and first transistors' collectors of the fourth transistor pair, respectively;

the emitters of the first and second emitter follower transistors are connected to the first potential terminal through the first emitter resistor;

the emitters of the third and fourth emitter follower transistors are connected to the first potential terminal through the second emitter resistor;

the differential input signals are first and second ones;

the first differential input signal is provided between the bases of the first and second transistors of the first transistor pair and between the bases of the first and second transistors of the fourth transistor pair; and

the second differential input signal is provided between the bases of the second and first transistors of the second transistor pair and between the bases of the second and first transistors of the third transistor pair,

so that a differential output signal of an XOR or non-XOR logic based on the first and second differential input signals is provided across the emitter resistors.

8. A differential ECL circuit according to claim 6, wherein:

the first transistor's collector of the second transistor pair is connected to the second transistor's collector of the fourth transistor pair;

the second transistor's collector of the second transistor pair is connected to the first transistor's collector of the first transistor pair;

the first transistor's collector of the third transistor pair is connected to the second transistor's collector of the first transistor pair;

the second transistor's collector of the third transistor pair is connected to the first transistor's collector of the fourth transistor pair;

the emitters of the first and third emitter follower transistors are connected to the first potential terminal through the second emitter resistor;

the emitters of the second and fourth emitter follower transistors are connected to the first potential terminal through the first emitter resistor;

the differential input signals are first, second and third ones;

the first differential input signal is provided between the bases of the first and second transistors of the first transistor pair;

the second differential input signal is provided between the bases of the first and second transistors of the fourth transistor pair; and

the third differential input signal is provided between the bases of the second and first transistors of the second transistor pair and between the bases of the first and second transistors of the third transistor pair,

so that the first or second differential input signal is selected depending upon the logic state of the third differential signal and is provided across the emitter resistors.

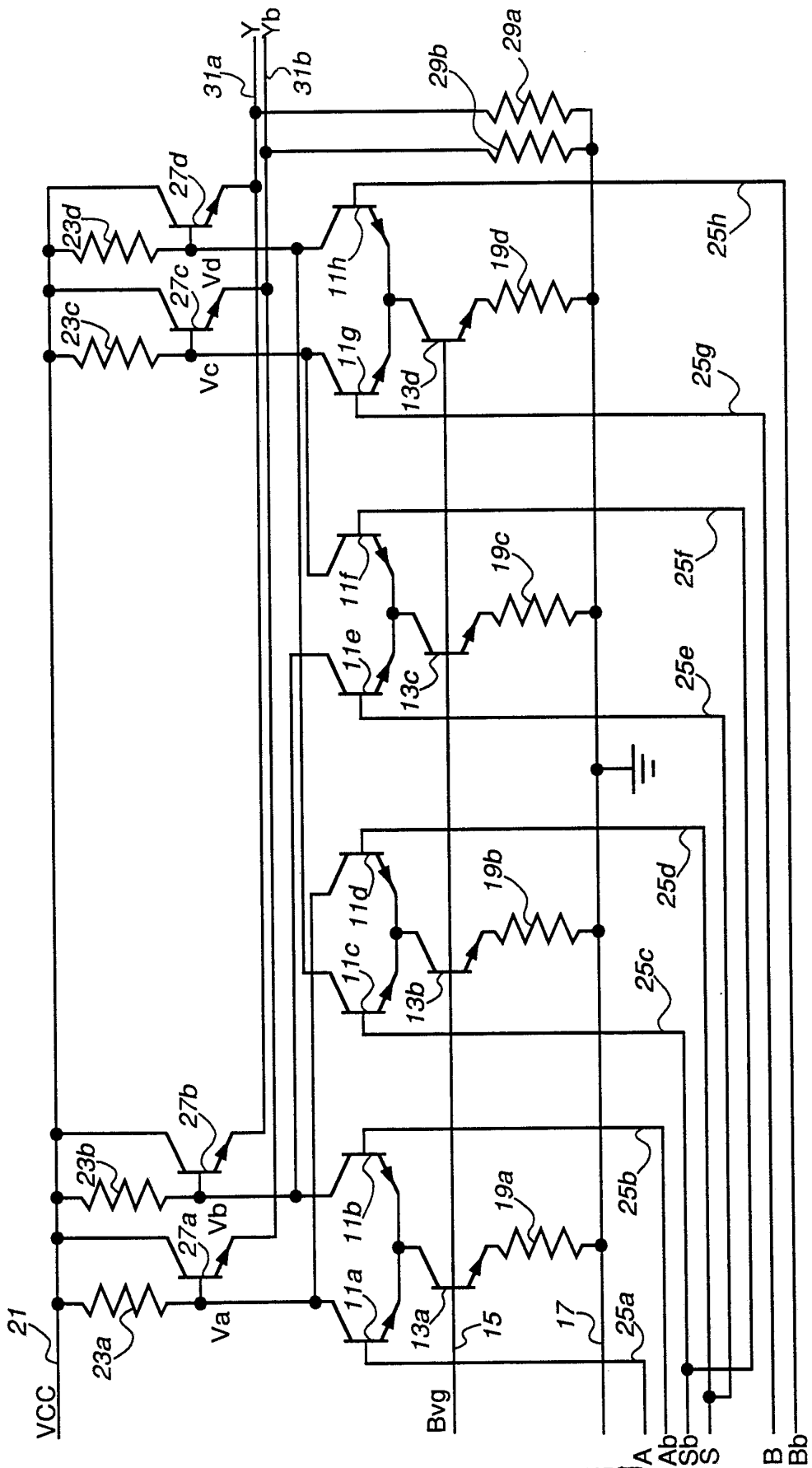
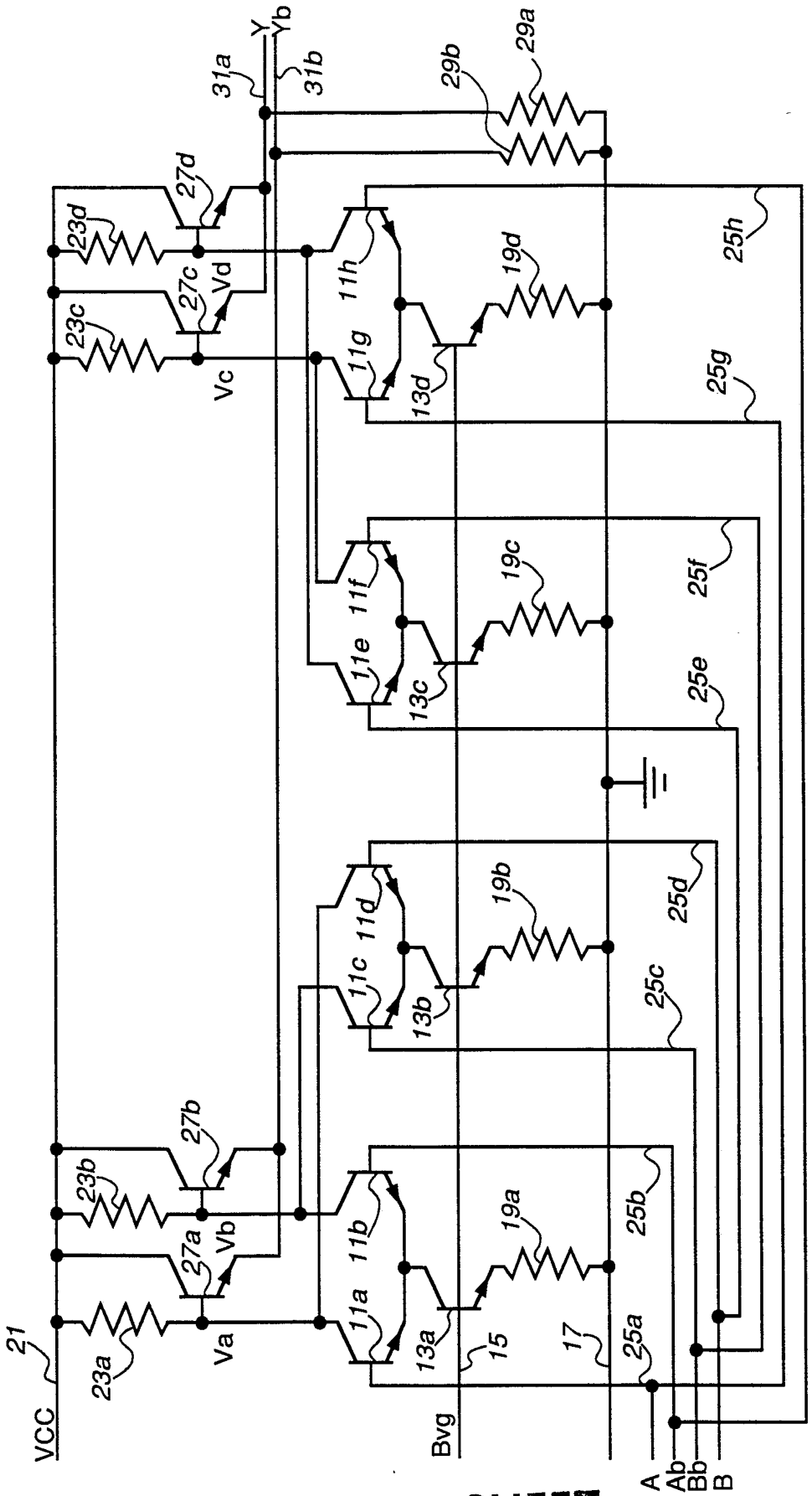

Y
Yb
31a
31b
29a
29b
27d
23d
27c
Vd
23c
Vc
11h
11g
19d
13d
25h
25g
11f
11e
19c
13c
25f
25e
11d
11c
19b
13b
25d
25c
27b
23b
27a
Vb
11b
11a
19a
13a
25b
25a
21
23a
Va
15
17
VCC
Bvg
A
Ab
Sb
S
B
Bb

FIG. 1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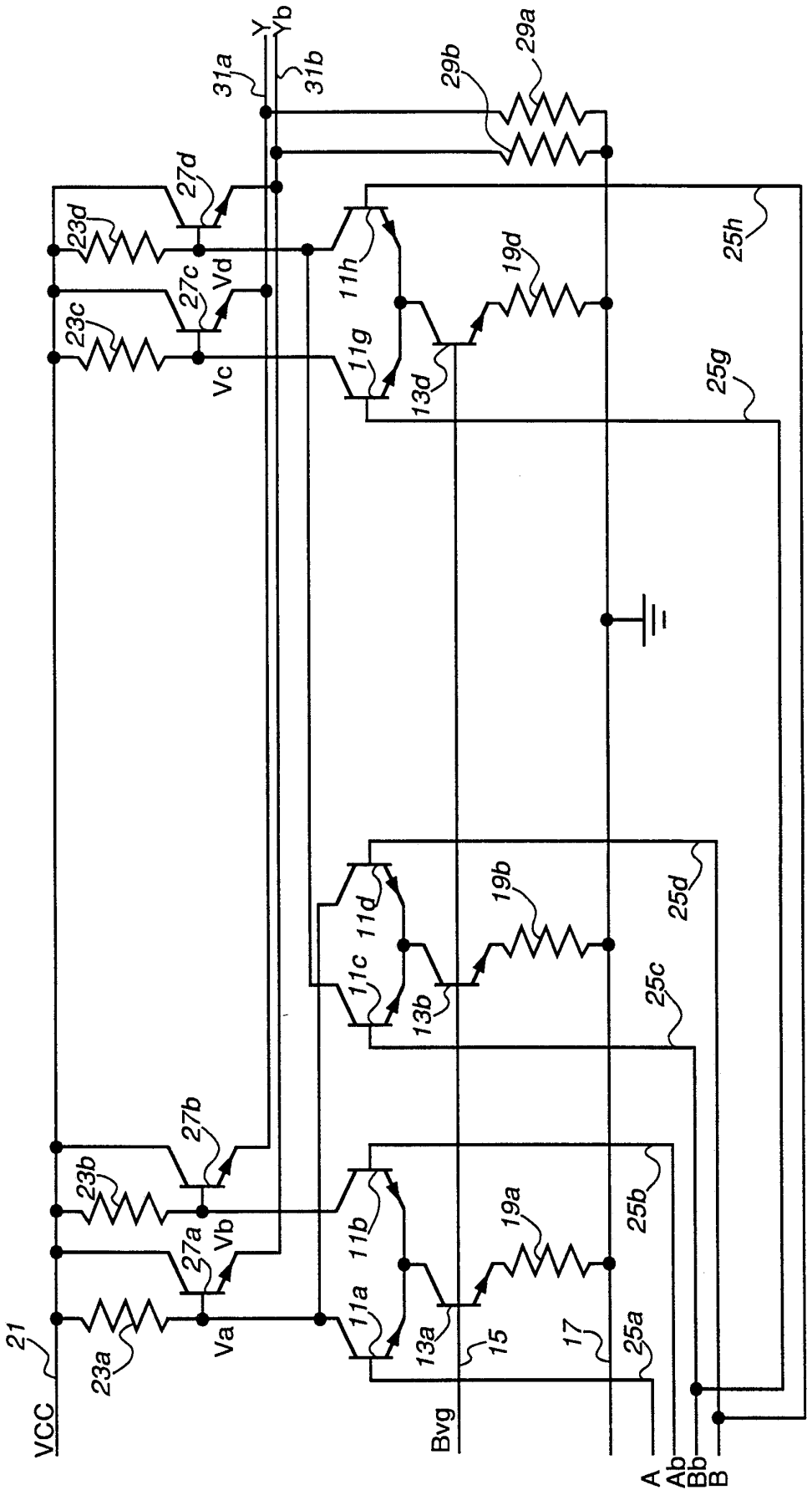
Yb
31a
31b
29b
29a
27d
23d
27c
Vd
23c
Vc
11h
11g
19d
13d
25h
25g
11f
11e
19c
13c
25f
25e
11d
11c
19b
13b
25d
25c
27b
23b
27a
Vb
11b
11a
19a
13a
25b
25a
21
23a
Va
VCC
15
17
Bvg
A
Ab
Bb
B

FIG. 2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Yb
31a
31b
29b
29a
27d
23d
27c
Vd
23c
Vc
11h
19d
25h
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13d
25g
11d
19b
25d
11c
13b
25c
27b
23b
27a
Vb
11b
19a
25b
23a
Va
11a
13a
15
17
25a
21
VCC
Bvg
A
Ab
Bb
B

FIG. 3

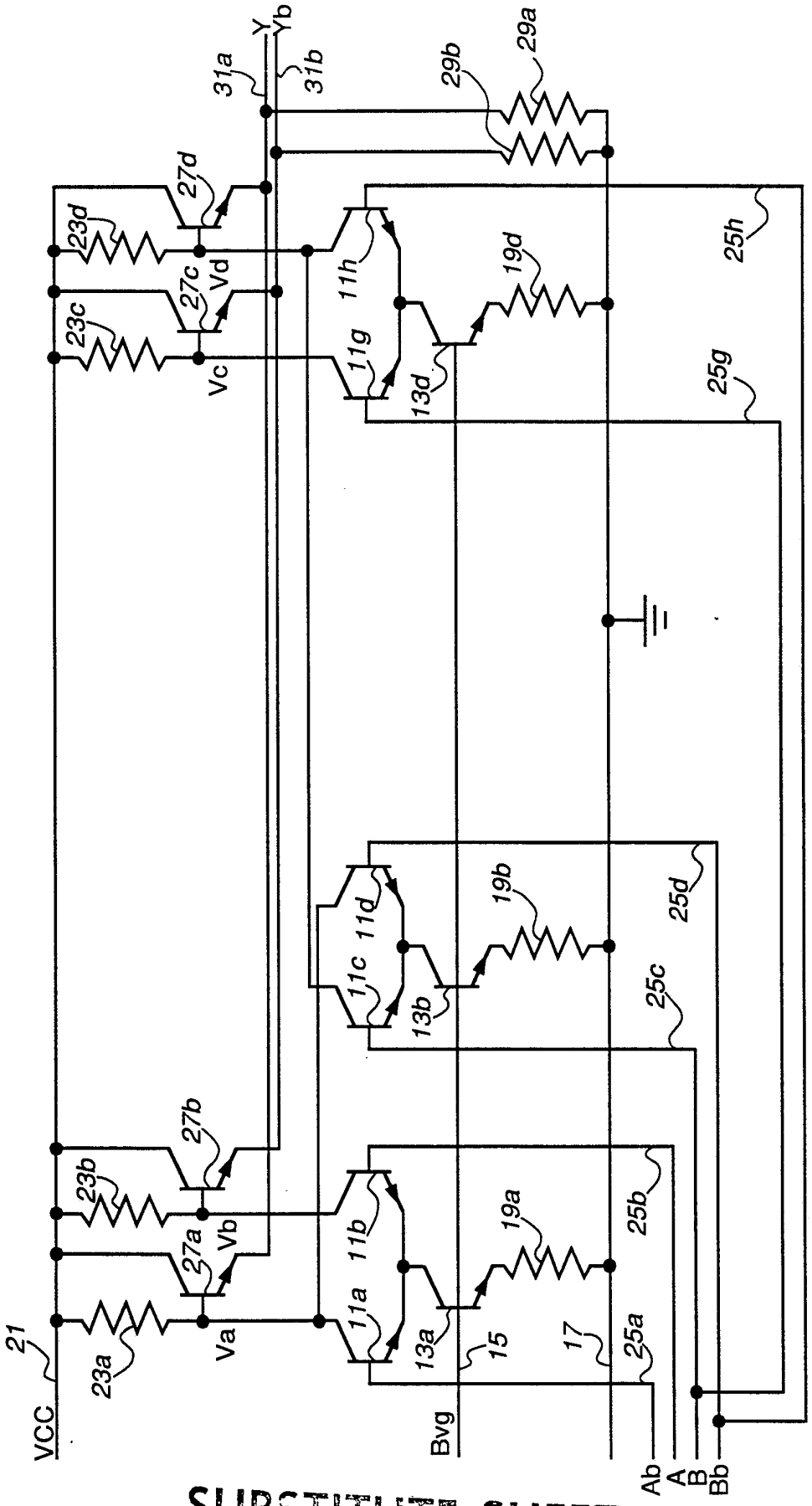
Y
Yb
31a
31b
29b
29a
27d
23d
27c
Vd
23c
Vc
11h
11g
19d
13d
25h
25g
11d
11c
19b
13b
25d
25c
27b
23b
27a
Vb
11b
11a
19a
13a
15
17
25b
25a
21
23a
Va
VCC
Bvg
Ab
A
B
Bb

FIG. 4

INTERNATIONAL SEARCH REPORT

International Application No PCT/CA 92/00494

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl.5 H 03 K 19/086 H 03 K 19/21 H 03 K 17/62

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl.5	H 03 K

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
X Y A	EP,A,0312731 (IBM) 26 April 1989 see column 2, line 11 - column 4, line 25 ---	1 2,5-8 3,4
Y	US,A,4686674 (LAM) 11 August 1987 see column 2, line 66 - column 3, line 30; figures 1,2 ---	2
Y	IBM TECHNICAL DISCLOSURE BULLETIN. vol. 9, no. 9, February 1967, NEW YORK US pages 1210 - 1211 EVANS 'exclusive-or complement circuit' see the whole document --- -/-	5-8

° Special categories of cited documents :[10]

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
29-01-1993	16. 02. 93
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	FEUER F.S.

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	DE,A,1906757 (CONTROL DATA) 11 December 1969 see the whole document -----	5-8

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. CA 9200494 SA 66151

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 10/02/93
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A- 0312731	26-04-89	US-A- 4833421	23-05-89
		JP-A- 1122205	15-05-89
US-A- 4686674	11-08-87	None	
DE-A- 1906757	11-12-69	FR-A- 1601911	21-09-70
		NL-A- 6900536	14-08-69
		US-A- 3535546	20-10-70