(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
05 July 2018 (05.07.2018)

WIPO | PCT

(10) International Publication Number
WO 2018/125201 A1

(51) International Patent Classification:
H01L 21/20 (2006.01) *H01L 21/768* (2006.01)
H01L 21/18 (2006.01) *H01L 21/762* (2006.01)
H01L 21/02 (2006.01)

(21) International Application Number:
PCT/US2016/069465

(22) International Filing Date:
30 December 2016 (30.12.2016)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:
— *of inventorship (Rule 4.17(iv))*

Published:
— *with international search report (Art. 21(3))*

WO 2018/125201 A1

(54) Title: SYNTHESIS OF POLYCARBOSILANES AND DERIVITIZATION TO HIGH DENSITY SIC FILL MATERIAL

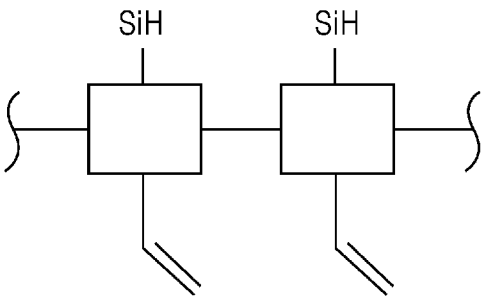


FIG. 1

(57) Abstract: A dielectric film, a device including a dielectric film and a method of forming a dielectric film on a integrated circuit substrate wherein the dielectric film includes cross-linked carbosilane units selected from linear monomer units or at least one linear monomer unit and at least one heterocyclic monomer unit, wherein the linear monomer units include a C_2 to C_8 straight or branched alkenyl or alkynyl and the at least one heterocyclic monomer unit includes a saturated or unsaturated moiety including an even numbered ring structure of alternating silicon and carbon atoms.

SYNTHESIS OF POLYCARBOSILANES AND DERIVITIZATION TO HIGH DENSITY SiC FILL MATERIAL

BACKGROUND

Field

Integrated circuit devices.

Description of Related Art

Dielectric materials having a dielectric constant less than a dielectric constant of silicon dioxide (low-k dielectric materials) are important to enabling new patterning schemes in lithographic processes. Spin coating or spin-on deposition is a procedure used to deposit generally uniform thin films onto integrated circuit chips that are, for example, formed on a single wafer (e.g., a silicon wafer) that is then diced to create individual chips. Spin coating or spin-on deposition may be used to deposit low-k dielectric materials into high aspect ratio trenches providing control over film thickness and gap fill.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a schematic of a homo-oligomer of similar carbosilane units.

Figure 2 shows a schematic of a co-oligomer of two dissimilar carbosilane units.

Figure 3 is a flow chart of a process to form a silicon carbide dielectric film on an integrated circuit substrate.

Figure 4 shows a cross-sectional side view of a portion of a integrated circuit substrate including a device layer, metallization to the device layer and a hard mask of a SiC dielectric material on the metallization.

Figure 5 shows a cross-sectional side view of an embodiment of a semiconductor device structure including a silicon carbide dielectric film.

Figure 6 shows a cross-sectional side view of another embodiment of a semiconductor device structure including a silicon carbide dielectric film or films.

Figure 7 is an interposer implementing one or more embodiments.

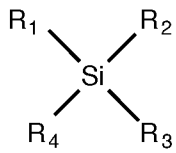
Figure 8 illustrates an embodiment of a computing device.

DETAILED DESCRIPTION

A dielectric film on an integrated circuit substrate including cross-linked carbosilane units is described. In one embodiment, the cross-linked carbosilane units are selected from linear monomer units or at least one linear monomer unit and at least one heterocyclic

monomer unit. A linear monomer unit as used in here includes a C_2 to C_8 straight or branched chain alkenyl or alkynyl and a heterocyclic monomer unit includes a saturated or unsaturated moiety including an even-numbered ring structure of alternating silicon and carbon atoms (e.g.,four to 10 ring members of silicon and carbon atoms). An integrated circuit device including a dielectric film as, for example, an interlayer dielectric film and/or an etch-selective layer is also described. A method of forming a dielectric film is further disclosed. In one embodiment, the method combines a first carbosilane unit with a second carbosilane unit. The oligomer or polymer precursor produced by the combination is then deposited on a substrate such as through the use of a solvent. In one embodiment, the deposition is performed by a spin coating technique. The deposited combination is then cross-linked to form a silicon carbide (SiC) dielectric film. The dielectric film synthesis and processing methods provide silicon carbide films with a minimal amount of oxygen atoms (e.g., two percent or less oxygen atoms). The film offers properties such as low shrinkage, high density, etch selectivity, gap fill and a dielectric constant less than a dielectric constant of silicon dioxide. The low-k dielectric film can be used as an interlayer dielectric, as a spacer material or as a hard mask to enable patterning schemes in which, for example, silicon may be etched selectively relative to other materials such as silicon nitride and silicon dioxide.

In one embodiment, a silicon carbide film is formed by a cross-linking of carbosilane units. The carbosilane units are linear monomer units or linear monomer units and at least one heterocyclic monomer unit. In one embodiment, linear monomer units include a general formula:

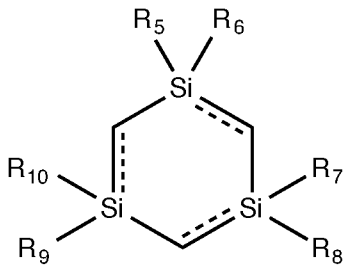


wherein R_1, R_2, R_3 and R_4 are each independently selected of a hydrogen or a C_2-C_4 straight or branched alkenyl or alkynyl, with the proviso that when one of R_1, R_2, R_3 and R_4 is a hydrogen, no more than another one of R_1, R_2, R_3 and R_4 is a hydrogen. Independently selected in this context means that R_1-R_4 may be the same or different or some combination where, for example, two or three may be the same. The proviso also provides that R_1-R_4 cannot each be a hydrogen.

In one embodiment, R_1, R_2, R_3 and R_4 are the same and are for example, vinyl ($-CH=CH_2$), propenyl ($-CH_2CH=CH_2$), butenyl ($-CH_2CH_2CH=CH_2$), ethynyl ($-C\equiv CH$), or

propynyl (-$CH_2C \equiv CH$). In another embodiment, one of R_1, R_2, R_3 and R_4 is hydrogen while the each of the other of R_1, R_2, R_3 and R_4 are each vinyl, propenyl, butenyl, ethynyl or propynyl or are not each the same moiety but are individually selected from vinyl, propenyl, butenyl, ethynyl or propynyl. In another embodiment, two of R_1, R_2, R_3 and R_4 are hydrogen and the other two of R_1, R_2, R_3 and R_4 are each vinyl, propynyl, butenyl, ethynyl, or propenyl or are not each the same moiety but are individually selected from vinyl, propenyl, butenyl, ethynyl or propynyl. In one embodiment, the unsaturated group (e.g., a double bond, a triple bond) is located at a terminal end of the group. The unsaturated side chains represented by, for example, an alkenyl or alkynyl group promote cross-linking reactions that densify a silicon carbide film and minimize evaporation at elevated temperatures. Strained organic rings (e.g., C_3-C_6 unsaturated rings) (e.g., cyclopropyl, cyclobutyl, cyclopentyl, cyclohexyl) and silylene groups (e.g., SiH_2) could also be incorporated on one or more of R_1, R_2, R_3 and R_4 to promote cross-linking reactions.

In addtion to linear monomer units, in one embodiment, a carbosilane unit includes at least one heterocyclic monomer unit. In one embodiment, the heterocyclic monomer unit is an even numbered ring structure of alternating silicon and carbon atoms with optional side chains on the silicon atoms independently selected from a C2-C4 alkenyl or alkynyl such as the alkenyls and alkynyls identified above. In one embodiment, the at least one heterocyclic monomer unit is a saturated or unsaturated moiety of 4 to 10 ring members of silicon and carbon atoms. In one embodiment, the at least one heterocyclic monomer unit has a formula:



wherein dashed lines represent an optional bond and R_5, R_6, R_7, R_8, R_9 and R_{10} are each independently selected of a hydrogen or a C_2-C_4 straight or branched alkenyl or alkynyl (R_5-R_{10} may be the same or different). Examples include, but are not limited to, where each of R_5-R_{10} are a hydrogen; where R_5, R_7 and R_9 are each a hydrogen and R_6, R_8 and R_{10} are each independently a C_2-C_4 straight or branched alkenyl or alkynyl; and where each of R_5-R_{10} is a C_2-C_4 straight or branched chain alkenyl or alkynyl. In another embodiment, the heterocyclic monomer unit is a saturated or unsaturated disilacyclobutane (C_2Si_2) with optional side chains on the silicon atoms such as described.

In one embodiment, each of R_5-R_{10} is individually selected from vinyl, propenyl, butenyl, ethynyl and propynyl. In another embodiment, one of R_5-R_{10} is a hydrogen (resulting in an SiH_2 when no double bond is present between the silicon atom and a carbon atom of the ring). In this embodiment, the other of R_5-R_{10} is independently selected from a straight or branched chain alkenyl or alkynyl such as vinyl, propenyl, butenyl, ethynyl and propynyl. In a further embodiment, two of R_5, R_6, and R_7 are a hydrogen and the other of R_5-R_{10} is individually selected from a straight or branched alkenyl or alkynyl such as propenyl, butenyl, ethynyl or propynyl.

In one embodiment, the carbosilane units, either linear monomer units or linear monomer units and at least one heterocyclic monomer unit are directly linked to form C-Si bonds or Si-Si bonds with no intermediates, such as oxygen there between. In one embodiment the resulting carbosilane polymer contains minimal oxygen such as an oxygen content of two percent or less. **Figure 1** illustrates a cross-linking of two similar carbosilane units to form an oligomer (a homo-oligomer). The cross-linking is directly through the reactive functional groups (e.g., R_1-R_{10}). **Figure 2** illustrates a cross-linking according to another embodiment involving two dissimilar carbosilane units (monomer units to form a co-oligomer).

In one embodiment, by varying the functional groups of the linear monomer units or heterocyclic monomer units, a silicon to carbon ratio in the resulting polycarbosilane polymer may be varied.

Figure 3 presents a flow chart of a method of forming a SiC film. In one embodiment, the carbosilane units, either linear monomer units or at least one heterocyclic monomer unit are combined to form an oligomer or polymer precursor or short chain polymer (block 310, **Figure 3**). Polymer synthesis includes dehydrogenative coupling involving two silane molecules coupling to form Si-Si bonds eliminating hydrogen gas. Hydrosilation is another process involving the insertion of a Si-H bond across unsaturated bonds such as alkynes, alkynes, carbonyls and a means to form Si-C bonds. In another embodiment a combination of dehydrogenative coupling and hydrosilation may be used to produce a polymer with Si-C and Si-Si bonds.

In one embodiment, a polymerization reaction employs a catalyst such as a homogenous catalyst including, but not limited to, rhodium (Rh), platinum (Pt), ruthenium (Ru), zirconium (Zr) and Lewis acids at relatively low catalyst loadings (e.g., 0.05-5 mol %). Alternatively, a heterogeneous catalyst such as a transition metal or metals (e.g., Rh and/or Pt) supported on a substrate may also be used. A heterogeneous catalyst allows purification

of the catalyst from the polymer following the polymerization reaction as such catalysts are, for example, a solid that may be separated from a solution of the polymer by filtration. Purification can be improved using metals scavengers, silica gel or alumina that lower metal contaminations to few parts per billion.

The polymerization of the carbosilane units produces a solution including oligomers of cross-linked carbosilane units (polymer precursors or short chain polymers) (block 320, **Figure 3**). To form a stable low-k dielectric, the oligomers and short chain polymers may be cross-linked further after being applied to a substrate. In one embodiment, oligomers and short chain polymers are combined with a solvent such as toluene to form a solution. The solution is applied to a substrate by a spin coating process to define a film of a desired thickness (block 330, **Figure 3**). Following deposition, the composition is subject to a cure process to drive off the solvent and further polymerize the oligomers and short chain polymers (block 340, **Figure 3**). Representative cure processes include, but are not limited to, a rapid thermal anneal, a high pressure anneal, a reactive gas anneal (e.g., oxygen, ammonia, silane, hydrogen, hydrogen/nitrogen, ethylene, acetylene or ultraviolet (UV) radiation, electron beam radiation, and a remote or direct plasma). In one embodiment, a catalyst such as the homogeneous catalysts listed including, but not limited to, rhodium (Rh), platinum (Pt), ruthenium (Ru), zirconium (Zr) and Lewis acids may be incorporated into the silicon carbide film during the cure. The following table presents representative cure conditions for representative cure processes to cure a SiC film:

Cure	Atmosphere	Temperature (°C)	Time (s)
Rapid thermal anneal	N2 or H2/N2 (1 atm)	650	60
High pressure anneal	N2 or NH3 (20 atm)	450	hours
Reactive gas anneal	O2 (2-3 atm)	400	minutes
UV radiation (200-400 nm)	N2	<400	minutes

Figure 4 shows a cross-sectional side view of a portion of a substrate having a device layer, metallization to the device layer and a dielectric film on the metallization including SiC as a hard mask. Substrate 410 is, for example, a semiconductor substrate such as a bulk semiconductor substrate (e.g., bulk silicon substrate) or a silicon on insulator (SOI) substrate. Formed on substrate 410 is device layer 415 of, for example, transistor devices (e.g., hundreds of thousands to millions of transistor devices) and possibly other devices (e.g., capacitors resistors, etc.). Disposed on device layer 415 is dielectric layer 417 such as an initial interlayer dielectric (ILD0) of silicon dioxide or a material having a dielectric constant less than silicon dioxide (a low-k material). Formed in ILD0 are contacts to ones of devices

in device layer 415 (not shown) and interconnect or metal layer 420 that is, for example, a series of metal lines or traces (e.g., copper traces) between device contacts that form circuits and transmit power throughout a substrate area. Overlying metal layer 420 and dielectric layer 417 is dielectric material 430 patterned to be disposed on lines or traces of metal layer 420. Disposed between openings in dielectric material 430 is hard mask 425 of, for example, a SiC film formed as described above. In one embodiment, dielectric material 430 is a material having etch characteristics different than hard mask 425 for a particular etchant. A representative material is silicon nitride. In this manner, dielectric material 430 may be selectively etched relative to hard mask 425. In one embodiment, dielectric material 430 may be selectively removed relative to hard mask 425 to expose lines or traces of metal layer 420 to allow electrically conductive interconnects to be connected to the lines or traces.

The example described in conjunction with **Figure 4** is one example of a use of a SiC film such as a described herein as a mask in integrated circuit processing. In another embodiment of a mask use, an SiC material deposited by spin coating may be used in multiple patterning techniques such as self-aligned double patterning to enhance feature density.

Figure 5 shows a cross-sectional schematic side view of an example semiconductor structure configured with a low-k interlayer dielectric in accordance with one embodiment of the present invention. This example case includes a metal oxide semiconductor (MOS) transistor formed on substrate 500. As will be appreciated, the transistor may be a planar configuration, or a non-planar configuration where the depicted side-view cross-section is taken parallel along a body or fin surrounded by dielectric material on the substrate. As will be further appreciated, any number of semiconductor devices may employ a low-k SiC dielectric or insulator material as described herein, and the disclosure is not intended to be limited to any particular type of integrated circuit.

As can be seen, a gate stack is formed over a channel region of the device, and includes gate dielectric layer 502, gate electrode 504, and optional hardmask 506. Spacers 510 are formed adjacent to the gate stack. Gate dielectric 502 can be, for example, any suitable oxide such as silicon dioxide (SiO_2) or a high-k gate dielectric materials. Examples of high-k gate dielectric materials include, for instance, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In general, the thickness of gate dielectric 502 should be

sufficient to electrically isolate gate electrode 504 from the source and drain contacts. In some specific example embodiments, high-k gate dielectric layer 502 may have a thickness in the range of 5 Å to around 100 Å thick (e.g., 10 Å). In some embodiments, additional processing may be performed on high-k gate dielectric layer 502, such as an annealing process to improve the quality of the high-k material. Gate electrode 504 can be, for example, polysilicon, silicon nitride, silicon carbide, or a metal layer (e.g., tungsten, titanium nitride, tantalum, tantalum nitride) although other suitable gate electrode materials can be used as well. A material of gate electrode 504, which may be a sacrificial material that is later removed for a replacement metal gate (RMG) process, has a representative thickness in the range of about 10 Å to 500 Å (e.g., 100 Å), in some example embodiments. Optional gate hard mask layer 506 can be used to provide certain benefits or uses during processing, such as protecting gate electrode 504 from subsequent etch and/or ion implantation processes. Hard mask layer 506 may be formed using typical hard mask materials, such as such as silicon dioxide, silicon nitride, and/or other conventional insulator materials. The gate stack can be formed as conventionally done or using any suitable custom techniques (e.g., conventional patterning process to etch away portions of the gate electrode and the gate dielectric layers to form the gate stack). Each of gate dielectric 502 and gate electrode 504 may be formed, for example, using conventional deposition processes such as chemical vapor deposition (CVD), atomic layer deposition (ALD), spin-on deposition (SOD), or physical vapor deposition (PVD). Alternate deposition techniques may be used as well, for instance, gate dielectric 502 and gate electrode 504 materials may be thermally grown. As will be appreciated, any number of other suitable materials, geometries, and formation processes can be used to implement an embodiment of the present invention, so as to provide a semiconductor device or structure having a low-k SiC dielectric as described herein. Spacers 5l0 may be formed, for example, using conventional materials such as silicon oxide, silicon nitride, or other suitable spacer materials. The width of the spacers SlO may generally be chosen based on design requirements for the transistor being formed.

Any number of suitable substrates can be used to implement substrate 500, including bulk substrates, semiconductors-on-insulator substrates (XOI, where X is a semiconoductor material such as silicon, germanium, or germanium-enriched silicon), and multi-layered structures, including those substrates upon which fins or nanowires can be formed prior to a subsequent gate patterning process. In some specific example cases, substrate 500 is a germanium or silicon or SiGe bulk substrate, or a germanium or silicon or SiGe on oxide substrate. Although a few examples of materials from which substrate 500 may be formed

are described here, other suitable materials that may serve as a foundation upon which semiconductor devices having a low-k dielectric may be built falls within the spirit and scope of the claimed invention.

With further reference to **Figure 5**, the example device also includes source/drain regions 512, which may be p-type or n-type. As will be appreciated, the composition, doping, and geometry of source/drain regions 512 will vary depending on factors such as the composition of substrate 500, polarity of the device, the use of grading for lattice matching/compatibility, and the overall desired thickness of the total source/drain deposition. Numerous material system and doping configurations can be implemented, as will be appreciated. In some example embodiments, source/drain regions 512 are implemented with doped silicon or silicon germanium. Liners and/or buffer layers may be provided as well, as sometimes done. In the example embodiment shown, source/drain regions 512 are implemented with a raised configuration and include source/drain extensions 512A or so-called tip regions in relatively close proximity to the channel region so as to impart a larger hydrostatic stress on the channel. Other embodiments may include tip regions implemented with a diffusion-based process where the tip regions generally do not induce a strain on the channel region.

As will be appreciated, any number of other transistor configurations may be implemented. For instance, the channel may be strained or unstrained, and the source/drain regions may or may not include tip regions formed in the area between the corresponding source/drain region and the channel region. In this sense, whether a transistor structure has strained or unstrained channels, or source/drain tip regions or no source/ drain tip regions, is not particularly relevant to various embodiments of the present invention, and the claimed invention is not intended to be limited to any particular such structural features. Rather, any number of transistor structures and types can benefit from employing a low-k dielectric as described herein.

As can be further seen, the device includes insulator layer 514 that has been deposited and then planarized down to hard mask 506. Insulator layer 514 may be formed, for example, using low-k dielectric (insulator) materials as provided herein. In such applications, insulator layer 514 is some- times referred to as an interlayer dielectric (ILD), and provides electrical insulation between the source/drain and gate electrodes, as well as between neighboring devices. The ILD also can be used to provide structural support. In another embodiment, hard mask 506 or spacers 510 are a low-k SiC dielectric material and insulator layer 514 is selected of another low-k dielectric material other than SiC.

The example embodiment of **Figure 5** further includes contact resistance reducing metal 516, which in some embodiments include silver, nickel, aluminum, titanium, gold, gold-germanium, nickel-platinum or nickel-aluminum, and/or other such resistance reducing metals or alloys. Contact plug metal 518, which in some embodiments includes aluminum or tungsten, although any suitably conductive contact metal or alloy can be used, such as silver, nickel-platinum or nickel-aluminum or other alloys of nickel and aluminum, or titanium, using conventional deposition processes. Metalization of the source/drain contacts can be carried out, for example, using a silicidation process (gener- ally, deposition of contact metal and subsequent annealing).

Figure 6 shows a cross-section side view of an example semiconductor structure configured with a low-k interlayer dielectric in accordance with another example embodiment of the present invention. As can be seen, **Figure 6** is drawn to reflect example real world process limitations, in that the features are not drawn with precise right angles and straight lines. This example semiconductor structure includes substrate 610 with multiple layers of dielectric (ILD 614A and ILD 614B) and inter-connect metal (metal (Ml) 618A and via 618B) formed thereon, with various devices formed in the substrate and some of the layers (such as device 610A, device 610B and device 610C), which can be, for example, transistors, diodes, capacitors, inductors or any other passive and/or active devices). As will be appreciated, actual details of the devices are not particularly relevant or otherwise necessary for understanding of the dicslosure. The dielectric material of ILD 614A and ILD 614B can be implemented with low-k SiC dielectric material as described herein and can be used, for example, to separate conductors from other conductors, or conductors from devices, or devices from devices, etc. The semiconductor configurations that can utilize such dielectric materials as provided herein are effectively unlimited, and **Figures 5-6** are merely provided as examples only and are not intended to limit the disclosure. Factors such as etch selectivity, desired electrical isolation, and/or distance between conductive features to be isolated can be considered in implementing a given configuration.

Figure 7 illustrates interposer 700 that includes one or more embodiments. Interposer 700 is an intervening substrate used to bridge a first substrate 702 to second substrate 704. First substrate 702 may be, for instance, an integrated circuit die. Second substrate 704 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of interposer 700 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, interposer 700 may connect an

integrated circuit die to ball grid array (BGA) 706 that can subsequently be connected to second substrate 704. In some embodiments, first and second substrates 702/704 are attached to opposing sides of interposer 700. In other embodiments, first and second substrates 702/704 are attached to the same side of interposer 700. In further embodiments, three or more substrates are interconnected by way of interposer 700.

Interposer 700 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

The interposer may include metal interconnects 708 and vias 710, including but not limited to through-silicon vias (TSVs) 712. Interposer 700 may further include embedded devices 714, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on interposer 700.

In accordance with embodiments, apparatuses or processes disclosed herein may be used in the fabrication of interposer 700.

Figure 8 illustrates computing device 800 in accordance with one embodiment. Computing device 800 may include a number of components. In one embodiment, these components are attached to one or more motherboards. In an alternate embodiment, these components are fabricated onto a single system-on-a-chip (SoC) die rather than a motherboard. The components in computing device 800 include, but are not limited to, integrated circuit die 802 and at least one communication chip 808. In some implementations communication chip 808 is fabricated as part of integrated circuit die 802. Integrated circuit die 802 may include CPU 804 as well as on-die memory 806, often used as cache memory, that can be provided by technologies such as embedded DRAM (eDRAM) or spin-transfer torque memory (STTM or STTM-RAM).

Computing device 800 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components include, but are not limited to, volatile memory 810 (e.g., DRAM), non-volatile memory 812 (e.g., ROM or flash memory), graphics processing unit 814 (GPU), digital signal processor 816, crypto processor 842 (a specialized processor that executes

cryptographic algorithms within hardware), chipset 820, antenna 822, display or a touchscreen display 824, touchscreen controller 826, battery 828 or other power source, a power amplifier (not shown), global positioning system (GPS) device 844, compass 830, motion coprocessor or sensors 832 (that may include an accelerometer, a gyroscope, and a compass), speaker 834, camera 836, user input devices 838 (such as a keyboard, mouse, stylus, and touchpad), and mass storage device 840 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

Communications chip 808 enables wireless communications for the transfer of data to and from computing device 800. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. Communication chip 808 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. Computing device 800 may include a plurality of communication chips 808. For instance, a first communication chip may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

Processor 804 of computing device 800 includes dielectric material isolating or masking electrical conductors and devices such as low-k SiC materials formed in accordance with embodiments presented above. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

Communication chip 808 may also include dielectric material isolating or masking electrical conductors and devices such as low-k SiC materials formed in accordance with embodiments presented above.

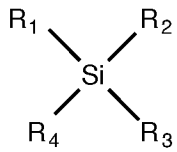
In further embodiments, another component housed within computing device 800 may contain dielectric material isolating or masking electrical conductors and devices such as low-k SiC materials formed in accordance with implementations presented above.

In various embodiments, computing device 800 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, computing device 800 may be any other electronic device that processes data.

EXAMPLES

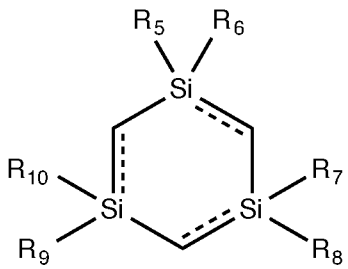
Example 1 is a dielectric film on a integrated circuit substrate including cross-linked carbosilane units selected from linear monomer units or at least one linear monomer unit and at least one heterocyclic monomer unit, wherein the linear monomer units include a C_2 to C_8 straight or branched alkenyl or alkynyl and the at least one heterocyclic monomer unit includes a saturated or unsaturated moiety including an even numbered ring structure of alternating silicon and carbon atoms.

In Example 2, the linear monomer unit of the dielectric film of Example 1 includes a general formula:



wherein R_1, R_2, R_3 and R_4 are each individually selected of a hydrogen or a C_2-C_4 straight or branched alkenyl or alkynyl, with the proviso that when one of R_1, R_2, R_3 and R_4 is a hydrogen, no more than another of R_1, R_2, R_3 and R_4 is a hydrogen.

In Example 3, the at least one heterocyclic monomer unit of the dielectric film of Example 1 or 2 includes a general formula:



wherein dashed lines represent an optional bond and R_5, R_6 and R_7 are each individually selected of a hydrogen or a C_2-C_4 straight or branched alkenyl or alkynyl.

In example 4, the heterocyclic monomer unit of the dielectric film of Example 3 is saturated.

In Example 5, an amount of oxygen atoms in the dielectric film of any of Examples 1-

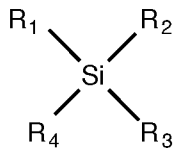
4 is two percent or less.

In Example 6, the monomer units of the dielectric film of any of Examples 1-4 are directly linked.

In Example 7, the carbosilane units of the dielectric film of any of Examples 1-4 are different.

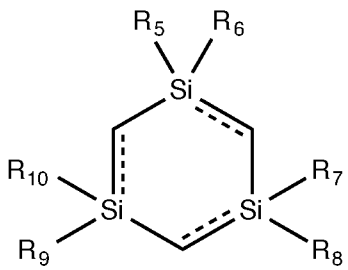
Example 8 is an integrated circuit including a dielectric film disposed on a substrate including a plurality of integrated circuit devices, the film included of cross-linked carbosilane units selected from linear monomer units or at least one linear monomer unit and at least one heterocyclic monomer unit, wherein the linear monomer units include a C_2 to C_8 straight or branched alkenyl or alkynyl and the at least one heterocyclic monomer unit includes a saturated or unsaturated moiety including an even numbered ring structure of alternating silicon and carbon atoms.

In Example 9, the linear monomer unit of the device of Example 8 includes a general formula:



wherein R_1, R_2, R_3 and R_4 are each individually selected of a hydrogen or a C_2-C_4 straight or branched alkenyl or alkynyl, with the proviso that when one of R_1, R_2, R_3 and R_4 is a hydrogen, no more than another of R_1, R_2, R_3 and R_4 is a hydrogen.

In Example 10, the at least one heterocyclic monomer unit of the device of Example 8 includes a general formula:



wherein dashed lines represent an optional bond and R_5, R_6 and R_7 are each individually selected of a hydrogen or a C_2-C_4 straight or branched alkenyl or alkynyl.

In Example 11, the heterocyclic monomer unit of the device of Example 10 is saturated.

In Example 12, an amount of oxygen atoms in the dielectric film of the device of Example 8 is two percent or less.

In Example 13, the monomer units of the device of Example 8 are directly linked.

In Example 14, the dielectric film of any of Examples 1-6 is a hard mask layer.

Example 15 is a method of forming a dielectric film including combining a first carbosilane unit with a second carbosilane unit wherein the first carbosilane unit and the second carbosilane unit are each selected from linear monomer units or one linear monomer unit and one heterocyclic monomer unit and the linear monomer unit includes a C_2 to C_8 straight or branched alkenyl or alkynyl and the one heterocyclic monomer unit includes a saturated or unsaturated moiety including an even numbered ring structure of alternating silicon and carbon atoms; and depositing the combination on a substrate; cross-linking the combination to form a dielectric film.

In Example 16, combining a first carbosilane unit with a second carbosilane unit in the method of Example 15 includes stimulating an oligomerization of the first carbosilane unit with the second carbosilane unit with a catalyst.

In Example 17, the catalyst of the device of Example 16 includes a transition metal catalyst.

In Example 18, the catalyst of the device of Example 17 includes a heterogenous transition metal catalyst.

In Example 19, the catalyst of the device of Example 16 includes a Lewis acid.

In Example 20, after combining and prior to depositing the combination on the substrate, the method of any of Examples 15-19 includes removing a portion of the catalyst from the combination.

In Example 21, cross-linking of the method of any of Examples 15-20 includes annealing the combination.

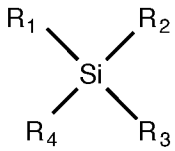
The above description of illustrated implementations, including what is described in the Abstract, is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific implementations of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope, as those skilled in the relevant art will recognize.

These modifications may be made in light of the above detailed description. The terms used in the following claims should not be construed to limit the invention to the specific implementations disclosed in the specification and the claims. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

CLAIMS

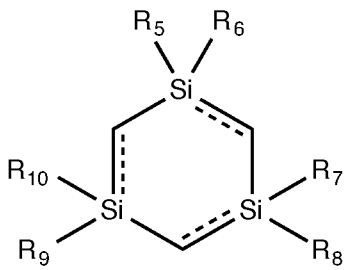
1. A dielectric film on a integrated circuit substrate comprising cross-linked carbosilane units selected from linear monomer units or at least one linear monomer unit and at least one heterocyclic monomer unit, wherein the linear monomer units comprise a C_2 to C_8 straight or branched alkenyl or alkynyl and the at least one heterocyclic monomer unit comprises a saturated or unsaturated moiety comprising an even numbered ring structure of alternating silicon and carbon atoms.

2. The dielectric film of claim 1, wherein the linear monomer unit comprises a general formula:



wherein R_1, R_2, R_3 and R_4 are each independently selected of a hydrogen or a C_2-C_4 straight or branched alkenyl or alkynyl, with the proviso that when one of R_1, R_2, R_3 and R_4 is a hydrogen, no more than another one of R_1, R_2, R_3 and R_4 is a hydrogen.

3. The dielectric film of claim 1, wherein the at least one heterocyclic monomer unit comprises a general formula:



wherein dashed lines represent an optional bond and R_5, R_6, R_7, R_8, R_9 and R_{10} are each individually selected of a hydrogen or a C_2-C_4 straight or branched alkenyl or alkynyl.

4. The dielectric film of claim 3, wherein the heterocyclic monomer unit is saturated.

5. The dielectric film of claim 1, wherein an amount of oxygen atoms in the dielectric film is two percent or less.

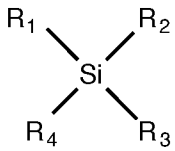
6. The dielectric film of claim 1, wherein the monomer units are directly linked.

7. The dielectric film of claim 1, wherein the carbosilane units are different.

8. An integrated circuit comprising:

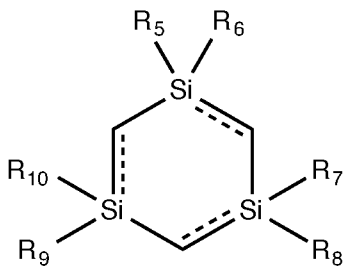
a dielectric film disposed on a substrate comprising a plurality of integrated circuit devices, the film comprised of cross-linked carbosilane units selected from linear monomer units or at least one linear monomer unit and at least one heterocyclic monomer unit, wherein the linear monomer units comprise a C_2 to C_8 straight or branched alkenyl or alkynyl and the at least one heterocyclic monomer unit comprises a saturated or unsaturated moiety comprising an even numbered ring structure of alternating silicon and carbon atoms.

9. The device of claim 8, wherein the linear monomer unit comprises a general formula:



wherein R_1, R_2, R_3 and R_4 are each independently selected of a hydrogen or a C_2-C_4 straight or branched alkenyl or alkynyl, with the proviso that when one of R_1, R_2, R_3 and R_4 is a hydrogen, no more than another of R_1, R_2, R_3 and R_4 is a hydrogen.

10. The device of claim 8, wherein the at least one heterocyclic monomer unit comprises a general formula:



wherein dashed lines represent an optional bond and R_5, R_6, R_7, R_8, R_9 and R_{10} are each independently selected of a hydrogen or a C_2-C_4 straight or branched alkenyl or alkynyl.

11. The device of claim 10, wherein the heterocyclic monomer unit is saturated.

12. The device of claim 8, wherein an amount of oxygen atoms in the dielectric film is

two percent or less.

13. The device of claim 8, wherein the monomer units are directly linked.

14. A method of forming a dielectric film comprising:

combining a first carbosilane unit with a second carbosilane unit wherein the first carbosilane unit and the second carbosilane unit are each selected from linear monomer units or one linear monomer unit and one heterocyclic monomer unit and the linear monomer unit comprises a C_2 to C_8 straight or branched alkenyl or alkynyl and the one heterocyclic monomer unit comprises a saturated or unsaturated moiety comprising an even numbered ring structure of alternating silicon and carbon atoms;

depositing the combination on a substrate; and

cross-linking the combination to form a dielectric film.

15. The method of claim 14, wherein combining a first carbosilane unit with a second carbosilane unit comprises stimulating an oligomerization of the first carbosilane unit with the second carbosilane unit with a catalyst.

16. The method of claim 15, wherein the catalyst comprises a transition metal catalyst.

17. The method of claim 16, wherein the catalyst comprises a heterogenous transition metal catalyst.

18. The method of claim 15, wherein the catalyst comprises a Lewis acid.

19. The method of claim 15, wherein after combining and prior to depositing the combination on the substrate, the method comprises removing a portion of the catalyst from the combination.

20. The method of claim 14, wherein cross-linking comprises annealing the combination.

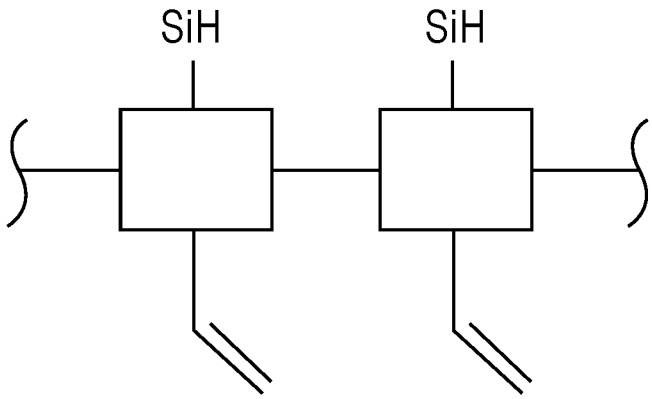


FIG. 1

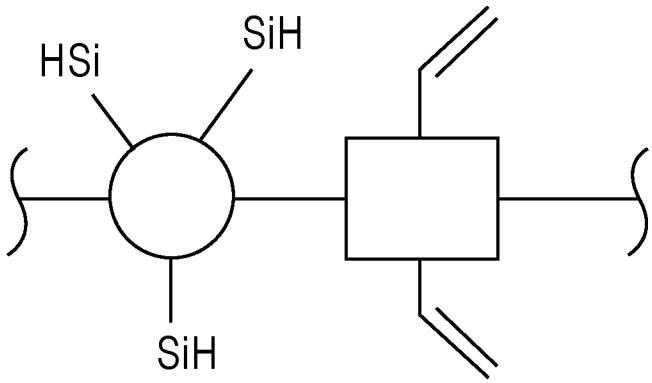


FIG. 2

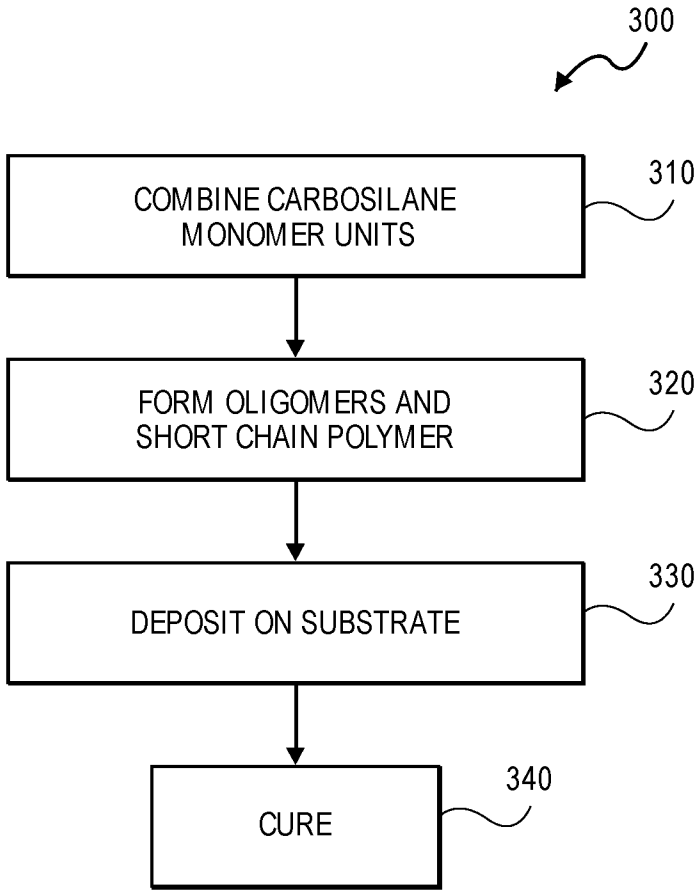

300
COMBINE CARBOSILANE MONOMER UNITS
310
FORM OLIGOMERS AND SHORT CHAIN POLYMER
320
DEPOSIT ON SUBSTRATE
330
CURE
340

FIG. 3

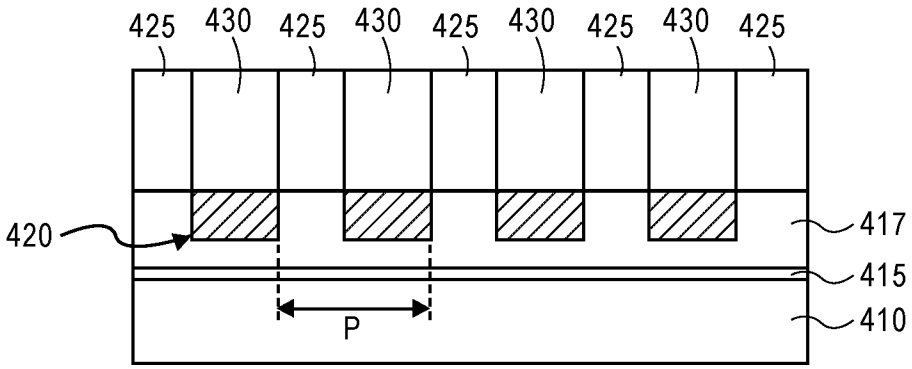

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FIG. 4

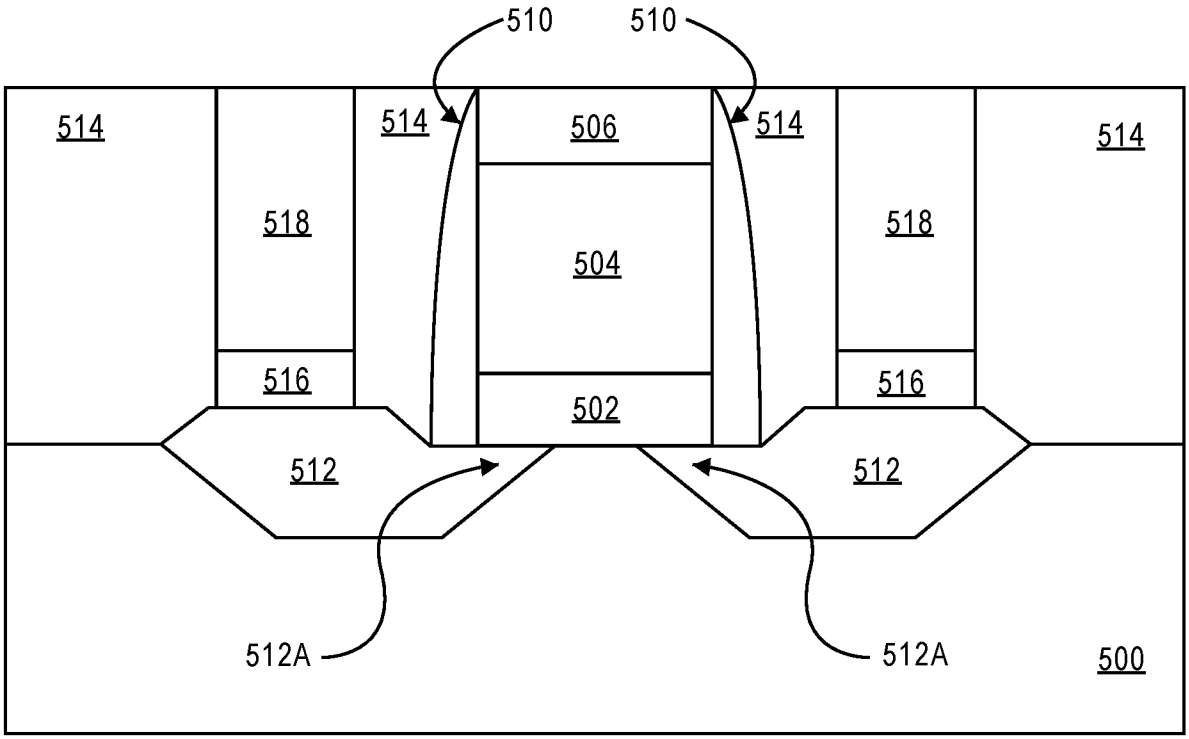

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512A
512A
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FIG. 5

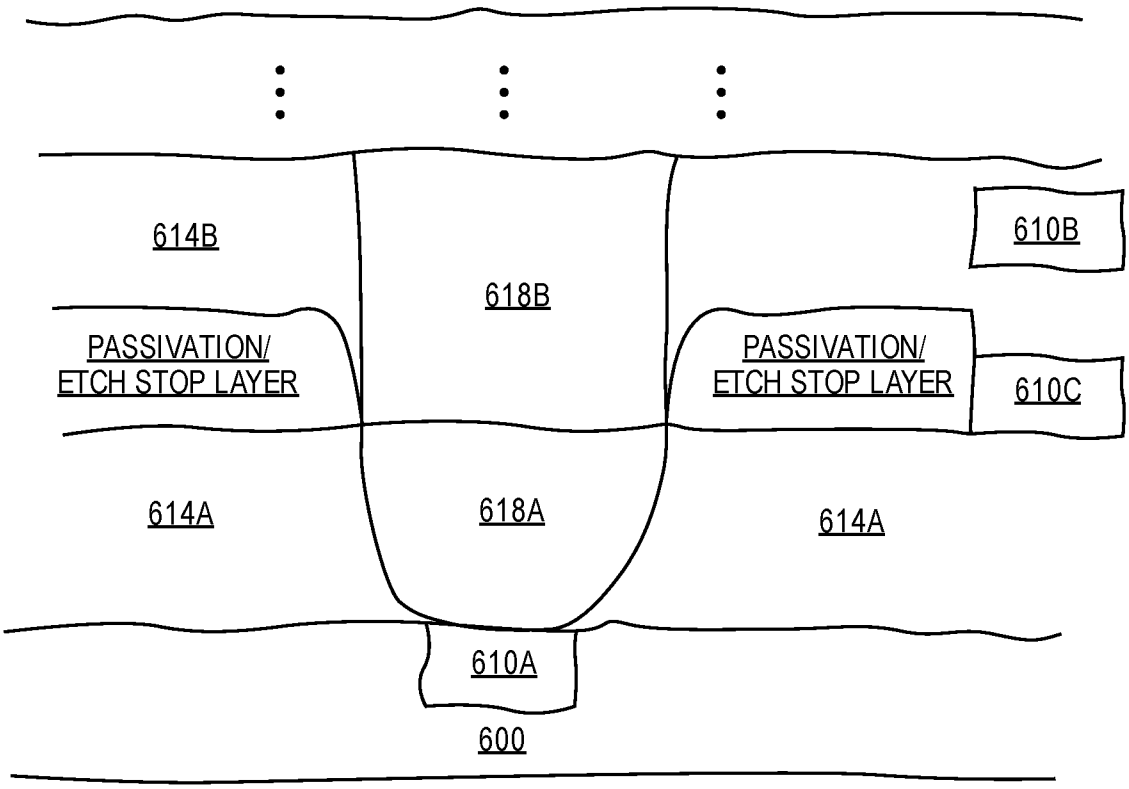

614B
610B
618B
PASSIVATION/
ETCH STOP LAYER
PASSIVATION/
ETCH STOP LAYER
610C
614A
618A
614A
610A
600

FIG. 6

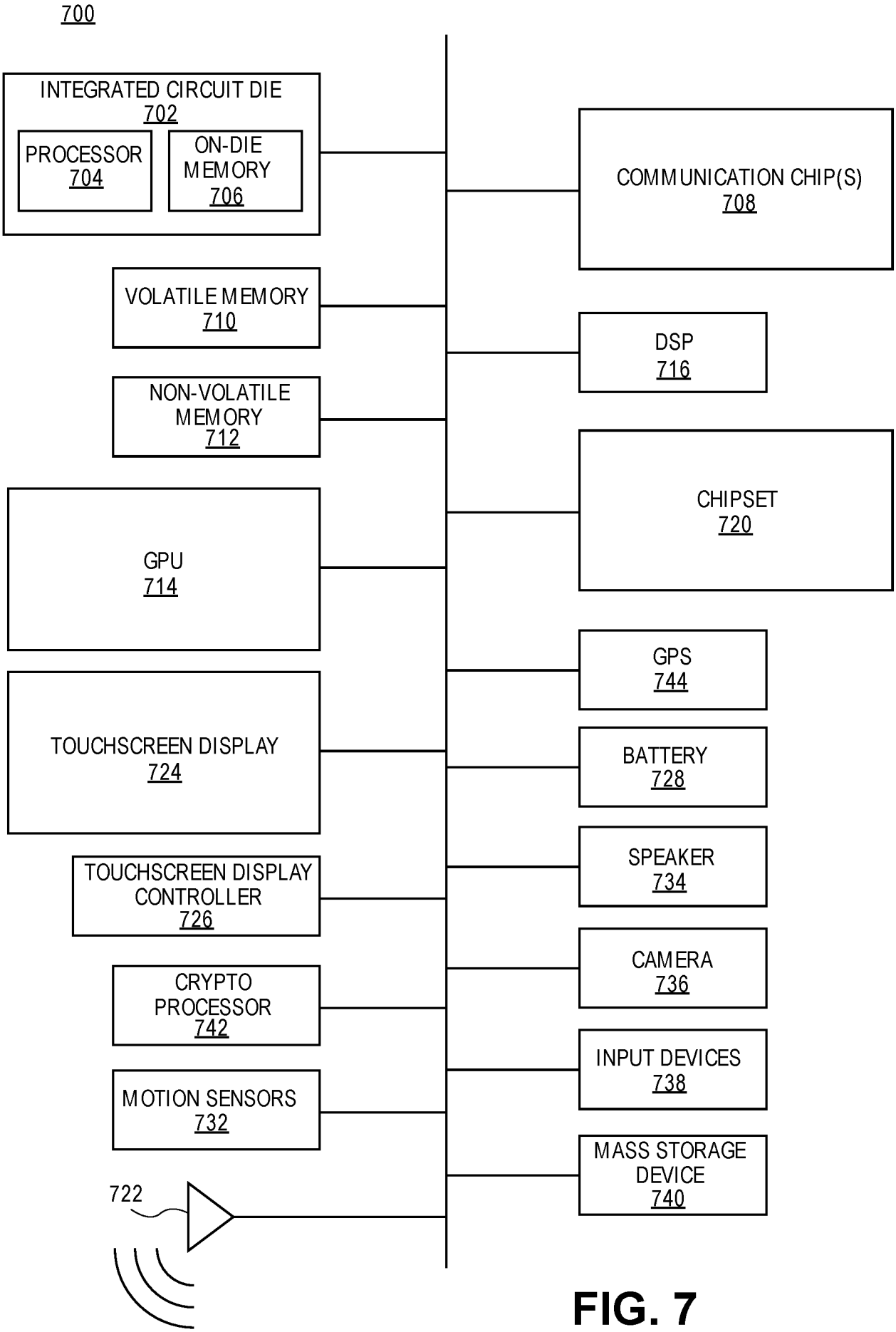

700
INTEGRATED CIRCUIT DIE
702
PROCESSOR
704
ON-DIE
MEMORY
706
VOLATILE MEMORY
710
NON-VOLATILE
MEMORY
712
GPU
714
TOUCHSCREEN DISPLAY
724
TOUCHSCREEN DISPLAY
CONTROLLER
726
CRYPTO
PROCESSOR
742
MOTION SENSORS
732
722
COMMUNICATION CHIP(S)
708
DSP
716
CHIPSET
720
GPS
744
BATTERY
728
SPEAKER
734
CAMERA
736
INPUT DEVICES
738
MASS STORAGE
DEVICE
740

FIG. 7

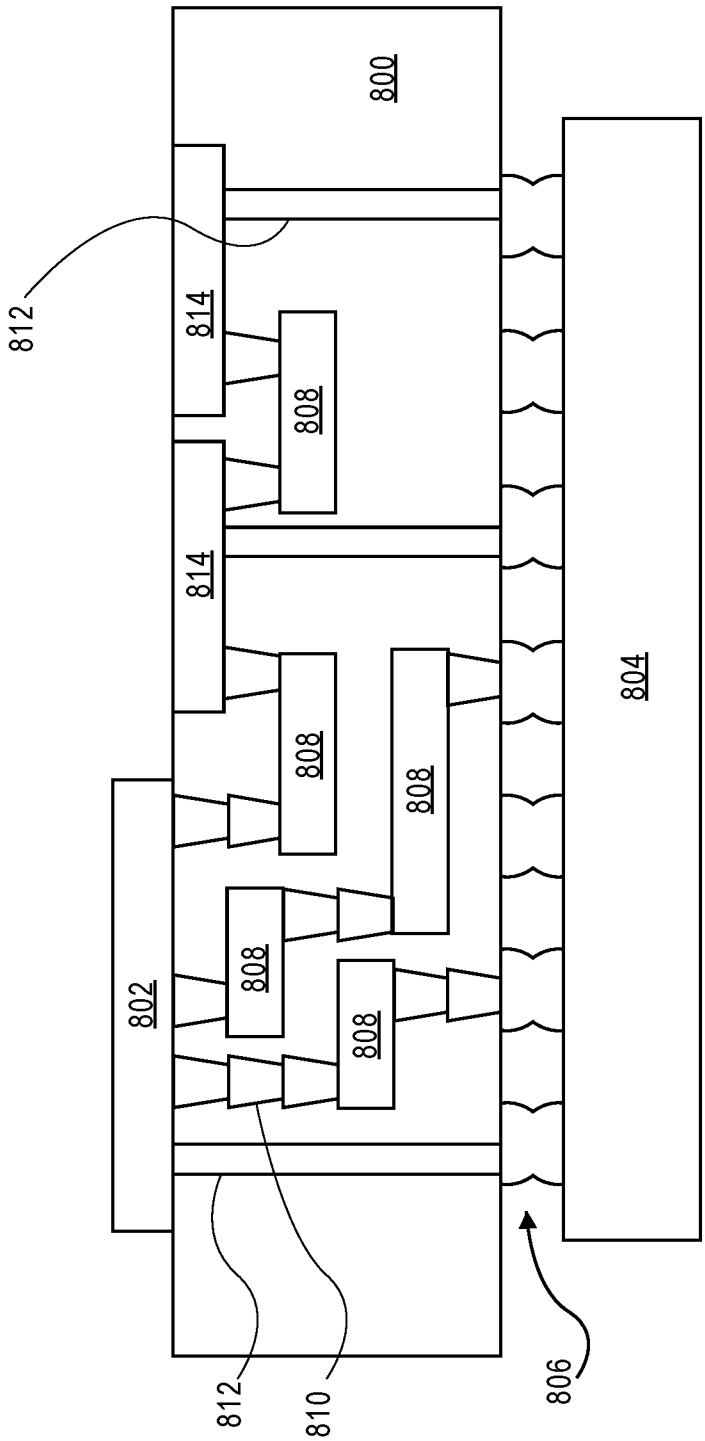


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/069465

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/20(2006.01)i, H01L 21/18(2006.01)i, H01L 21/02(2006.01)i, H01L 21/768(2006.01)i, H01L 21/762(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/20; H01L 21/768; C08G 2/00; H01L 21/02; H01L 29/06; H01L 21/314; B05D 3/06; C09D 183/02; H01L 23/485; H01L 21/18; H01L 21/762

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: dielectric film, integrated circuit, cross-linked carbosilane, linear monomer unit, tetravinylsilane, heterocyclic monomer unit, trisilacyclohexane, combining, depositing, substrate, cross-linking, catalyst

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014-0004358 A1 (BLACKWELL, JAMES M. et al.) 02 January 2014 See paragraphs [0011]-[0018], [0030]-[0044]; claims 1, 25; and figures 2, 6, 7.	1-20
A	US 2014-0038427 A1 (WEIDMAN, TIMOTHY W. et al.) 06 February 2014 See claims 1-13.	1-20
A	US 2005-0182151 A1 (APEN, PAUL et al.) 18 August 2005 See claims 32-42.	1-20
A	US 2012-0161295 A1 (MICHALAK, DAVID J. et al.) 28 June 2012 See claims 1-22.	1-20
A	US 2013-0320520 A1 (MICHALAK, DAVID J. et al.) 05 December 2013 See claims 1-18.	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 September 2017 (26.09.2017)	**27 September 2017 (27.09.2017)**

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Telephone No. +82-42-481-8474

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/069465

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		US 9269652 B2	23/02/2016
		WO 2013-095539 A1	27/06/2013