

[54] **INTRUSION DETECTOR ALARM SYSTEM
HAVING LOGIC CIRCUITRY FOR
INHIBITING FALSE ALARMS**

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340/409

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340/214, 409, 415

[56] **References Cited**
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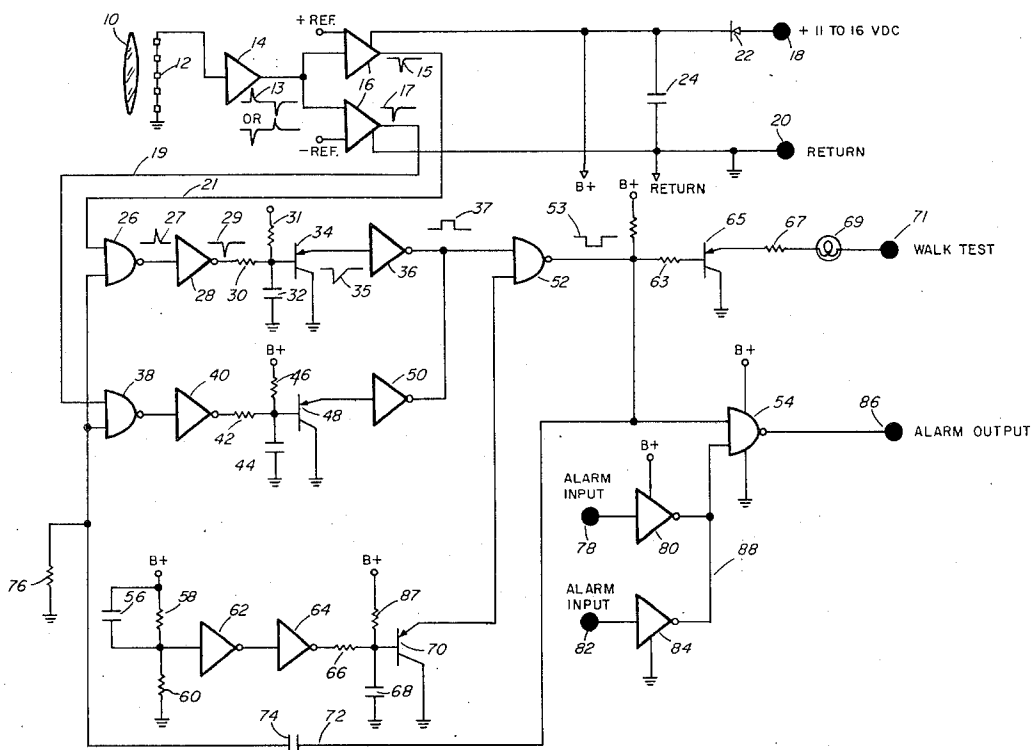
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[57] **ABSTRACT**

Passive intrusion detector logic circuitry is provided which requires two input signals within a specified time period, provides surveillance of all input and output wire terminations, and no possibility of an alarm condition existing at the time when the power is turned on. The circuitry adheres to the Underwriters' Laboratories internal interference specification and incorporates a walk-test circuit for on-line system tests. The above reduction in the possibility of false alarm rate and the tamper-proof provisions are accomplished using two high-noise-immunity logic hex gates and four transistors. An alarm condition exists when two signals occur at the input to the logic circuitry within five seconds of each other, with all other possibilities seen by the circuitry as a safe condition. This reduces the possibility of false alarms due to sudden surges on the supply line, hot air currents, etc. Also, an alarm condition will occur if any one or all of the external connections to the intrusion detector are cut. An alarm inhibit circuit is incorporated in the logic circuitry to delay any alarm from occurring for approximately 25 seconds to take care of the settling time needed at the preamp section after power turn-on or intermittent power interruptions during the operation.

2 Claims. 2 Drawing Figures



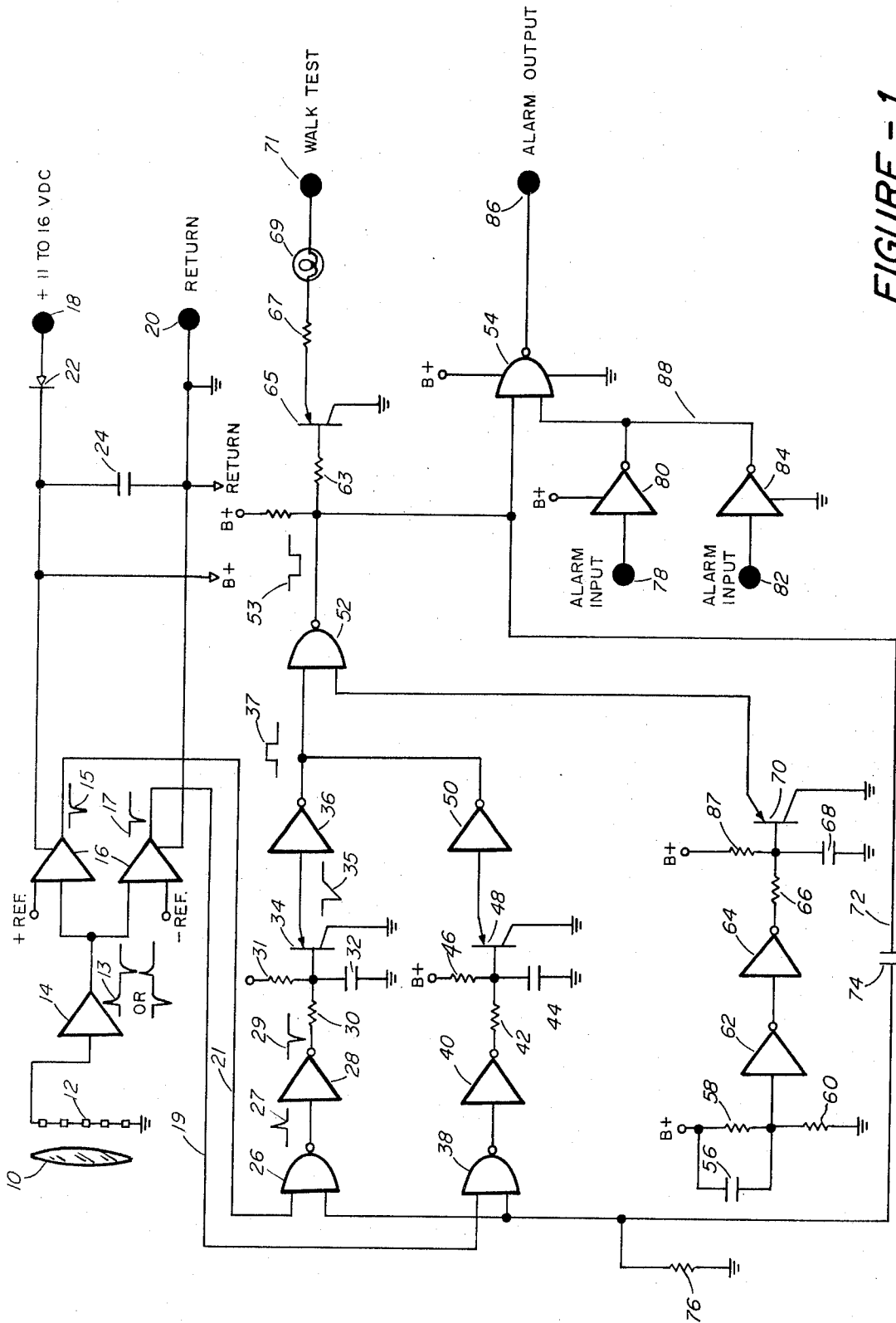


FIGURE -1

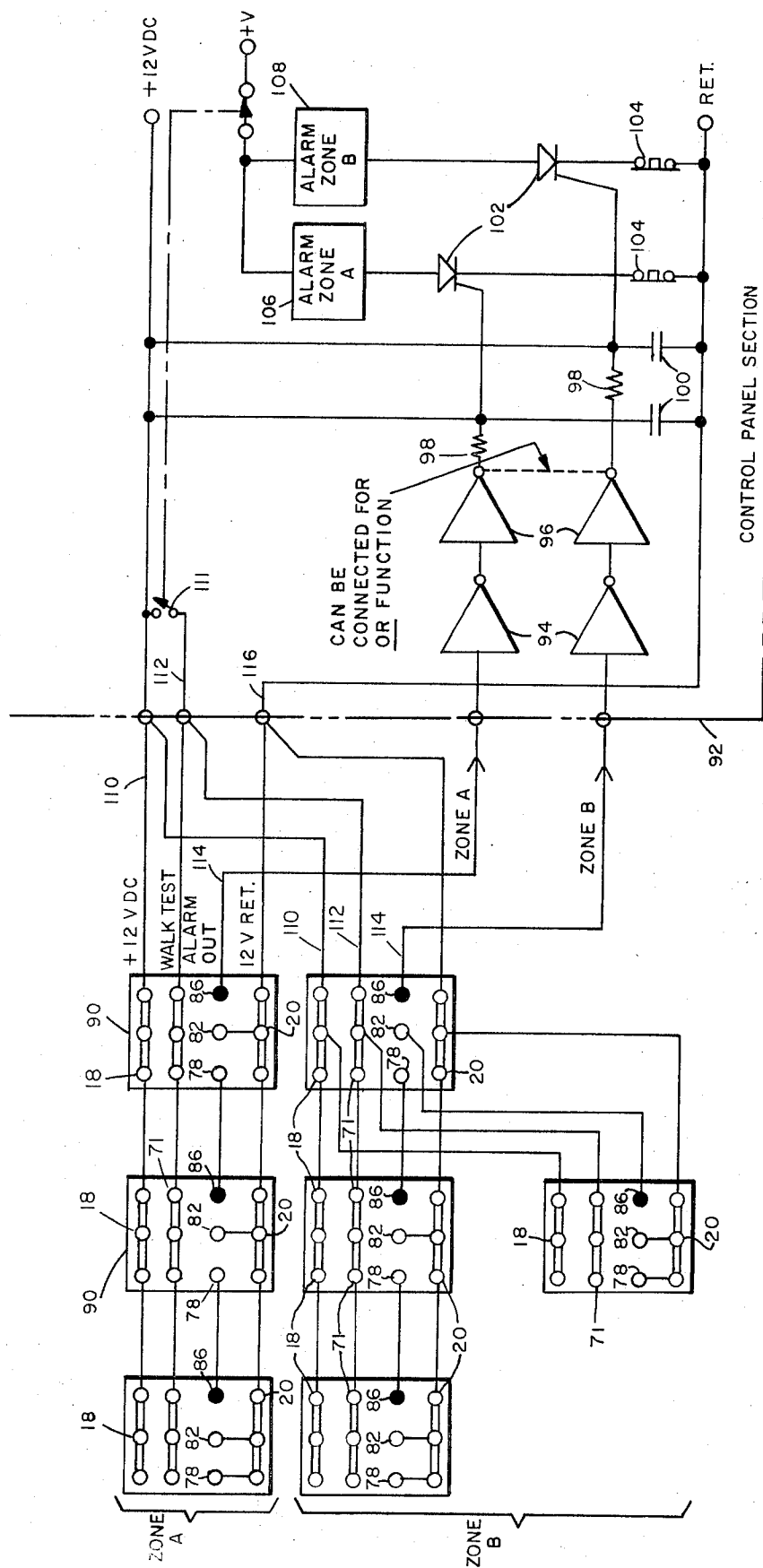


FIGURE-2

INTRUSION DETECTOR ALARM SYSTEM HAVING LOGIC CIRCUITRY FOR INHIBITING FALSE ALARMS

BACKGROUND OF THE INVENTION

Numerous passive-type infrared intrusion alarm systems have been proposed in which the radiation generated by the intruder is detected by an infrared detector, producing a detector output which is processed and used to provide an alarm, either visually or audibly, or by some other means, such as dialing a telephone number or transmitting a signal to a central alarm station to indicate the presence of an intruder. One of the principal problems associated with such systems is to cut down the possibility of false alarms. Since everything above absolute zero emits infrared radiation of varying amounts, the system will detect temperature changes no matter what brings about the temperature change, for example, changing background levels, heaters or airconditioners going on or off, etc. If the false alarm rate is too high, the purpose of the system is defeated. Also, any system that is provided must be capable of providing alarms when the system is tampered with, such as the lines being cut, but at the same time it must be able to be tested so that those supervising it know when it is operating properly. The system must also meet Underwriter Laboratories specifications on power interruptions so that alarms will not be given on momentary changes or surges in the power sources. Furthermore, to be feasible such circuitry must be simple, relatively inexpensive, and small in size so that it cannot be readily detected by intruders.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a new and improved intrusion detector logic circuitry which is relatively tamper-proof.

A further object of this invention is to provide a new and improved intrusion detector logic circuitry which reduces the possibility of false alarms.

Still another object of this invention is to provide a new and improved intrusion detector logic circuit having no possibility of an alarm condition when the power is turned on, and which adheres to the Underwriters' Laboratories internal interference specification.

Still another object of this invention is to provide a new and improved intrusion detector logic circuitry which has a small part count and minimal power requirements.

In carrying out this invention in one illustrative embodiment thereof, the intrusion detector logic circuitry embodied in this invention requires two input signals within a specified time period before an alarm condition exists. The circuitry requires two high noise immunity logic (i.e. high threshold logic) hex gates and four transistors. An alarm inhibit circuit is incorporated therein to prevent an alarm condition at the time of power turn-on, and to take care of momentary interruptions in the power supply, which adheres to the Underwriters' Laboratories internal interference specification. The circuit also includes a walk-test circuit which may be utilized to test the logic without activating the system alarm.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of the new and im-

proved intrusion detector logic circuitry embodied in this invention.

FIG. 2 is a schematic diagram showing one form of terminal and control panel schematic which may be utilized employing the logic circuitry of FIG. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following description, and for ease of terminology, "logic-0" refers to conduction, 0 voltage level, or low state, while "logic-1" refers to non-conducting, plus voltage level, or high state. An alarm condition is referred to as an alarm and a safe condition means no alarm.

Referring now to FIG. 1, radiation is applied from a field of view and focused by a lens 10 on a detector array 12. An infrared intrusion sensor such as that disclosed in application Ser. No. 317,983 filed concurrently herewith, which is assigned to the assignee of the present invention, is an illustrative example of one form of sensor which may be utilized. Various detector arrays may be utilized, but all that is essential is that a plurality of signals are generated as an intruder moves across the various detectors' fields of view. In the aforesaid application, detectors are arranged in columns which are alternately positive- and negative-going, such that when an intruder crosses the field of view, positive- and negative-going pulses are alternately generated in accordance with the movement. Signals from the detector array 12 are applied to a preamplifier 14 and from there in the form of waveforms 13 to a dual threshold detector 16 which, if the signals are of sufficient amplitude, produces output signals 15 and 17 which are applied via lines 19 and 21 to the logic circuitry. Power is applied to the system through input terminals 18 and 20 via a diode 22 and across a capacitor 24. The capacitor 24 maintains the DC input voltage for a finite period and diode 22 prevents the capacitor from discharging into the power supply during power interruptions.

The signal 15 is applied via line 21 to one of the two inputs of a two input NAND gate 26, the output 27 thereof being applied to an inverter 28 whose output is shown in waveform 29. Signal 29 is applied via resistor 30 to the base of an emitter-follower transistor 34. B+ is supplied via resistor 31 and the base of transistor 34 is connected via capacitor 32 to a ground. The output of transistor 34 is shown by waveform 35 which is applied to inverter 36 whose output is shown at 37. Elements 26 through 36 comprise a retriggerable one-shot circuit which has trigger inputs via line 21 and 72. Waveform 17 is applied via line 19 to the input of gate 38 to inverter 40, and via resistor 42 to the base of an emitter-follower transistor 48 with B+ supplied via resistor 46 and a capacitor 44 connected to the base of transistor 48. The output of transistor 48 is applied to inverter 50, whose output is again shown as waveform 37. The elements 38 through 50 also comprise a retriggerable one-shot circuit with the trigger input being applied via line 21 and 72. Each retriggerable one-shot circuit has a common retrigger input via line 72. The line 72 input initiates a timing cycle to both one-shots simultaneously, and will be explained hereinafter. In operation, there will be a positive output pulse 37 at the output of inverters 36 and 50, if the negative trigger pulses at the input lines 21 and 19 occur within 5 seconds of each other. This is due to the fact that inverters

36 and 50 are the equivalent of a wired NOR gate. The waveform 37 (high output) will only occur at the combined output of inverters 36 and 50 if the input to inverter 36 and the input to inverter 50 are both low and both occur within a 5-second interval. The waveform 37 indicates an alarm condition. The alarm condition can only occur if the pulses 15 and 17 on lines 21 and 19 cause capacitors 32 and 44 to discharge, generating a 5-second low state at the inputs of inverters 36 and 50. Unless both signals are at the input of inverters 36 and 50 within 5 seconds of each other, no alarm state (waveform 37) at the combined output of gates 36 and 50 will exist. The timing cycles are determined by resistor 31 and capacitor 32, and resistor 46 and capacitor 44, respectively. Accordingly, if an intruder walks between two detector fields within a 5-second interval, an output occurs in the form of waveform 37 at the outputs of inverters 36 and 50. Resistor 31 and capacitor 32, and resistor 46 and capacitor 44 generate 5-second pulses, and transistors 34 and 48 act as buffers to isolate resistor 31 and resistor 46, respectively. Thus, if the second pulse occurs within the 5-second period, an output in the form of waveform 37 appears. This output is applied to a gate 52. The elements 26, 38, 28, 36, 42 and 50 may be provided in the form of an integrated current (IC) referred to as a HiNIL (high noise immunity logic) hex gate, made by Teledyne, Inc.

An alarm inhibit is provided in the form of a voltage divider 58 and 60, having B+ supplied thereto and a capacitor 56 connected across resistor 58, the output of which is applied to inverter 62 which is connected to another inverter 64 and through an RC network 66 and 68 to an emitter-follower transistor 70. The transistor output is connected to the input of inverter gate 52. For an output waveform 53 to occur from gate 52, the output of transistor 70 must be high, thus non-conductive, for an alarm pulse to be generated. The output of transistor 70 will be high if capacitor 68 is charged to a voltage greater than the threshold of gate 52 minus the V_{BE} drop at transistor 70. When power is first turned on, capacitor 68 has no charge, thus inhibiting gate 52 for approximately 25 seconds, the time period of which is determined by the time constant of RC circuit 87 and 68. Capacitor 68 can charge only if the output of inverter 64 is high or non-conducting, which will be the case if the power supply voltage is equal to or greater than 10 v. as monitored by the voltage divider 58 and 60. If the supply voltage drops below 10 volts even for a fraction of a second, inverter 62 input drops below its threshold level and causes the output of inverter 64 to go low. This causes the discharge of capacitor 68 through resistor 66 within approximately 3 milliseconds to start a new inhibit cycle of gate 52 on the restoration of the supply voltage to its normal operating level. Diode 22 momentarily reverses bias when the supply voltage drops, thus slowing the discharge of capacitor 24, which is the supply voltage decoupling capacitor. This is required for the logic circuitry to be operational long enough to allow inverter 64 output to go low and discharge capacitor 68, starting a new inhibit cycle every time the supply voltage drops below 10 volts.

The gate 52 thus has two inputs, one from the outputs of inverters 36 and 50 and one from the output of the inhibit circuit from transistor 70. For an alarm pulse 53 to occur at the output of gate 52, waveform 37 must appear at the input of gate 52, and transistor 70 must be nonconductive, or high. At the instant that the output

of gate 52 goes toward a negative state an alarm condition exists, indicated by waveform 53, and both one-shots are retriggered via line 72, capacitor 74, and resistor 76, which assures that a 5-second alarm pulse at the output of gate 52 occurs regardless of the time difference between the input signals to the gates 26 and 38. The waveform 53 is applied to an output gate 54 which inverts the waveform 53 and provides an alarm output at terminal 86. Output gate 54 also has applied thereto line 88 from alarm input gates 80 and 84, whose input lines 78 and 82 are from other alarm outputs being monitored, or when not in use alarm inputs 78 and 82 are tied to terminal 20 (return). The alarm output at terminal 86 provides no output if both inputs to the gate 54 are high. An alarm state will occur at output terminal 86 if any one of the inputs from gates 52, 80, or 84 is low. The output of inverters 80 and 84 will go low if either alarm input terminal 78 or 82 goes high. In normal operation, either one or both of the inputs 78 and 82 are connected to another intrusion sensor unit output line, thus monitoring its condition. The terminals 18, 20, 86, 78, 82, and 71 (walk test) all exist at each individual intrusion sensor unit and may be used individually or interconnected with similar units to monitor larger areas as described hereafter.

The monitoring of a plurality of intrusion sensor units utilizing the intrusion detector logic circuitry described in FIG. 1 may be achieved in one form using the arrangement shown in FIG. 2. A plurality of terminal boards 90 are serially interconnected for a given zone A for attaching thereto in series a plurality of intrusion sensor units shown in FIG. 1 and each having terminals 18, 20, 86, 78, 82 and 71 connected to one terminal board 90 as shown in FIG. 2. A four-wire system is provided in the form of line 110 which represents the B+ or source of potential, a walk-test line 112, an alarm output line 114, and a return or ground line 116. Zone B has attached thereto a plurality of intrusion sensor units showing a serial-parallel type of arrangement. The alarm output lines 114 of zone A and zone B are fed to a control panel section 92, including inverter gates 94 and 96 through R-C networks 98 and 100 to fire when activated, silicon controlled rectifiers 102 to provide an alarm for zone A at 106 or for zone B at 108. The alarm may be either visual or audible, or may be used to automatically dial a telephone number at another central alarm station. The alarm input terminals 78 and 82 must be connected to another sensor alarm output line 86 for monitoring purposes, or be connected to the return 20 or ground line 116. As is shown in FIG. 2, each alarm output terminal 86 connects to another sensor alarm input terminal 78, or must be terminated into gates 94 and 96, or an equivalent load tied to a B+ source of potential which would be used to monitor that sensor. In the disclosed arrangement, an alarm condition occurs if any one or all of the connections 110 through 116 are interrupted or cut. This is accomplished at the alarm output by grounding the alarm input of the subsequent sensor or input line to the control panel 92. If the alarm output line 86 is cut, the return 116 or sink current is removed, or if the B+ line 110 is cut, the operating potential for output gate 54 (FIG. 1) is removed, or if the return line 116 is severed, no return path exists for the sink current. Any one of these conditions causes the input of the gate 94 to go high, causing an alarm state. As described above, there are also two alarm input terminals 78 and 82 (see FIG.

1), which are used for monitoring the states of other intrusion sensor units. These inputs must be low for a safe, or "no alarm," condition. All unused alarm input terminals must be tied to ground. Any one input going high will cause an alarm condition. At the initial application of power to the sensor circuitry, an alarm condition prevails at the signal inputs 78 and 82. This is because the preamp section of the logic circuitry has exceedingly high gain, is AC-coupled, and takes approximately 10 to 15 seconds to stabilize. As has already been described, an alarm inhibit circuit is incorporated to delay any alarm state from occurring at the alarm output 86 for approximately 25 seconds. The alarm inhibit circuit also takes care of momentary breaks in the power supply.

In order to test the system to see if it is working without setting off alarms, a walk-test circuit is provided. The walk-test line 112 includes a switch 111 for removing B+ from alarms 106 and 108 as shown in FIG. 2 and for applying B+ to the walk-test circuitry shown in FIG. 1, which includes resistor 63, transistor 65, resistor 67, and a lamp 69 (see FIG. 1). In operation, switch 111 shown in FIG. 2 must first be closed, and then when the guard steps into the field of view of the detector array 12 (FIG. 1), an alarm condition occurs causing cut-off transistor 65 to begin to conducting, lighting the lamp 69 (FIG. 1), showing the guard that that sensor head is working. When the walk-tests of all of the units are made, the walk-test switch 111 is disengaged to remove B+ from all the walk-test circuits of the units being monitored. The typical alarm control panel 92 (FIG. 2) also includes reset switches 104 for resetting the alarms 106 and 108 via the silicon controlled rectifiers 102. Thus, after an alarm 106 and/or 108 is activated, they will stay activated till reset by switches 104.

Accordingly, an alarm system is provided which requires two input signals within a specified time period, reducing the possibility of false alarms which are generated due to conditions other than interruption by an intruder. Surveillance is also provided on all input and output wire terminations for sounding an alarm if any of the wires are cut. Due to the alarm inhibit circuit, there is no possibility of an alarm condition existing at the time of power turn-on, which also operates to prevent alarms during temporary power interruptions. The circuitry also provides a walk-test capability in which the equipment can be checked without producing an

alarm. The logic circuitry is all performed by two HiNIL (high noise immunity logic) hex inverter gate such as Teledyne's 300 series or equivalent, which are compact, have high noise immunity and require little power.

Since other modifications, varied to fit particular operating requirements and environments, will be apparent to those skilled in the art, the invention is not considered limited to the examples chosen for purposes of disclosure, and covers all changes and modifications which do not constitute departures from the true spirit and scope of this invention.

I claim:

1. Intrusion detector logic circuitry for producing an output alarm signal on a predetermined input signal sequence from a detector array comprising, in combination,

a. a passive detector array having a predetermined field of view for producing a signal sequence when an intruder moves in the field of view of said detector array,

b. means for applying said signal sequence to one of the inputs of a pair of dual input retriggerable one-shot circuits having a single output at which an alarm signal is generated when said signal sequence occurs within a predetermined time interval,

c. gating means having first and second inputs and an output, said single output of said pair of retriggerable one-shot circuits coupled to said first input of said gating means for passing an alarm signal to said output thereof, and

d. feedback means coupled between the output of said gating means to the other inputs of said dual input retriggerable one-shot circuits for retriggering said one-shot circuits to assure an alarm signal at the output of said gating means of predetermined duration regardless of the time difference in the input signal sequence as long as the sequence occurs within a predetermined time interval.

2. The intrusion logic circuitry set forth in claim 1 having an alarm inhibit circuit coupled between a source of power for the logic circuitry and said second input of said gating means for inhibiting said gating means for a predetermined time interval when the power is first turned on or subsequently interrupted.

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