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(54) Title: SHARED METALLIC SOURCE/DRAIN CMOS CIRCUITS AND METHODS THEREOF

(57) Abstract: A circuit includes a first transistor formed on the substrate and a second transistor formed on the substrate adjacent the first transistor. A source region of one of the first and second transistors and a drain region of the other one of the first and second transistors are the same and comprise substantially the same one or more materials.

SHARED METALLIC SOURCE/DRAIN CMOS CIRCUITS AND METHODS THEREOF

[0001] This application claims the benefit of U.S. Provisional Patent Application Serial No. 60/783,875, filed March 20, 2006, which is hereby incorporated by reference in its entirety.

FIELD OF THE INVENTION

[0002] The present invention generally relates to complementary metal–oxide–semiconductor (CMOS) circuits and, more particularly, to shared metallic source/drain CMOS circuits and methods thereof.

BACKGROUND

[0003] The ability to scale CMOS technology to allow for faster circuit speeds and higher circuit density presents several challenges. These challenges include the ability to control leakage currents and short-channel effects and to increase drain saturation current while reducing the power supply voltage and maintaining control of device parameters.

[0004] To meet the demands for scalability of CMOS technology several approaches have been identified. These approaches can be considered "nonclassical" because they incorporate advanced MOSFET structures that are often combined with material enhancements, such as new gate stack materials.

[0005] One of these approaches for a Schottky CMOS circuit uses platinum silicide (PtSi) source/drain regions to an n-type silicon body region for a Schottky PFET and an erbium silicide ($ErSi_2$) source/drain regions to a p-type silicon body region for a Schottky NFET. In the Schottky PFET, the barrier height between PtSi and n-type silicon is about 0.85eV (electron-volts). Inverting the silicon to p-type (with a negative gate bias) changes the barrier height to about 0.27eV (the difference between the silicon bandgap and the equilibrium mode barrier height, 1.12eV-0.85eV = 0.27eV). This lower barrier height provides an easier means for carriers to "jump over" the barrier. This is called thermionic

current or thermionic emission current and is the dominant current mechanism in inversion mode operation for these devices.

[0006] The Schottky barriers to the body region also have a particular barrier width. Rather than inverting the body region, one can accumulate majority carriers (with a positive gate bias in the PFET) in the body at the gate-dielectric-to-body interface. The effect in a Schottky barrier field effect transistor (SBFET) is an increase in the energy gradient at the source/body and drain/body interfaces which decreases the barrier width. If the gate-modulated barrier width is small enough, carriers can traverse the barrier via quantum mechanical tunneling. Therefore, tunneling current is the modulated current mechanism in accumulation mode operation. The ability of an SBFET to operate in accumulation mode and inversion mode is what makes the device ambipolar. This is a relatively well-known effect in SBFETs, although it is often times overlooked in discussions about Schottky CMOS.

[0007] This approach using PtSi source/drain regions and/$ErSi_2$ source/drain regions is fairly promising from a CMOS technology standpoint, however one of its disadvantages is the use of rare earth metals to form silicides of a low inversion mode barrier height in the source/drain regions and that these metals are different materials for desirable p-channel and n-channel operation. Rare earth metals are expensive and thus from high volume manufacturing standpoint it is difficult to make a convincing argument that long-term sustainability would be practical with this approach.

[0008] Another technology that uses Schottky source/drain regions are carbon nanotube transistors (CNTFETs). It was found that the metallic contact to the nanotubes is a Schottky junction and that modulation of this junction explains the current-voltage characteristics of these devices. Thus, SBFETs and CNTFETs are largely the same, except that they use a different type of semiconductor (silicon vs. carbon). Accordingly, the approaches taken to optimize CNTFET performance can be and have been applied to SBFETs. In particular, the bulk switching approach has been demonstrated with CNTFETs, although the nature of

the carbon nanotube prevents the metal contact to also act as inter-device isolation.

SUMMARY

[0009] A circuit in accordance with embodiments of the present invention includes a first transistor formed on the substrate and a second transistor formed on the substrate adjacent the first transistor. A source region of one of the first and second transistors and a drain region of the other one of the first and second transistors are the same and comprise substantially the same one or more materials.

[0010] A method of making a circuit in accordance with other embodiments of the present invention includes providing a substrate and forming first and second transistors on the substrate with the second transistor adjacent to the first transistor. A source region of one of the first and second transistors and a drain region of the other one of the first and second transistors are the same and comprise substantially the same one or more materials.

[0011] A method for making a circuit in accordance with other embodiments of the present invention includes forming at least one active region in a substrate and doping the active region for a first transistor and a second transistor. At least one metal is deposited at least in a source region of one of the first and second transistors and a drain region of the other one of the first and second transistors. Silicidation is performed at least once on the deposited metal so that the source region of one of the first and second transistors and the drain region of the other one of the first and second transistors are the same and comprise substantially the same metal silicide

[0012] With the present invention, one of the source/drain regions for a pair of transistors, such as for pull-up and pull-down networks of a logic gate, are the same exact metal/metal silicide. Additionally, this metal/metal silicide also acts as an isolation region between the transistors which allows for the elimination of the conventional isolation region between those devices. As a result, with the shared source drain region and the elimination of the conventional isolation

region, the transistors can be placed closer together on the same substrate, thus decreasing the two-dimensional surface area consumption on the substrate without reducing the size of the transistors.

[0013] Another advantage of the present invention is that the first level for interconnects is on the same lithography level as that of the shared source drain region. In other words, the shared, source drain region is at the same level where wiring connections are made. Since the shared source drain region is made of metal or metal silicide and the resistivity is low, this shared, source drain region can be used for wiring. As a result, not only is the circuit simplified, but also the process for making the circuit is simplified which results in a decrease in manufacturing cost. With the present invention, typically it is possible to cut the number of front end processing steps by about thirty percent.

[0014] Further, the decrease in manufacturing time and cost with the present invention also results in an increase in the throughput of circuit fabrication which can be realized. Since manufacturing processes consume energy, the decrease in manufacturing time has the added effect of reducing pollution and manufacturing waste.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIG. 1 is a cross sectional view of a shared metallic source/drain CMOS circuit in accordance with embodiments of the present invention;

[0016] FIGS. 2A-2P are top and side cross-sectional views of a method for making shared metallic source/drain CMOS circuit in accordance with embodiments of the present invention is illustrated;

[0017] FIG. 3 is a simplified band diagram of the shared metallic source/drain CMOS circuit formed in accordance with the method disclosed in FIGS. 2A-2P;

[0018] FIG. 4 is a simplified band diagram of the shared metallic source/drain CMOS circuit formed in accordance with the method disclosed in FIGS. 2A-2P with the input voltage equal to ground (Gnd); and

[0019] FIG. 5 is a simplified band diagram of the shared metallic source/drain CMOS circuit formed in accordance with the method disclosed in FIGS. 2A-2P with the input voltage equal to V_{dd};

[0020] FIG. 6 is a table which provides ITS and fluorine co-implant Splits and extracted EOT values;

[0021] FIG. 7 is a graph of inverter voltage transfer characteristics (VTCs) for mask-defined gate lengths ($L_{g,m}$) from 2 μm down to 0.6 μm, mask defined width (W_m) of 1 μm, and a power supply voltage (V_{DD});

[0022] FIG. 8 is a graph of NFET and PFET I_{DS} vs. V_{DS} from $L_{g,m}$ = 0.6 μm inverter in FIG. 2. $|V_g - V_{tlin}|$ = 0-5 V in 1 V increments

[0023] FIG. 9 is a graph of normalized C-V curves for n-type and p-type structures at 100 kHz and 1 MHz where C_{acc} is the accumulation mode capacitance and V_{mid} is the voltage where C/C_{acc} = 0.5;

[0024] FIG. 10A is a graph of NFET I_{DS} vs. V_{DS} for splits 1-3 and transfer characteristics with $V_g - V_{tlin}$ = 0-5 V in 1 V increments;

[0025] FIG. 10B is a graph of NFET I_{DS} vs. V_{GS} for splits 1 and 2 with $L_{g,m}$ = 2 μm and W_m = 1 μm;

[0026] FIG. 11A is a graph of PFET I_{DS} vs. V_{DS} for splits 1-3 and transfer characteristics with $|V_g - V_{tlin}|$ = 0-5 V in 1 V increments;

[0027] FIG. 11B is a graph of PFET I_{DS} vs. V_{GS} both for splits 1-3 . $L_{g,m}$ = 2 μm and W_m = 1 μm;

[0028] FIG. 12A is a graph of transfer characteristics for $L_{g,m}$ = 2 μm, W_m = 1 μm NFET and PFET from split 2; and

[0029] FIG. 12B is a graph of corresponding VTC is with V_{DD} = 3 V, and is overlayed with output current to demonstrate the effect of BTBT.

DETAILED DESCRIPTION

[0030] A CMOS circuit 10 in accordance with embodiments of the present invention is illustrated in FIG. 1. The circuit 10 includes an NFET 12 and a PFET 14 which share a fully silicided, source/drain region 16, although the circuit could comprise other types and numbers of devices and components in other configurations. The present invention provides a number of advantages including providing a CMOS circuit where the components can be placed closer together without having to decrease the size of the components.

[0031] Referring more specifically to FIG. 1, the circuit 10 includes a substrate 20 with a silicon layer 22, although substrate 20 could be made of other types and numbers of layers, such as one or more layers of polysilicon, strained silicon, silicon germanium, or any other semiconductor in crystalline, polycrystalline, or amorphous form by way of example only. The substrate 20 also has a buried oxide layer 24, although the substrate 20 could have other types and numbers of insulating layers, such as glass or no insulating layer if the dielectric is air by way of example only.

[0032] The NFET 12 is formed in the silicon layer 22 and includes a drain region 26, a gate region 28 on a gate dielectric layer 46, and the shared, source drain region 16 and the PFET 14 also is formed in the silicon layer 22 and includes a drain region 30, a gate region 32 on a gate dielectric layer 46, and the same, shared, source drain region 16, although other types and numbers of transistors or other logic gates with other types and numbers of elements could be formed on the substrate 20. By way of example only, the transistors 12 and 14 formed on the substrate 20 could comprise two or more CMOS transistors, MOSFETs, Schottky barrier FETs, or other logic switching gates. The drain region 26, the gate region 28, the shared source/drain region 16, the drain region 30 and the gate region 32 are each silicide regions, although one or more of the regions could be doped. Additionally, in this example, region 34 is doped with an n-type dopant, such as phosphorus or arsenic by way of example only, and region 36 is the doped with a p-type dopant, such as boron by way of example only, although one or more of the regions 16, 26, 28, 30, and 32 could be doped in other

manners or undoped. An input terminal 15 is coupled to the gate regions 28 and 32 and an output terminal is coupled to the shared source/drain region 16, although other types and numbers of connections could be used.

[0033] An n-doped or halo region 34 is formed adjacent the shared source/drain region 16 substantially around the gate region 28 and a p-doped or halo region 36 is formed adjacent the shared source/drain region 16 substantially around the gate region 32, although other types and numbers of doped regions with other dopants and in other configurations and locations can be used. The n-doped or halo region 34 and the p-doped or halo region 36 serve to reduce the Schottky barrier height at the metal-semiconductor (M-S) junction. This happens as a result of two effects – dipole lowering and image force lowering. If, for example, an n-type dopant atom exists on the silicon side of the M-S junction, it creates a dipole at the M-S junction that will lower the electron Schottky barrier height (SBH) by some amount (which depends on the amount of dopants at the interface – more dopants results in more barrier lowering). This is the dipole lowering effect. If the doped extension region also happens to not be fully depleted (i.e., if the lateral junction depth is long enough), then there also exists a large electric field in the silicon adjacent to the M-S junction. This field gives rise to an "image field" extending from the metal, which, in the n-type dopant example, lowers the electron SBH. If the doped extension is fully depleted (i.e., if the depletion region extending from the M-S junction consumes the entire doped extension region), then the only contribution to Schottky barrier lowering (SBL) is dipole lowering. If the doped extension is not fully depleted, then image force lowering also contributes (The same case applies to holes for p-type dopants at the M-S interface). Currently, there is no complete or physically rigorous quantification of at exactly which point the doped extension region becomes fully depleted. However, for the high dopant concentrations needed to significantly lower the SBH (~ $1x10^{20}$ dopants/cm^3), it is thought that this "crossover point" exists for doped extension junction depths on the order of 5 nm. In either case (fully depleted or not fully depleted), however large dopant concentrations (~ $1x10^{20}$ cm^{-3}) are needed to have a significant barrier lowering effect, which is the purpose that these doped regions 34 and 36 serve.

[0034] A sidewall spacer 38 is formed around the gate region 28 of the NFET 12 and a sidewall spacer 40 is formed around the gate region 32 of the PFET 14, although other numbers and types of spacers can be used. The sidewall spacers 38 and 40 are made of silicon nitride, although other types and numbers of materials could be used.

[0035] The shared source drain region 16 is a fully silicide source/drain region that is made of any metal and/or its alloy with another metal or series of metals that reacts with a semiconductor to form a metal-semiconductor alloy, such as Ni, NiPt, and Co by way of example only. The shared, source drain region 16 extends substantially from the buried oxide layer 24 or other insulating layer or layer to a surface of the circuit 10 and acts as an isolation region between the NFET 12 and the PFET 14. This allows for the elimination of a conventional isolation region between the NFET 12 and the PFET 14.

[0036] Accordingly, with the present invention, the shared source/drain region 16 for the NFET 12 and the PFET 14 with the elimination of the conventional isolation region allows for a greater density of transistors on the substrate 20 to be achieved without requiring a reduction in the size of any of the transistors. Additionally, the present invention provides the shared, source drain region 16 on the same level and other wiring interconnections facilitating a simpler contact and manufacturing scheme.

[0037] A method for making a circuit 10 in accordance with embodiments of the present invention is illustrated and described with reference to FIGS. 2A-2P. Initially, a substrate 20 with a silicon layer 22 and a buried oxide layer 24 in the silicon layer 22 is provided, although other types and numbers of substrates made of other types and numbers of layers of material with or without an insulating layer could be used. The silicon layer 22 can be doped or undoped.

[0038] Next, as shown in FIGS. 2A-2B an etch mask 42 is selected and placed over the silicon layer 22 to define regions of silicon layer 22 which will be etched away to form active regions 22(1)-22(5) (shown in FIGS. 2C through 2F), although other manners for forming the active regions could be used.

Additionally, although in this example five active regions 22(1)-22(5) are formed in the silicon layer 22, other numbers, types and shapes of active regions could be formed in the substrate 20. Next, the active regions 22(1)-22(5) are etched from the silicon layer 22 and then the etch mask 42 is removed as shown in FIGS. 2C and 2D.

[0039] Next, an inter-circuit isolation layer 44 is deposited in etched regions between and around the active regions 22(1)-22(5) as shown in FIGS. 2E and 2F. The inter-circuit isolation layer 44 is made of oxide, although other types and numbers of materials could be used to form this isolation layer.

[0040] Next, focusing more specifically on active region 22(1) in this example, a gate dielectric layer 46 is deposited on active region 22(1) as shown in FIG. 2G, although the gate dielectric layer 46 can be formed in other manners, such as being grown, and in other locations and configurations. The gate dielectric layer 46 is made of oxide, although other types and numbers of materials could be used. Additionally, at this time the active region 22(1) for the NFET 12 and the PFET 14 is lightly doped (~ $1x10^{15}$ atoms/cm^3), although other types and amounts of dopants can be used or the active region 22(1) can be left undoped. Generally, light doping is usually viewed as in the $10^{15} - 10^{17}$ range, while moderate doping is in the $10^{17} - 10^{18\text{-}19}$ range, and high doping is 10^{19}+.

[0041] Next, a gate layer 48 is deposited on the gate dielectric layer 46 as shown in FIG. 2H, although the gate layer 48 can be formed in other manners, such as being grown, and in other locations and configurations. The gate layer 48 is made of polysilicon, although other types and numbers of materials could be used.

[0042] Next, an etch mask (not shown) is selected and placed over the gate layer 48 to define gate region 28 and gate region 32 as shown in FIG. 2I, although other manners for forming the gate regions could be used and other types and numbers of regions could be formed in the gate layer 48. Next, the gate region 28 and the gate region 32 are etched from the gate layer 48 and then the etch mask is removed.

[0043] Next, a silicon nitride layer (not shown) is deposited over the gate region 28 and the gate region 32 on silicon layer 22(1), although the silicon nitride layer could be formed in other manners and other types and numbers of layers could be used. Next, the silicon nitride layer is anisotropically etched to form sidewall spacer 38 which extends around gate region 28 and sidewall spacer 40 which extends around gate region 32 as shown in FIG. 2J, although other manners for forming sidewall spacers 38 and 40 could be used, such as by oxidizing the sidewalls of gate region 28 and gate region 32 if these regions are made of polysilicon for example. In this embodiment, the sidewall spacers 38 and 40 each have a width on the order of the thickness of the gate material. For example, if the polysilicon deposited for the gate is 50 nm thick, then the sidewall spacer, after an anisotropic etch, will be ~ 50 nm wide. This value can be adjusted, though, by changing the sidewall spacer etch conditions, such as gas flow, pressure, and power by way of example only.

[0044] Next, a metal layer 47 is deposited over exposed portions of the silicon layer 22(1), the gate region 28, the gate region 32, the sidewall spacer 38 and the sidewall spacer 40 as shown in FIG. 2K, although manners for forming the metal layer 47 and other types and numbers of layers could be used. In this example, the metal layer 47 is made of Ni, although any metal and/or its alloy with another metal or series of metals that reacts with a semiconductor to form a metal-semiconductor alloy could be used.

[0045] Next, full silicidation of the metal layer 47 is performed in one step as shown in FIG. 2L, although other amounts and numbers of steps of silicidation can be used. In this example, silicidation is performed by rapid thermal processing (RTP), although other processes for silicidation could be used. Silicidation is simply a process to elevate the wafer to a temperature sufficient to allow the metal/alloy to react with the silicon. In the example of nickel silicide, this happens over the range of ~ 280-700 °C. Within this temperature range, one can form different "phases" of silicides. At low temperatures (up to ~ 450 °C), the nickel silicide is nickel rich (Ni_2Si). Raising the temperature further forms a monosilicide phase (NiSi) up to ~ 650-700 °C, where a silicon rich phase is then formed ($NiSi_2$). It is desirable to have a monosilicide phase for nickel silicide,

since it has the lowest sheet resistance, but a one step silicidation process at, for example, 600 °C can result in excess silicidation for small features. What is typically performed, then, is a two step process, where the first step takes place at a low temperature (e.g., 300 °C), which forms the nickel rich phase. Then the unreacted nickel is etched away, and a second thermal step takes place at a higher temperature (e.g., 550 °C) to form the monosilicide phase. Different silicides exhibit different behavior during the silicidation step, but generically speaking, they go from metal rich, to monosilicide, to silicon rich phases as the silicidation temperature is progressively increased. Some silicides never reach a silicon rich phase due to the nature of the silicide, and some silicides are preferred to have in a metal rich or silicon rich phase.

[0046] This silicidation forms the shared source/drain region 16 for the NFET 12 and the PFET 14 where the region 16 acts as a source for NFET 12 and also acts as a drain for PFET 14. Additionally, when the shared source/drain region 16 is fully silicided, the region acts as an inter-isolation region between the source of NFET 12 and drain of PFET 14 without the need for an additional isolation region. To act as an isolation region, the silicide which forms the shared source/drain region 16 extends the entire depth of the body region of the circuit 10 down to the buried oxide layer 24. This is what facilitates isolation between the NFET 12 and PFET 14. This isolation is purely inter-device isolation, and that inter-circuit isolation would, in most cases, still require the use of conventional isolation techniques, such as shallow trench isolation or MESA isolation by way of example only.

[0047] Next, an implant mask 48 is deposited on the gate region 28 and adjacent portions of silicon layer 22(1) for the NFET 12 while gate region 32 and adjacent portions of silicon layer 22(1) for the PFET 14 are exposed as shown in FIG. 2M, although the implant mask 48 could be formed in other manners and other types and numbers of layers could be used. Next, a doping implantation into the silicide is performed on the exposed gate region 32 and adjacent portions of silicon layer 22(1) to form a doped portion in shared source/drain region 16, a doped gate region 32, and a doped source region 30 for the PFET 14, although other manners for forming the PFET 14 could be used.

[0048] Next, an implant mask 50 is deposited on the gate region 32 and adjacent portions of silicon layer 22(1) for the PFET 14 while gate region 28 and adjacent portions of silicon layer 22(1) for the NFET 12 are exposed as shown in FIG. 2N, although the implant mask 50 could be formed in other manners and other types and numbers of layers could be used. Next, a doping implantation into and through the silicide is performed on the exposed gate region 28 and adjacent portions of silicon layer 22(1), although other manners for forming the PFET 14 could be used.

[0049] Next, thermal diffusion is performed on exposed portions of silicon layer 22(1), the drain region 26, gate region 28, shared source/drain region 16, gate region 32, and source region 30 which forms doped or halo region 34 adjacent shared source/drain region 16 and adjacent region 26 and doped or halo region 36 adjacent shared source/drain region 16 and adjacent region 30 as shown in FIG. 2O, although other manners for making the doped regions 34 and 36 can be used.

[0050] In this embodiment, there are two approaches for forming the doped regions 34 and 36, although other types and numbers of approaches could be used. The first approach is implant-to-silicide (ITS) as illustrated and described herein. With this approach, dopants are implanted into the silicide and a thermal step is performed to drive the dopants into the silicon. This thermal step is at ~ 600 °C, which is low for diffusion in silicon, but high for diffusion in metal. As a result, the dopants diffuse very fast in the silicide and quite slow in the silicon, resulting in a reasonably shallow doped extension near the M-S junction.

[0051] Another approach which can be used is often know by several different names, such as dopant pile-up, dopant segregation (DS), or silicidation-induced impurity segregation (SIIS), where dopants are implanted into the silicon first and then the silicidation step is performed. As the silicidation proceeds, dopants "segregate" at the silicidation front, or in other words, they tend to prefer staying in the silicon versus being consumed by the silicide. As a result of this, the silicide acts as something of a snowplow, piling up dopants at and near the M-

S junction as the silicidation proceeds. Currently, this is a popular way of forming doped extensions due to the simplicity of the process and the ability to form extremely shallow/abrupt junctions with very high dopant concentration, which is perhaps more difficult with the ITS approach. The dopant concentration must be very high (~ $1x10^{20}$ cm^{-3}) to have a significant effect on improving the performance of a SBFET. As for the minimum thickness of this region, some feel that the region should be fully depleted (i.e., small junction, ~ 5 nm or so) to achieve the benefits of what would be a "pure" Schottky junction with a small barrier height. However, the barrier lowering offered by the dopants with this approach is limited to only dipole lowering. If the region is not fully depleted (i.e., larger junction, ~ 10 nm or so, depending on the dopant concentration), then image force lowering adds to the barrier lowering to achieve an even smaller barrier height, while the leakage current is also further reduced. However, this may impose other restrictions on the device structure (e.g., sidewall spacer thickness) to optimize performance. With these embodiments of the present invention, the doped extension region should have a high dopant concentration sufficient to significantly increase current injection at the M-S junction, while also having a junction depth of the right size to optimize whatever tradeoff may exist between on state and off state current in a given device structure (e.g., FinFET, planar SOI, etc.)

[0052] The resulting CMOS circuit 10 with an NFET 12 and PFET 14 with the same shared source/drain region 16 is illustrated in FIG. 2P.

[0053] Accordingly, as illustrated above the present invention can be made using conventional integrated circuit fabrication techniques. Although one example of a method for making a circuit in accordance with embodiments of the present invention is described above, other methods for making the circuit with other types and numbers of steps in other orders can be used. For example, any process or combination of processes to form the gate regions, gate dielectric, and sidewall spacers can be used. Additionally, for bulk-switching SBFETs, the appropriate dopants are implanted into the appropriate source, gate, and drain regions for the transistors before or after the silicide is formed. For SBFETs using

a "tuned" silicide, the species implantation is typically performed before the metal for the shared source/drain region is deposited.

[0054] One approach to achieve single metal Schottky CMOS is through what are called "bulk switching" devices. In such devices, the Schottky source/drain regions are placed adjacent to implanted doped regions (referred to as source/drain extensions, doped extensions, or halo regions) of high dopant concentration. This is illustrated in FIGS. 2A-2P and in the simplified band diagrams FIGS. 3-5. The reason for this is that gate modulation of a Schottky barrier is actually not as effective as a conventional thermal barrier, and so the doped region "modifies" the Schottky barrier to make it very small. This results in conventional thermal barrier modulation over a larger range of gate biases, thus enhancing the sensitivity of current flow to gate bias. Although the device, in effect, acts as a conventional MOSFET in this case, the differentiating factor is the existence of a source/drain region composed primarily of metal or metal silicide as opposed to doped silicon. As any given silicide presents a Schottky barrier to both electrons and holes, the same exact device structure can be used for NFETs and PFETs, with the only difference being the implanted species to form the doped regions in each device.

[0055] By way of example only, fabrication of one example of a circuit 10 in accordance with embodiments of the present invention is discussed below:

[0056] The process flow started with p-type (boron-doped, 14-22 Ω-cm, or 4-8x10^{14} cm^{-3}) UNIBOND SOI wafers with a body thickness, t_{body}, of 100 nm and a buried oxide (BOX) thickness of 200 nm. After defining the active regions, phosphorus was implanted into selected regions for n-well formation at 50 keV with a 5x10^{11} cm^{-2} dose and a subsequent four hour furnace anneal at 1000 °C in N_2. Simulation showed the resultant n-well profile to be uniform throughout the entire body region with a concentration of 1x10^{15} cm^{-3} after all thermal processing. A 9 nm gate oxide was thermally grown, after which 130 nm of undoped polysilicon with a 100 nm nitride cap were deposited via LPCVD. After gate patterning, a 30 nm thick oxide sidewall spacer was grown. The oxide over

the source/drain regions was then removed in a dry etch with CHF_3 and O_2 and the nitride cap was stripped in phosphoric acid at 175 °C.

[0057] A 30s, 50:1 HF dip, followed by a 1 min rinse in DI water and then a spin rinse/dry, was performed. The wafers were immediately loaded into a sputter chamber and placed under vacuum. Nickel was then sputter deposited to ~ 45 nm after reaching a base pressure of 1-2 μtorr. The silicidation step was performed at 500 °C for 1 min in N_2 via RTA, and unreacted nickel was removed in a 2:1 H_2O_2:H_2SO_4 mixture at 90 °C. Although a two-step silicidation process is more suitable for aggressive scales, in this study, the devices are large enough to warrant a one-step silicidation without the risk of shorting across the body region.

[0058] An implant-to-silicide (ITS) process was performed for both the NFETs (phosphorus implant) and the PFETs (BF_2 implant). For all implants, the dose and energy were $4x10^{15}$ cm^{-2} and 34 keV, respectively. To form the doped regions, a subsequent thermal anneal was performed via RTA at 600 °C or 700 °C for 30 min in 10 min pulses (table shown in FIG. 6). For some splits, fluorine was blanket implanted ($4x10^{15}$ cm^{-3} at 34 keV) before the n- and p-type doped implant windows were defined. The primary purpose of the fluorine implant was to increase the thermal stability of the NiSi (from 600 °C to 750 °C), thus reducing defects at the M-S junction and potentially facilitating higher active dopant concentrations in the doped regions (i.e., higher drive current). While fluorine is already present in the BF_2 implant to serve this purpose, it is not present during the phosphorus implant, and so the upper thermal limit is restricted by the NFETs to 600 °C due to silicide agglomeration.

[0059] After the doped region formation, aluminum metallization was performed with an evaporation/liftoff process. The cross-section of the final circuit, an inverter in this example, is illustrated in FIG. 1, which shows the NFET 12 and PFET 14 sharing a fully silicided (FUSI) source/drain region 16 at the output terminal 18. Simultaneously, this region 16 acts as isolation between the NFET 12 and PFET 14, facilitating a simpler contact scheme while maintaining or

increasing the local interconnect pitch and reducing the gate pitch for increased circuit density with devices of a given size.

[0060] Set forth below are results and analysis of the circuit 10 and characteristics of the circuit 10 which was fabricated in the example as described above:

[0061] Referring to FIG. 7, inverter voltage transfer characteristics (VTCs) for mask-defined gate lengths ($L_{g,m}$) from 2 μm down to 0.6 μm, mask defined width (W_m) of 1 μm, and a power supply voltage (V_{DD}) of 3 V are illustrated. These results are from split 1, as shown in the table in FIG. 6. The poorer pull-up performance relative to the pull-down performance is due to excessive NFET leakage as illustrated in FIG. 8, which shows punchthrough-like characteristics. In particular, the NFET behavior in FIG. 8 at low V_{GS} and V_{DS} ~ 1.2 V and ~ 4 V shows two "kinks," indicating two diodes in parallel, where one diode has a lower threshold voltage and a high resistive component, while the other diode has a higher threshold voltage and a low resistive component. This can be explained by the n-type doped region not extending the full body thickness, but instead forming a doped region near the top of the body, while at the bottom of the body there exists a leaky/defective Schottky junction devoid of a sufficient quantity of dopants. This is not a limitation of the basic device structure, as the result merely suggests the importance of NFET performance on the phosphorus profile throughout the silicide thickness, which can be altered by modulating the phosphorus implant energy and/or silicide or body thickness. Alternatively, one can also reduce this leakage by forming the doped regions with a dopant pile-up approach as opposed to an ITS approach, where the dopants are implanted into the silicon first, and then a silicidation is performed to "pile up" the dopants at and near the M-S interface.

[0062] Some more insight into the physical mechanisms of the NFET leakage is gained through capacitance-voltage (C-V) analysis. The C-V structure used has a 500 μm x 500 μm gate, surrounded by the source/drain silicide. The doped region between this silicide and the body region acts as the body contact. FIG. 9 shows normalized C-V curves for structures with the n-type doped

contacting the n-type body region and the p-type doped region contacting the p-type body region after a post-ITS anneal at 600 °C for 30 min (no fluorine co-implant). While the p-type structure depletes fully, the n-type structure does not. Since the extracted EOT shown in FIG. 9 is thicker than the physical oxide thickness (due to the gate oxide existing in series with some amount of unsilicided, undoped polysilicon), it is highly unlikely that the phosphorus implant punched through the gate stack, which would increase the body doping and therefore body capacitance. The source/drain capacitance, therefore, is the cause of this increased capacitance floor observed in FIG. 8. The frequency dependence of these curves suggests that the NFET source/drain capacitance is artificially high due to defect-induced leakage at the M-S junction toward the source/drain-BOX interface, perhaps due to silicide agglomeration in this region. This agrees well with the current-voltage data shown in FIG. 8.

[0063] Referring to FIGS. 10A and 10B, the NFET I_{DS} vs. V_{DS} and transfer characteristics, respectively, for the three process splits, are shown while FIGS. 11A and 11B show the same for the PFET. For both devices, $L_{g,m} = 2$ μm and $W_m = 1$ μm. Split 3 is not shown in FIG. 10B, as it is little more than a log-linear curve, which FIG. 5A already suggests. Both FIGS. 10A, 10B, 11A, and 11B show that, between splits 1 and 2, both the NFET and PFET achieve higher drive current without a fluorine co-implant for a given post-ITS anneal, which suggests that the co-implanted fluorine reduces dopant diffusion within the silicide, thus reducing the size and concentration of the doped region extending from the silicide. For the NFET, the fluorine co-implant actually increases drain-induced barrier lowering (DIBL) and subthreshold swing (SS), while only SS is increased for the PFET. This is explained by fluorine acting as an n-type dopant in addition to a diffusion inhibitor, spreading out the tail of the n-type doped region (while also reducing the interface concentration) and counterdoping and/or reducing diffusion of the p-type doped region. As a result, for the PFET, the influence of the Schottky barrier at the M-S junction is increased, consequently increasing SS, which FIG. 11B shows. For the NFET, the influence of the Schottky barrier is also increased, as shown in FIG. 10A, where the curves for split 2 exhibit some sub-linear behavior.

[0064] The original purpose of the fluorine co-implant, however, was to facilitate higher temperature post-ITS anneals, and that the higher temperature may outweigh any adverse effect of the fluorine on device performance. At least in terms of drive current, this seems to be the case for the NFET (FIG. 10A). Split 3 restores the performance in the linear region compared to split 2, even improving on what is achieved with split 1 with much higher drive current. Notably, most of the increase in drive current is attributed to the increased leakage; however, to a first order approximation, subtracting this leakage (~ 90 μA/μm at V_{DS} = 5 V) still yields an increase in drive current over Split 1 by ~ 25 μA/μm. As mentioned earlier, this leakage can be improved upon by spreading the as-implanted phosphorus profile out more within the silicide, either by thinning the body region and/or increasing the implant energy.

[0065] The exact opposite effect of fluorine happens for the PFET at 700 °C, however (FIGS. 11A and 11B). While the DIBL and SS performance of split 3 is comparable to split 2, the drive current is considerably lower than both splits 1 and 2. That the drive current changes inversely with temperature suggests a stronger thermal activation dependence for fluorine than boron in the temperature range of interest and that, again, the fluorine is counterdoping the p-type doped region. As a result, inverter VTCs could not be demonstrated with split 3, as the PFET drive capability cannot outweigh the NFET leakage. A well-engineered metallic source/drain (MSD) CMOS circuit fabricated using an ITS process, then, would mask the fluorine co-implant from the PFETs.

[0066] Although anomalous compared to the rest of the available test samples, one sample from split 2 did indeed yield reasonable NFET performance as shown in FIG. 12A, due to a doped region that consumes a larger percentage of the body thickness. However, that the NFET off state remains flat at ~ 60 pA/μm (for V_{DS} = 0.1 V) while the PFET off state drops below 1 pA/μm suggests that minority carrier tunneling through the NFET doped region is greater than through the PFET doped region. This could be due to a smaller lateral junction depth and/or a lower dopant concentration at the M-S interface, either of which will enhance said tunneling injection due to a narrower or lower effective tunneling

barrier to minority carriers, respectively. The GIDL-like leakage in the saturation mode curves in FIG. 12A is due to band-to-band tunneling (BTBT) at the drain-body barrier, as well as some tunneling through the doped region, as discussed previously. Although this may limit inverter performance for non-optimized devices, as FIG. 12B shows for the devices from FIG. 12A, doped regions can be engineered to eliminate this effect for a given operating voltage by changing factors such as the dopant concentration in this region, the junction depth of this region, and the gate overlap/underlap to this region.

[0067] Accordingly, a metallic source/drain (MSD) CMOS on a silicon on insulator substrate in accordance with embodiments of the present invention has been demonstrated. As described and illustrated herein, the present invention enables an increase in the density of devices, such as transistors, on the substrate without having to scale down the size of the devices.

[0068] Having thus described the basic concept of the invention, it will be rather apparent to those skilled in the art that the foregoing detailed disclosure is intended to be presented by way of example only, and is not limiting. Various alterations, improvements, and modifications will occur and are intended to those skilled in the art, though not expressly stated herein. These alterations, improvements, and modifications are intended to be suggested hereby, and are within the spirit and scope of the invention. Additionally, the recited order of processing elements or sequences, or the use of numbers, letters, or other designations therefore, is not intended to limit the claimed processes to any order except as may be specified in the claims. Accordingly, the invention is limited only by the following claims and equivalents thereto.

CLAIMS

What is claimed is:

1. A circuit comprising:

a first transistor formed on a substrate; and

a second transistor formed on the substrate adjacent the first transistor, wherein a source region of one of the first and second transistors and a drain region of the other one of the first and second transistors are the same and comprise substantially the same one or more materials.

2. The circuit as set forth in claim 1 wherein the substrate comprises silicon on at least one insulating layer.

3. The circuit as set forth in claim 1 wherein the first and second transistors comprise an NFET and a PFET.

4. The circuit as set forth in claim 1 wherein the first and second transistors each comprise a MOSFET.

5. The circuit as set forth in claim 4 wherein the MOSFET comprises a Schottky barrier MOSFET.

6. The circuit as set forth in claim 1 further comprising at least one doped region with at least one dopant formed adjacent the source region and the drain region that comprise the same one or more materials.

7. The circuit as set forth in claim 6 further comprising another doped region with at least one other dopant formed adjacent the source region and the drain region that comprise the same one or more materials.

8. The circuit as set forth in claim 1 wherein the same one or more materials comprise one of metal and a metal-semiconductor alloy.

9. The circuit as set forth in claim 1 wherein the source region and the drain region that comprise the same one or more materials extends substantially from an insulating layer in the substrate to a surface to isolate the first transistor from the second transistor.

10. The circuit as set forth in claim 1 wherein the source region and the drain region that comprise the same one or more materials is at a first level which receives one or more wiring connections.

11. The circuit as set forth in claim 1 further comprising a gate region for each of the first and second transistors, at least one of the gate regions having a sidewall spacer around a portion of the gate region.

12. A method of making a circuit, the method comprising:
providing a substrate; and
forming first and second transistors on the substrate, the second transistor is formed adjacent to the first transistor, wherein a source region of one of the first and second transistors and a drain region of the other one of the first and second transistors are the same and comprise substantially the same one or more materials.

13. The method as set forth in claim 12 wherein the providing a substrate further comprises:
forming an insulating layer in the substrate; and
depositing silicon on the insulating layer.

14. The method as set forth in claim 12 wherein the first and second transistors comprise an NFET and a PFET.

15. The method as set forth in claim 12 wherein the first and second transistors each comprise a MOSFET.

16. The method as set forth in claim 15 wherein the MOSFET comprises a Schottky barrier MOSFET.

17. The method as set forth in claim 12 further comprising forming at least one doped region with at least one dopant adjacent the source region and the drain region that comprise the same one or more materials.

18. The method as set forth in claim 17 further comprising forming another doped region with at least one other dopant adjacent the source region and the drain region that comprise the same one or more materials.

19. The method as set forth in claim 12 wherein the same one or more materials comprise one of metal and a metal-semiconductor alloy.

20. The method as set forth in claim 12 wherein the source region and the drain region that comprise the same one or more materials extends substantially from an insulating layer in the substrate to a surface to isolate the first transistor from the second transistor.

21. The method as set forth in claim 12 wherein the source region and the drain region that comprise the same one or more materials is at a first level which receives one or more wiring connections.

22. The method as set forth in claim 12 further comprising forming a sidewall spacer around at least one gate region for each of the first and second transistors.

23. A method for making a circuit, the method comprising:
forming at least one active region in a substrate;
doping the active region for a first transistor and a second transistor;

depositing at least one metal at least in source region of one of the first and second transistors and a drain region of the other one of the first and second transistors; and

performing silicidation at least once on the deposited metal, the source region of one of the first and second transistors and the drain region of the other one of the first and second transistors are the same and comprise substantially the same metal-semiconductor alloy.

24. The method as set forth in claim 23 further comprising:

forming an insulating layer in the substrate; and

depositing silicon on the insulating layer.

25. The method as set forth in claim 23 wherein the first and second transistors comprise an NFET and a PFET.

26. The method as set forth in claim 23 wherein the first and second transistors each comprise a MOSFET.

27. The method as set forth in claim 26 wherein the MOSFET comprises a Schottky barrier MOSFET.

28. The method as set forth in claim 23 further comprising performing implantation to form at least one doped region adjacent one portion of the metal-semiconductor alloy.

29. The method as set forth in claim 23 further comprising:

forming a gate region for each of the first and second transistors; and

forming another source region for the other one of the first and second transistors and another drain region for the other one of the first and second transistors.

30. The method as set forth in claim 23 further comprising forming a sidewall spacer around at least one of the gate regions for each of the first and second transistors.

31. The method as set forth in claim 23 wherein the metal-semiconductor alloy extends substantially from an insulating layer in the substrate to a surface to isolate the first transistor from the second transistor.

32. The method as set forth in claim 23 wherein the metal-semiconductor alloy is at a first level which receives one or more wiring connections.

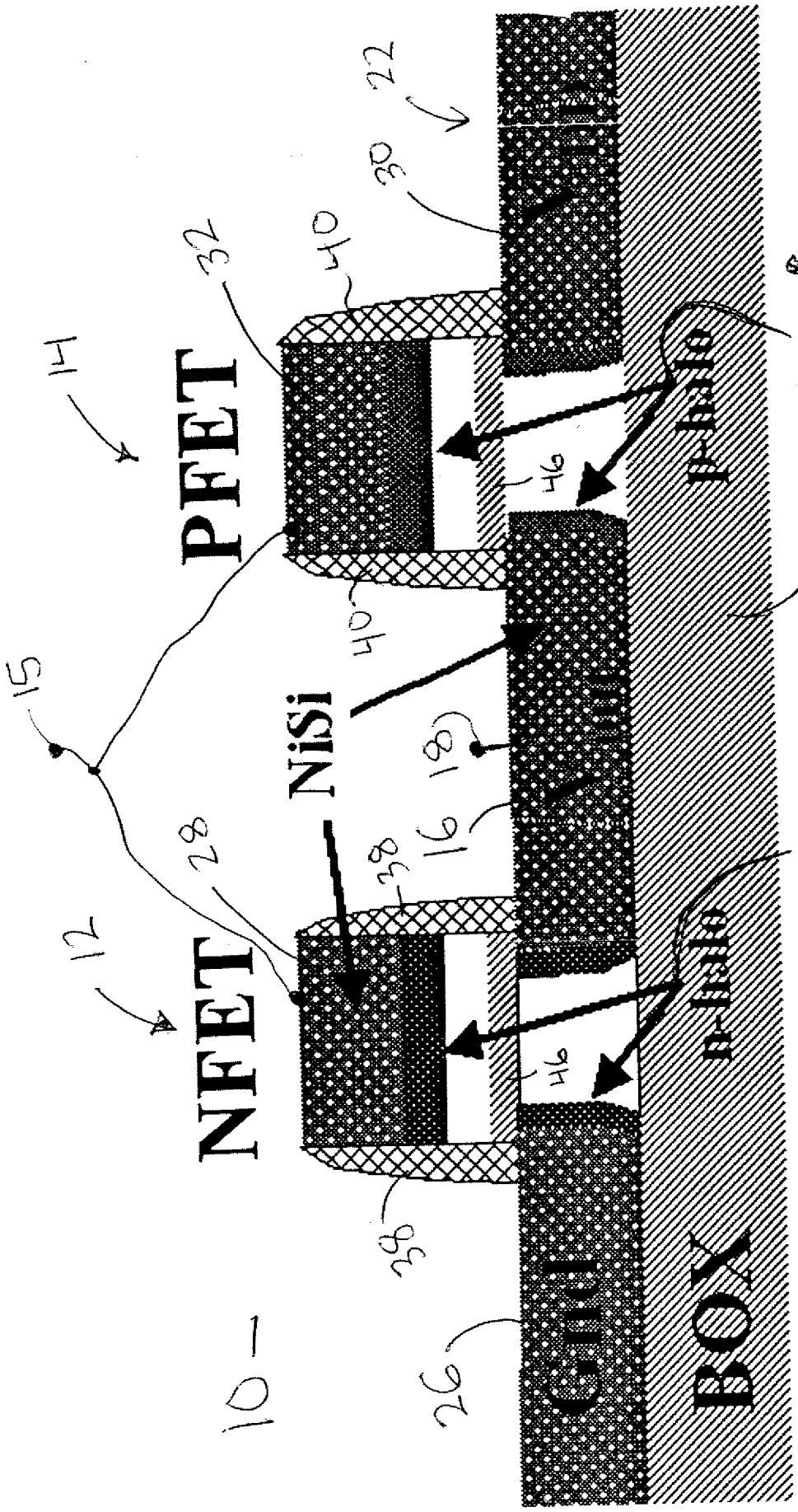

PFET
NFET
NiSi
n-type
n-type
BOX
10
12
14
15
16
18
20
22
24
26
28
30
31
32
34
36
38
40
46

FIG. 1

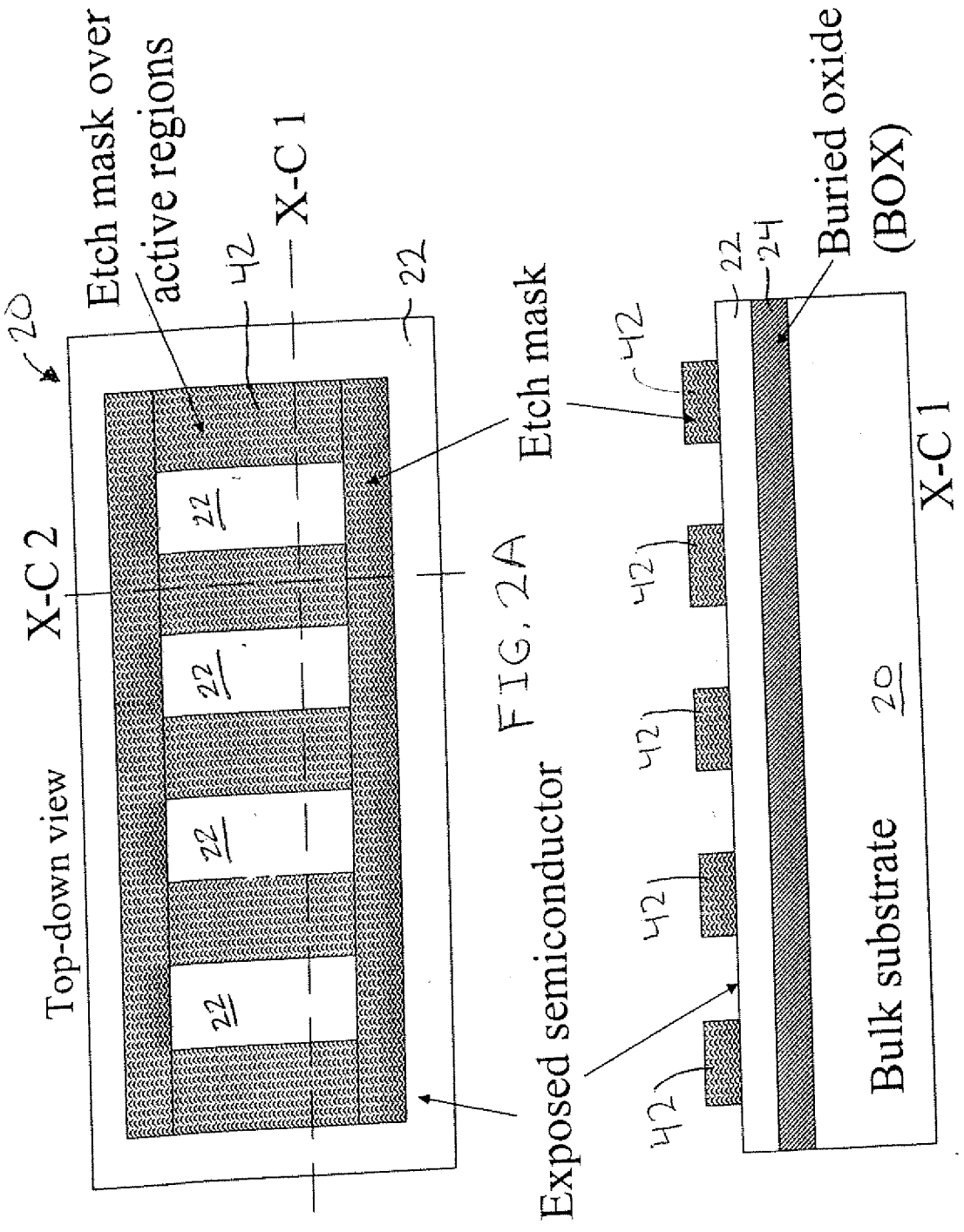


FIG. 2A

FIG. 2B

Step 1: Define inter-circuit isolation regions/active regions

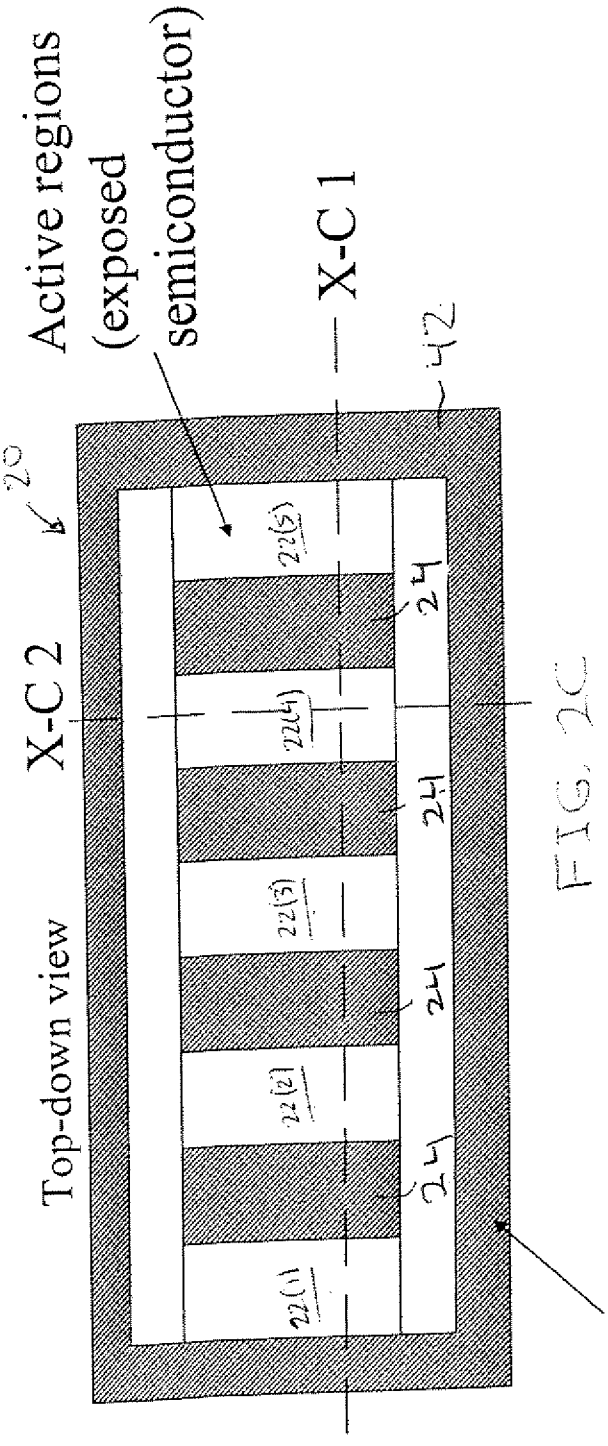


FIG. 2C

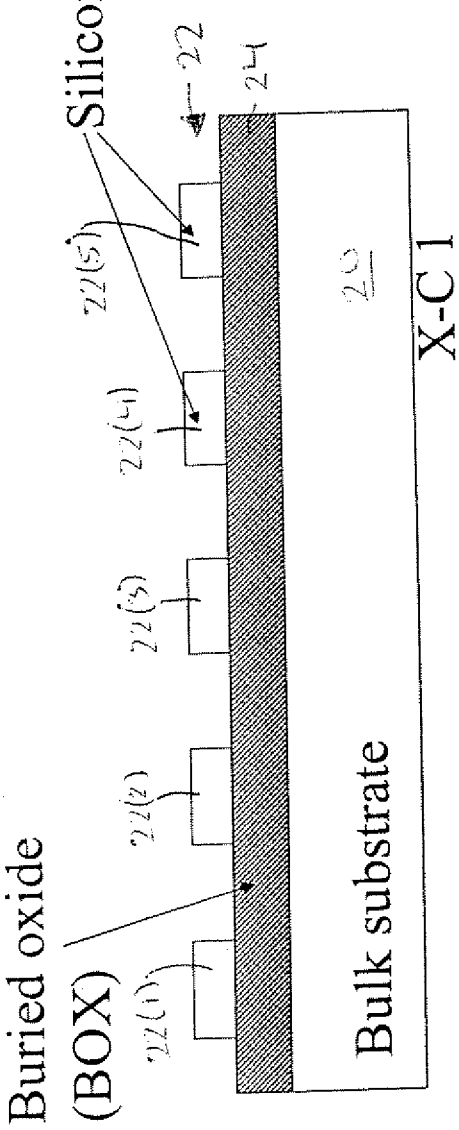


FIG. 2D

Step 2: Etch active regions, then remove etch mask.

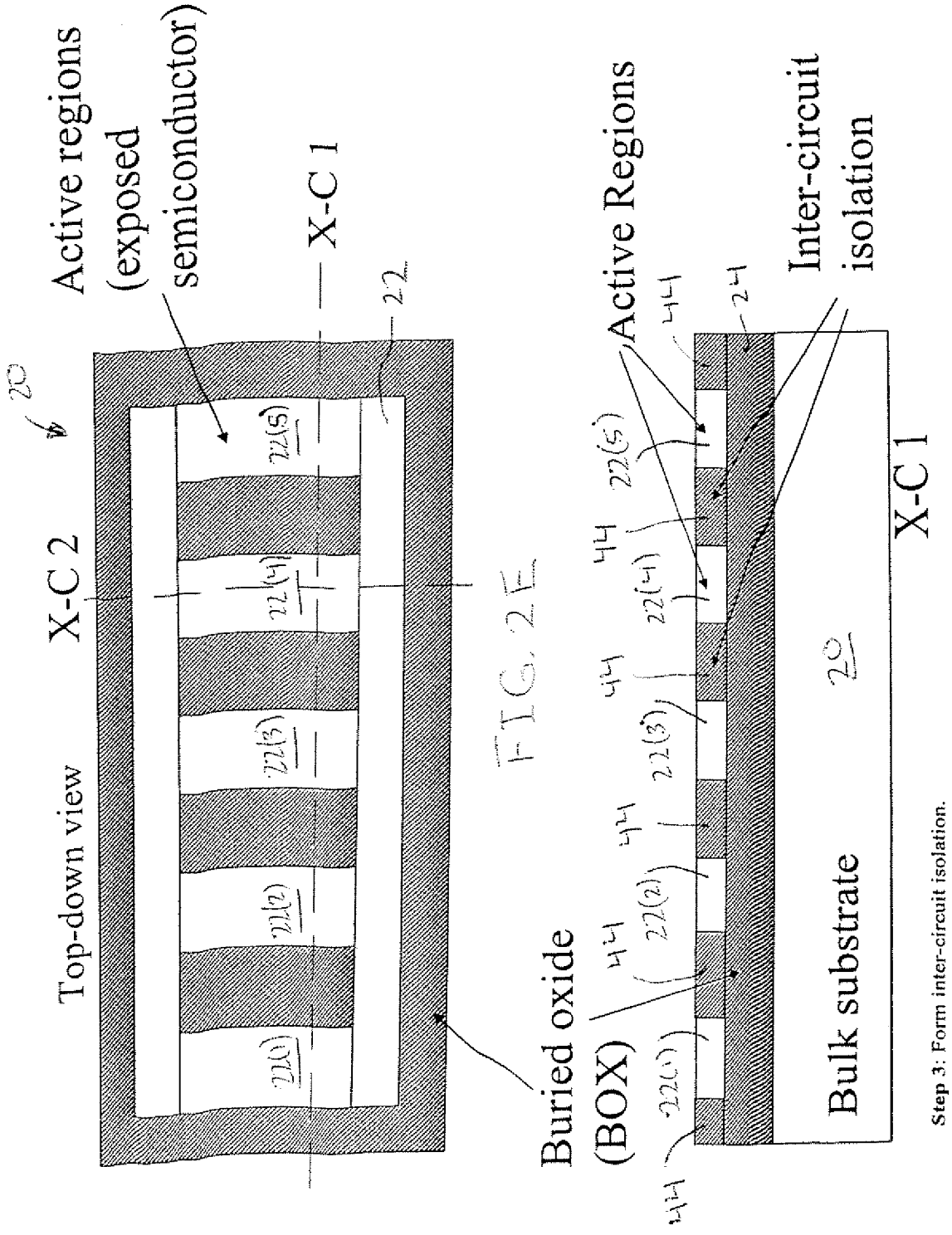
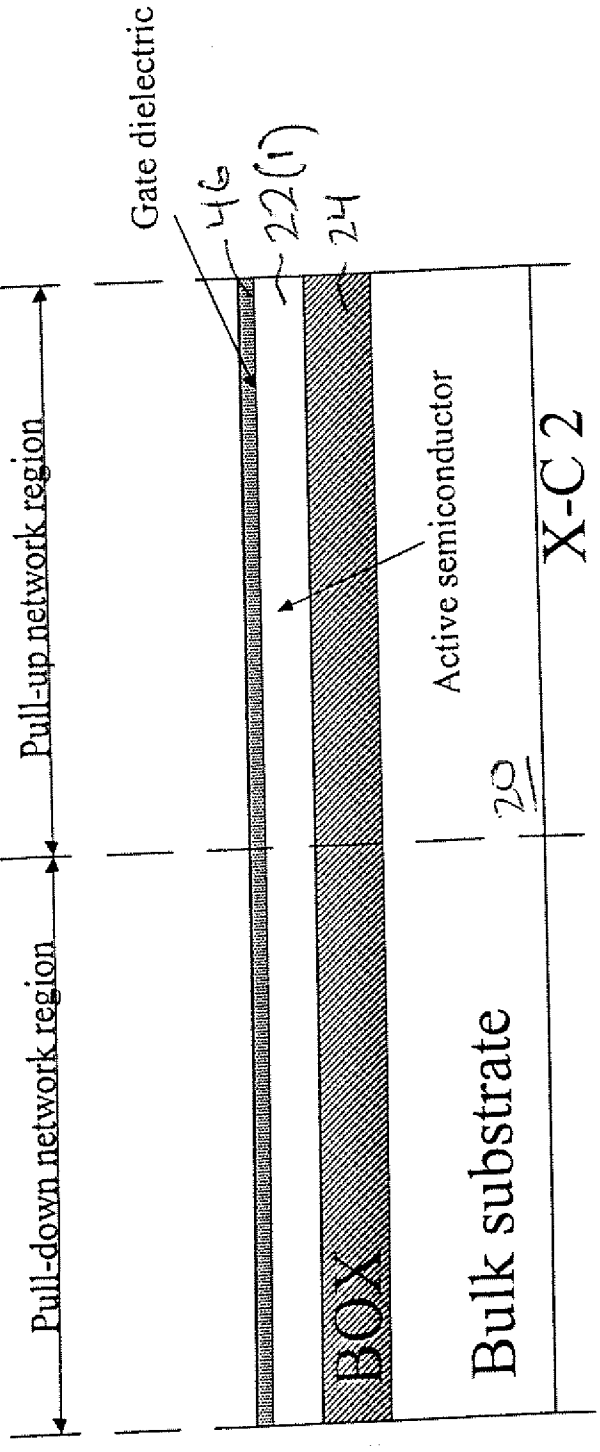


FIG. 2E

FIG. 2F

Step 3: Form inter-circuit isolation.



Step 4: Grow or deposit gate dielectric.

FIG. 2G

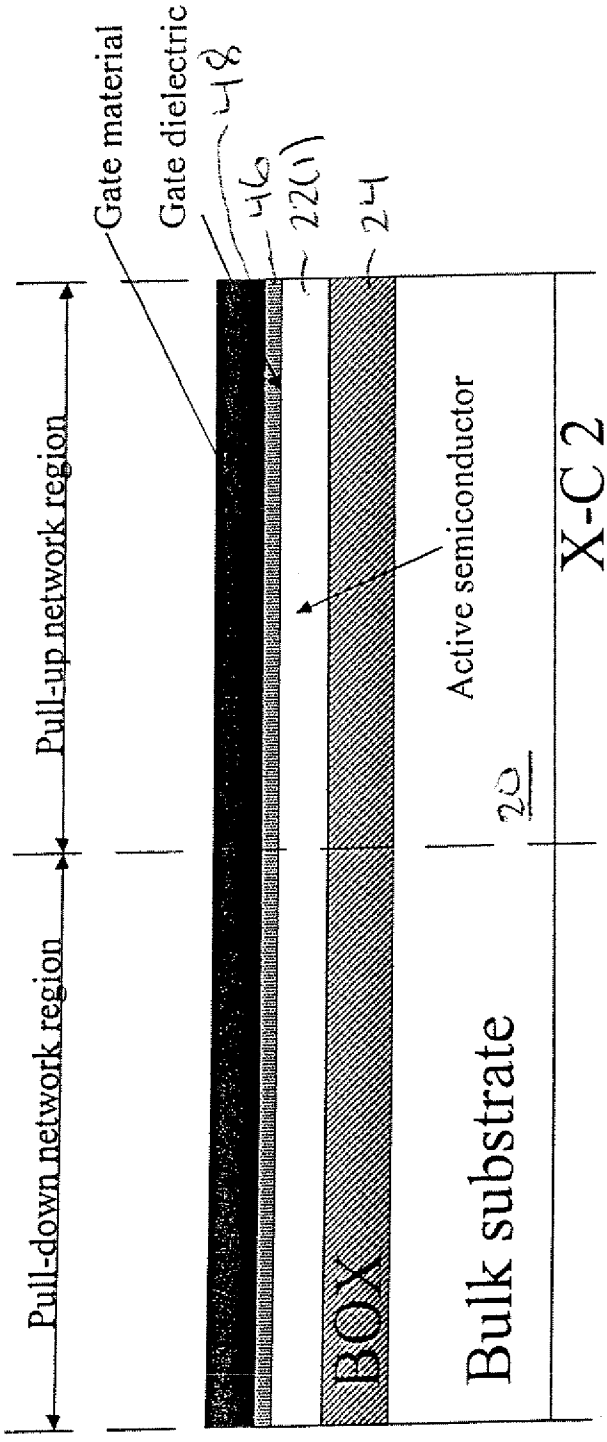


FIG. 2H

Step 5: Deposit gate material.

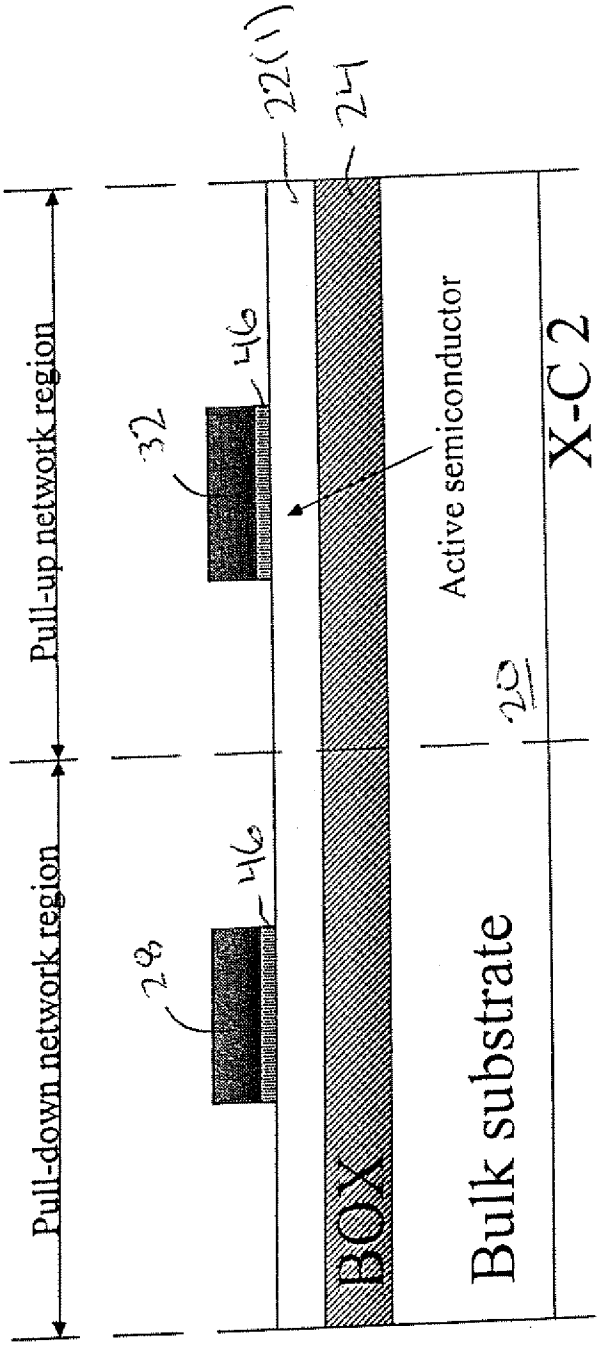


FIG. 2I

Step 6: Pattern gates.

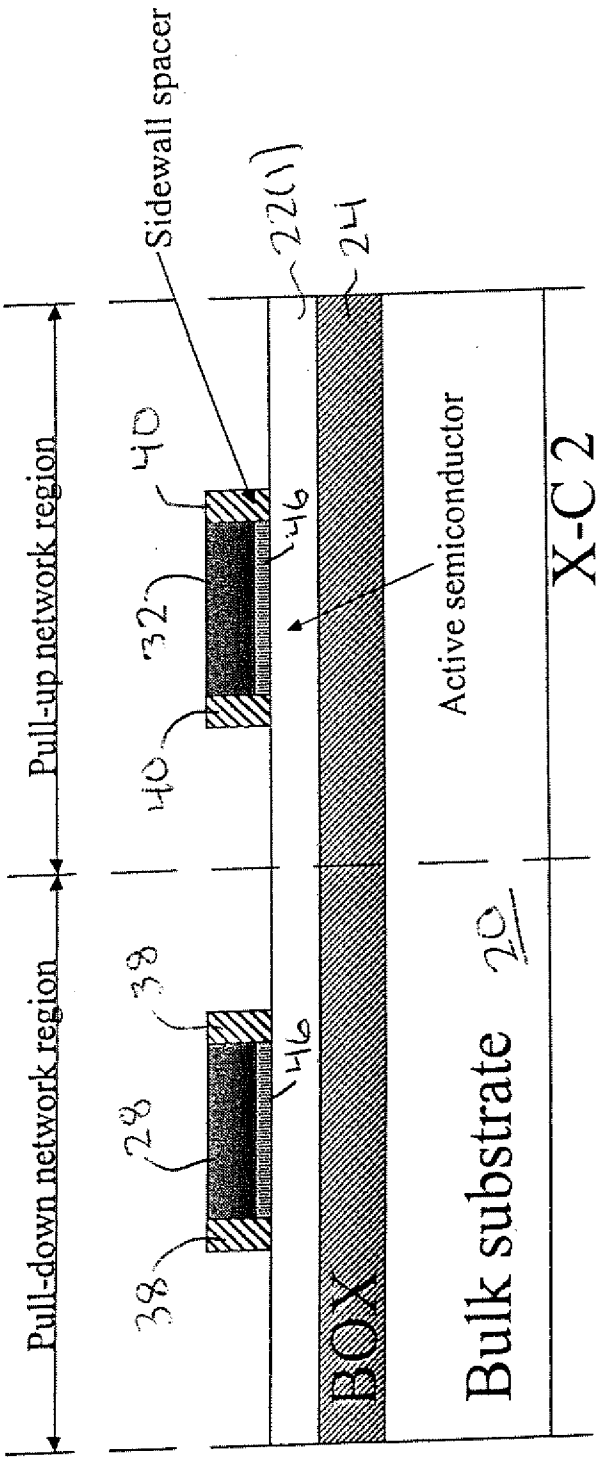
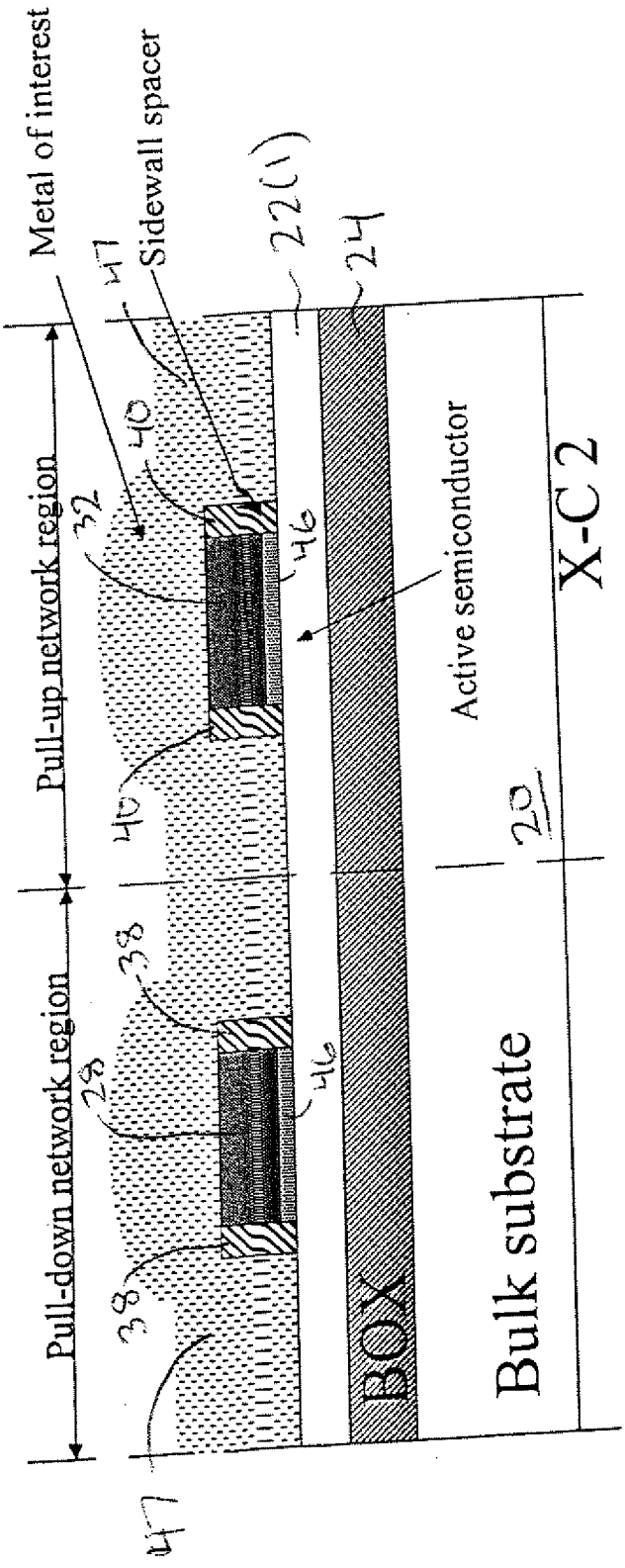


FIG. 2J

Step 7: Form sidewall spacers. This can be done by depositing and anisotropically etching a film (such as silicon nitride), or by oxidizing the gate sidewalls (provided the gate is made of polysilicon), or both.



Step 8: Deposit metal of interest (to be used to form the silicide).

FIG. 2K

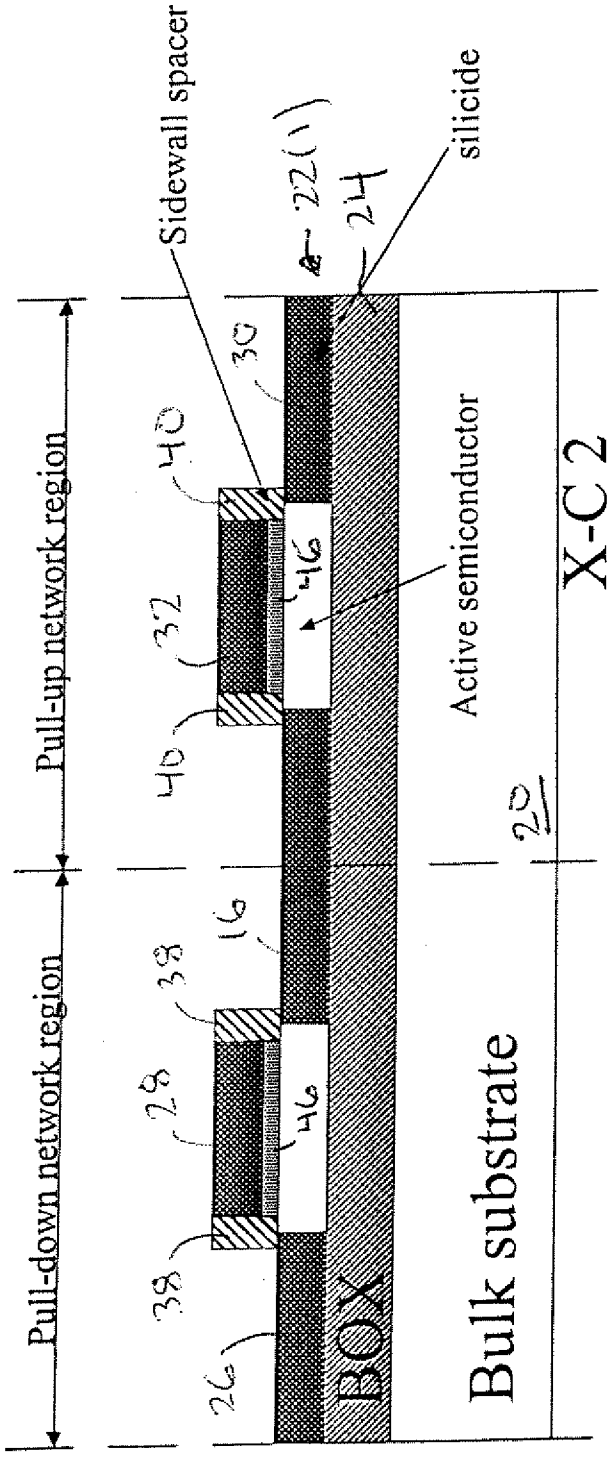
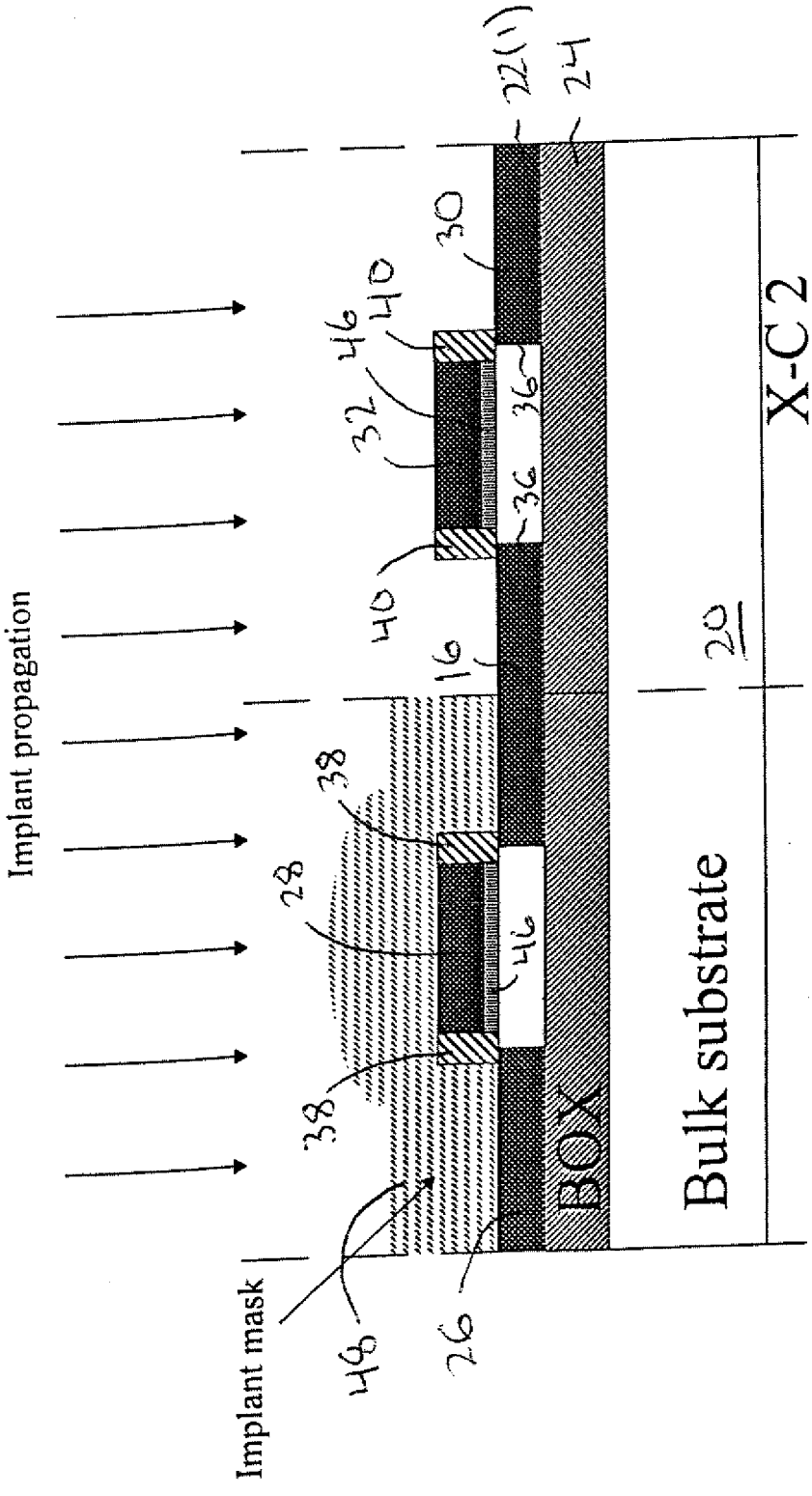


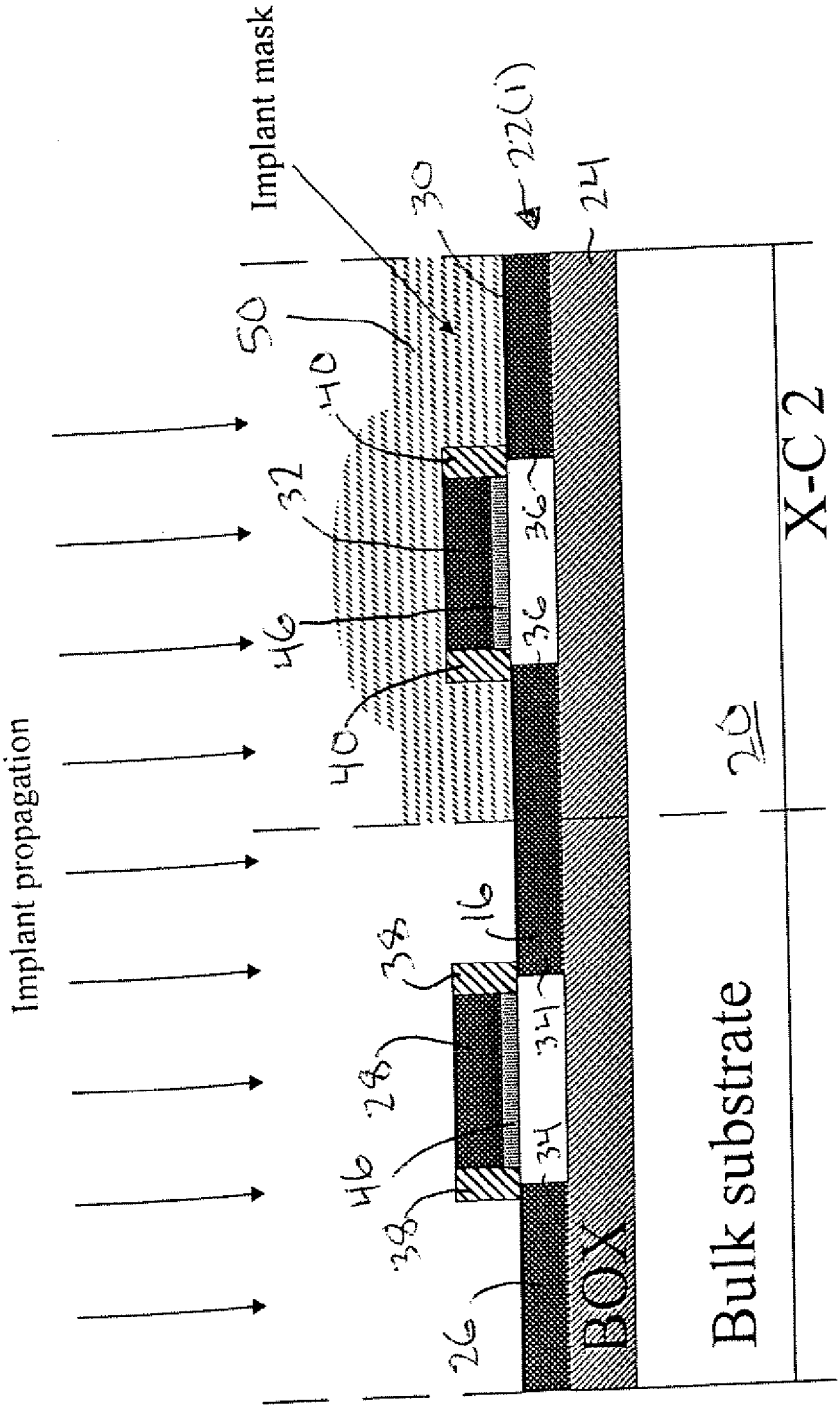
FIG. 2L

Step 9: Perform silicidation, *ensuring full silicidation of the active semiconductor*. If the gate is a polysilicon gate, it can be made thin enough to become fully silicided (shown here). The source/drain silicide may or may not traverse laterally to the point that it becomes overlapped by the gate (in this illustration, it does not).



Step 10: Mask off either pull-up or pull-down region and perform halo implantation (into the silicide) for the other network region using the appropriate species.

FIG. 2M



Step 11: Repeat for other network region.

FIG. 2N

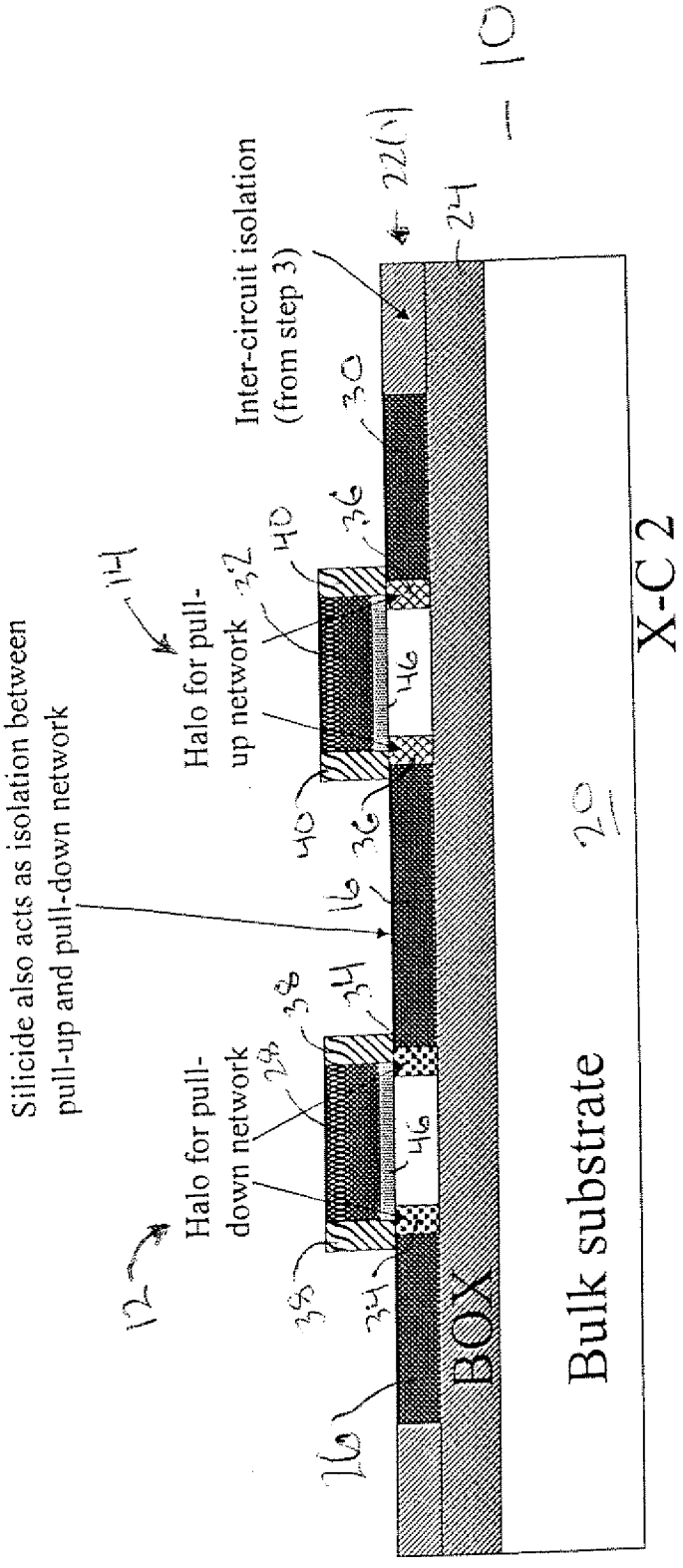
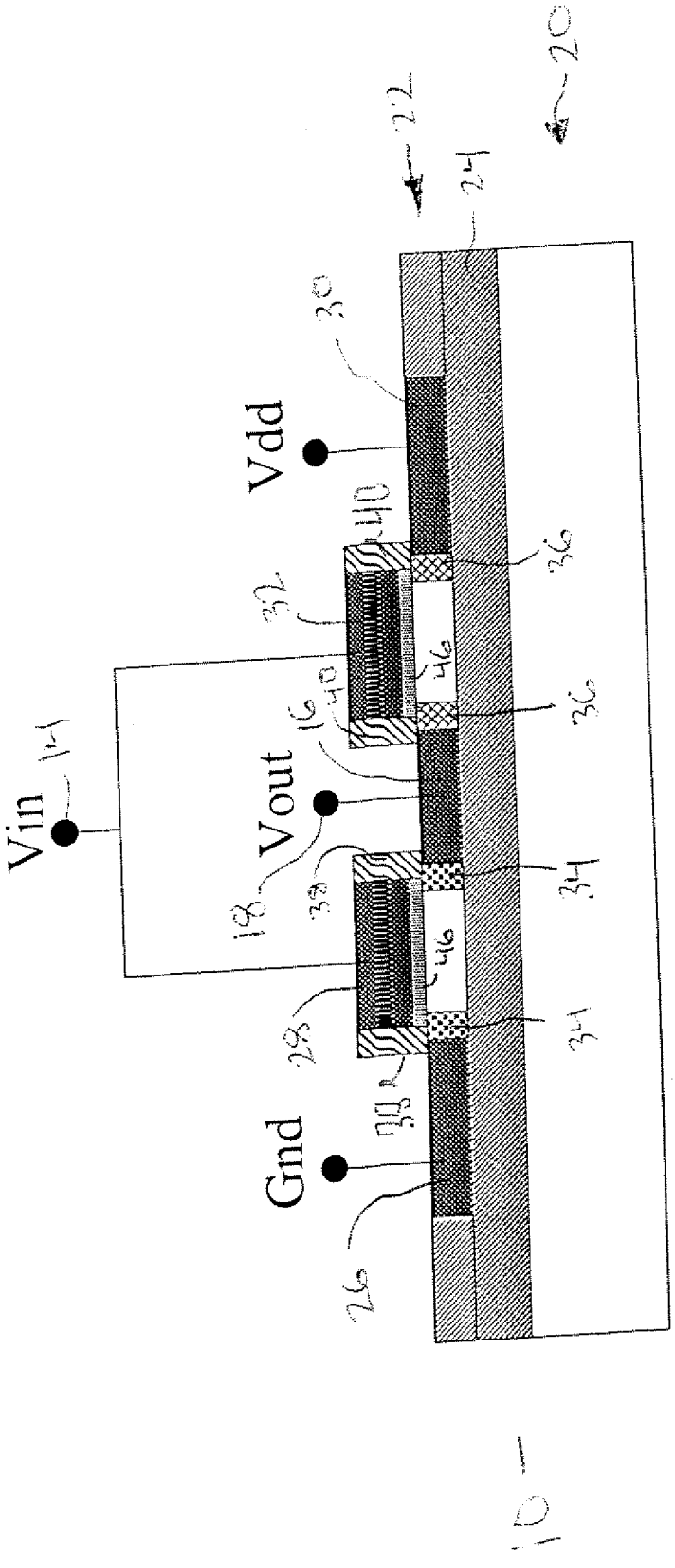


FIG. 20

Step 12: Perform thermal diffusion (this forms the halo regions as the dopants segregate from the silicide into the silicon).



Silicide isolation between pull-up and pull-down network allows for smaller device-to-device pitch

FIG. 2P

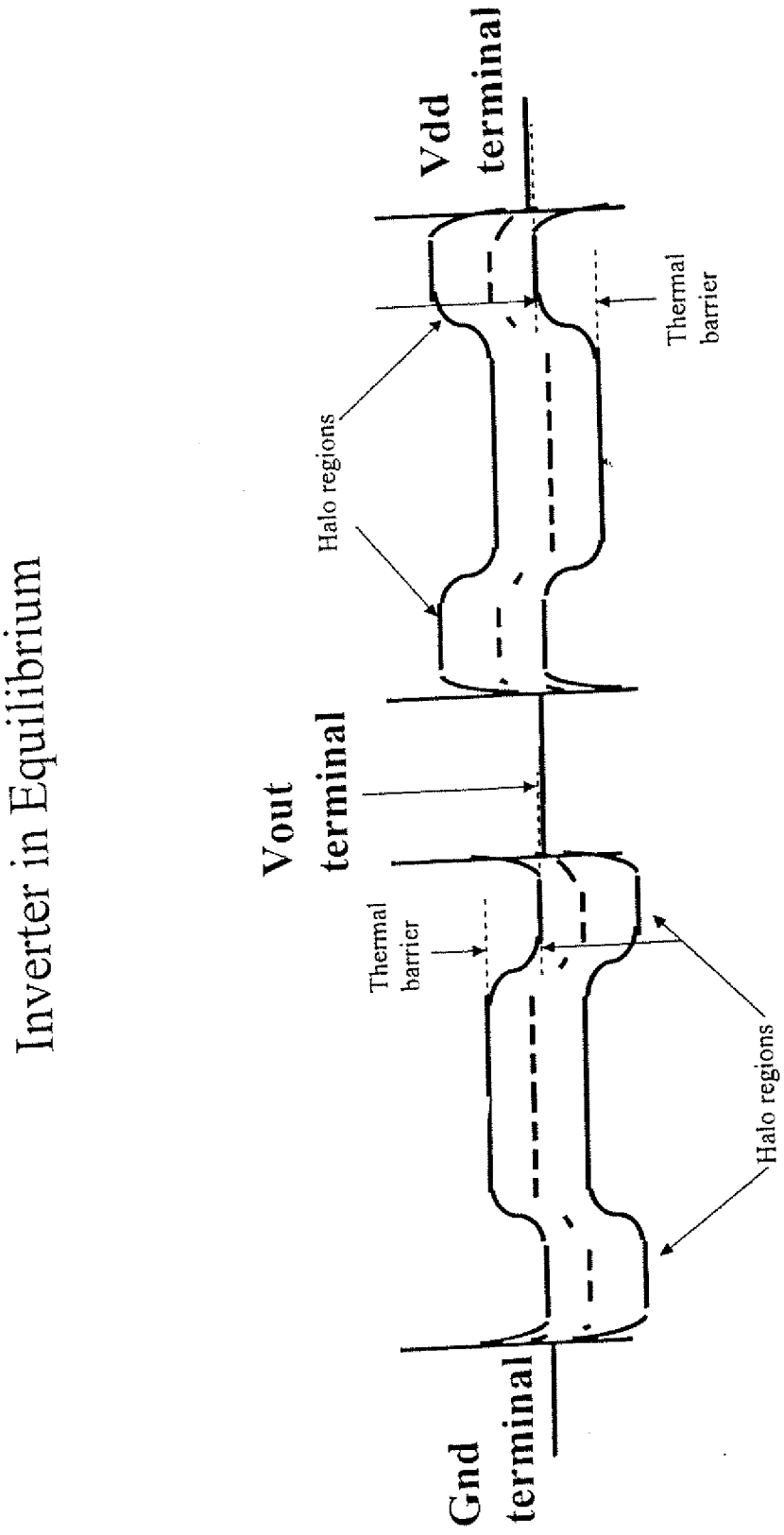
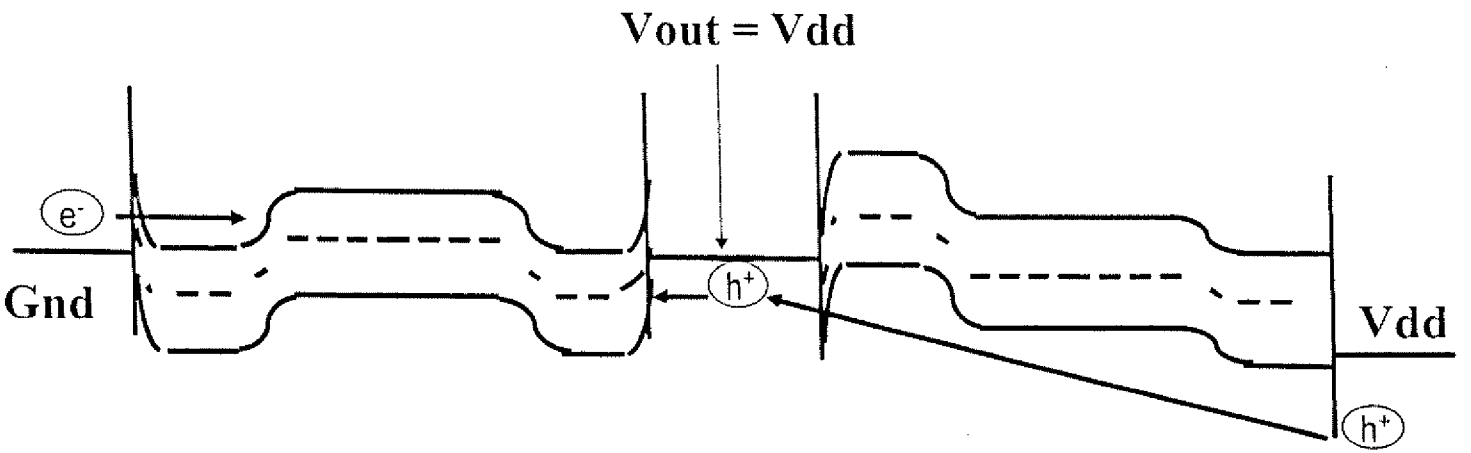

Inverter in Equilibrium
Vdd terminal
Halo regions
Thermal barrier
Vout terminal
Thermal barrier
Halo regions
Gnd terminal
Pull-up network
Pull-down network

FIG. 3

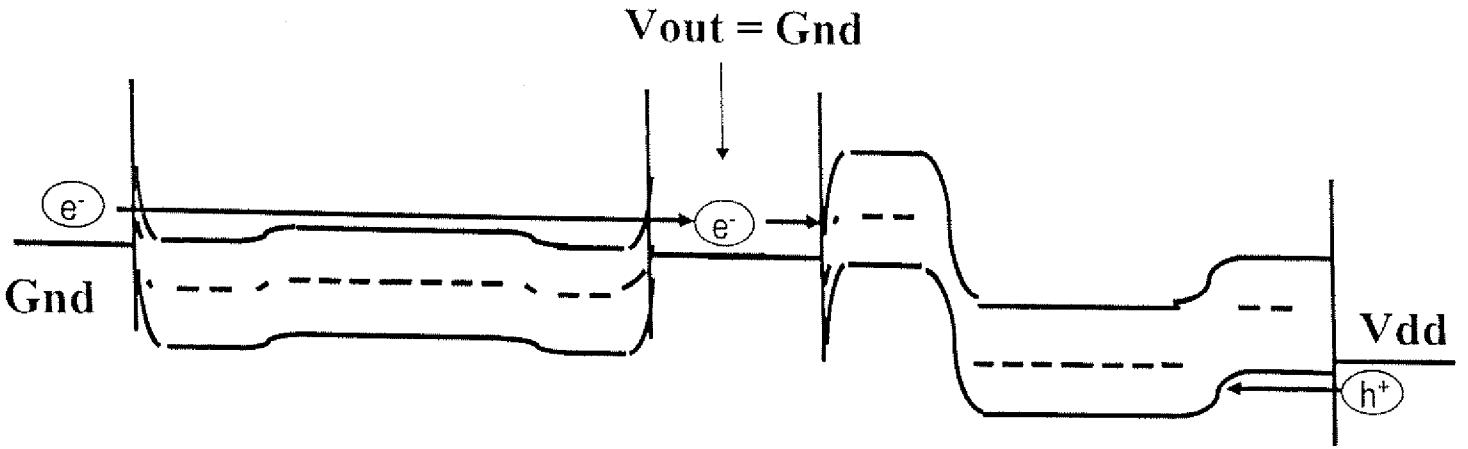
Input voltage = Gnd



P-channel device (pull-up network) turns on and brings Vout to Vdd. Thermal barrier in n-channel device (pull-down network) prevents current flow, so device remains off.

FIG. 4

Input voltage = Vdd



N-channel device turns on and brings Vout to Gnd. Thermal barrier in p-channel device prevents current flow, so device shuts off.

FIG. 5

Split	F^{19} co-implant (Y/N)	Post-ITS anneal (°C/min)	N/PFET well type	N/PFET *EOT* (nm)
1	N	600/30	P/N	18.4/19.2
2	Y	600/30	N/P	17.6/18.6
3	Y	700/30	P/N	15/19.8

FIG. 6

FIG.7

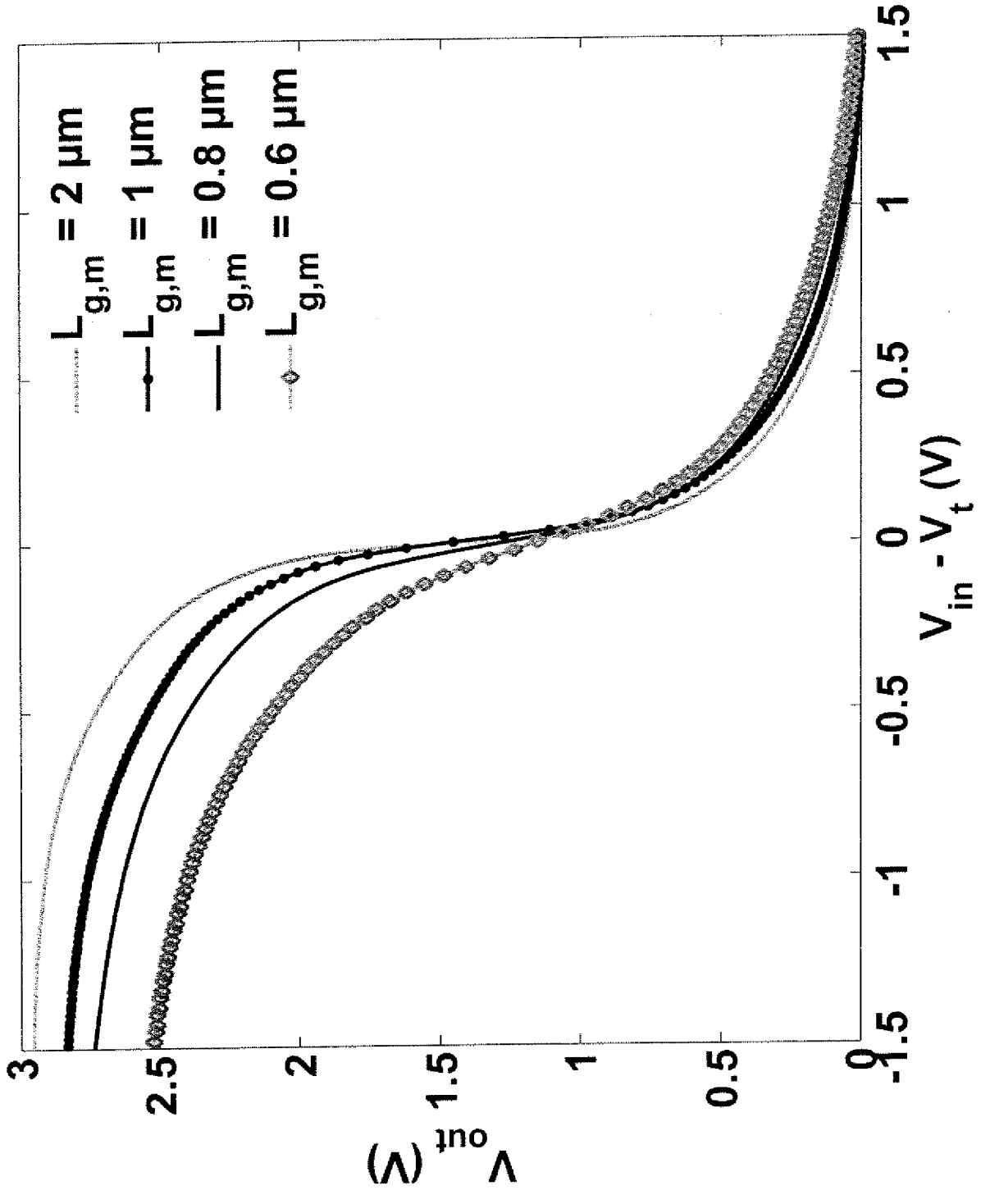

$L_{g,m}$ = 2 µm
$L_{g,m}$ = 1 µm
$L_{g,m}$ = 0.8 µm
$L_{g,m}$ = 0.6 µm
V_{out} (V)
V_{in} - V_t (V)
3
2.5
2
1.5
1
0.5
0
-1.5
-1
-0.5
0
0.5
1
1.5

FIG. 8

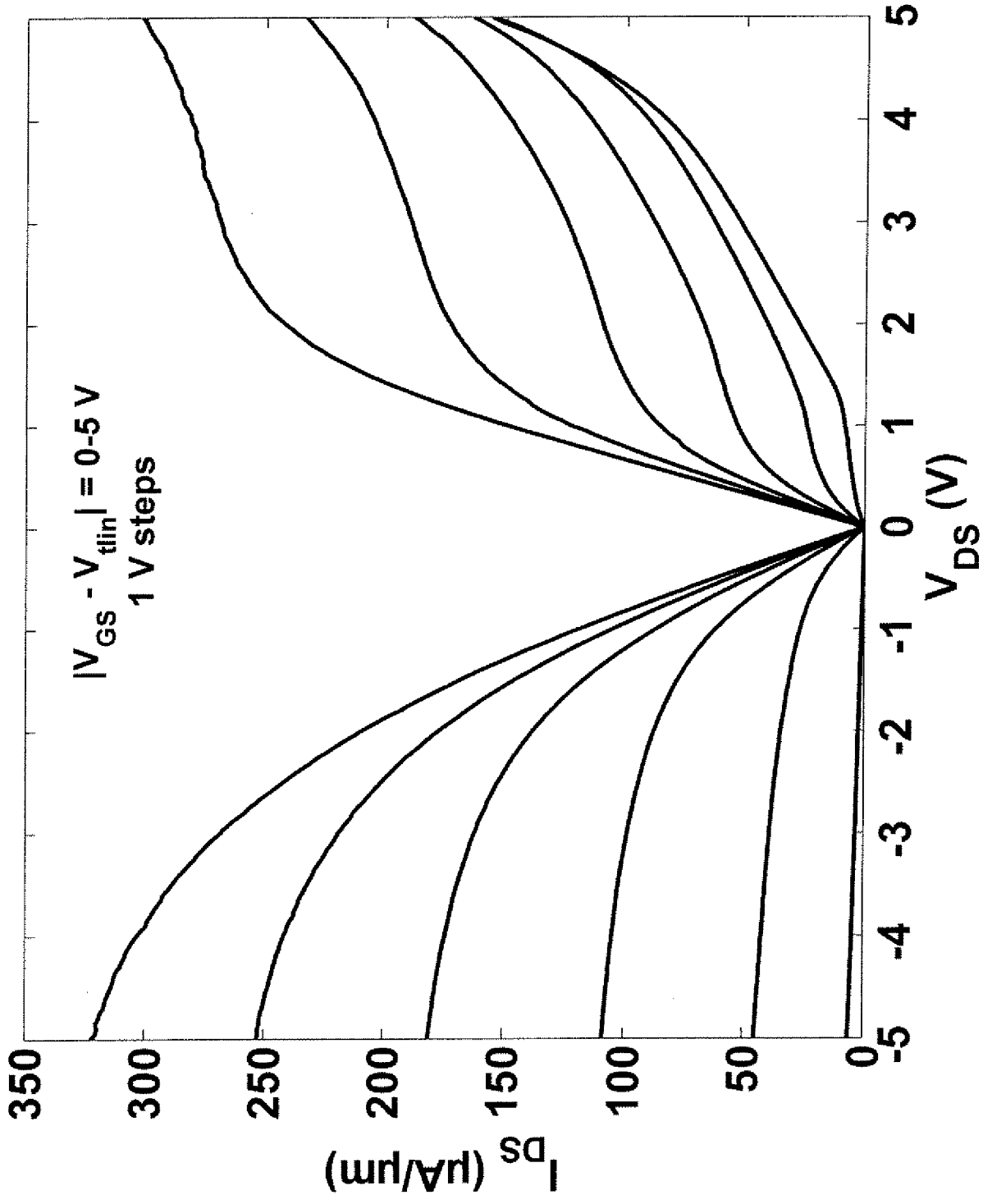
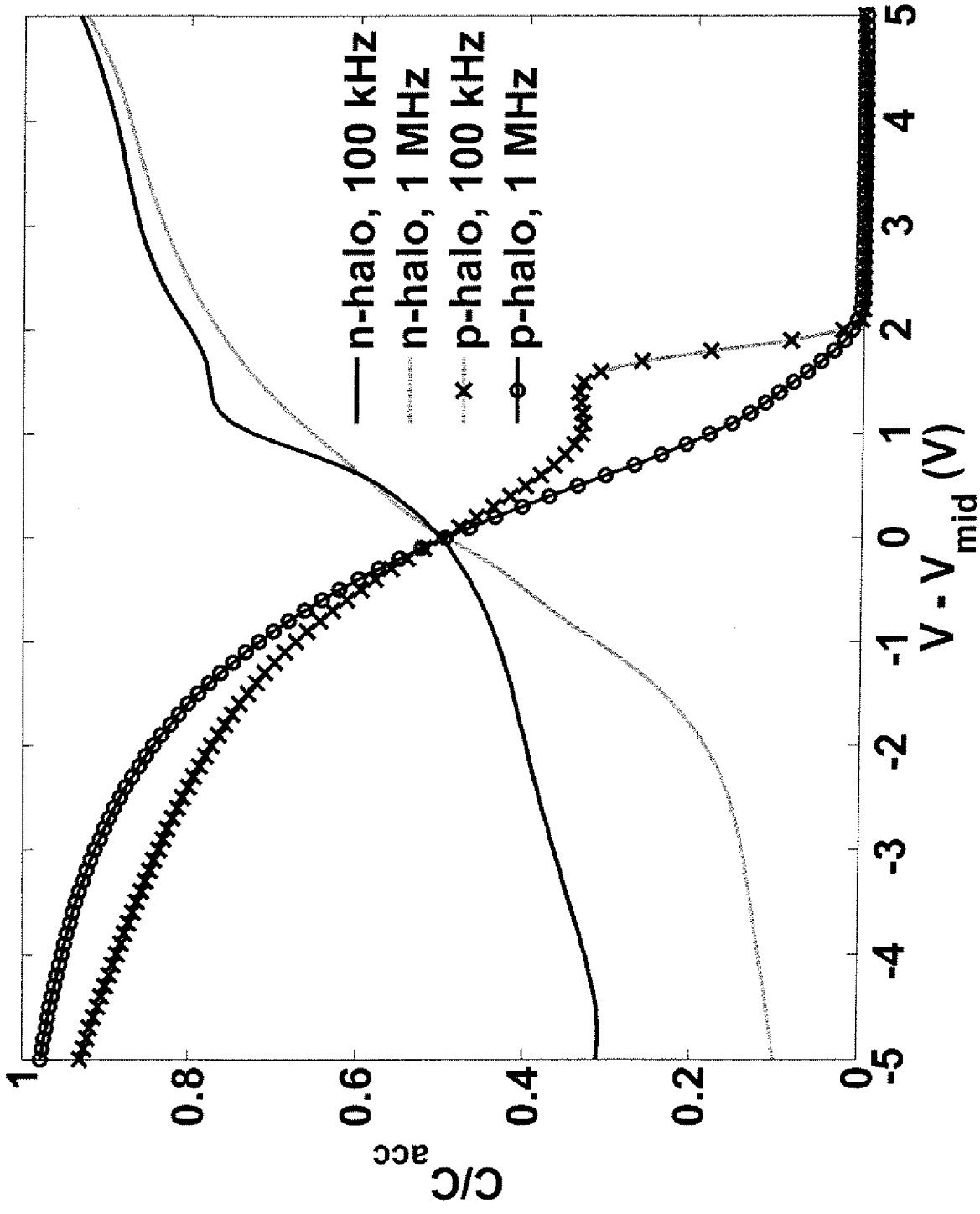

$|V_{GS} - V_{tlin}| = 0\text{-}5$ V
1 V steps
I_{DS} (μA/μm)
V_{DS} (V)
350
300
250
200
150
100
50
0
-5
-4
-3
-2
-1
0
1
2
3
4
5

FIG. 9


n-halo, 100 kHz
n-halo, 1 MHz
p-halo, 100 kHz
p-halo, 1 MHz
C/C_acc
V - V_mid (V)
1
0.8
0.6
0.4
0.2
0
-5
-4
-3
-2
-1
0
1
2
3
4
5

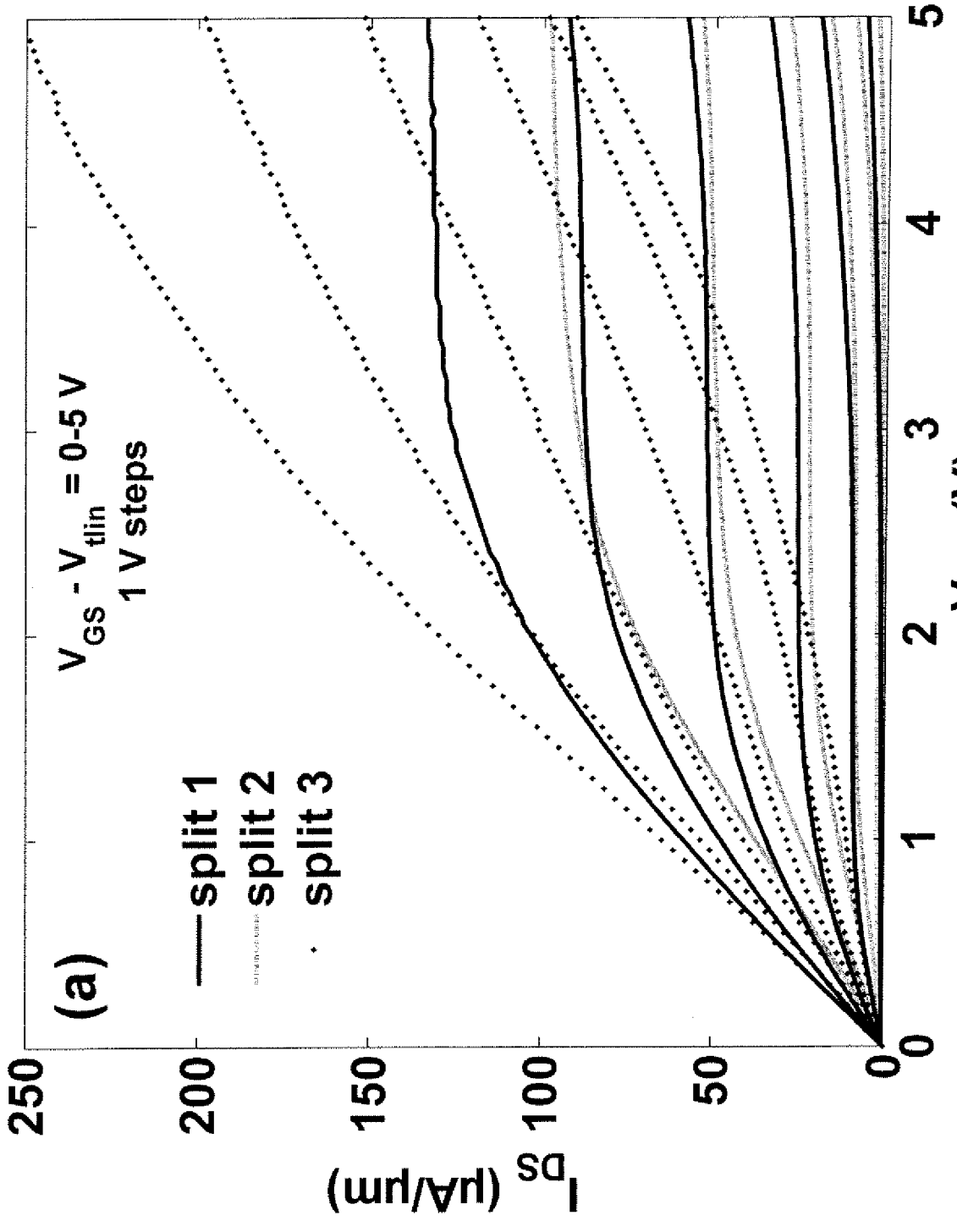

(a)
split 1
split 2
split 3
$V_{GS} - V_{tlin}$ = 0-5 V
1 V steps
I_{DS} (μA/μm)
V_{DS} (V)
0
50
100
150
200
250
0
1
2
3
4
5

FIG. 1DA

FIG. 10B

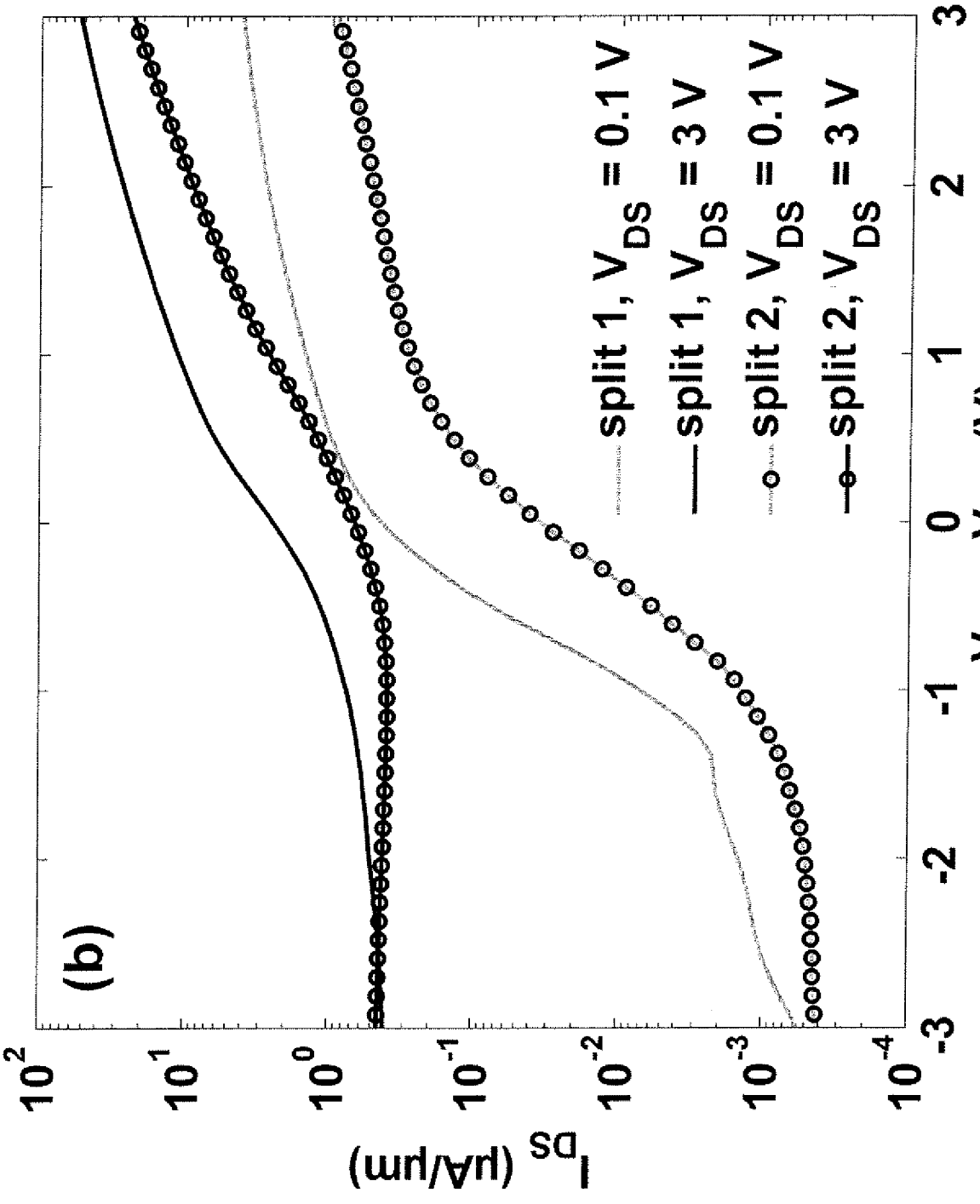

(b)
split 1, V_{DS} = 0.1 V
split 1, V_{DS} = 3 V
split 2, V_{DS} = 0.1 V
split 2, V_{DS} = 3 V
I_{DS} (μA/μm)
V_{GS} - V_{tlin} (V)
10^{2}
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
-3
-2
-1
0
1
2
3

FIG. 11A

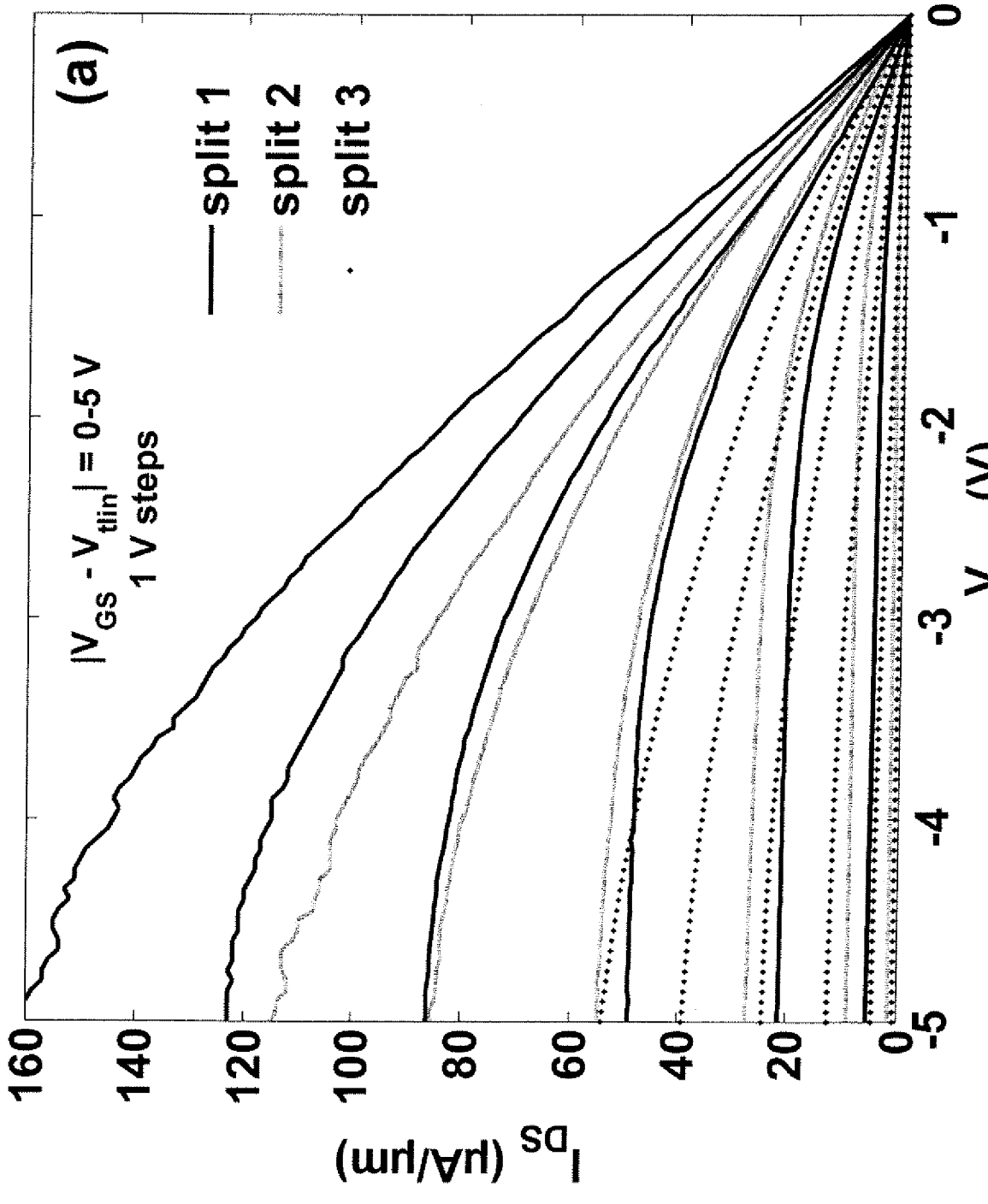

(a)
split 1
split 2
split 3
$|V_{GS} - V_{tlin}| = 0\text{-}5$ V
1 V steps
I_{DS} (μA/μm)
V_{DS} (V)
160
140
120
100
80
60
40
20
0
-5
-4
-3
-2
-1
0

FIG. 11B

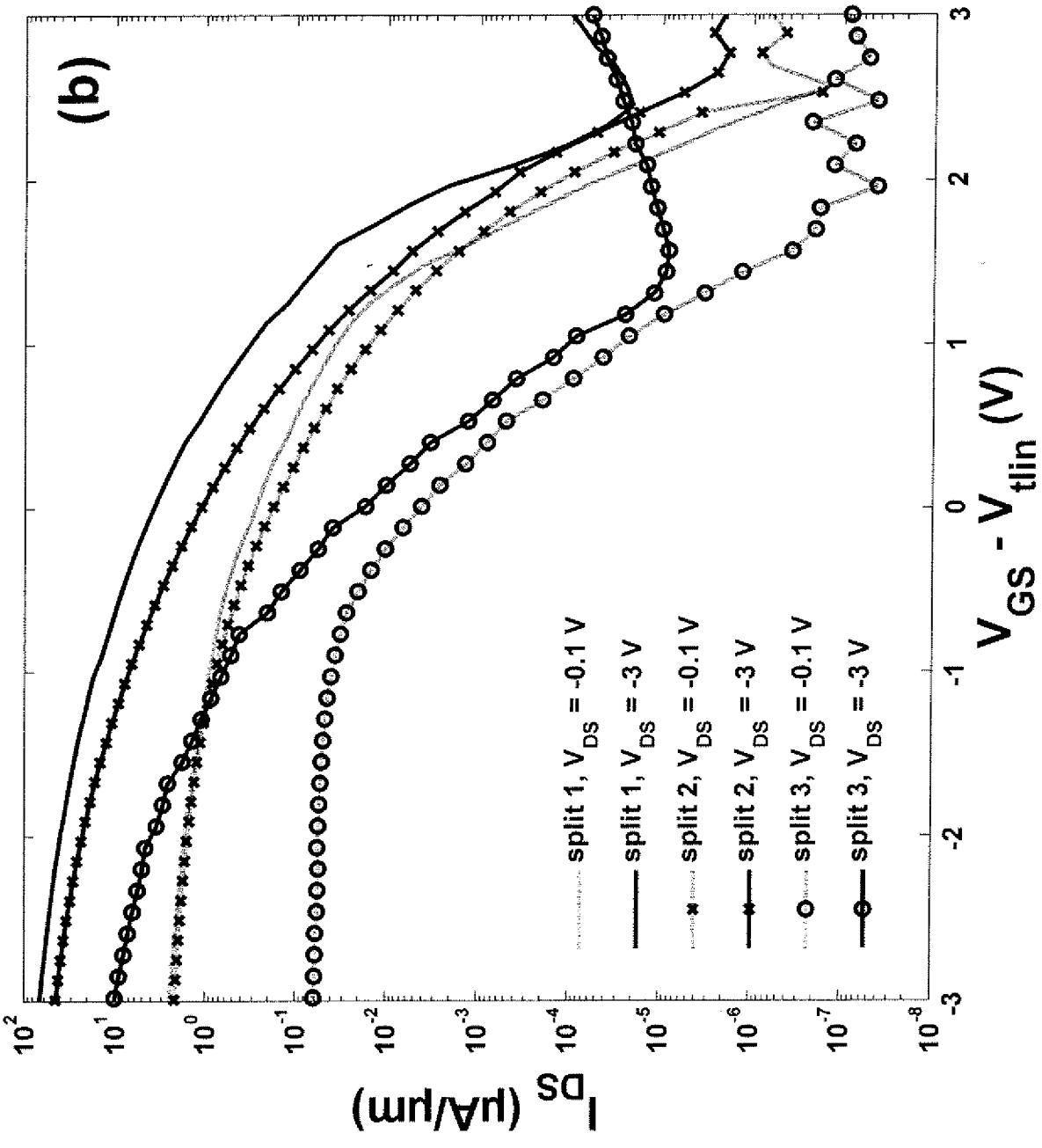
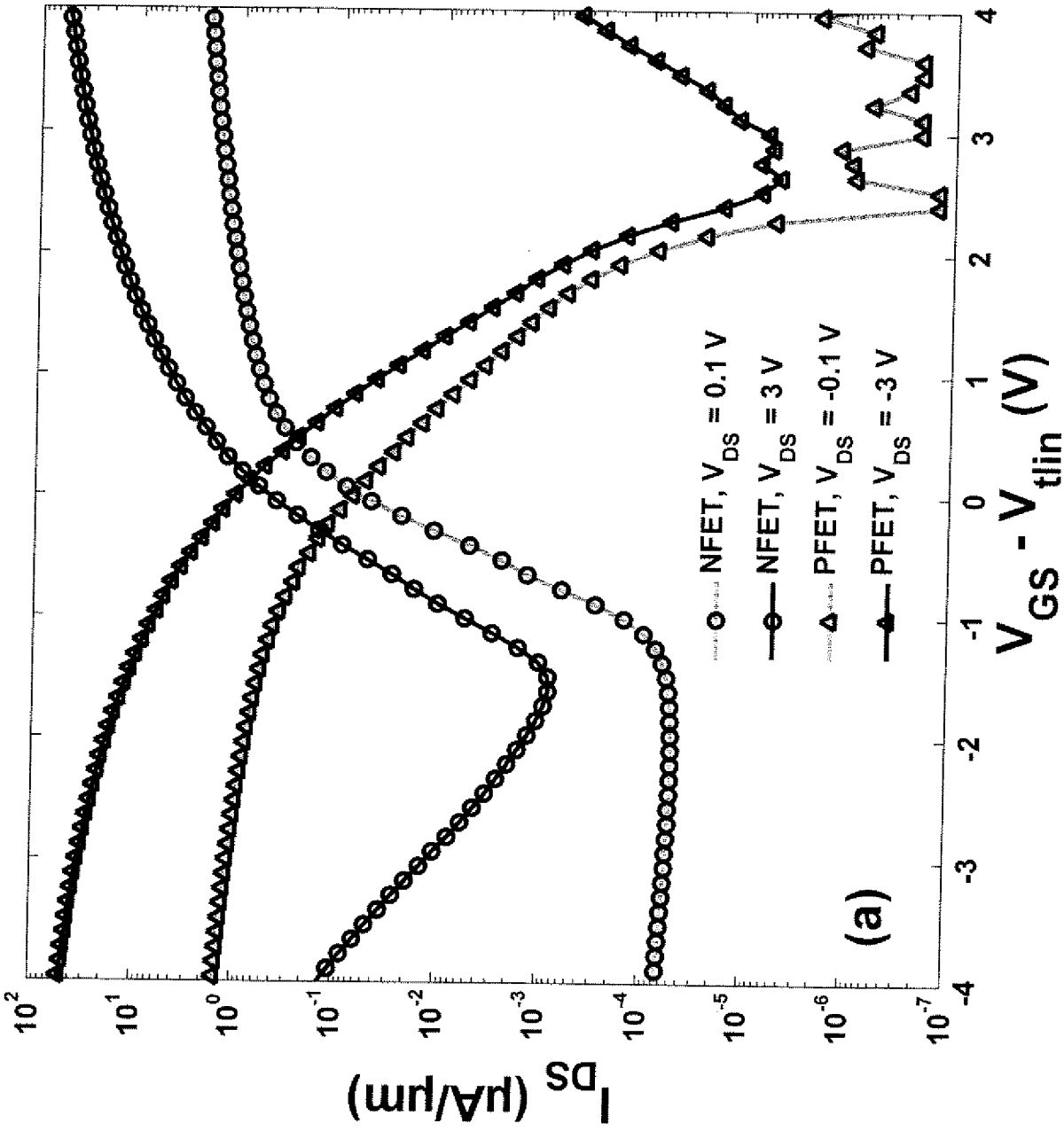

(b)
I_{DS} (μA/μm)
V_{GS} - V_{tlin} (V)
split 1, V_{DS} = -0.1 V
split 1, V_{DS} = -3 V
split 2, V_{DS} = -0.1 V
split 2, V_{DS} = -3 V
split 3, V_{DS} = -0.1 V
split 3, V_{DS} = -3 V

FIG. 12A


I_{DS} (μA/μm)
10^{2}
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
-4
-3
-2
-1
0
1
2
3
4
V_{GS} - V_{tlin} (V)
NFET, V_{DS} = 0.1 V
NFET, V_{DS} = 3 V
PFET, V_{DS} = -0.1 V
PFET, V_{DS} = -3 V
(a)

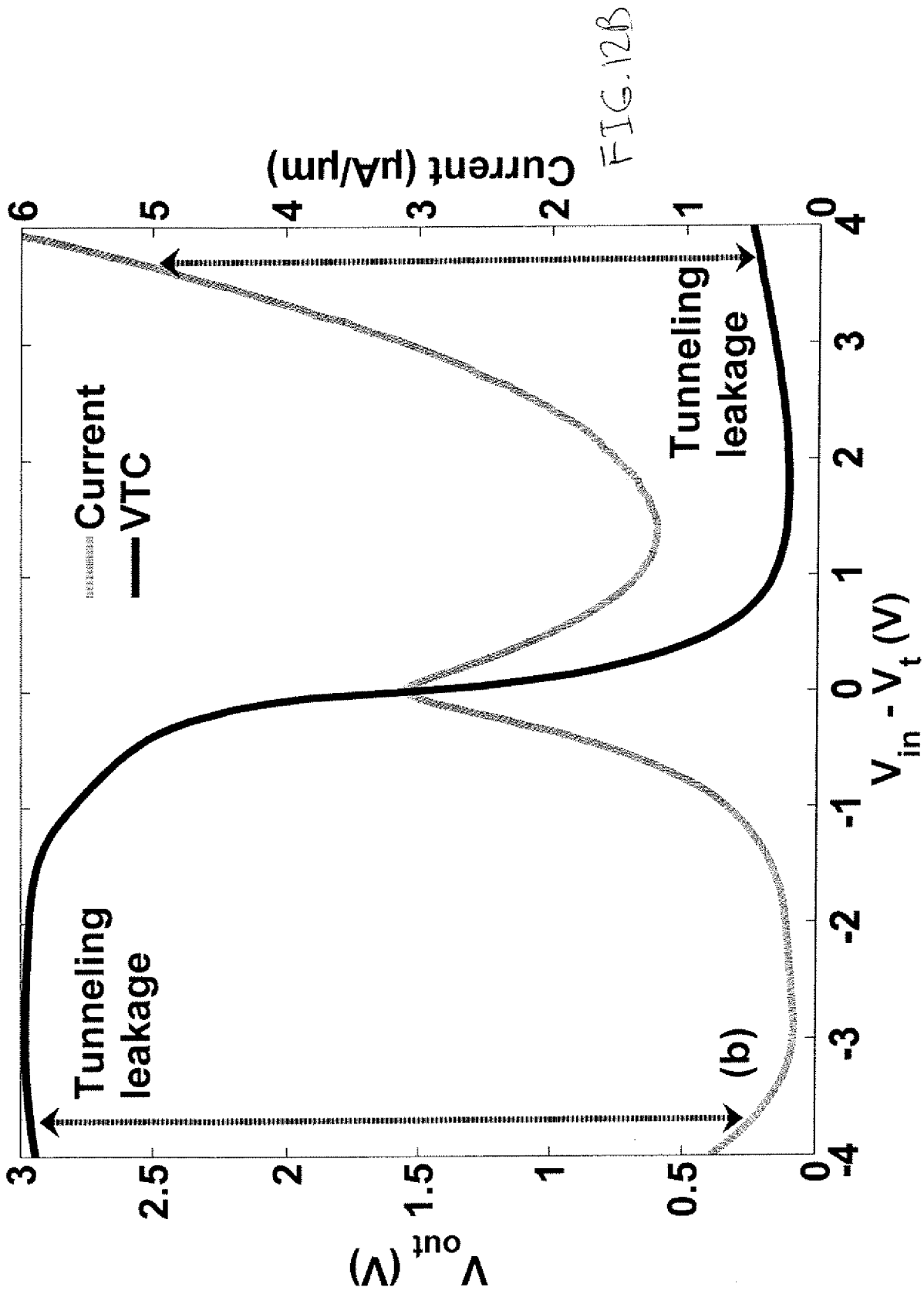

Current (μA/μm)
V_out (V)
V_in - V_t (V)
Current
VTC
Tunneling leakage
Tunneling leakage
(b)

FIG. 12B