



(51) International Patent Classification:

H02M 1/42 (2007.01) F04B 49/03 (2006.01)
H02P 27/08 (2006.01) H02M 1/00 (2007.01)

(21) International Application Number:

PCT/US2017/027710

(22) International Filing Date:

14 April 2017 (14.04.2017)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

| | | |
|------------|----------------------------|----|
| 62/323,532 | 15 April 2016 (15.04.2016) | US |
| 62/323,607 | 15 April 2016 (15.04.2016) | US |
| 62/323,563 | 15 April 2016 (15.04.2016) | US |
| 15/487,101 | 13 April 2017 (13.04.2017) | US |
| 15/487,027 | 13 April 2017 (13.04.2017) | US |

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

- with international search report (Art. 21(3))
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))

(54) Title: SWITCH ACTUATION MEASUREMENT CIRCUIT FOR VOLTAGE CONVERTER

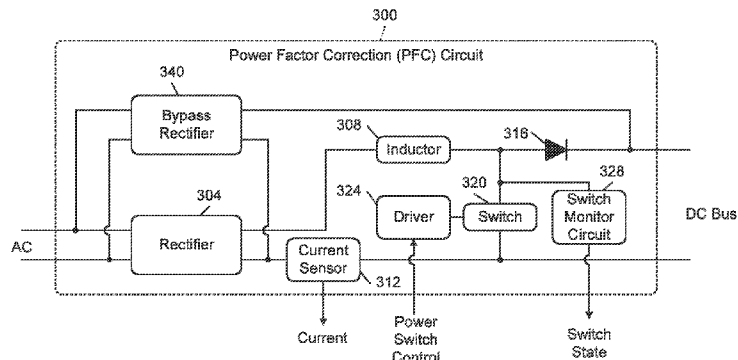


FIG. 3A

(57) Abstract: A drive includes an inverter power circuit that applies power to an electric motor of a compressor from a direct current (DC) voltage bus. A power factor correction (PFC) circuit outputs power to the DC voltage bus based on input alternating current (AC) power. The PFC circuit includes: (i) a switch having a first terminal, a second terminal, and a control terminal; (ii) a driver that switches the switch between open and closed states based on a control signal; (iii) an inductor that charges and discharges based on switching of the switch; and (iv) a circuit that outputs a signal indicating whether the switch is in the open state or the closed state based on a voltage across the first and second terminals of the switch.

WO 2017/181071 A1

SWITCH ACTUATION MEASUREMENT CIRCUIT FOR VOLTAGE CONVERTER

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a PCT International Application of U.S. Application No. 15/487,101, filed April 13, 2017, and U.S. Application No. 15/487,027, filed April 13, 2017. This application claims the benefit of the earlier filing date and right of priority to U.S. Provisional Application No. 62/323,563, filed on April 15, 2016, U.S. Provisional Application No. 62/323,532, filed on April 15, 2016, and U.S. Provisional Application No. 62/323,607, filed on April 15, 2016. The entire disclosures of the applications referenced above are incorporated herein by reference.

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FIELD

[0002] The present disclosure relates to a voltage converters and, more particularly, to circuits for measuring switching of a voltage converter.

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BACKGROUND

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[0003] The background description provided here is for the purpose of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent it is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present disclosure.

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[0004] Electric motors are used in a wide variety of industrial and residential applications including, but not limited to, heating, ventilating, and air conditioning (HVAC) systems. For example only, an electric motor may drive a compressor in an HVAC system. One or more additional electric motors may also be implemented in the HVAC system. For example only, the HVAC system may include another electric motor that drives a fan associated with a condenser. Another electric motor may be included in the HVAC system to drive a fan associated with an evaporator.

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SUMMARY

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[0005] In a feature, a drive is described. An inverter power circuit applies power to an electric motor of a compressor from a direct current (DC) voltage bus. A power factor correction (PFC) circuit outputs power to the DC voltage bus based on input alternating current (AC) power. The PFC circuit includes: (i) a switch having a first terminal, a second terminal, and a control

terminal; (ii) a driver that switches the switch between open and closed states based on a control signal; (iii) an inductor that charges and discharges based on switching of the switch; and (iv) a circuit that outputs a signal indicating whether the switch is in the open state or the closed state based on a voltage across the first and second terminals of the switch.

5 [0006] In further features, the drive further includes a control module that generates the control signal based on the signal indicating whether the switch is in the open state or the closed state.

[0007] In further features, the control module measures a period between: (i) a first time when the control signal transitions from a first state for transitioning the switch one of: (a) from the open state to the closed state; and (b) from the closed state to the open state; and (ii) a second time, after the first time, when the signal transitions from a first state to a second indicating that the one of: (a) the switch transitioned from the open state to the closed state; and (b) the switch transitioned from the closed state to the open state. The control module generates the control signal based on the period.

15 [0008] In further features, the circuit generates the signal indicating that the switch is in the closed state when the voltage across the first and second terminals of the switch is less than a predetermined voltage.

[0009] In further features, the circuit generates the signal indicating that the switch is in the open state when the voltage across the first and second terminals is greater than a predetermined voltage.

20 [0010] In further features, the second terminal of the switch is connected to a ground potential.

[0011] In further features, the circuit includes a node that is connected to a first voltage at the first terminal of the switch when the switch is in the closed state and that is connected to a second voltage when the switch is in the open state.

25 [0012] In further features, the circuit further includes: a first voltage divider that generates a third voltage based on a fourth voltage at the node; a second voltage divider that generates a fifth voltage based on a sixth voltage at the second terminal of the switch; and a comparator that generates the signal indicating whether the switch is in the open state or the closed state based on a comparison of the third voltage and the fifth voltage.

30 [0013] In further features, the comparator generates the signal indicating that the switch is in the open state when the third voltage is greater than the fifth voltage.

[0014] In further features, the comparator generates the signal indicating that the switch is in the closed state when the third voltage is less than the fifth voltage.

[0015] In a feature, a method includes: applying power to an electric motor of a compressor from a direct current (DC) voltage bus; and, by a power factor correction (PFC) circuit, providing power to the DC voltage bus based on input alternating current (AC) power, the providing power to the DC bus voltage including switching a switch of the PFC circuit between
5 open and closed states based on a control signal, wherein the switch includes a first terminal, a second terminal, and the control terminal. The method further includes outputting a signal indicating whether the switch is in the open state or the closed state based on a voltage across the first and second terminals of the switch.

[0016] In further features, the method further includes generating the control signal based on
10 the signal indicating whether the switch is in the open state or the closed state.

[0017] In further features, the method further includes measuring a period between: (i) a first time when the control signal transitions from a first state for transitioning the switch one of: (a) from the open state to the closed state; and (b) from the closed state to the open state; and (ii) a second time, after the first time, when the signal transitions from a first state to a second
15 indicating that the one of: (a) the switch transitioned from the open state to the closed state; and (b) the switch transitioned from the closed state to the open state. Generating the control signal includes generating the control signal based on the period.

[0018] In further features, outputting the signal indicating whether the switch is in the open state or the closed state includes generating the signal indicating that the switch is in the closed
20 state when the voltage across the first and second terminals of the switch is less than a predetermined voltage.

[0019] In further features, outputting the signal indicating whether the switch is in the open state or the closed state includes generating the signal indicating that the switch is in the open
25 state when the voltage across the first and second terminals is greater than a predetermined voltage.

[0020] In further features, the second terminal of the switch is connected to a ground potential.

[0021] In further features, the method further includes: connecting a node to a first voltage at the first terminal of the switch when the switch is in the closed state; and connecting the node to a second voltage when the switch is in the open state.

[0022] In further features, the method further includes: by a first voltage divider, generating a third voltage based on a fourth voltage at the node; and by a second voltage divider, generating a fifth voltage based on a sixth voltage at the second terminal of the switch. Outputting the signal indicating whether the switch is in the open state or the closed state includes outputting the

signal indicating whether the switch is in the open state or the closed state based on a comparison of the third voltage and the fifth voltage.

5 [0023] In further features, outputting the signal indicating whether the switch is in the open state or the closed state includes generating the signal indicating that the switch is in the open state when the third voltage is greater than the fifth voltage.

[0024] In further features, outputting the signal indicating whether the switch is in the open state or the closed state includes generating the signal indicating that the switch is in the closed state when the third voltage is less than the fifth voltage.

10 [0025] In a feature, a drive for an electric motor of a compressor is described. The drive includes: an inverter power circuit that applies power to an electric motor of a compressor from a direct current (DC) voltage bus; and a power factor correction (PFC) circuit that outputs power to the DC voltage bus based on input alternating current (AC) power. The PFC circuit includes: (i) a switch; (ii) a driver that connects a control terminal of the switch to a first reference potential when a control signal is in a first state and that connects the control terminal of the
15 switch to a second reference potential when the control signal is in a second state, wherein the first reference potential is one of greater than and less than the second reference potential, where the switch operates in an open state when the first reference potential is connected to the control terminal and operates in a closed state when the second reference potential is connected to the control terminal; and (iii) an inductor that charges and discharges based on switching of the
20 switch. The drive also includes a control module that generates the control signal based on a measured current through the inductor and a predetermined current through the inductor.

[0026] In further features, the control module transitions the control signal to the first state when the measured current through the inductor is greater than the predetermined current through the inductor.

25 [0027] In further features, the control module maintains the control signal in the first state for a predetermined period after transitioning the control signal to the first state.

[0028] In further features, the PFC circuit further includes a clamp switch that selectively connects the control terminal of the switch to the first reference potential.

30 [0029] In further features, the clamp switch connects the control terminal of the switch to the first reference potential when a second control signal is in a first state, where the control module sets the second control signal to the first state while the control signal is in the first state.

[0030] In further features, the clamp switch creates an open circuit between the control terminal of the switch and the first reference potential when the second control signal is in a second state.

5 [0031] In further features, the driver switches the switch between the open and closed states at a frequency of at least 50 Kilohertz (KHz).

[0032] In further features, the PFC circuit further includes a snubber circuit connected in parallel with the switch.

[0033] In further features, the PFC circuit further includes a damping circuit connected between the control terminal of the switch and the first reference potential.

10 [0034] In further features, the first reference potential is a ground potential.

[0035] In a feature, a method includes: by an inverter power circuit, applying power to an electric motor of a compressor from a direct current (DC) voltage bus; and, by a power factor correction (PFC) circuit, providing power to the DC voltage bus based on input alternating current (AC) power. The providing power includes: by a driver of the PFC circuit, connecting a control terminal of a switch of the PFC circuit to a first reference potential when a control signal is in a first state; and by the driver of the PFC circuit, connecting the control terminal of the switch of the PFC circuit to a second reference potential when the control signal is in a second state. The first reference potential is one of greater than and less than the second reference potential. The switch operates in an open state when the first reference potential is connected to the control terminal and operates in a closed state when the second reference potential is connected to the control terminal. An inductor of the PFC circuit charges and discharges based on switching of the switch. The method further includes generating the control signal based on a measured current through the inductor and a predetermined current through the inductor.

25 [0036] In further features, generating the control signal includes transitioning the control signal to the first state when the measured current through the inductor is greater than the predetermined current through the inductor.

[0037] In further features, generating the control signal further includes maintaining the control signal in the first state for a predetermined period after transitioning the control signal to the first state.

30 [0038] In further features, the method further includes selectively switching a clamp switch of the PFC circuit thereby selectively connecting the control terminal of the switch to the first reference potential.

[0039] In further features: selectively switching the clamp switch of the PFC circuit includes switching the clamp switch of the PFC circuit to connect the control terminal of the switch to the first reference potential when a second control signal is in a first state; and the method further includes setting the second control signal to the first state while the control signal is in the first state.

[0040] In further features, selectively switching the clamp switch of the PFC circuit thereby creating an open circuit between the control terminal of the switch and the first reference potential when the second control signal is in a second state.

[0041] In further features, generating the control signal includes transitioning the control signal between the first and second states at a frequency of at least 50 KiloHertz (KHz).

[0042] In further features, the first reference potential is a ground potential.

[0043] In further features, the first reference potential is a negative potential.

[0044] In further features, the second reference potential is a positive potential.

[0045] Further areas of applicability of the present disclosure will become apparent from the detailed description, the claims and the drawings. The detailed description and specific examples are intended for purposes of illustration only and are not intended to limit the scope of the disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0046] The present disclosure will become more fully understood from the detailed description and the accompanying drawings, wherein:

[0047] FIG. 1 is a functional block diagram of an example refrigeration system;

[0048] FIG. 2 is a block diagram of an example implementation of the compressor motor drive of FIG. 1;

[0049] FIG. 3A is a block diagram of an example implementation of the power factor correction (PFC) circuit of FIG. 2;

[0050] FIG. 3B is a block diagram of another example implementation of the PFC circuit of FIG. 2;

[0051] FIG. 4 is a functional block diagram of an example implementation of the gate driver of the PFC circuit of FIG. 2;

- [0052] FIGs. 5A and 5B are circuit diagrams of example implementations of the gate driver of the PFC circuit of FIG. 2;
- [0053] FIG. 6 is a functional block diagram of an example implementation of the switch monitor circuit of the power factor correction circuit;
- 5 [0054] FIG. 7 is a circuit diagram of an example implementation of the switch monitor circuit of the power factor correction circuit;
- [0055] FIG. 8 is a functional block diagram of an example implementation of the control module;
- [0056] FIG. 9 is a functional block diagram of an example implementation of a current control
10 module of the control module;
- [0057] FIG. 10 is a flowchart depicting an example method of controlling switching of the switch of the power factor correction circuit; and
- [0058] FIG. 11 is a flowchart depicting an example method of determining turn ON and turn OFF delays of the switch of the power factor correction circuit.
- 15 [0059] In the drawings, reference numbers may be reused to identify similar and/or identical elements.

DETAILED DESCRIPTION

REFRIGERATION SYSTEM

- [0060] FIG. 1 is a functional block diagram of an example refrigeration system 100 including a
20 compressor 102, a condenser 104, an expansion valve 106, and an evaporator 108. According to the principles of the present disclosure, the refrigeration system 100 may include additional and/or alternative components, such as a reversing valve or a filter-drier. In addition, the present disclosure is applicable to other types of refrigeration systems including, but not limited to, heating, ventilating, and air conditioning (HVAC), heat pump, refrigeration, and chiller systems.
- 25 [0061] The compressor 102 receives refrigerant in vapor form and compresses the refrigerant. The compressor 102 provides pressurized refrigerant in vapor form to the condenser 104. The compressor 102 includes an electric motor that drives a pump. For example only, the pump of the compressor 102 may include a scroll compressor and/or a reciprocating compressor.
- [0062] All or a portion of the pressurized refrigerant is converted into liquid form within the
30 condenser 104. The condenser 104 transfers heat away from the refrigerant, thereby cooling the refrigerant. When the refrigerant vapor is cooled to a temperature that is less than a saturation

temperature, the refrigerant transforms into a liquid (or liquefied) refrigerant. The condenser 104 may include an electric fan that increases the rate of heat transfer away from the refrigerant.

[0063] The condenser 104 provides the refrigerant to the evaporator 108 via the expansion valve 106. The expansion valve 106 controls the flow rate at which the refrigerant is supplied to the evaporator 108. The expansion valve 106 may include a thermostatic expansion valve or may be controlled electronically by, for example, a system controller 130. A pressure drop caused by the expansion valve 106 may cause a portion of the liquefied refrigerant to transform back into the vapor form. In this manner, the evaporator 108 may receive a mixture of refrigerant vapor and liquefied refrigerant.

[0064] The refrigerant absorbs heat in the evaporator 108. Liquid refrigerant transitions into vapor form when warmed to a temperature that is greater than the saturation temperature of the refrigerant. The evaporator 108 may include an electric fan that increases the rate of heat transfer to the refrigerant.

[0065] A utility 120 provides power to the refrigeration system 100. For example only, the utility 120 may provide single-phase alternating current (AC) power at approximately 230 Volts root mean squared (V_{RMS}). In other implementations, the utility 120 may provide three-phase AC power at approximately 400 V_{RMS} , 480 V_{RMS} , or 600 V_{RMS} at a line frequency of, for example, 50 or 60 Hz. When the three-phase AC power is nominally 600 V_{RMS} , the actual available voltage of the power may be 575 V_{RMS} .

[0066] The utility 120 may provide the AC power to the system controller 130 via an AC line, which includes two or more conductors. The AC power may also be provided to a drive 132 via the AC line. The system controller 130 controls the refrigeration system 100. For example only, the system controller 130 may control the refrigeration system 100 based on user inputs and/or parameters measured by various sensors (not shown). The sensors may include pressure sensors, temperature sensors, current sensors, voltage sensors, etc. The sensors may also include feedback information from the drive control, such as motor currents or torque, over a serial data bus or other suitable data buses.

[0067] A user interface 134 provides user inputs to the system controller 130. The user interface 134 may additionally or alternatively provide the user inputs directly to the drive 132. The user inputs may include, for example, a desired temperature, requests regarding operation of a fan (e.g., a request for continuous operation of the evaporator fan), and/or other suitable inputs. The user interface 134 may take the form of a thermostat, and some or all functions of the

system controller (including, for example, actuating a heat source) may be incorporated into the thermostat.

5 [0068] The system controller 130 may control operation of the fan of the condenser 104, the fan of the evaporator 108, and the expansion valve 106. The drive 132 may control the compressor 102 based on commands from the system controller 130. For example only, the system controller 130 may instruct the drive 132 to operate the motor of the compressor 102 at a certain speed or to operate the compressor 102 at a certain capacity. In various implementations, the drive 132 may also control the condenser fan.

10 [0069] A thermistor 140 is thermally coupled to the refrigerant line exiting the compressor 102 that conveys refrigerant vapor to the condenser 104. The variable resistance of the thermistor 140 therefore varies with the discharge line temperature (DLT) of the compressor 102. As described in more detail, the drive 132 monitors the resistance of the thermistor 140 to determine the temperature of the refrigerant exiting the compressor 102.

15 [0070] The DLT may be used to control the compressor 102, such as by varying capacity of the compressor 102, and may also be used to detect a fault. For example, if the DLT exceeds the threshold, the drive 132 may power down the compressor 102 to prevent damage to the compressor 102.

DRIVE

20 [0071] In FIG. 2, an example implementation of the drive 132 includes an electromagnetic interference (EMI) filter and protection circuit 204, which receives power from an AC line. The EMI filter and protection circuit 204 reduces EMI that might otherwise be injected back onto the AC line from the drive 132. The EMI filter and protection circuit 204 may also remove or reduce EMI arriving from the AC line. Further, the EMI filter and protection circuit 204 protects against power surges, such as may be caused by lightning, and/or other other types of power surges and sags.

25 [0072] A charging circuit 208 controls power supplied from the EMI filter and protection circuit 204 to a power factor correction (PFC) circuit 212. For example, when the drive 132 initially powers up, the charging circuit 208 may place a resistance in series between the EMI filter and protection circuit 204 and the PFC circuit 212 to reduce the amount of current inrush. 30 These current or power spikes may cause various components to prematurely fail.

[0073] After initial charging is completed, the charging circuit 208 may close a relay that bypasses the current-limiting resistor. For example, a control module 220 may provide a relay

control signal to the relay within the charging circuit 208. In various implementations, the control module 220 may assert the relay control signal to bypass the current-limiting resistor after a predetermined period of time following start up, or based on closed loop feedback indicating that charging is near completion.

5 [0074] The PFC circuit 212 converts incoming AC power to DC power. The PFC circuit 212 may not be limited to PFC functionality — for example, the PFC circuit 212 may also perform voltage conversion functions, such as acting as a boost circuit and/or a buck circuit. In some implementations, the PFC circuit 212 may be replaced by a non-PFC voltage converter. The DC power may have voltage ripples, which are reduced by filter capacitance 224. Filter
10 capacitance 224 may include one or more capacitors arranged in parallel and connected to the DC bus. The PFC circuit 212 may attempt to draw current from the AC line in a sinusoidal pattern that matches the sinusoidal pattern of the incoming voltage. As the sinusoids align, the power factor approaches one, which represents the greatest efficiency and the least demanding load on the AC line.

15 [0075] The PFC circuit 212 includes one or more switches that are controlled by the control module 220 using one or more signals labeled as power switch control. The control module 220 determines the power switch control signals based on a measured voltage of the DC bus, measured current in the PFC circuit 212, AC line voltages, temperature or temperatures of the PFC circuit 212, and the measured state of a power switch in the PFC circuit 212. While the
20 example of use of measured values is provided, the control module 220 may determine the power switch control signals based on an estimated voltage of the DC bus, estimated current in the PFC circuit 212, estimated AC line voltages, estimated temperature or temperatures of the PFC circuit 212, and/or the estimated or expected state of a power switch in the PFC circuit 212. In various implementations, the AC line voltages are measured or estimated subsequent to the
25 EMI filter and protection circuit 204 but prior to the charging circuit 208.

[0076] The control module 220 is powered by a DC–DC power supply 228, which provides a voltage suitable for logic of the control module 220, such as 3.3 Volts, 2.5 Volts, etc. The DC–DC power supply 228 may also provide DC power for operating switches of the PFC circuit 212 and an inverter power circuit 232. For example only, this voltage may be a higher voltage than
30 for digital logic, with 15 Volts being one example.

[0077] The inverter power circuit 232 also receives power switch control signals from the control module 220. In response to the power switch control signals, switches within the inverter power circuit 232 cause current to flow in respective windings of a motor 236 of the compressor 102. The control module 220 may receive a measurement or estimate of motor

current for each winding of the motor 236 or each leg of the inverter power circuit 232. The control module 220 may also receive a temperature indication from the inverter power circuit 232.

[0078] For example only, the temperature received from the inverter power circuit 232 and the temperature received from the PFC circuit 212 are used only for fault purposes. In other words, once the temperature exceeds a predetermined threshold, a fault is declared and the drive 132 is either powered down or operated at a reduced capacity. For example, the drive 132 may be operated at a reduced capacity and if the temperature does not decrease at a predetermined rate, the drive 132 transitions to a shutdown state.

[0079] The control module 220 may also receive an indication of the discharge line temperature from the compressor 102 using the thermistor 140. An isolation circuit 260 may provide a pulse-width-modulated representation of the resistance of the thermistor 140 to the control module 220. The isolation circuit 260 may include galvanic isolation so that there is no electrical connection between the thermistor 140 and the control module 220.

[0080] The isolation circuit 260 may further receive protection inputs indicating faults, such as a high-pressure cutoff or a low-pressure cutoff, where pressure refers to refrigerant pressure. If any of the protection inputs indicate a fault and, in some implementations, if any of the protection inputs become disconnected from the isolation circuit 260, the isolation circuit 260 ceases sending the PWM temperature signal to the control module 220. Therefore, the control module 220 may infer that a protection input has been received from an absence of the PWM signal. The control module 220 may, in response, shut down the drive 132.

[0081] The control module 220 controls an integrated display 264, which may include a grid of LEDs and/or a single LED package, which may be a tri-color LED. The control module 220 can provide status information, such as firmware versions, as well as error information using the integrated display 264. The control module 220 communicates with external devices, such as the system controller 130 in FIG. 1, using a communications transceiver 268. For example only, the communications transceiver 268 may conform to the RS-485 or RS-232 serial bus standards or to the Controller Area Network (CAN) bus standard.

PFC CIRCUITS

[0082] In FIG. 3A, a PFC circuit 300 is one implementation of the PFC circuit 212 of FIG. 2. The PFC circuit 300 includes a rectifier 304 that converts incoming AC into pulsating DC. In various implementations, the rectifier 304 includes a full-wave diode bridge. The DC output of the rectifier 304 is across first and second terminals. The first terminal is connected to an

inductor 308, while the second terminal is connected to a current sensor 312. An opposite end of the inductor 308 is connected to a node that is common to the inductor 308, an anode of a diode 316, and a first terminal of a switch 320.

[0083] The PFC circuit 300 generates a DC bus, where a first terminal of the DC bus is connected to a cathode of the diode 316 while a second terminal of the DC bus is connected to the second output terminal of the rectifier 304 via the current sensor 312. The current sensor 312 can, therefore, sense the current within the switch 320 as well as the current in the DC bus and current in the inductor 308. The second terminal of the DC bus is also connected to a second terminal of the switch 320.

[0084] A driver 324 receives the power switch control signal from the control module 220 of FIG. 2 and rapidly charges or discharges a control terminal of the switch 320. For example, the switch 320 may be a field effect transistor with a gate terminal as the control terminal. More specifically, the switch 320 may be a power metal-oxide-semiconductor field-effect transistor (MOSFET), such as the STW38N65M5 power MOSFET from STMicroelectronics. The driver 324, in response to the power switch control signal, charges or discharges the capacitance at the gate of the field effect transistor.

[0085] A switch monitor circuit 328 measures whether the switch is on or off. This closed loop control enables the control module 220 to determine whether the switch 320 has reacted to a command provided by the power switch control signal and may also be used to determine how long it takes the switch 320 to respond to that control signal. The measured switch state is output from the switch monitor circuit 328 back to the control module 220. The control module 220 may update its control of the power switch control signal to compensate for delays in turning on and/or turning off the switch 320.

[0086] In FIG. 3A, the inductor, the switch 320, and the diode 316 are arranged in a boost configuration. In brief, the switch 320 closes, causing current through the inductor 308 to increase. Then the switch 320 is opened, but the current through the inductor 308 cannot change instantaneously because the voltage across an inductor is proportional to the derivative of the current. The voltage across the inductor 308 becomes negative, meaning that the end of the inductor 308 connected to the anode of the diode 316 experiences a voltage increase above the voltage output from the rectifier 304.

[0087] Once the voltage at the anode of the diode 316 increases above the turn-on voltage of the diode 316, the current through the inductor 308 can be fed through the diode 316 to the DC

bus. The current through the inductor 308 decreases and then the switch 320 is closed once more, causing the current and the inductor 308 to increase.

[0088] In various implementations, the switch 320 may be turned on until the current sensor 312 determines that a predetermined threshold of current has been exceeded. At that time, the switch 320 is turned off for a specified period of time. This specified period may be adaptive, changing along with the voltage of the DC bus as well as the voltage of the AC input change. However, the off time (when the switch 320 is open) is a specified value. Once a time equal to the specified value has elapsed, the switch 320 is turned back on again and the process repeats. The off time can be fixed or variable. In the case of the off time being variable, the off time can be limited to at least a predetermined minimum off time.

[0089] To reduce the physical size and parts cost of the PFC circuit 300, the inductance of the inductor 308 (which may be the largest contributor to the physical size of the PFC circuit 300) may be lowered. However, with a lower inductance, the inductor 308 will saturate more quickly. Therefore, the switch 320 will have to operate more quickly. While more quickly and smaller are relative terms, present power switching control operates in the range of 10 kilohertz to 20 kilohertz switching frequencies. In the present application, the switching frequency of the switch 320 may be increased to more than 50 kilohertz, more than 100 kilohertz, or more than 200 kilohertz. For example, the switching frequency of the switch may be controlled to be approximately 200 kilohertz.

[0090] The switch 320 is therefore chosen to allow for faster switching as well as to have low switching losses. With faster switching, the inductance of the inductor 308 can be smaller. In addition, the diode 316 may need to be faster. Silicon carbide diodes may have fast response times. For example, the diode 316 may be an STPSC2006CW Silicon Carbide dual diode package from STMicroelectronics.

[0091] In order to accurately drive the switch 320 when operating at higher speeds, the control strategy must similarly be accelerated. For example only, the control module 220 may include multiple devices, such as a microcontroller configured to perform more involved calculations and an FPGA (field programmable gate array) or PLD (programmable logic device) configured to monitor and respond to inputs in near real time. In this context, near real time means that the time resolution of measurement and time delay in responding to inputs of the FPGA or PLD is negligible compared to the physical time scale of interest. For faster switching speeds, the near real time response of the FPGA/PLD may introduce non-negligible delays. In such cases, the delay of the FPGA/PLD and driving circuitry may be measured and compensated for. For

example, if the turn-off of a switch occurs later than needed because of a delay, the turn-off can be instructed earlier to compensate for the delay.

5 [0092] A bypass rectifier 340 is connected in parallel with the rectifier 304 at the AC line input. A second output terminal of the bypass rectifier 340 is connected to the second terminal rectifier 304. However, a first output terminal of the bypass rectifier 340 is connected to the cathode of the diode 316.

10 [0093] As a result, when the PFC circuit 300 is not operating to boost the DC bus voltage, the bypass rectifier 340 will be active when the line-to-line voltage of the AC input exceeds the voltage across the DC bus. The bypass rectifier 340, in these situations, diverts current from passing through the diode 316. Because the inductor 308 is small, and the switch 320 switches rapidly, the diode 316 is also selected to exhibit fast switching times. The diode 316 may, therefore, be less tolerant to high currents, and so current is selectively shunted around the diode 316 by the bypass rectifier 340.

15 [0094] In addition, the current path through the rectifier 304 and the diode 316 experiences three diode voltage drops or two diode voltage drops and the switch voltage drop, while the path through the bypass rectifier 340 experiences only two diode voltage drops. While the single phase AC input in FIG. 3A is associated with a boost converter topology, the present disclosure also encompasses a buck converter topology or a buck-boost converter topology.

20 [0095] In FIG. 3B, a buck converter topology is shown with a three-phase AC input signal. Note that the principles of the present disclosure also apply to a boost converter or buck-boost converter topology used with a three-phase AC input. A PFC circuit 350 represents another implementation of the PFC circuit 212 of FIG. 2.

25 [0096] A three-phase rectifier 354 receives three-phase AC and generates pulsating DC across first and second terminals. A switch 358 is connected between the first terminal of the three-phase rectifier 354 and a common node. The common node is connected to an inductor 366 and a cathode of a power diode 370.

30 [0097] An anode of the power diode 370 is connected to a second terminal of the three-phase rectifier 354. An opposite terminal of the inductor 366 establishes one terminal of the DC bus, while the second output of the three-phase rectifier 354 establishes the other terminal of the DC bus. In the configuration shown in FIG. 3B, the switch 358, the inductor 366, and the diode 370 are configured in a buck topology.

[0098] A current sensor 362 is connected in series between the anode of the diode 370 and the DC bus. In other implementations, the current sensor 362 may be located in series with the

inductor 366. In other implementations, the current sensor 362 may be located in series with the switch 358. In other implementations, the current sensor 362 may be located in series between the anode of the diode 370 and the second output of the three-phase rectifier 354. The current sensor 362 measures current through the inductor 366 as well as current through the DC bus and provides a current signal indicative of the amount of the current.

[0099] A driver 374 drives a control terminal of the switch 358 based on a power switch control signal from the control module 220 in FIG. 2. A switch monitor circuit 378 detects whether the switch 358 has opened or closed and reports the switch state to the control module 220. With the location of the current sensor 362, the current sensor 362 will measure approximately zero current when the switch 358 is open. The switch monitoring circuits 328 and 378 provide accurate information regarding timing of the actual switching and protect the switches (320 and 358) from possible damage, such as from too high of current and/or sustained oscillation between open and closed states.

[0100] The driver 324 is a high frequency switching driver that operates the switch 320 to control charging and discharging of the inductor 308. Based on signals from the control module 220, the driver 324 alternately controls the switch 320 between a closed state and an open state. The inductor 308 charges when the switch 320 is in the closed state, and the inductor 308 discharges when the switch 320 is in the open state. While the example of the gate driver is shown and will be discussed, the following may also be applicable to drivers of other types of switches including switches that have a gate terminal and switches that do not have a gate terminal.

[0101] As discussed further below, the control module 220 generates the signals to maintain the switch 320 in the closed state until the current through the inductor 308 becomes greater than a predetermined current, such as a demanded current through the inductor 308. When the current through the inductor 308 becomes greater than the predetermined current, the control module 220 generates the signals to transition the switch 320 to the open state. The control module 220 then generates the signals to maintain the switch 320 in the open state for a predetermined period, such as a desired OFF period of the switch, before generating the signals to transition the switch 320 to the closed state.

[0102] Generally speaking, the components of the PFC circuit 212 (e.g., the driver 324 or 374, the switch control circuit, the clamp circuit, the damping circuit, and the one or more ferrite beads) are selected and designed to minimize turn ON and turn OFF delays of the switch (e.g., the switch 320 or 358) and minimize unintended oscillation of the switch between the open and closed states.

[0103] With reference to FIG. 4, an example implementation of the driver 324 and the switch 320 is presented. The switch 320 can be switched between the open and closed states at greater than a predetermined frequency. This enables the inductor 308 to be smaller and less costly than if the switch 320 could only be switched at lower frequencies. An example of the switch 320 is
5 switch part number STW38N65M5 MOSFET or a variant thereof, manufactured by STMicroelectronics. The predetermined frequency may be 50 Kilohertz (KHz), greater than 50 KHz, greater than 75 KHz, greater than 100 KHz, greater than 125 KHz, greater than 150 KHz, greater than 175 KHz, or greater than 200 KHz.

[0104] The driver 324 includes a switch control circuit 402, a clamp circuit 404, and a
10 damping circuit 406. The switch control circuit 402 selectively transitions the switch 320 between the open and closed states based on or at the predetermined frequency, based on or to maintain inductor current at a predetermined maximum current, or based on or to maintain inductor current within a predetermined current range. In the example of transitioning the switch
15 320 between the open and closed states based on or at the predetermined frequency, an average or instantaneous frequency of transitioning the switch 320 between the open and closed states may be controlled based on or at the predetermined frequency. For example, the switch control circuit 402 may control switching of the switch 320 using peak mode control with a variable desired OFF period, such as described in commonly assigned U.S. App. No. 15/419,423, filed on January 30, 2017, titled "Switch Off Time Control Systems And Methods" which claims the
20 benefit of U.S. Prov. App. No. 62/323,538, filed on April 15, 2016, the disclosures of which are incorporated in their entireties. The damping circuit 406 may also include a series element, such as a gate resistor and/or a ferrite bead, such as shown in the examples of FIGs. 5A and 5B.

[0105] The clamp circuit 404 is a protection circuit that couples a control terminal of the switch 320 to ground when the switch 320 is to be in the open state. The damping circuit 406 is
25 provided to minimize or prevent oscillation of the switch 320 between the open state and the closed state. The clamp circuit 404 and/or the damping circuit 406 may be omitted in various implementations.

[0106] The switch control circuit 402 and the clamp circuit 404 control the switch 320 based on the signals from the control module 220. The signals from the control module 220 may
30 include a switch control signal 408 that is provided to the switch control circuit 402 and a clamp control signal 410 that is provided to the clamp circuit 404. The switch control signal 408 and the clamp control signal 410 may be, for example, pulse width modulation (PWM) signals. As discussed above, the switch control signal 408 and/or the clamp control signal 410 may be set based on peak mode control where the switching frequency may vary.

[0107] The switch control circuit 402 may include a filter 412, a driver 414, and an amplifier 416. The filter 412 filters the switch control signal 408 to remove noise from the switch control signal 408. The driver 414 generates a control signal according to the switch control signal 408. The amplifier 416 amplifies the control signal and applies a resulting voltage (via a low impedance) to the control terminal of the switch 320 via line 418. In various implementations, the amplifier 416 may be omitted.

[0108] The control module 220 may set the switch control signal 408 to a first state (e.g., 1) to operate the switch 320 in the closed state. The control module 220 may set the switch control signal 408 to a second state (e.g., 0) to operate the switch 320 in the open state. Based on the switch control signal 408 being in the first state, the amplifier 416 applies a voltage (e.g., 15 V) to the control terminal of the switch 320 to operate the switch 320 in the closed state. Based on the switch control signal 408 being in the second state, the amplifier 416 connects the control terminal of the switch 320 to ground to operate the switch 320 in the open state.

[0109] The clamp circuit 404 includes a filter 420 and a driver 422. The filter 420 filters the clamp control signal 410 to remove noise from the clamp control signal 410. According to the clamp control signal 410, the driver 422 controls the state of a clamp switch 424. The clamp switch 424 is coupled between the control terminal of the switch 320 and ground.

[0110] The control module 220 may set the clamp control signal 410 to a first state (e.g., 1) to operate the clamp switch 424 in the open state. The control module 220 may set the clamp control signal 410 to a second state (e.g., 0) to operate the clamp switch 424 in the closed state. Based on the clamp control signal 410 being in the first state, the driver 422 operates the clamp switch 424 in the open state. Based on the clamp control signal 410 being in the second state, the driver 422 operates the clamp switch 424 in the closed state. When the clamp switch 424 is in the closed state, the clamp switch 424 connects the control terminal of the switch 320 to ground.

[0111] The clamp switch 424 acts as a secondary control to place the switch 320 in the open state. Generally speaking, the control module 220 generates the switch control signal 408 and the clamp control signal 410 such that the switch 320 and the clamp switch 424 are in opposite states.

[0112] For example, at some times, the control module 220 may set the switch control signal 408 to the first state and the clamp control signal 410 to the first state. In this situation, the amplifier 416 connects the control terminal of the switch 320 to voltage such that the switch 320 is in the closed state, and the clamp switch 424 serves as an open circuit between the control terminal of the switch 320 and ground.

[0113] At other times, the control module 220 may set the switch control signal 408 to the second state and the clamp control signal 410 to the second state. In this situation, the amplifier 416 connects the control terminal of the switch 320 to ground such that the switch 320 is in the open state. The clamp switch 424 also connects the control terminal of the switch 320 to ground to help ensure that the switch 320 is in the open state and/or to help transition the switch 320 to the open state faster.

[0114] As stated above, the control module 220 generally generates the switch control signal 408 and the clamp control signal 410 such that the switch 320 and the clamp switch 424 are in opposite states. However, the control module 220 may generate the switch control signal 408 and the clamp control signal 410 to provide dead time during which both the clamp switch 424 and the switch 320 are in the open state at the same time before one of the clamp switch 424 and the switch 320 is transitioned to the closed state.

[0115] For example, the control module 220 may transition the switch control signal 408 to the first state a predetermined period after transitioning the clamp control signal 410 to the first state. The control module 220 may also transition the switch control signal 408 to the second state a predetermined period before transitioning the clamp control signal 410 to the second state. As such, both the switch 320 and the clamp switch 424 will be in the open state for some period before one of the switch 320 and the clamp switch 424 is transitioned to the closed state. This prevents the possibility of both the clamp switch 424 and the switch 320 being in the closed state at the same time.

[0116] FIG. 5A illustrates an example implementation of the driver 324. As an example, the switch 320 may be an n-type metal–oxide–semiconductor field-effect transistor (MOSFET) 502. A snubber circuit 504 may be connected in parallel with the MOSFET 502. The snubber circuit 504 suppresses rapid rises in voltage across the MOSFET 502 as the MOSFET 502 is being switched between the open and closed states.

[0117] The gate terminal (i.e., control terminal) of the MOSFET 502 is coupled to the driver 324. The MOSFET 502 should be in the closed state when the voltage is applied to the gate terminal of the MOSFET 502. The MOSFET 502 should be in the open state when the gate terminal of the MOSFET 502 is connected to ground.

[0118] The driver 320 may include a dual driver module 506 that includes two drivers that operate as the driver 414 for the switch control circuit 402 and the driver 422 for the clamp circuit 404. The dual driver module 506 includes terminals PWM_1, PWM_2, OUT_1, and OUT_2. The PWM_1 terminal receives the switch control signal 408, which is labeled as

“PFC_OUT” in the example of FIG. 5. The PWM_2 terminal receives the clamp control signal 410, which is labeled as “PFC_CLAMP” in the example of FIG. 5.

5 [0119] The PWM_1 and the PWM_2 terminals may be coupled to RC filters to filter noise provided in the switch control signal 408 and clamp control signal 410, respectively. For example, the PWM_1 terminal is coupled to resistors R161 and R164 and capacitor C92, which form an example of the filter 412 of FIG. 4. The PWM_2 terminal is coupled to resistors R158 and R163 and capacitor C93, which form an example of the filter 420 of FIG. 4.

10 [0120] The dual driver module 506 also includes a first enable input terminal, labeled EN_1, and a second enable input terminal, labeled EN_2. When a signal received at the first enable input terminal is in a first state, the dual driver module 506 may maintain the switch 320 in the open state, regardless of the switch control signal 408. When the signal at the first enable input is in a second state, the switch 320 may be switched between the open and closed states based on the state of the switch control signal 408. When a signal received at the second enable input terminal is in a first state, the clamp switch 424 may be maintained in the open state. When the
15 signal at the second enable input is in a second state, the clamp switch 424 may be switched between the open and closed states based on the state of the clamp control signal 410. In various implementations, the signal applied to the second enable input terminal may be maintained in the second state to allow switching of the clamp switch 424.

20 [0121] Push-pull amplifier 508 is an example of the amplifier 416. The dual driver module 506 controls a signal applied to the push-pull amplifier 508 based on the state of the switch control signal 408. The push-pull amplifier 508 may include an NPN-bipolar junction transistor (BJT) 510 and a PNP-BJT 512 configured as emitter followers. While the example of BJTs is provided, another suitable type of switch may be used. Additionally, other configurations are possible with different configurations of P and N type switches.

25 [0122] The push-pull amplifier 508 is coupled to the gate terminal of the MOSFET 502 via the line 418 and connects the gate terminal of the MOSFET 502 to voltage or ground based on the signal from the dual driver module 506 generated based on the switch control signal 408. The OUT_1 terminal may be connected to the base terminal of the NPN-BJT 510 and the base terminal of the PNP-BJT 512. While the example of the OUT_1 terminal being connected to the
30 base terminals of both the NPN-BJT 510 and the PNP-BJT 512 is provided, separate output terminals may be connected to the base terminals of the NPN-BJT 510 and the PNP-BJT 512.

[0123] FIG. 5B illustrates another example implementation of the driver 324. As shown in FIG. 5B, the push-pull amplifier 508 may be omitted.

[0124] Referring again to FIG. 5A, when the dual driver module 506 outputs a signal in a first state via the OUT_1 terminal, the NPN-BJT 510 connects its collector and emitter terminals to electrically couple the gate terminal of the MOSFET 502 to a reference voltage 514. The reference voltage 514 may be approximately 15 V or another suitable voltage. The connection of the gate terminal of the MOSFET 502 to the reference voltage 514 operates the MOSFET 502 in the closed state. When the dual driver module 506 outputs the signal in the first state via the OUT_1 terminal, the PNP-BJT 512 operates in the open state to disconnect the line 418 from ground.

[0125] When the dual driver module 506 outputs the signal in a second state via the OUT_1 terminal, the PNP-BJT 512 connects its collector and emitter terminals to electrically couple the gate terminal of the MOSFET 502 to ground. The connection of the gate terminal of the MOSFET 502 to ground operates the MOSFET 502 in the open state. When the dual driver module 506 outputs the signal in the second state via the OUT_1 terminal, the NPN-BJT 510 operates in the open state to disconnect the reference voltage 514 from the line 418.

[0126] The dual driver module 506 outputs a signal corresponding to the clamp control signal 410 from the OUT_2 terminal. A PNP-BJT 520 is an example of the clamp switch 424. The OUT_2 terminal of the dual driver module 506 is coupled to the PNP-BJT 520 via a resistor R168. The PNP-BJT 520 connects and disconnects the gate terminal of the MOSFET 502 to and from ground based on the signal from the dual driver module 506 output via the OUT_2 terminal. For example, the PNP-BJT 520 may connect the gate terminal of the MOSFET 502 with ground when the signal from the dual driver module 506 is in a first state (e.g., 15 V). The PNP-BJT 520 may create an open circuit and disconnect the gate terminal of the MOSFET 502 from ground when the signal from the dual driver module 506 is in a second state (e.g., ground or negative voltage). While the example of the PNP-BJT 520 is provided as an example of the clamp switch 424, the clamp switch 424 could be a PNP FET. In this example, the base-emitter junction reverse bias rating would be greater than the applied gate voltage (e.g., 15 V).

[0127] An example of the damping circuit 406 includes a ferrite bead FB10, a resistor R166, a Zener diode D45, a resistor R167, and a capacitor C94. The damping circuit 406 may, however, include different and/or another suitable arrangement of components.

[0128] In summary, the driver 324 controls charging and discharging of the inductor 308 by opening and closing the switch 320. To prevent oscillation of the switch 320, the driver 320 may include a damping circuit that absorbs excess energy caused by high frequency switching of the switch 320. The driver 320 may also include a clamp circuit that clamps the switch 320 to ground to operate the switch 320 in the open state when the switch 320 is to be in the open state.

While the example of connecting and clamping the control terminal of the switch 320 to ground to operate the switch 320 in the open state is provided, the present application is also applicable to other implementations using other reference potentials to operate the switch 320 in the open and closed states. For example, in the example of FIG. 3B, the control terminal of the switch 358
5 may be connected to ground to operate the switch 358 in the closed state and may be connected and clamped to a positive or negative voltage (e.g., -4 V to -7 V) to operate the switch 358 in the open state.

[0129] FIG. 6 is a functional block diagram of an example implementation of a switch monitor circuit, such as the switch monitor circuit 328 of FIG. 3A. FIG. 7 is a circuit diagram of an
10 example implementation of a switch monitor circuit, such as the switch monitor circuit 328 of FIG. 3A.

[0130] As shown in FIGs. 6 and 7, a node 604 is connected to a first terminal (e.g., drain (D) terminal or collector terminal) of the switch 320. A diode 608 may be implemented between the node 604 and the first terminal of the switch 320. The node 604 is also connected to a first
15 reference voltage (V REF1) 612 via a pull-up resistor 616. For example only, the first reference voltage 612 may be approximately 15 V or another suitable voltage.

[0131] A first voltage divider 620 divides a voltage at the node 604 and, as a result of the division, outputs a first voltage to a comparator 624. A combination of resistors providing an
example implementation of the first voltage divider 620 is provided in FIG. 7. A filter circuit
20 628 may be implemented to filter the voltage at the node 604 and input a filtered voltage to the first voltage divider 620.

[0132] A second voltage divider 632 divides a voltage at a second terminal (e.g., source (S) terminal or emitter terminal) of the switch 320 and, as a result of this division, outputs a second
voltage to the comparator 624. A combination of resistors providing an example implementation
25 of the second voltage divider 632 is provided in FIG. 7. The filter circuit 628 may also filter the voltage at the second terminal of the switch 320 and input a filtered voltage to the second
voltage divider 632. A combination of resistors and capacitors providing an example
implementation of the filter circuit 628 is also provided in FIG. 7.

[0133] The second terminal of the switch 320 is connected to ground. Ground may refer to a
30 reference ground potential or an actual ground potential. To prevent ground bounce, the voltage at the second terminal of the switch 320 or at a location closer to the second terminal of the
switch 320 may be used instead of ground for the second voltage input to the comparator 624
and, more specifically, the filter circuit 628.

[0134] The first voltage input to the comparator 624 serves as a threshold indicative of whether the switch 320 is in the closed state or the open state when compared with the second voltage input to the comparator 624. For example only, the first voltage divider 620 may output the first voltage to the comparator 624 at approximately 2 V to approximately 3 V or one or more other suitable voltages.

[0135] The second voltage input to the comparator 624 varies based on whether the switch 320 is in the closed state or the open state. For example only, when the switch 320 is in the closed state, the second voltage divider 632 may decrease the second voltage input to the comparator 624 to less than the first voltage input to the comparator 624. The first voltage divider 620 may decrease the first voltage input to the comparator 624 when the switch 320 is in the closed state, for example, to provide hysteresis. The first voltage divider 620 may decrease the first voltage, for example, to a lower voltage between 2 V and 3 V.

[0136] When the switch 320 is in the open state, the second voltage divider 632 may increase the second voltage input to the comparator 624 to greater than the first voltage input to the comparator 624. The first voltage divider 620 may increase the first voltage input to the comparator 624 when the switch 320 is in the open state, for example, to provide hysteresis. The first voltage divider 620 may increase the first voltage, for example, to a higher voltage between 2 V and 3 V. The higher voltage is greater than the lower voltage.

[0137] Whether the first voltage input to the comparator 624 is greater than or less than the second voltage input to the comparator 624 therefore indicates whether the switch 320 is in the closed state or in the open state.

[0138] The comparator 624 generates the switch state signal based on a comparison of the first and second voltages output by the first and second voltage dividers 620 and 632, respectively. The switch state signal indicates whether the switch 320 is in the open state or the closed state. For example, the comparator 624 may set the switch state signal to a first state when the first voltage output by the first voltage divider 620 is greater than the second voltage output by the second voltage divider 632. The switch state signal being in the first state may therefore indicate that the switch 320 is in the open state. The comparator 624 may set the switch state signal to a second state when the first voltage output by the first voltage divider 620 is less than the second voltage output by the second voltage divider 632. The switch state signal being in the second state may therefore indicate that the switch 320 is in the closed state.

[0139] While the example of a single threshold (first voltage) has been discussed, multiple thresholds may be compared with the second voltage output by the second voltage divider 632.

For example, the comparator 624 may set the switch state signal to the first state when the second voltage output by the second voltage divider 632 is greater than, for example, a first threshold voltage. The comparator 624 may set the switch state signal to the second state when the second voltage output by the second voltage divider 632 is less than a second threshold voltage that is less than the first threshold voltage. This example is similar to the first voltage divider 620 varying the first voltage from the lower voltage to the higher voltage and vice versa, but involves the use of two different voltage dividers.

[0140] As discussed further below, the control module 220 controls switching of the switch 320 based on the switch state signal. For example, the control module 220 determines a turn OFF delay period of the switch 320 and a turn ON delay period of the switch 320 based on the switch state signal. The turn OFF delay period corresponds to a period between when the control module 220 outputs a signal to transition the switch 320 to the open state and when the switch 320 reaches the open state, as indicated by the switch state signal. The turn ON delay period corresponds to a period between when the control module 220 outputs a signal to transition the switch 320 to the closed state and when the switch 320 reaches the closed state, as indicated by the switch state signal. The control module 220 may control switching timing of the switch 320 based on the turn ON and turn OFF delay periods.

[0141] FIG. 8 is a functional block diagram of the control module 220. A desired voltage module 704 determines a desired DC bus voltage. The desired DC bus voltage may be a fixed predetermined value or may be variable. The desired voltage module 704 may determine the desired DC bus voltage, for example, based on a peak voltage of the AC line (V_{PEAK}) and/or at least one of a plurality of system parameters.

[0142] For example only, the plurality of system parameters may include, but are not limited to, actual and commanded compressor speed, actual and estimated inverter output power, actual and estimated drive output power, input and output current, drive input voltage, inverter output voltage, estimated motor torque, various temperatures, and a demand from the condenser 104. The various temperatures may include, for example, temperatures of the PFC circuit 212, the inverter power circuit 232, circuit boards, the compressor scroll, and the motor 236. By way of example, a look-up table may include a desired DC bus voltage V_{DES} corresponding to possible AC peak voltages V_{PEAK} and each of the different combinations of the plurality of system parameters. The desired voltage module 704 may determine the desired DC bus voltage using the look-up table. For values between entries of the look-up table, the desired voltage module 704 may determine the desired DC bus voltage using interpolation. Further example discussion regarding setting the desired DC bus voltage is provided in the U.S. Prov. App. titled "Power

Factor Correction Circuits and Methods Including Partial Power Factor Correction Operation for Boost and Buck Power Converters,” Attorney Docket No. 0315-000927-US-PS1, filed on April 15, 2016, which is incorporated herein in its entirety.

5 [0143] A voltage control module 708 determines a difference between the desired DC bus voltage and the measured DC bus voltage. The voltage control module 708 determines a first current demand based on the difference. More specifically, the voltage control module 708 determines the first current demand based on adjusting the difference toward or to zero.

10 [0144] The voltage control module 708 applies a filter to the first current demand and determines an initial current demand based on the first and filtered current demands. The voltage control module 708 weights the contributions of the first and filtered current demands to the initial current demand based on the magnitude of the difference between the measured and desired DC bus voltages. More specifically, the voltage control module 708 applies a greater weight to the filtered current demand when the magnitude of the difference is low. The voltage control module 708 increases the weighting of the first current demand and decreases the
15 weighting of the filtered current demand as the difference increases. The voltage control module 708 may, for example, set the initial current demand based on or equal to a sum of the (weighted) first and filtered current demands.

20 [0145] A current demand module 712 may apply a filter to the initial current demand, such as a notch filter. The current demand module 712 may also perform one or more signal processing functions to reduce noise in the initial current demand. The current demand module 712 multiplies the (filtered) initial current demand with a reference signal to produce a final current demand. While the example of the current demand module 712 filtering the initial current demand is provided, the current demand module may not filter the initial current demand in other examples. In such a case, the initial current demand may be multiplied with the reference
25 signal to produce the final current demand.

[0146] A reference generation module 716 determines zero crossings of the AC line and the reference signal. Based on the zero crossings, the reference generation module 716 generates the reference signal to track the AC input voltage in phase and frequency. In this way, the final current demand follows the AC input voltage, for example, to maximize power factor.

30 [0147] A current control module 720 generates the switch control signal 408 to control switching of the switch 320. More specifically, the current control module 720 transitions the switch 320 to the open state when the measured current through the inductor 308 is greater than the final current demand through the inductor 308. The current control module 720 then

maintains the switch 320 in the open state for a desired OFF period. The desired OFF period may be a fixed value or may be a variable. The current control module 720 transitions the switch 320 to the closed state until the measured current through the inductor 308 again becomes greater than the final current demand through the inductor 308. The current control module 720 may also generate the clamp control signal 410, as described above. While this example is discussed, the current control module 720 may alternatively transition the switch 320 from OFF to ON when the measured current becomes less than the final current demand, maintain the switch 320 ON for a (variable) desired ON period, and transition the switch 320 from ON to OFF once the desired ON period has passed. The desired ON period may be determined similarly to the desired OFF period.

[0148] FIG. 9 is a functional block diagram of an example implementation of the current control module 720. The current control module 720 controls switching of the switch 320 based on a comparison of the final current demand through the inductor 308 with the measured current through the inductor 308. The measured current may be measured using the current sensor 312. The current control module 720 controls timing of the switching of the switch 320 considering measurement delays (e.g., of the current measurement) and other delays.

[0149] A comparison module 804 sets a comparison signal to a first state when the measured current is less than the final current demand. The comparison module 804 sets the comparison signal to a second state when the measured current is greater than the final current demand.

[0150] A switching control module 808 controls switching of the switch 320 based on the comparison of the measured current with the final current demand. More specifically, the switching control module 808 sets the switch control signal 408 based on the comparison of the measured current with the final current demand. For example, the switching control module 808 generates the switch control signal 408 to transition the switch 320 to the open state (OFF/not conducting) when the comparison signal transitions from the first state to the second state. The switching control module 808 generates the switch control signal 408 to maintain the switch 320 in the open state for a desired OFF period. More specifically, the switching control module 808 generates the switch control signal 408 to maintain the switch 320 in the open state until an OFF period is greater than the desired OFF period. The OFF period corresponds to the period since the switching control module 808 last generated the switch control signal 308 to transition the switch 320 to the open state.

[0151] A timer module 812 increments the OFF period when the comparison signal is in the second state. More specifically, the timer module 812 increments the OFF period when the switch 320 is OFF. In this manner, the OFF period tracks the period elapsed since the switching

control module 808 last transitioned the switch 320 from ON to OFF (i.e., the measured current became greater than the final current demand). The timer module 1012 resets the OFF period when the switching control module 808 transitions the switch 320 from OFF to ON.

[0152] When the OFF period is greater than (or equal to) the desired OFF period, the switching control module 808 generates the switch control signal 408 to transition the switch 320 to the closed state (ON/conducting). The switching control module 808 then generates the switch control signal 408 to maintain the switch 320 in the closed state until the comparison signal is next in the second state. Under relatively steady state load conditions, the turning ON of the switch 320 may occur at approximately a beginning of a next predetermined switching period.

[0153] The predetermined switching periods (t_p) correspond to the predetermined switching frequency. As described above, the predetermined switching frequency may be at least 50 KHz and may be approximately 200 kilohertz (kHz) or another suitable frequency. The predetermined switching periods correspond to 1 divided by the predetermined switching frequency. The switching control module 808 may control the switch 320 to be in the closed state (conducting) and the open state (not conducting) for different portions of each predetermined switching period.

[0154] A desired OFF period module 816 may set the desired OFF period. For example only, the desired OFF period module 816 may set the desired OFF period to a predetermined fixed value. Alternatively, the desired OFF period module 816 may determine the desired OFF period based on one or more parameters. Further example discussion regarding determining the desired OFF period is provided in the U.S. Prov. App. titled "Switch Off Time Control Systems and Methods," Attorney Docket No. 0315-000924-US-PS1, filed on April 15, 2016, which is incorporated herein in its entirety. While the example of a sinusoidal AC input has been described, the present application is also applicable to other types of inputs including rectified inputs resulting from rectification of AC inputs.

[0155] The switching control module 808 also compensates for the turn ON delay period of the switch 320 and the turn OFF delay period of the switch 320. The turn ON delay period corresponds to the period between a first time when the switching control module 808 generates the switch control signal 408 to transition the switch 320 from the open state to the closed state and a second time when the switch 320 actually reaches the closed state (conductance) in response. The turn OFF delay period corresponds to the period between a first time when the switching control module 808 generates the switch control signal 408 to transition the switch 320 to the open state and a second time when the switch 320 actually reaches the open state

(non-conductance) in response. The switch state signal from the switch monitoring circuit 328 is used to determine when the switch 320 reaches the open state and the closed state.

5 **[0156]** To account for the turn ON delay period, the switching control module 808 should hypothetically generate the switch control signal 408 to transition the switch 320 to the closed state before the OFF period reaches the desired OFF period. The switching control module 808 should also hypothetically generate the switch control signal 408 to transition the switch 320 to the open state before the current becomes greater than the final current demand due to the turn OFF delay period.

10 **[0157]** The switching control module 808 could adjust the desired OFF period based on the turn ON delay period and the turn OFF delay period. For example, the switching control module 808 could add the turn OFF delay period and subtract the turn ON delay period from the desired OFF period. This (adjusted) desired OFF period will be compared with the OFF period from the timer module 812 to determine when to transition the switch 320 to the closed state. The use of the (adjusted) desired OFF period may prevent switching too early.

15 **[0158]** Other alternatives for this compensation are also possible. For example, the switching control module 808 could generate the switch control signal 408 to transition the switch 320 to the open state when the measured current is greater than a current threshold that is less than the final current demand. The switching control module 808 could generate the switch control signal 408 to transition the switch 320 to the closed state when the turn ON delay period before the
20 OFF period reaches the desired OFF period.

[0159] A delay determination module 824 determines the turn ON delay period and the turn OFF delay period. For example, the delay determination module 824 may reset and start a timer when the switching control module 808 generates the switch control signal 408 to transition the switch 320 from the open state to the closed state. The delay determination module 824 may
25 monitor the switch state signal and set the turn ON delay period based on or to the period indicated by the timer when the switch state signal indicates that the switch 320 transitioned from the open state to the closed state.

[0160] The delay determination module 824 may reset and start a timer when the switching control module 808 generates the switch control signal 408 to transition the switch 320 from the
30 closed state to the open state. The delay determination module 824 may monitor the switch state signal and set the turn OFF delay period based on or to the period indicated by the timer when the switch state signal indicates that the switch 320 transitioned from the closed state to the open state.

[0161] While the delay determination module 824 is shown as being implemented within the current control module 720, the delay determination module 824 may be implemented externally to the current control module 720 and may be implemented externally to the control module 220. Also, while the example of turning the switch 320 OFF when the measured current becomes greater than the final current demand and maintaining the switch 320 OFF for the desired OFF period thereafter, the switching control module 808 may alternatively turn the switch 320 ON for a desired ON period. More specifically, the switching control module 808 may turn the switch 320 ON when the measured current falls below the final current demand, maintain the switch 320 ON for a desired ON period, and turn the switch 320 OFF when the desired ON period has passed after the turning of the switch 320 ON. A desired ON period module (not shown) determines the desired ON period. Written generally, for a boost converter, the desired ON period module may determine the desired ON period based on the input voltage, the output voltage, and the predetermined switching period. The desired ON period module may determine the desired ON period using one of a function and a look-up table that relates input voltages and output voltages to desired ON times given the predetermined switching period. For values between entries of the look-up table, the desired ON period module 816 may determine the desired ON period using interpolation.

[0162] As an alternative to determining the turn ON delay period and the turn OFF delay period based on the switch state signal, the delay determination module 824 may retrieve the turn ON delay period and the turn OFF delay period from memory. In this example, the turn ON delay period and the turn OFF delay period may be predetermined values set/calibrated based on data sheet information.

[0163] As yet another alternative, the delay determination module 824 may determine a total delay period (inclusive of both the turn ON delay period and the turn OFF delay period). The delay determination module 824 may set the total delay period, for example, based on or equal to the period between consecutive instances when the switch control module 808 generates the switch control signal 408 to transition the switch 320 from the closed state to the open state. Alternatively, consecutive instances when the switch control module 808 generates the switch control signal 408 to transition the switch 320 from the open state to the closed state may be used. The switching control module 808 could adjust the desired OFF period based on the total delay period. For example, the switching control module 808 could subtract the total delay period from the desired OFF period or decrease the desired OFF period as a function of the total delay period.

[0164] In all of the above examples, the delay determination module 824 may limit the determined delay period(s) to between predetermined upper and lower limit values.

Additionally, the delay determination module 824 may scale the one or more of determined delay period(s) and/or one or more components of one or more of the determined delay

5 period(s), such as the turn OFF delay period and not the turn ON delay period, based on the input and output voltages and one or more predetermined scalar values. The delay determination module 824 may scale the one or more determined delay period(s) and/or one or more components of one or more of the determined delay period(s), for example, using one or more functions and/or mappings that relate the input voltage, the output voltage, and the one or more
10 predetermined scalar values to scalar values. The delay determination module 824 may multiply a scalar value determined based on a given set of input voltage, output voltage, and predetermined scalar value(s) to the one or more determined delay period(s) and/or one or more components of one or more of the determined delay period(s). As an example only, the delay determination module 824 may determine scalar values using the relationship:

$$15 \quad \frac{VAC}{(VDC-VAC)} * Pred,$$

where VAC is the input voltage, VDC is the output voltage, and Pred is a predetermined scalar value. For example only, the predetermined scalar value may be 0.707 or another suitable value.

[0165] A fault module 828 may diagnose a switching fault based on the turn ON delay period, the turn OFF delay period, or the period tracked by the timers. For example, the fault module
20 828 may indicate that a switching fault has occurred when the turn ON delay period, the turn OFF delay period, or one of the periods tracked by the timers (to determine the turn ON and OFF delay periods) is greater than a predetermined period. The turn ON delay period (or the associated timer) being longer than the predetermined period may indicate that the switch 320 failed to transition to the closed state (or at least not fully closed/partially open, e.g., due to high
25 current) within the predetermined period after controlled to do so. The turn OFF delay period (or the associated timer) being longer than the predetermined period may indicate that the switch 320 failed to transition to the open state within the predetermined period after controlled to do so.

[0166] The fault module 828 may take one or more remedial actions when a switching fault is
30 diagnosed. For example, the fault module 828 may store an indicator of the presence of a switching fault in memory. Additionally or alternatively, the fault module 828 may illuminate a fault indicator 832 when a switching fault is diagnosed. Additionally or alternatively, the fault module 828 may generate the switch control signal 408 and the clamp control signal 410 to

operate the switch 320 in the open state. The fault module 828 may take one or more other remedial actions additionally or alternatively when a switching fault is diagnosed.

[0167] FIG. 10 includes a flowchart depicting an example method of controlling the switch 320 based on the desired OFF period. Control begins with 904 where the switching control module 808 determines whether the switch 320 is in the open state. If 904 is true, control transfers to 928, which is discussed further below. If 904 is false, control continues with 908.

[0168] At 908, the desired OFF period module 816 determines the desired OFF period. At 912, the switching control module 808 may adjust the desired OFF period based on the turn ON delay period and the turn OFF delay period. For example, the switching control module 808 may sum the desired OFF period with the turn OFF delay period and subtract the turn ON delay period.

[0169] The comparison module 804 may determine whether the measured current is greater than the final current demand at 916. The determination of the final current demand is discussed above. If 916 is false, the timer module 812 resets the OFF period and the switching control module 808 maintains the switch 320 in the closed state at 920, and control ends. If 916 is true, control continues with 924.

[0170] The switching control module 808 generates the switch control signal 408 to transition the switch 320 to the open state at 924 when the measured current is greater than the final current demand. At 928, the switching control module 808 may determine whether the OFF period of the switch 320 is greater than the desired OFF period. If 928 is false, the switching control module 808 maintains the switch 320 in the open state at 932, and control ends. If 928 is true, the switching control module 808 generates the switch control signal 408 to transition the switch 320 to the closed state at 936, and control ends. In various implementations, the switching control module 808 may wait for, or ensure that, the measured current is less than the final current demand before generating the output signal to turn the switch 320 ON at 936.

While control is shown as ending, the example of FIG. 10 is illustrative of one control loop and control may return to 904 for a next control loop.

[0171] FIG. 11 is a flowchart including an example method of determining the turn ON or turn OFF delay period of the switch 320. Control begins with 1004 where the delay determination module 824 determines whether the switch control signal 408 has transitioned, such as to transition the switch 320 from the open state to the closed state. If 1004 is true, control continues with 1008. If 1004 is false, control may end.

[0172] At 1008, the delay determination module 824 may reset and start a timer. The timer therefore tracks the period since the switch control signal 408 transitioned. At 1012, the delay

determination module 824 determines whether the switch state signal transitioned to the state associated with the transition in the switch control signal 408. If 1012 is false, the delay determination module 824 increments the timer at 1016 and returns to 1012. The fault module 828 may diagnose a switching fault and take one or more remedial actions when the timer is greater than the predetermined period. If 1012 is true, the delay determination module 824 may set the turn ON delay period or the turn OFF delay period based on or equal to the period tracked by the timer at 1020.

[0173] For example, when the switch control signal 408 was for transitioning the switch 320 from the open state to the closed state, the delay determination module 824 sets the turn ON delay period for the switch 320 based on the period of the timer. When the switch control signal 408 was for transitioning the switch 320 from the closed state to the open state, the delay determination module 824 sets the turn OFF delay period for the switch 320 based on the period of the timer. While control is shown as ending, the example of FIG. 11 is illustrative of one control loop and control may return to 1004 for a next control loop.

[0174] The foregoing description is merely illustrative in nature and is in no way intended to limit the disclosure, its application, or uses. The broad teachings of the disclosure can be implemented in a variety of forms. Therefore, while this disclosure includes particular examples, the true scope of the disclosure should not be so limited since other modifications will become apparent upon a study of the drawings, the specification, and the following claims. It should be understood that one or more steps within a method may be executed in different order (or concurrently) without altering the principles of the present disclosure. Further, although each of the embodiments is described above as having certain features, any one or more of those features described with respect to any embodiment of the disclosure can be implemented in and/or combined with features of any of the other embodiments, even if that combination is not explicitly described. In other words, the described embodiments are not mutually exclusive, and permutations of one or more embodiments with one another remain within the scope of this disclosure.

[0175] Spatial and functional relationships between elements (for example, between modules, circuit elements, semiconductor layers, etc.) are described using various terms, including “connected,” “engaged,” “coupled,” “adjacent,” “next to,” “on top of,” “above,” “below,” and “disposed.” Unless explicitly described as being “direct,” when a relationship between first and second elements is described in the above disclosure, that relationship can be a direct relationship where no other intervening elements are present between the first and second elements, but can also be an indirect relationship where one or more intervening elements are

present (either spatially or functionally) between the first and second elements. As used herein, the phrase at least one of A, B, and C should be construed to mean a logical (A OR B OR C), using a non-exclusive logical OR, and should not be construed to mean “at least one of A, at least one of B, and at least one of C.”

5 [0176] In the figures, the direction of an arrow, as indicated by the arrowhead, generally demonstrates the flow of information (such as data or instructions) that is of interest to the illustration. For example, when element A and element B exchange a variety of information but information transmitted from element A to element B is relevant to the illustration, the arrow may point from element A to element B. This unidirectional arrow does not imply that no other
10 information is transmitted from element B to element A. Further, for information sent from element A to element B, element B may send requests for, or receipt acknowledgements of, the information to element A.

[0177] In this application, including the definitions below, the term “module” or the term “controller” may be replaced with the term “circuit.” The term “module” may refer to, be part
15 of, or include: an Application Specific Integrated Circuit (ASIC); a digital, analog, or mixed analog/digital discrete circuit; a digital, analog, or mixed analog/digital integrated circuit; a combinational logic circuit; a field programmable gate array (FPGA); a processor circuit (shared, dedicated, or group) that executes code; a memory circuit (shared, dedicated, or group) that stores code executed by the processor circuit; other suitable hardware components that
20 provide the described functionality; or a combination of some or all of the above, such as in a system-on-chip.

[0178] The module may include one or more interface circuits. In some examples, the interface circuits may include wired or wireless interfaces that are connected to a local area network (LAN), the Internet, a wide area network (WAN), or combinations thereof. The functionality of
25 any given module of the present disclosure may be distributed among multiple modules that are connected via interface circuits. For example, multiple modules may allow load balancing. In a further example, a server (also known as remote, or cloud) module may accomplish some functionality on behalf of a client module.

[0179] Some or all hardware features of a module may be defined using a language for
30 hardware description, such as IEEE Standard 1364-2005 (commonly called “Verilog”) and IEEE Standard 1076-2008 (commonly called “VHDL”). The hardware description language may be used to manufacture and/or program a hardware circuit. In some implementations, some or all features of a module may be defined by a language, such as IEEE 1666-2005 (commonly called “SystemC”), that encompasses both code, as described below, and hardware description.

[0180] The term code, as used above, may include software, firmware, and/or microcode, and may refer to programs, routines, functions, classes, data structures, and/or objects. The term shared processor circuit encompasses a single processor circuit that executes some or all code from multiple modules. The term group processor circuit encompasses a processor circuit that, in combination with additional processor circuits, executes some or all code from one or more modules. References to multiple processor circuits encompass multiple processor circuits on discrete dies, multiple processor circuits on a single die, multiple cores of a single processor circuit, multiple threads of a single processor circuit, or a combination of the above. The term shared memory circuit encompasses a single memory circuit that stores some or all code from multiple modules. The term group memory circuit encompasses a memory circuit that, in combination with additional memories, stores some or all code from one or more modules.

[0181] The term memory circuit is a subset of the term computer-readable medium. The term computer-readable medium, as used herein, does not encompass transitory electrical or electromagnetic signals propagating through a medium (such as on a carrier wave); the term computer-readable medium may therefore be considered tangible and non-transitory. Non-limiting examples of a non-transitory computer-readable medium are nonvolatile memory circuits (such as a flash memory circuit, an erasable programmable read-only memory circuit, or a mask read-only memory circuit), volatile memory circuits (such as a static random access memory circuit or a dynamic random access memory circuit), magnetic storage media (such as an analog or digital magnetic tape or a hard disk drive), and optical storage media (such as a CD, a DVD, or a Blu-ray Disc).

[0182] The apparatuses and methods described in this application may be partially or fully implemented by a special purpose computer created by configuring a general purpose computer to execute one or more particular functions embodied in computer programs. The functional blocks and flowchart elements described above serve as software specifications, which can be translated into the computer programs by the routine work of a skilled technician or programmer.

[0183] The computer programs include processor-executable instructions that are stored on at least one non-transitory computer-readable medium. The computer programs may also include or rely on stored data. The computer programs may encompass a basic input/output system (BIOS) that interacts with hardware of the special purpose computer, device drivers that interact with particular devices of the special purpose computer, one or more operating systems, user applications, background services, background applications, etc.

- [0184]** The computer programs may include: (i) descriptive text to be parsed, such as HTML (hypertext markup language), XML (extensible markup language), or JSON (JavaScript Object Notation) (ii) assembly code, (iii) object code generated from source code by a compiler, (iv) source code for execution by an interpreter, (v) source code for compilation and execution by a just-in-time compiler, etc. As examples only, source code may be written using syntax from languages including C, C++, C#, Objective-C, Swift, Haskell, Go, SQL, R, Lisp, Java®, Fortran, Perl, Pascal, Curl, OCaml, Javascript®, HTML5 (Hypertext Markup Language 5th revision), Ada, ASP (Active Server Pages), PHP (PHP: Hypertext Preprocessor), Scala, Eiffel, Smalltalk, Erlang, Ruby, Flash®, Visual Basic®, Lua, MATLAB, SIMULINK, and Python®.
- [0185]** None of the elements recited in the claims are intended to be a means-plus-function element within the meaning of 35 U.S.C. §112(f) unless an element is expressly recited using the phrase “means for,” or in the case of a method claim using the phrases “operation for” or “step for.”

CLAIMS

What is claimed is:

1. A drive, comprising:
 - an inverter power circuit that applies power to an electric motor of a compressor
 - 5 from a direct current (DC) voltage bus;
 - a power factor correction (PFC) circuit that outputs power to the DC voltage bus based on input alternating current (AC) power, the PFC circuit including:
 - (i) a switch having a first terminal, a second terminal, and a control
 - terminal;
 - 10 (ii) a driver that switches the switch between open and closed states based on a control signal;
 - (iii) an inductor that charges and discharges based on switching of the switch; and
 - (iv) a circuit that outputs a signal indicating whether the switch is in the
 - 15 open state or the closed state based on a voltage across the first and second terminals of the switch.
2. The drive of claim 1 further comprising a control module that generates the control signal based on the signal indicating whether the switch is in the open state or the closed state.
- 20 3. The drive of claim 2 wherein the control module measures a period between:
 - (i) a first time when the control signal transitions from a first state for transitioning the switch one of:
 - (a) from the open state to the closed state; and
 - (b) from the closed state to the open state; and
 - 25 (i) a second time, after the first time, when the signal transitions from a first state to a second indicating that the one of:
 - (a) the switch transitioned from the open state to the closed state; and
 - (b) the switch transitioned from the closed state to the open state,
 - wherein the control module generates the control signal based on the period.

4. The drive of claim 1 wherein the circuit generates the signal indicating that the switch is in the closed state when the voltage across the first and second terminals of the switch is less than a predetermined voltage.
5. The drive of claim 1 wherein the circuit generates the signal indicating that the switch is in the open state when the voltage across the first and second terminals is greater than a predetermined voltage.
6. The drive of claim 1 wherein the second terminal of the switch is connected to a ground potential.
7. The drive of claim 1 wherein the circuit includes a node that is connected to a first voltage at the first terminal of the switch when the switch is in the closed state and that is connected to a second voltage when the switch is in the open state.
8. The drive of claim 7 wherein the circuit further includes:
 - a first voltage divider that generates a third voltage based on a fourth voltage at the node;
 - a second voltage divider that generates a fifth voltage based on a sixth voltage at the second terminal of the switch; and
 - a comparator that generates the signal indicating whether the switch is in the open state or the closed state based on a comparison of the third voltage and the fifth voltage.
9. The drive of claim 8 wherein the comparator generates the signal indicating that the switch is in the open state when the third voltage is greater than the fifth voltage.
10. The drive of claim 8 wherein the comparator generates the signal indicating that the switch is in the closed state when the third voltage is less than the fifth voltage.
11. A method, comprising:
 - applying power to an electric motor of a compressor from a direct current (DC) voltage bus;
 - by a power factor correction (PFC) circuit, providing power to the DC voltage bus based on input alternating current (AC) power, the providing power to the DC bus

voltage including switching a switch of the PFC circuit between open and closed states based on a control signal,

wherein the switch includes a first terminal, a second terminal, and the control terminal; and

5 outputting a signal indicating whether the switch is in the open state or the closed state based on a voltage across the first and second terminals of the switch.

12. The method of claim 11 further comprising generating the control signal based on the signal indicating whether the switch is in the open state or the closed state.

13. The method of claim 12 further comprising measuring a period between:

10 (i) a first time when the control signal transitions from a first state for transitioning the switch one of:

 (a) from the open state to the closed state; and

 (b) from the closed state to the open state; and

15 (i) a second time, after the first time, when the signal transitions from a first state to a second indicating that the one of:

 (a) the switch transitioned from the open state to the closed state; and

 (b) the switch transitioned from the closed state to the open state,

wherein generating the control signal includes generating the control signal based on the period.

20 14. The method of claim 11 wherein outputting the signal indicating whether the switch is in the open state or the closed state includes generating the signal indicating that the switch is in the closed state when the voltage across the first and second terminals of the switch is less than a predetermined voltage.

25 15. The method of claim 11 wherein outputting the signal indicating whether the switch is in the open state or the closed state includes generating the signal indicating that the switch is in the open state when the voltage across the first and second terminals is greater than a predetermined voltage.

16. The method of claim 11 wherein the second terminal of the switch is connected to a ground potential.

17. The method of claim 11 further comprising:
connecting a node to a first voltage at the first terminal of the switch when the switch is in the closed state; and
connecting the node to a second voltage when the switch is in the open state.
- 5 18. The method of claim 17 further comprising:
by a first voltage divider, generating a third voltage based on a fourth voltage at the node; and
by a second voltage divider, generating a fifth voltage based on a sixth voltage at the second terminal of the switch,
10 wherein outputting the signal indicating whether the switch is in the open state or the closed state includes outputting the signal indicating whether the switch is in the open state or the closed state based on a comparison of the third voltage and the fifth voltage.
19. The method of claim 18 wherein outputting the signal indicating whether the switch is in the open state or the closed state includes generating the signal indicating that the switch is in the open state when the third voltage is greater than the fifth voltage.
15
20. The method of claim 18 wherein outputting the signal indicating whether the switch is in the open state or the closed state includes generating the signal indicating that the switch is in the closed state when the third voltage is less than the fifth voltage.
20
21. A drive for an electric motor of a compressor, the drive comprising:
an inverter power circuit that applies power to an electric motor of a compressor from a direct current (DC) voltage bus;
a power factor correction (PFC) circuit that outputs power to the DC voltage bus
25 based on input alternating current (AC) power, the PFC circuit including:
(i) a switch;
(ii) a driver that connects a control terminal of the switch to a first reference potential when a control signal is in a first state and that connects the control terminal of the switch to a second reference potential when the control signal is in a
30 second state, wherein the first reference potential is one of greater than and less than the second reference potential,

wherein the switch operates in an open state when the first reference potential is connected to the control terminal and operates in a closed state when the second reference potential is connected to the control terminal; and

5 (iii) an inductor that charges and discharges based on switching of the switch; and

a control module that generates the control signal based on a measured current through the inductor and a predetermined current through the inductor.

22. The drive of claim 21, wherein the control module transitions the control signal to the first state when the measured current through the inductor is greater than the
10 predetermined current through the inductor.

23. The drive of claim 22, wherein the control module maintains the control signal in the first state for a predetermined period after transitioning the control signal to the first state.

24. The drive of claim 21 wherein the PFC circuit further includes a clamp switch that
15 selectively connects the control terminal of the switch to the first reference potential.

25. The drive of claim 24 wherein the clamp switch connects the control terminal of the switch to the first reference potential when a second control signal is in a first state, wherein the control module sets the second control signal to the first state while the control signal is in the first state.

20 26. The drive of claim 25 wherein the clamp switch creates an open circuit between the control terminal of the switch and the first reference potential when the second control signal is in a second state.

27. The drive of claim 21 wherein the driver switches the switch between the open and closed states at a frequency of at least 50 Kilohertz (KHz).

25 28. The drive of claim 21 wherein the PFC circuit further includes a snubber circuit connected in parallel with the switch.

29. The drive of claim 21, wherein the PFC circuit further includes a damping circuit connected between the control terminal of the switch and the first reference potential.

30. The drive of claim 21 wherein the first reference potential is a ground potential.
31. A method, comprising:
by an inverter power circuit, applying power to an electric motor of a compressor from a direct current (DC) voltage bus;
5 by a power factor correction (PFC) circuit, providing power to the DC voltage bus based on input alternating current (AC) power, the providing power including:
by a driver of the PFC circuit, connecting a control terminal of a switch of the PFC circuit to a first reference potential when a control signal is in a first state; and
by the driver of the PFC circuit, connecting the control terminal of the
10 switch of the PFC circuit to a second reference potential when the control signal is in a second state,
wherein the first reference potential is one of greater than and less than the second reference potential,
wherein the switch operates in an open state when the first reference
15 potential is connected to the control terminal and operates in a closed state when the second reference potential is connected to the control terminal, and
wherein an inductor of the PFC circuit charges and discharges based on switching of the switch; and
generating the control signal based on a measured current through the inductor
20 and a predetermined current through the inductor.
32. The method of claim 31, wherein generating the control signal includes transitioning the control signal to the first state when the measured current through the inductor is greater than the predetermined current through the inductor.
33. The method of claim 32, wherein generating the control signal further includes
25 maintaining the control signal in the first state for a predetermined period after transitioning the control signal to the first state.
34. The method of claim 31 further comprising selectively switching a clamp switch of the PFC circuit thereby selectively connecting the control terminal of the switch to the first reference potential.

35. The method of claim 34 wherein:
selectively switching the clamp switch of the PFC circuit includes switching the clamp switch of the PFC circuit to connect the control terminal of the switch to the first reference potential when a second control signal is in a first state; and
- 5 the method further includes setting the second control signal to the first state while the control signal is in the first state.
36. The method of claim 35 wherein selectively switching the clamp switch of the PFC circuit thereby creating an open circuit between the control terminal of the switch and the first reference potential when the second control signal is in a second state.
- 10 37. The method of claim 31 wherein generating the control signal includes transitioning the control signal between the first and second states at a frequency of at least 50 Kilohertz (KHz).
38. The method of claim 31 wherein the first reference potential is a ground potential.
- 15 39. The method of claim 31 wherein the first reference potential is a negative potential.
40. The method of claim 31 wherein the second reference potential is a positive potential.

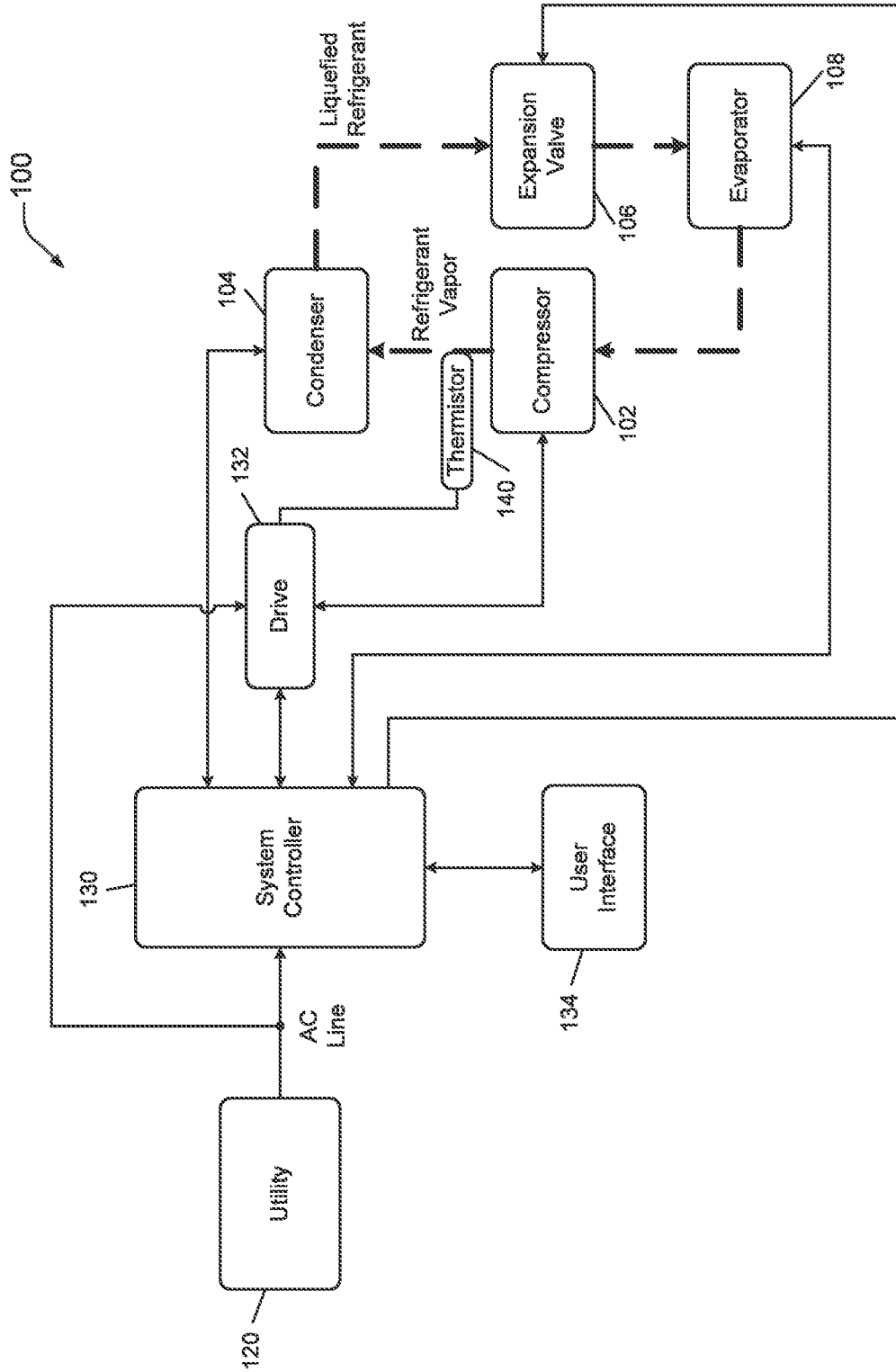


FIG. 1

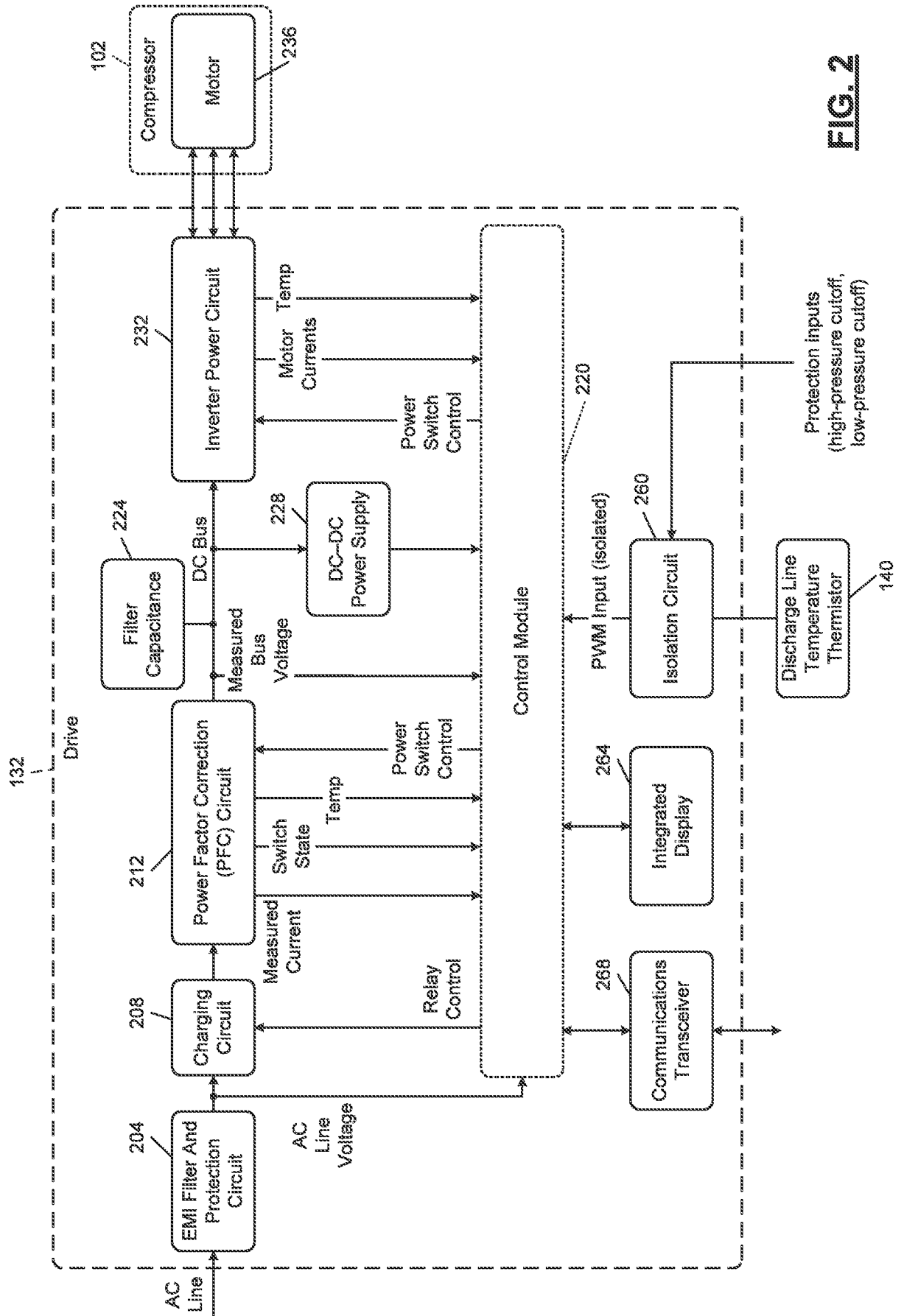


FIG. 2

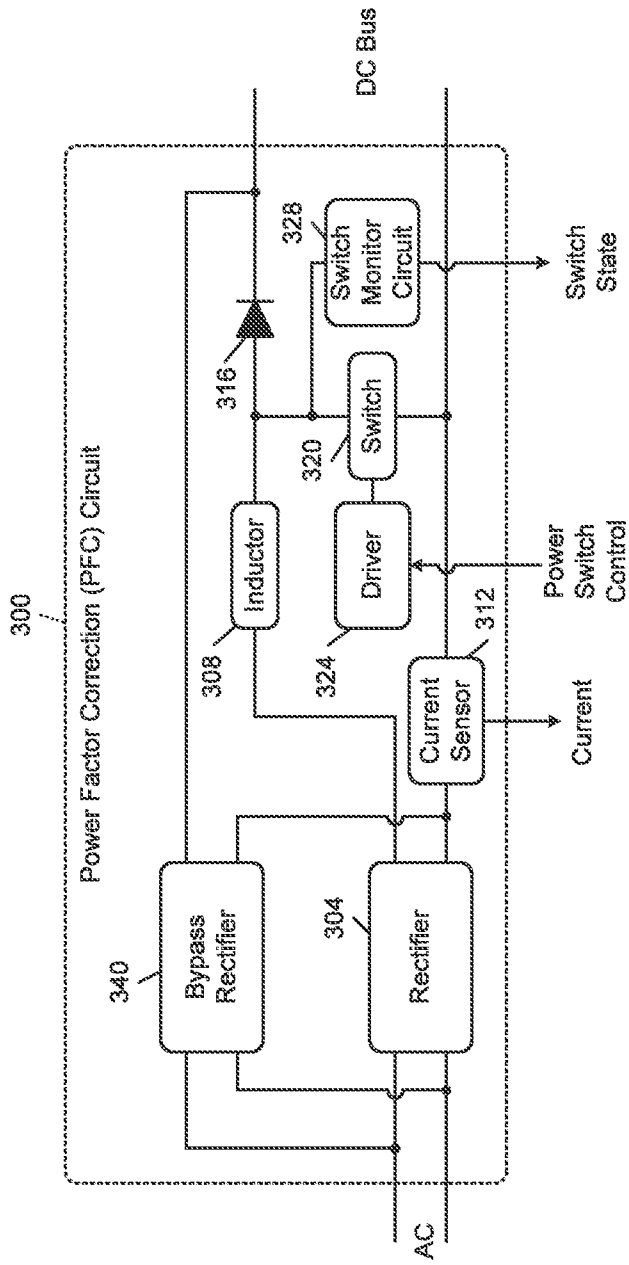


FIG. 3A

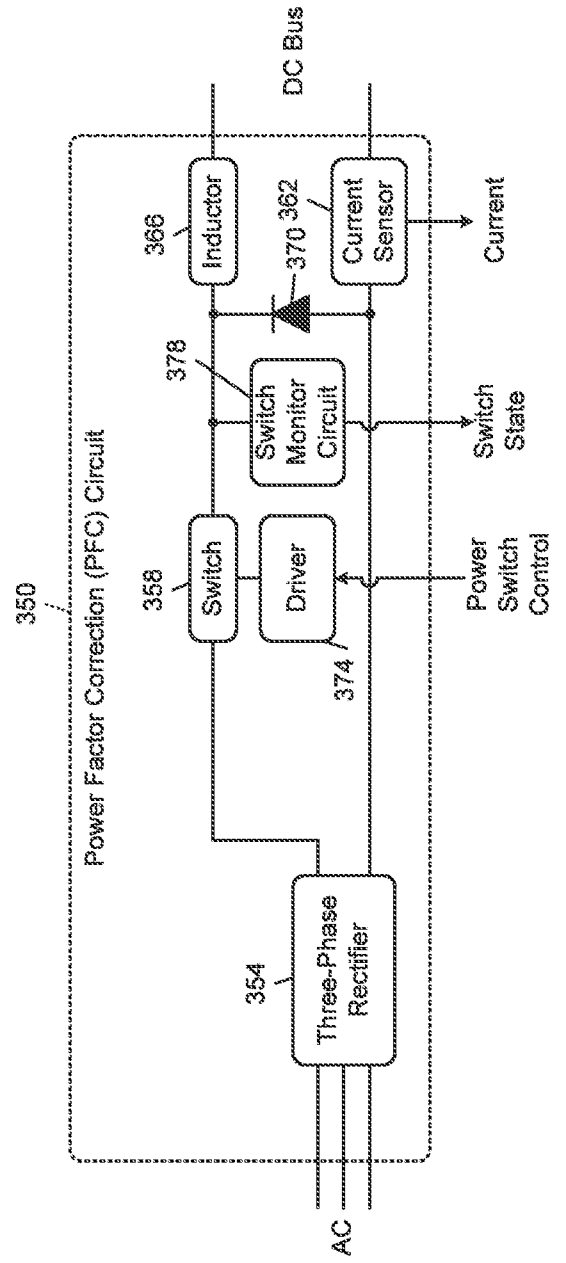


FIG. 3B

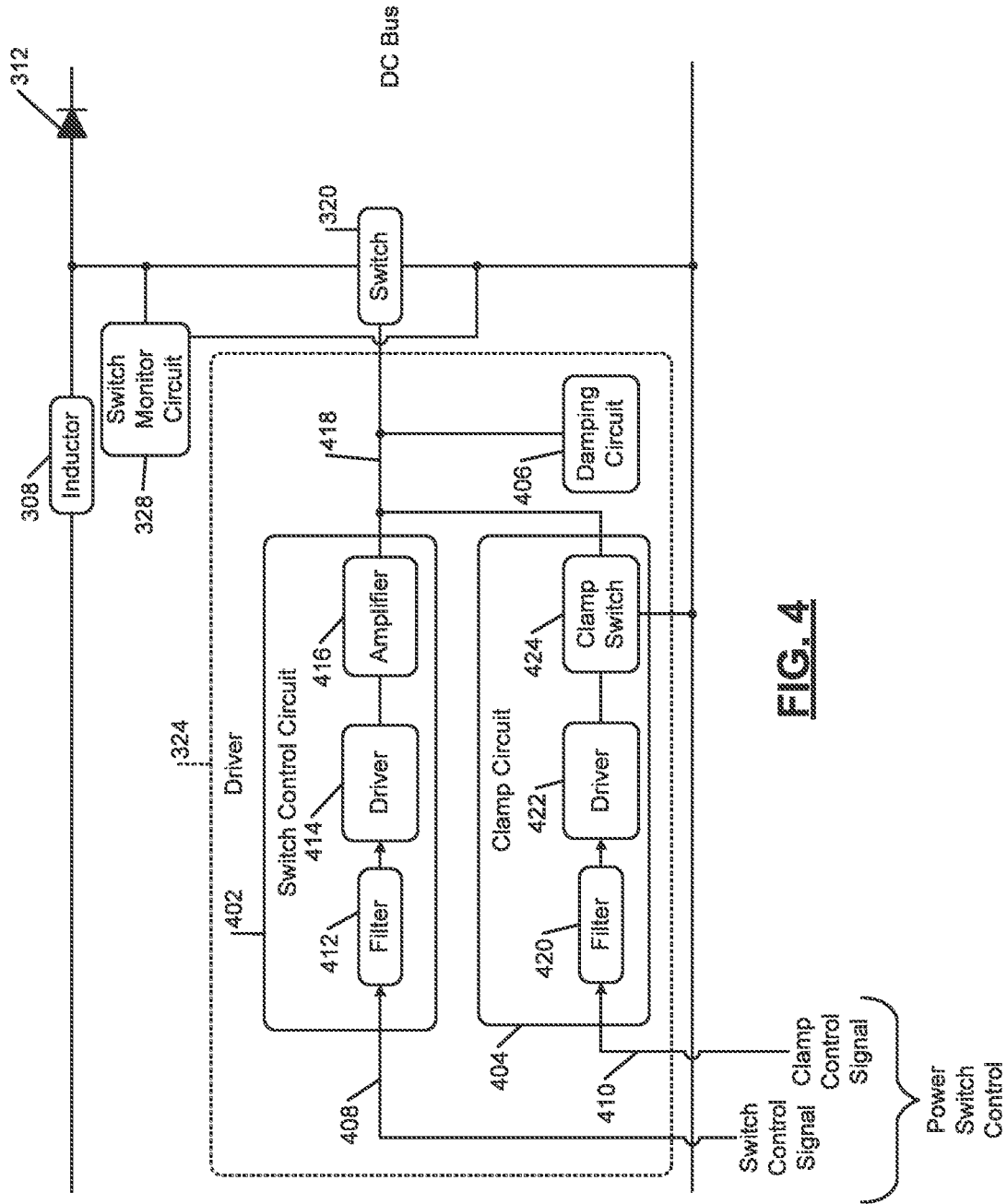


FIG. 4

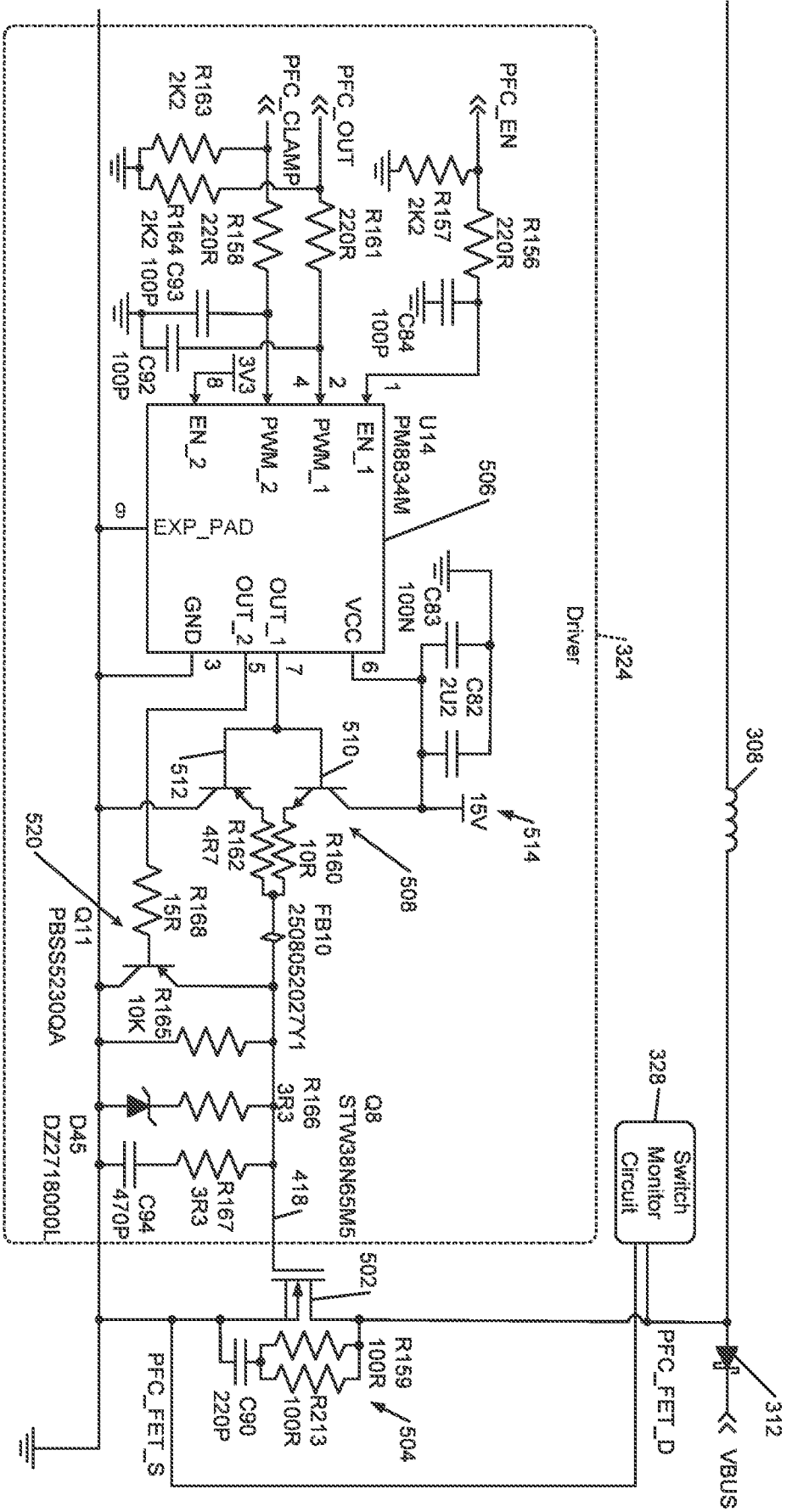


FIG. 5A

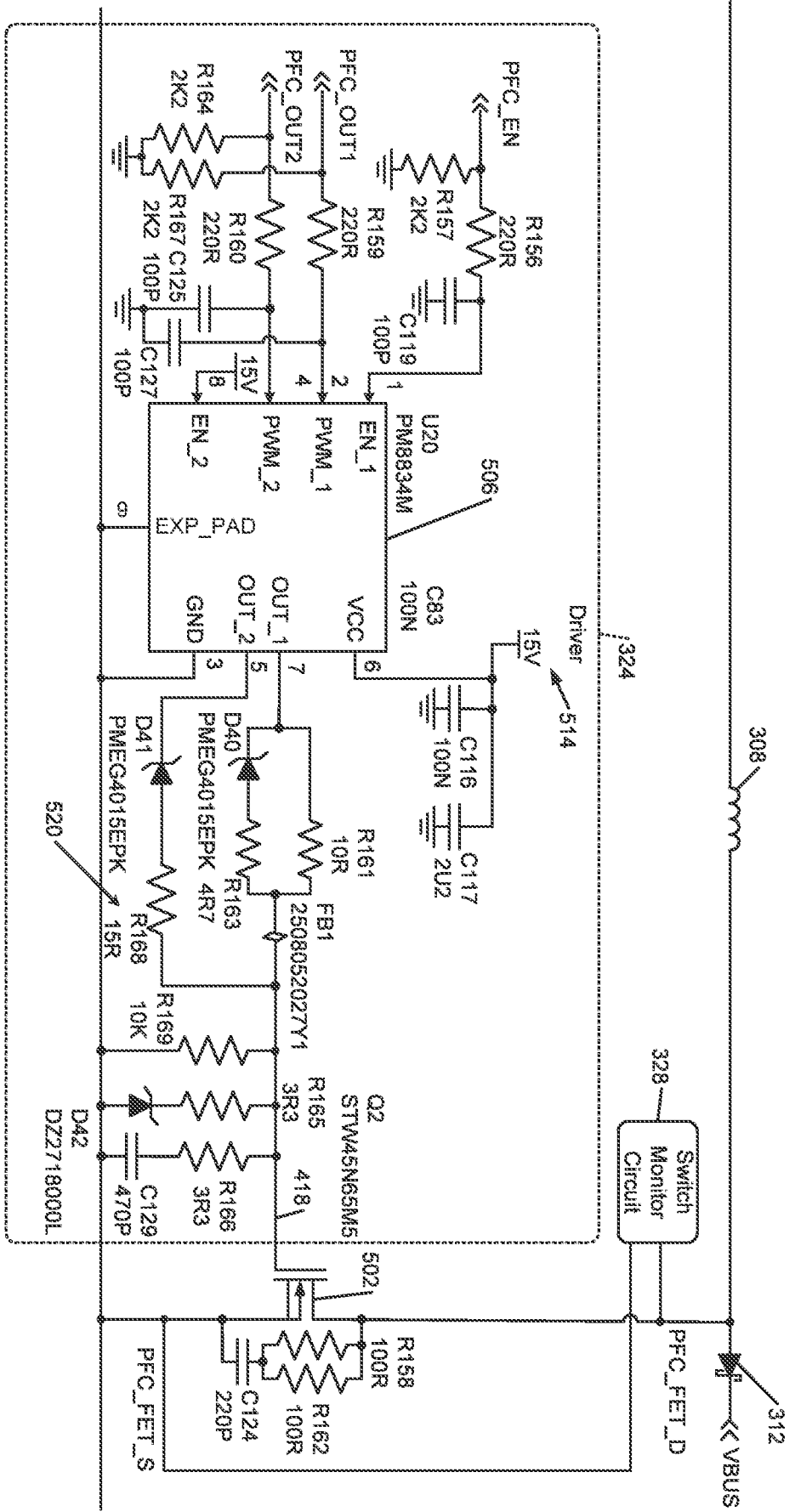


FIG. 5B

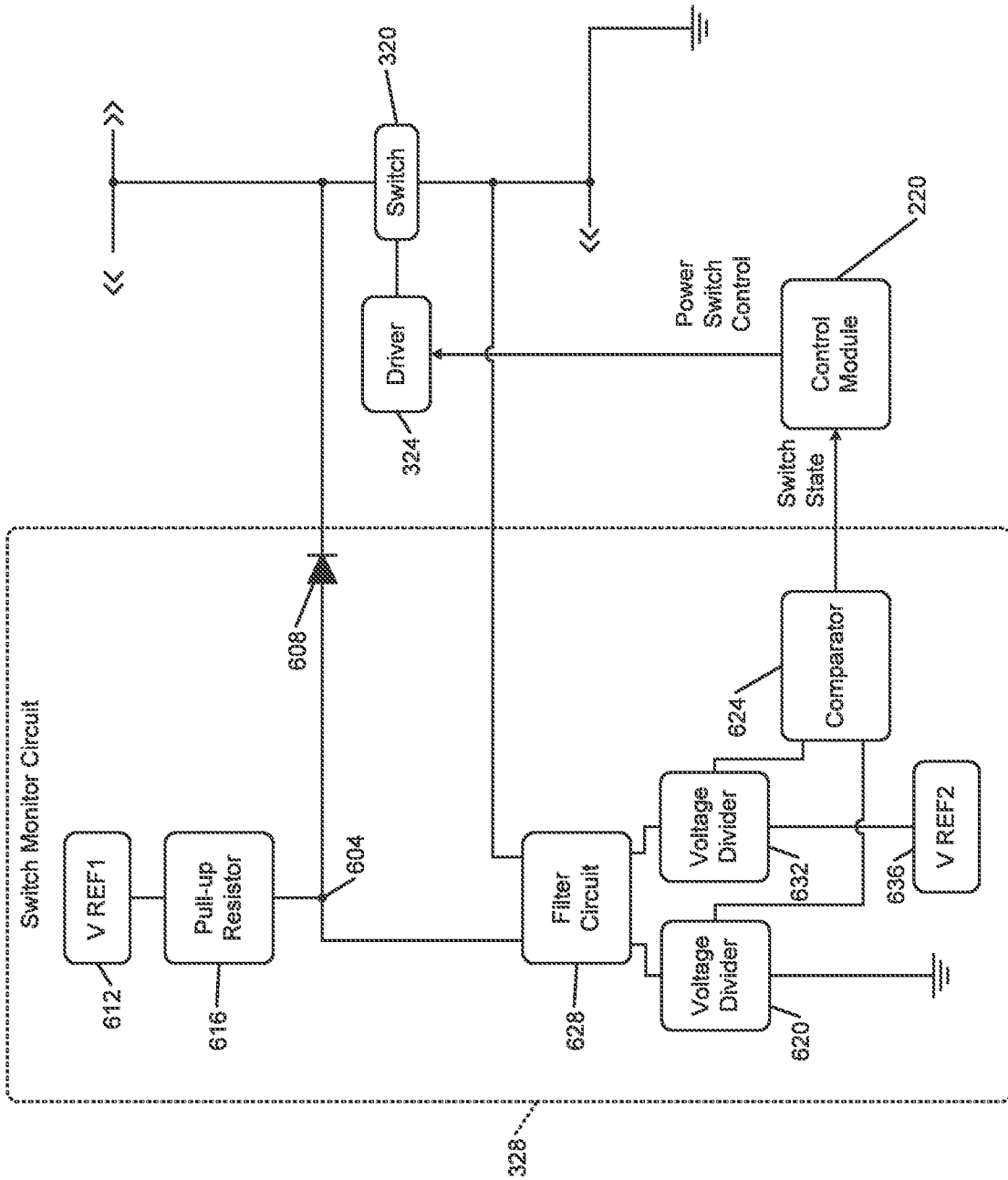


FIG. 6

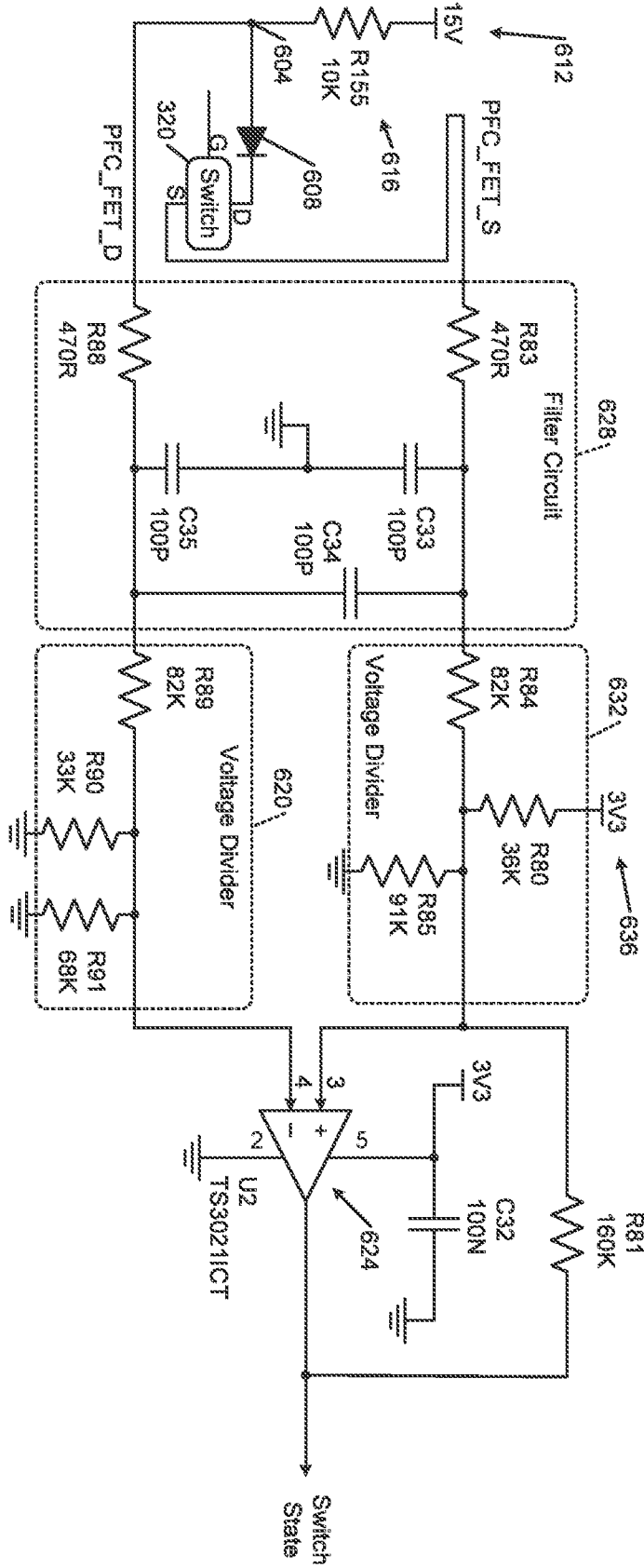


FIG. 7

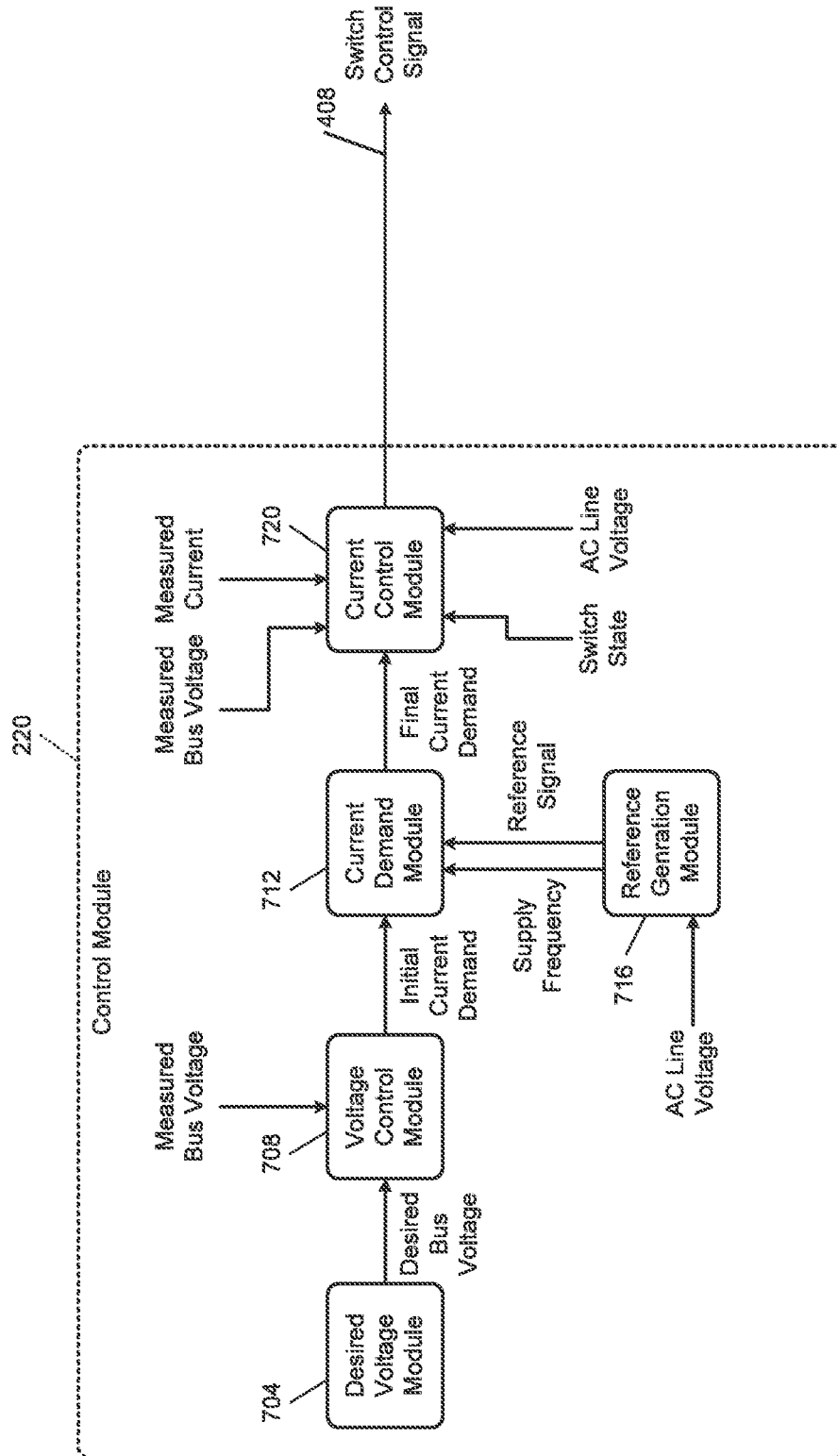


FIG. 8

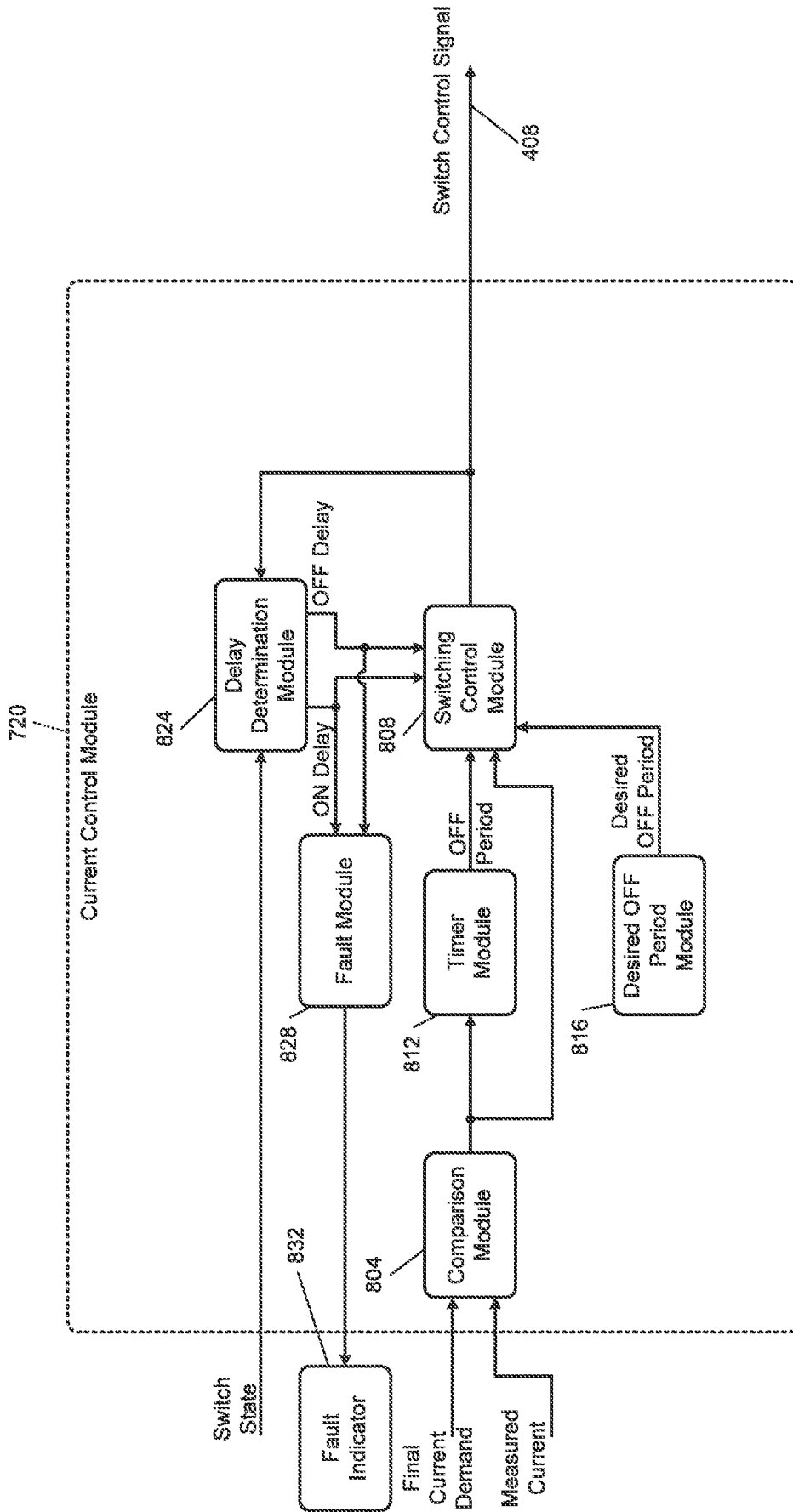


FIG. 9

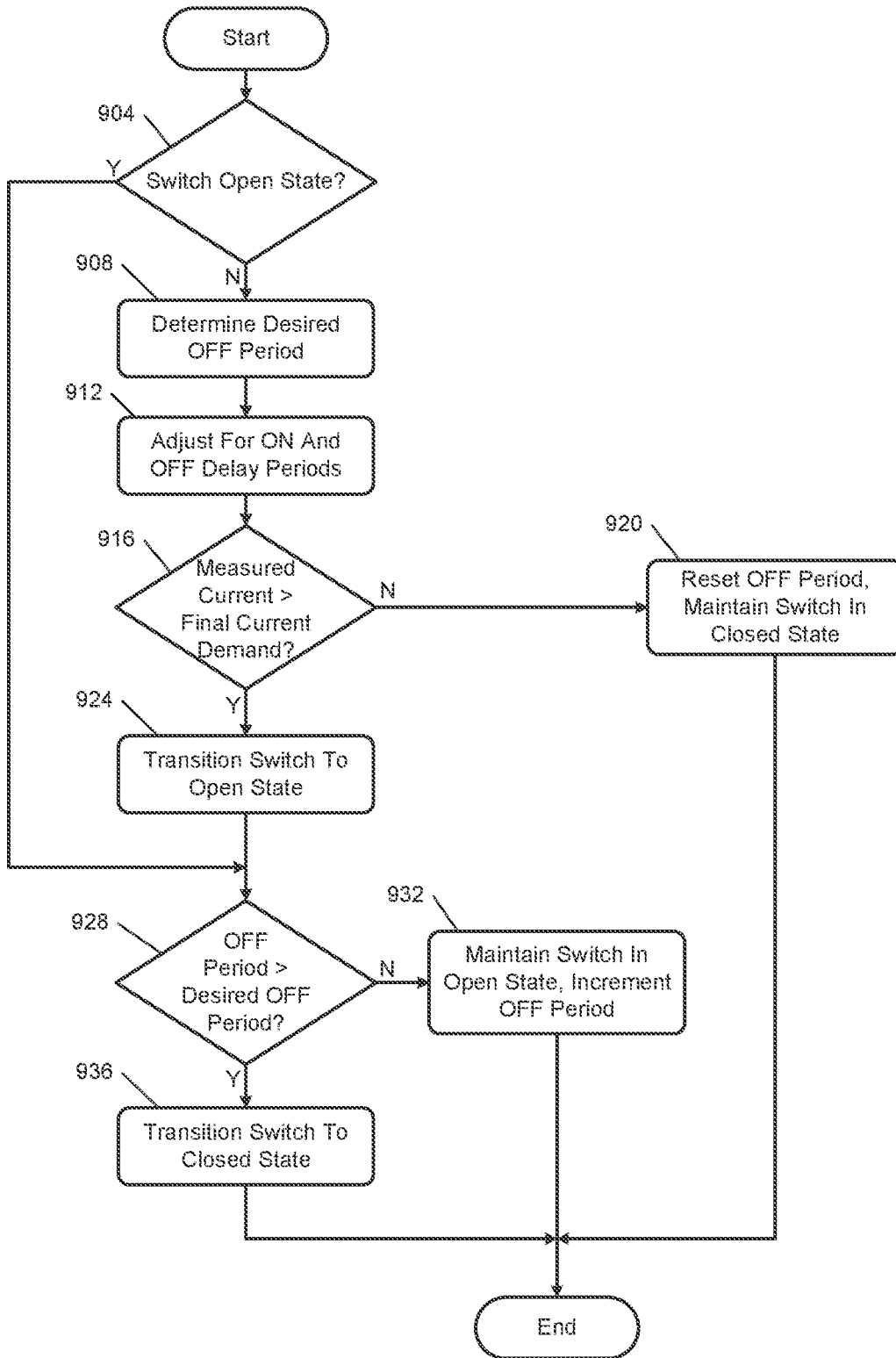


FIG. 10

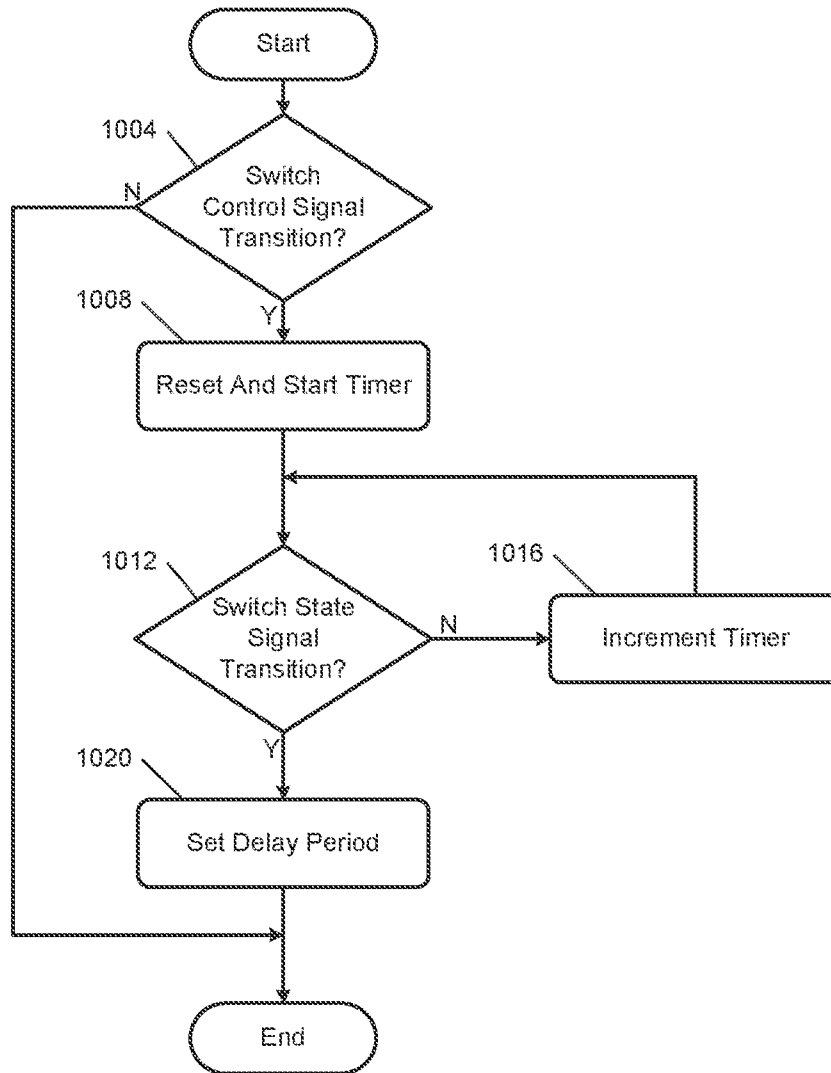


FIG. 11

A. CLASSIFICATION OF SUBJECT MATTER**H02M 1/42(2007.01)i, H02P 27/08(2006.01)i, F04B 49/03(2006.01)i, H02M 1/00(2007.01)j**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02M 1/42; H02M 3/335; E05F 15/20; G01R 31/00; F24F 11/02; G01R 31/02; H01H 9/54; F25B 1/00; H02P 27/08; F04B 49/03; H02M 1/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: inverter, compressor, voltage bus, PFC circuit, control, state

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| Y | AMIT KUMAR SINHA et al., 'SEPIC Based PFC Converter for PMBLDCM Drive in Air conditioning.', In: International Journal of advanced computer Research (ISSN (print): 2249-7277, ISSN (online): 2277-7970), March 2013, Volume 3, Number 1, Issue 8, pages 36-41 See pages 37-39 and figures 1-4. | 1-40 |
| Y | JP 11-237427 A (RINNAI CORP.) 31 August 1999 See paragraphs 18-38 and figures 1-4. | 1-20 |
| Y | US 4437146 A (RALPH F. CARPENTER) 13 March 1984 See column 3, line 11-column 8, line 9 and figures 1-5. | 21-40 |
| A | JP 2006-134607 A (OMRON CORP.) 25 May 2006 See the entire document. | 1-40 |
| A | KR 10-2013-0067440 A (LG ELECTRONICS INC.) 24 June 2013 See the entire document. | 1-40 |

 Further documents are listed in the continuation of Box C. See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

18 September 2017 (18.09.2017)

Date of mailing of the international search report

20 September 2017 (20.09.2017)

Name and mailing address of the ISA/KR

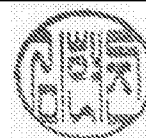
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/027710

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
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| JP 2006-134607 A | 25/05/2006 | JP 4475097 B2 | 09/06/2010 |
| KR 10-2013-0067440 A | 24/06/2013 | KR 10-1331955 B1 | 22/11/2013 |