

[54] CATHODE RAY TUBE STROKE WRITING
USING DIGITAL TECHNIQUES

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[52] U.S. Cl. 340/324 A, 315/18

[51] Int. Cl. G06f 3/14

[58] Field of Search..... 340/324 A; 315/18

[56] **References Cited**

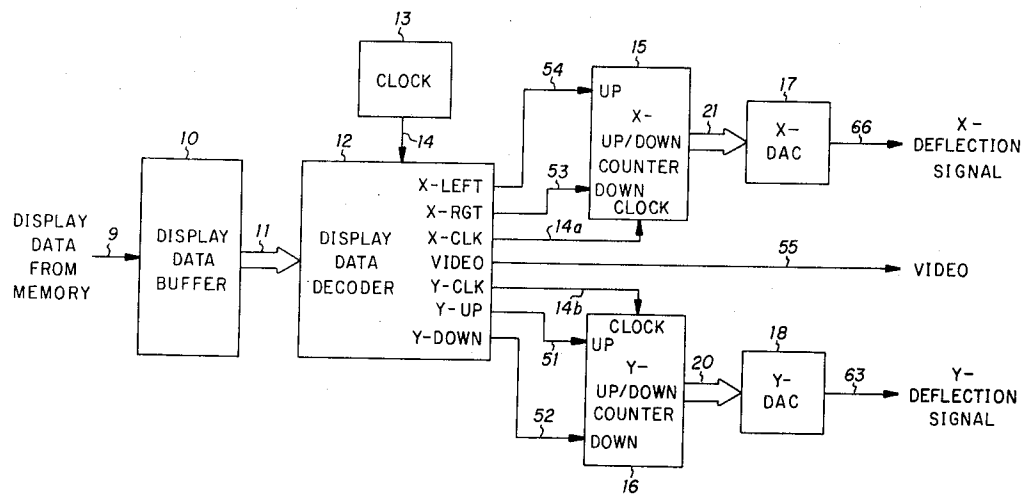
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Primary Examiner—David L. Trafton
Attorney—Richard W. Anderson et al.

[57] **ABSTRACT**

A digitally controlled stroke writing system for displaying a selected imagery on a cathode ray tube defines the imagery as a sequence of straight line strokes of predetermined length and line slope. Each stroke is comprised of plural clock rate defined segments and is commanded by a five-bit binary stroke command word respective bits of which selectively command beam deflection up, down, left, right and video on/off. A pair of binary counters to which a clock defined pulse train is available are caused to count up, down, or hold in response to applied up-down and left-right stroke command word bits, respectively, and develop respective moving digital deflection codes definitive of horizontal and vertical beam deflections. Digital-to-analogue conversion of the running digital deflection codes provides beam deflection signals, while the video on/off command bits of the five-bit binary stroke command words simultaneously control cathode ray tube beam blanking to permit stroke retrace segments within the stroke sequence with maintenance of uniform image brightness. Sloped stroke lines may be selectively defined by control of the ratio of repetition rates of the clock defined pulse trains applied to the respective binary counters.

7 Claims, 9 Drawing Figures



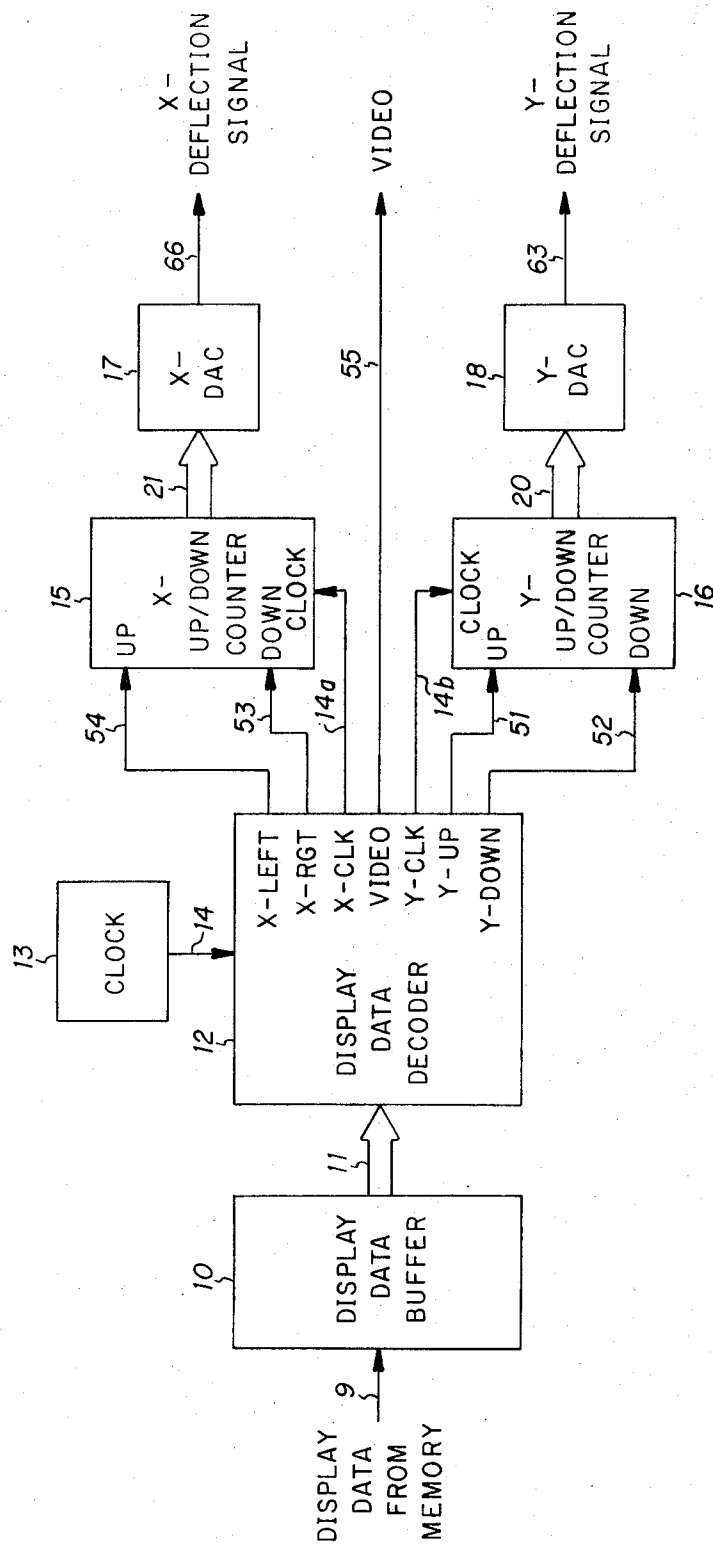
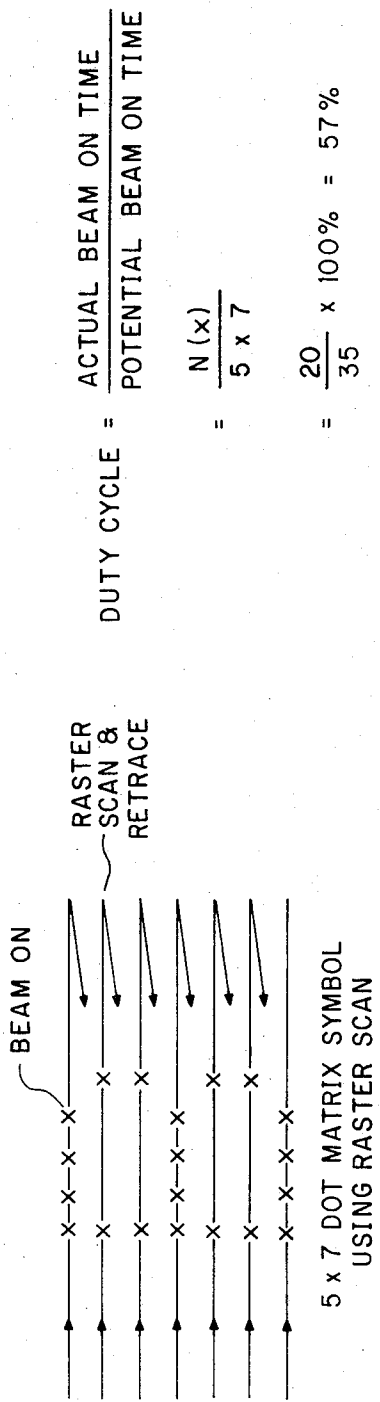
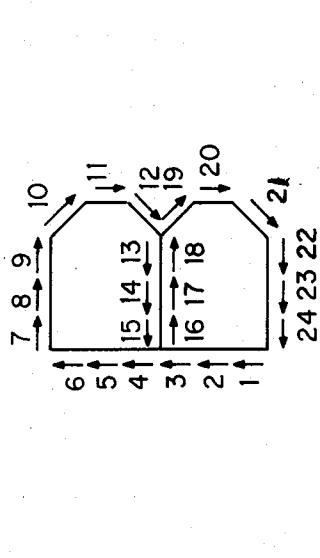


FIG. 1



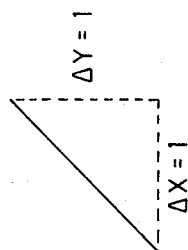
$$\begin{aligned} \text{DUTY CYCLE} &= \frac{\text{ACTUAL BEAM ON TIME}}{\text{POTENTIAL BEAM ON TIME}} \\ &= \frac{N(x)}{5 \times 7} \\ &= \frac{20}{35} \times 100\% = 57\% \end{aligned}$$



$$\begin{aligned} \text{DUTY CYCLE} &= \frac{\text{ACTUAL BEAM ON TIME}}{\text{POTENTIAL BEAM ON TIME}} \\ &= \frac{N(\rightarrow)}{24} \\ &= \frac{21}{24} \times 100\% = 87\% \end{aligned}$$

FIG. 2

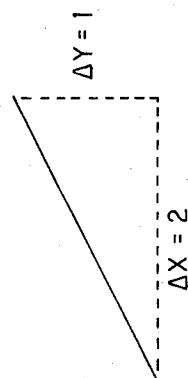
BASE FREQUENCY - 2 MHZ



$$M = \frac{\Delta X}{\Delta Y} = 1$$

$$\therefore \Delta X_f = 2 \text{ MHZ}$$

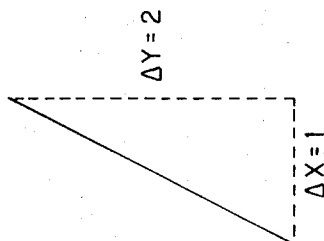
$$\Delta Y_f = 2 \text{ MHZ}$$



$$M = \frac{\Delta Y}{\Delta X} = \frac{1}{2}$$

$$\therefore \Delta X_f = 2 \text{ MHZ}$$

$$\Delta Y_f = 1 \text{ MHZ}$$



$$M = \frac{\Delta X}{\Delta Y} = \frac{1}{2}$$

$$\therefore \Delta Y_f = 2 \text{ MHZ}$$

$$\Delta X_f = 1 \text{ MHZ}$$

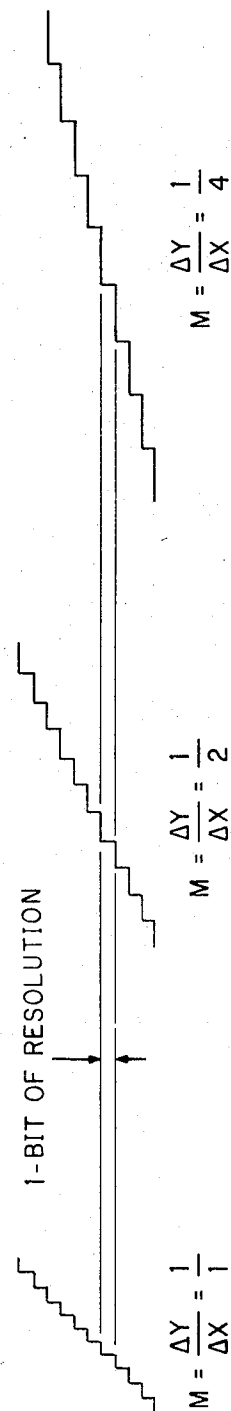


FIG. 3

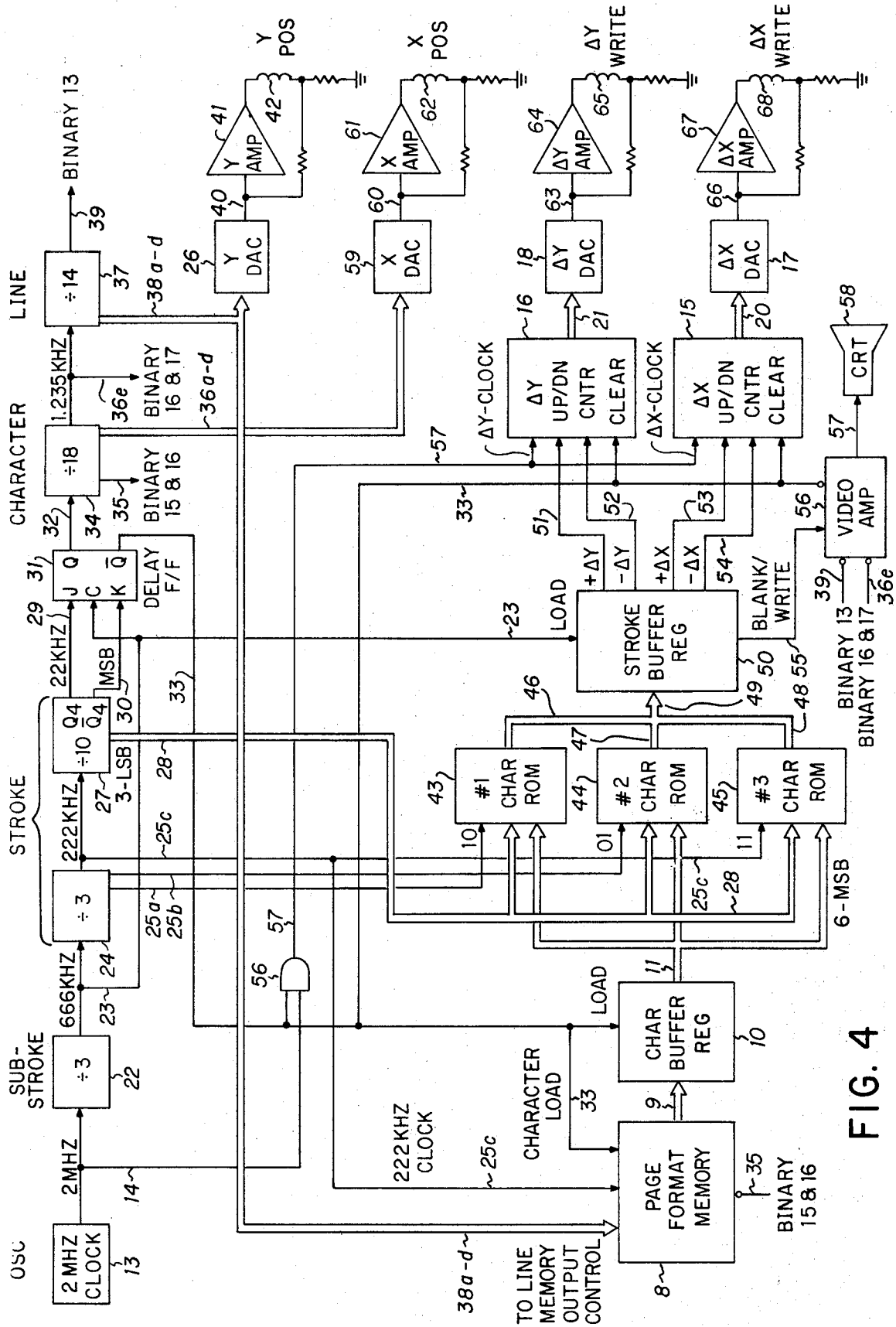


FIG. 4

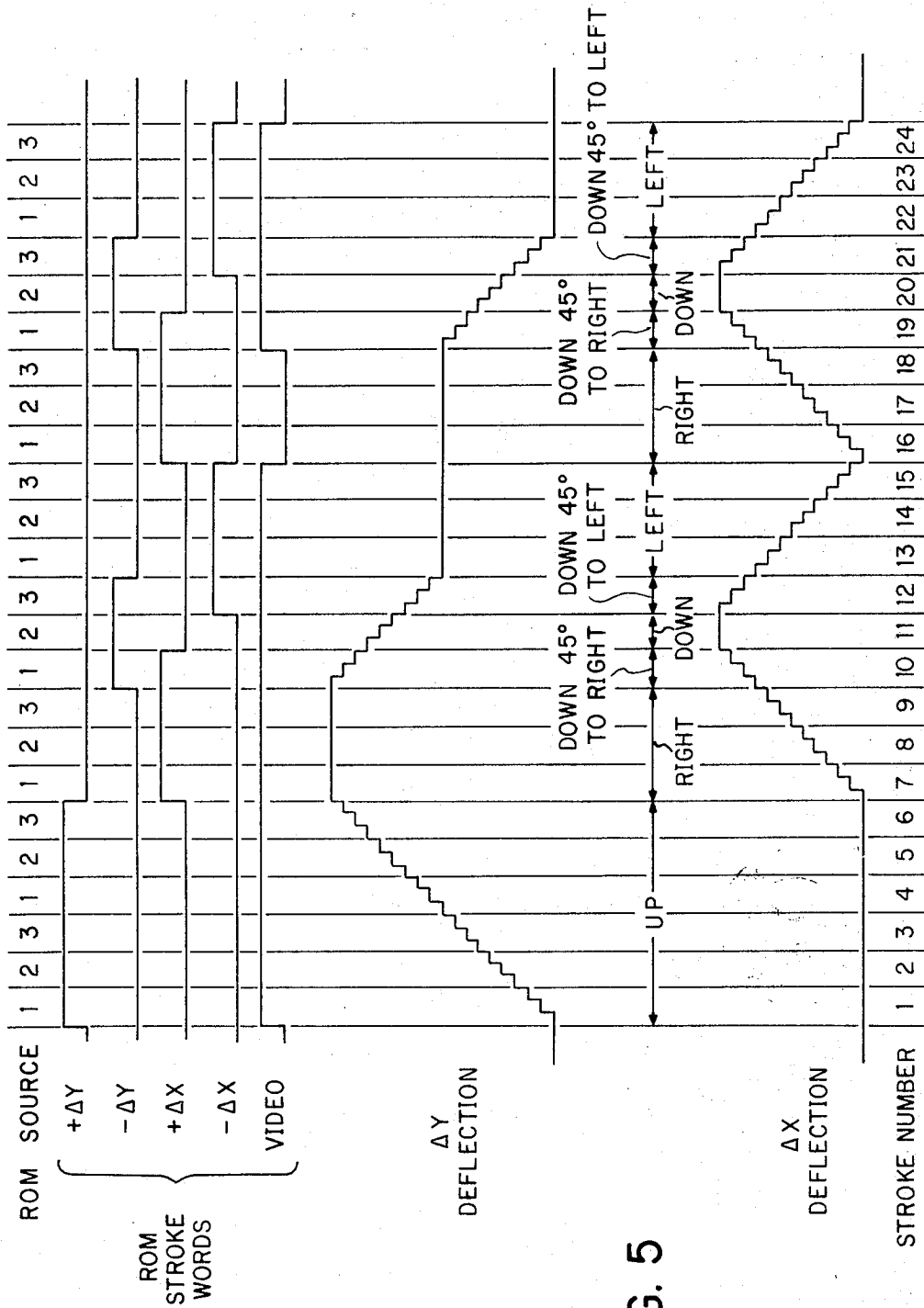


FIG. 5

FIG. 6

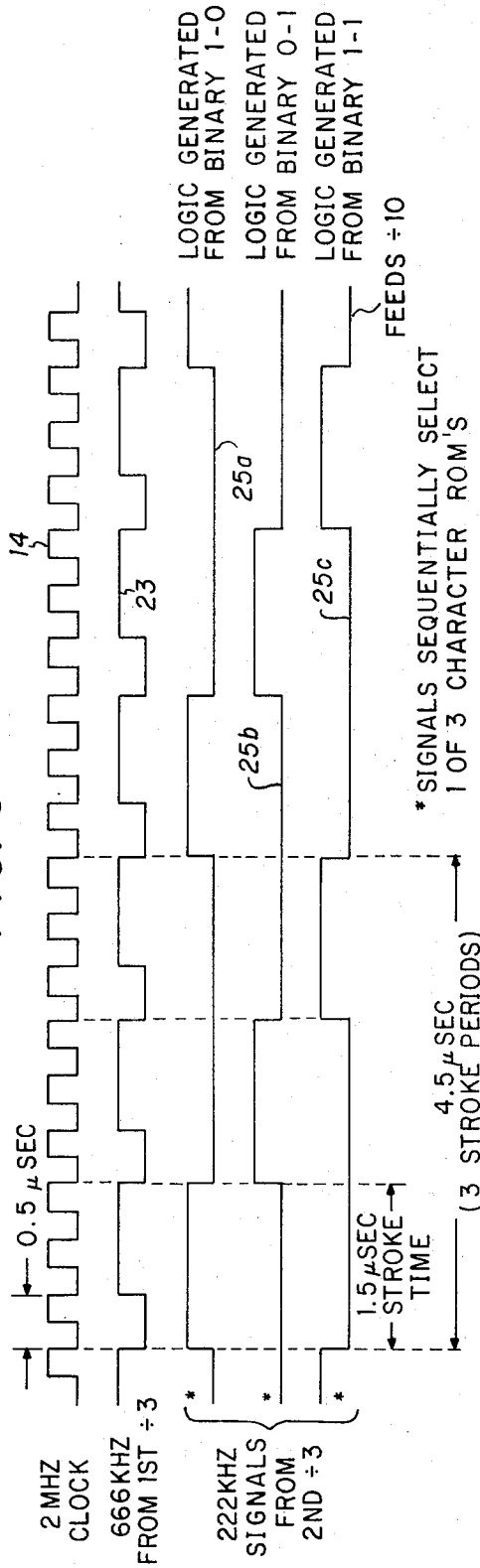


FIG. 7

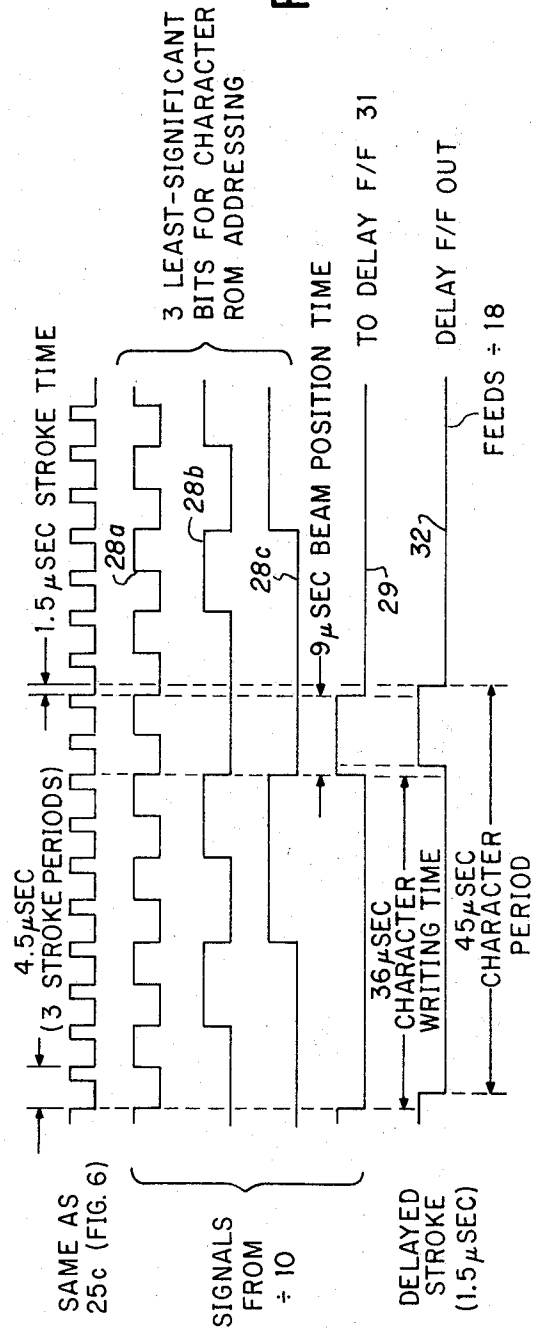


FIG. 8

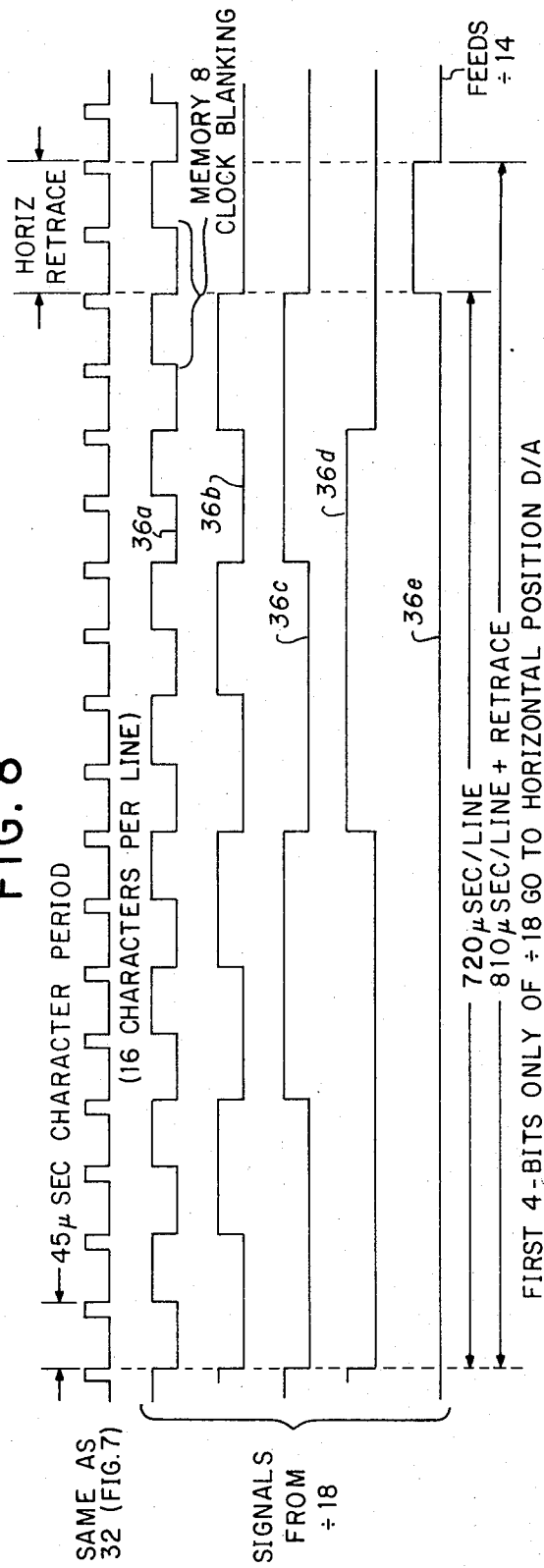
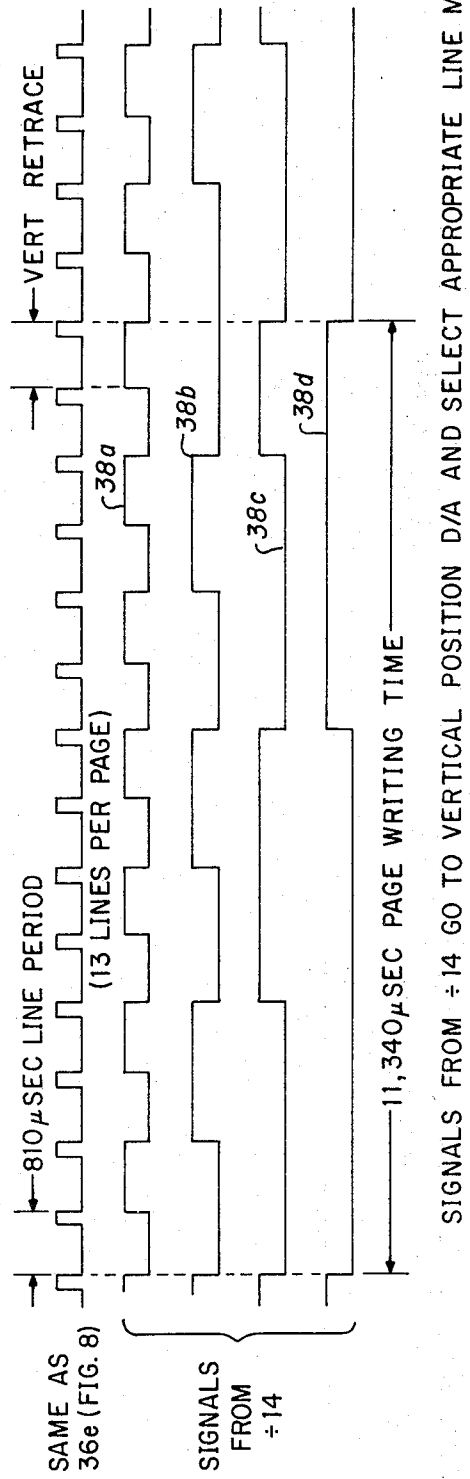


FIG. 9



CATHODE RAY TUBE STROKE WRITING USING DIGITAL TECHNIQUES

GENERAL OBJECT

This invention relates generally to the technique of displaying graphics and alphanumeric symbology on a cathode ray tube screen and more particularly to a digital-stroke writing technique and application thereof by means of which the necessary deflection and video signals required to display graphics and alphanumeric symbology on a CRT screen are realized.

DISCUSSION OF PRIOR ART

The display of graphics and alphanumeric symbology on cathode ray tubes has become increasingly popular and finds wide usage in conjunction with computer operated systems wherein stored information may be recalled from a central memory band and visually displayed for perusal by the operator. The use of cathode ray tube alphanumeric displays is widely employed in airports to provide remote controlled and instantaneously updatable display information concerning flight arrivals, departures, and other data pertinent to the aircraft schedules.

A commonly employed cathode ray tube character display employs a 5×7 dot matrix wherein predetermined permutations of energized dots collectively display selected ones of a predetermined character repertoire. A commonly employed repertoire or character writing capability is 64 characters which allows provision for the alphabet plus the various mathematical symbology. The 5×7 matrix patterns are displayed by use of a character generator which forms voltage patterns of ones and zeros needed to form numbers, letters, and symbols to be displayed on the 5×7 dot matrix. Each of the specific patterns for the repertoire of characters is commonly stored at specific addresses in a read-only memory with each character occupying a 35 bit matrix in the memory. Such systems employ 6-bit address code (the 6 bits define 64 characters) and when the 6-bit address code associated with a particular character is applied to six address lines associated with the read-only memory, the address is decoded by an address decoder that selects the assigned (associated) 5×7 matrix in the memory. With the matrix address completed by selection of a character to be displayed, one of the five columns in the matrix (or conversely one of the five rows in the matrix) is energized and a word of parallel bits corresponding to that particular column or row appears at the output. The five columns (or rows) of the matrix are sequentially energized by a master timing means to provide a five word sequence of seven parallel bits per word for each character which is selected by the address input.

The 5×7 matrix display approach exhibits an inherently low duty cycle since the time that the beam is energized to display or enunciate the dots as compared to the potential beam-on time to display all 35 dots in such a matrix, is considerably lower than, for example, that realized by character generation schemes where the character is actually traced out on the face of the cathode ray tube by deflection control.

Character writers employing stroke writing techniques as opposed to dot matrix energization techniques have an inherently greater duty cycle with an attendant important increase in beam-on time; thus, for a particular desired brightness of image display, stroke

writing systems may employ lower CRT beam currents than those necessary to produce the same brightness of images with raster scan displays.

Known stroke writing displays employ a myriad of complex and necessarily precise analogue ramp generators and function generators by means of which the various beam deflection stroke commands may be formulated in a particular sequence to trace out a selected character on the face of the cathode ray tube. Because analogue function generators inherently suffer from a lack of stability and thus consistently such devices tend with aging of components to produce variations in the form of the character traced by a sequence of function generation strokes, resulting in a display which in some cases may become unreadable.

The present invention, in contradistinction to known CRT character writing devices, employs digital techniques throughout to generate a series of deflection yoke commands on a clock controlled basis which, when taken in sequence, completely trace out a selected character on a CRT screen on a stroke basis. The system to be described herein includes standard digital to analogue converters only to transform output digital data, defining a sequence of strokes to command a given character to be written, into useful analogue signals for use by the deflection system of the cathode ray tube. As such the system to be described provides a brighter, more readable, image and enjoys the consistency and reliability of digital circuitry.

SPECIFIC OBJECTS AND FEATURES

Accordingly, the primary object of the present invention is the provision of a digital system for displaying graphics and alphanumeric symbology on a cathode ray tube wherein the only analogue portion of the system is in the form of a digital-to-analogue converter to transform digital data commanding necessary deflection and video signals required to display selected graphics and alphanumeric terminology into analogue beam deflection signals.

A further object of the present invention is the provision of a cathode ray tube stroke writing system of a type permitting brighter images to be displayed at lower cathode ray tube beam currents than with conventional displays.

A still further object of the present invention is the provision of a cathode ray tube stroke writing system by means of which more readable symbology may be displayed than by conventional dot matrix symbology.

A still further object of the present invention is the provision of a cathode ray tube stroke writing system purely digital in nature as to generating command sequences by means of which characters are displayed and which does not require precision analogue function generators as are employed in conventional stroke writing displays.

A further object of the present invention is the provision of a cathode ray tube stroke writing system by means of which the beam of the cathode ray tube may be caused to trace vertical or horizontal lines in either direction during the deflection sequence defining a selected character to be displayed, and which may produce variable slope beam deflection commands by relative control of vertical and horizontal clock rates rather than by variable slope analogue ramp generators commonly employed in the art.

The present invention is featured in the provision of a purely digital character generating device operating in conjunction with a read-only memory and a master timing system under the influence of a precise system clock. The system generates, for each selected character to be displayed, a sequence of preassigned stroke segments, each segment being comprised of a 5-bit stroke word in the form of $+\Delta Y$, $-\Delta Y$, $+\Delta X$, $-\Delta X$, and write/blank. The five bits provide directional signals to move the beam and write or blank the beam as required. ΔX and ΔY up/down counters divide the selected strokes into three segments, thereby providing a smooth transition from beginning to end of each stroke and from stroke to stroke.

BRIEF DESCRIPTION OF DRAWINGS

These and other objects and features of the present invention will become apparent upon reading the following description with reference to the accompanying drawings in which:

FIG. 1 is a generalized functional diagram of a digital stroke writing system in accordance with the present invention;

FIG. 2 is a diagrammatic representation illustrating comparison techniques conventional dot matrix symbology and the stroke writing technique of the present invention for an exemplified character B;

FIG. 3 is a diagrammatic representation of the line drawing capability of the present invention;

FIG. 4 is a detailed functional block diagram of an embodiment of the present invention as employed for alphanumeric display of 64 characters on a 16 characters per line and 13 lines per page basis;

FIG. 5 illustrates the sequence of 5-bit words which form the character B of FIG. 2; and

FIGS. 6, 7, 8 and 9 represent operational waveforms of the embodiment of FIG. 4.

GENERAL OPERATIONAL CONCEPT

A basic functional block diagram of the digital stroke writing technique of the present invention is illustrated in FIG. 1. Data 9 to be displayed is transferred from some form of memory to a display data buffer 10. Buffer 10 addresses, through paralleled output lines 11, a display data decoder 12 and thus describes to the display data decoder 12 the graphics/symbology to be displayed. A clock 13 supplies a master timing input 14 to the display data decoder 12 to sequence the display data decoder in orderly fashion through the routines necessary to generate the appropriate signals to fulfill the command from the display data buffer.

The display data decoder 12, which might comprise one or more read-only memories (ROM's), is depicted as generating seven discrete signals identified as:

1. deflect beam left
2. deflect beam right
3. deflect beam up
4. deflect beam down
5. vertical clock rate
6. horizontal clock rate
7. video (write/blank on CRT).

The first six signals of the above discrete list are generally utilized to command vertical and horizontal up/down counters depicted as X-up/down counter 15 and Y-up/down counter 16. The outputs 21 and 20 from these respective counters will be seen to represent an exact moving digital deflection code of the trace being

displayed on the cathode ray tube. These digital deflection codes, depicted as paralleled outputs 20 and 21 from the respective counters, are processed by respective digital to analogue converters 17 and 18, depicted as X-DAC and Y-DAC. The digital to analogue converters 17 and 18 convert the moving digital deflection codes (applied from the respective counters) to analogue X and Y beam deflection signals. The video signal 14 from the display data decoder may command the write/blank circuits of the cathode ray tube synchronously with the X and Y deflection signals.

The X-clock and Y-clock outputs 14a and 14b depicted in FIG. 1 as applied as clock inputs of the respective X and Y up/down counters and, as will be further described, determine the relative rates at which the count in the respective counters increase or decreases during the time duration of left-right or up-down commands applied, and thus will collectively define the slope of a straight line segment traced on the cathode ray tube.

GENERAL DIGITAL STROKE WRITING TECHNIQUE

The digital stroke writing technique of the present invention is based upon a predefinition or assignment of a given number of sequentially effected beam strokes to trace out a given character. Reference is made to FIG. 2, which illustrates the previously referenced 5×7 dot matrix symbology as compared to the digitally stroked symbology using the digitally controlled stroke scan of the present invention. With reference to FIG. 2 it is seen that the conventional 5×7 dot matrix symbology employing raster scan provides a duty cycle, in terms of ratio of actual beam-on time to potential beam-on time, of 57 percent. The similarly defined duty cycle of the digitally stroked symbol in accordance with the present invention defines a duty cycle of 87 percent. The dot matrix approach generates dot patterns to define a symbol while the digitally stroked symbol in accordance with the present invention causes the beam to actually trace out the complete character in a continuous fashion. In a detailed embodiment of the invention to be described, each symbol is traced by a maximum of 24 sequential strokes. The stroke sequence tracing out the character B depicted in FIG. 2 illustrates the 24 strokes which may be sequentially effected to trace out the character. It is noted that the stroked character B of FIG. 2, as accomplished by the present invention, causes considerably more phosphor to be energized than is energized in the raster scan method, and thereby readability of the symbol is enhanced. It might be further noted with reference to FIG. 2 that the strokes defining the letter B are comprised of Y-deflection only, X-deflection only, and simultaneous X- and Y-deflection at the same clock rate with relative plus and minus commands to effect positive and negative 45° slopes.

EXAMPLIFIED FORMAT OF STROKE WORK SEQUENCED BEAM DEFLECTION

With reference to FIG. 5, each of the 24 strokes comprising the letter B depicted in FIG. 2 is illustrated in terms of the 5-bit word from the display data decoder. The 5-bit word is comprised of $\pm\Delta Y$ commands, $\pm\Delta X$ commands and a video command (write/blank). Now if the clock rate is defined such that each of the 24 strokes comprising the character B is three clock peri-

ods in length, the Y deflection signal is seen to be comprised of six sequential strokes of $+\Delta Y$ followed sequentially by three $+\Delta X$ strokes, one stroke of combination $-\Delta Y$ and $+\Delta X$, one stroke of $-\Delta Y$, one stroke of combination $-\Delta Y$ and $-\Delta X$, three strokes of $-\Delta X$, three strokes of $+\Delta X$, one combination stroke of $-\Delta Y$ $+\Delta X$, one stroke of $-\Delta Y$, one combination stroke of $-\Delta Y$ $-\Delta X$, and three strokes of $-\Delta X$, to complete the 24-stroke sequence. It is to be noted that each of the strokes comprises three clock periods such that the X and Y deflection signals, which are the analogue of the counts in the respective X and Y counters, are caused to be incremented by step increases or decreases, each deflection signal step defined by a three-count step in the counters. It may further be evidenced from FIG. 5, and with reference also to FIG. 2, that the "video" bit of the 5-bit command emanating from the display data decoder as applied to the counters, commands that video (the CRT beam) be blanked during the retrace defined by strokes 16, 17 and 18 of the character B and, that during the remainder of the strokes the beam is commanded to be "on". Thus the exemplified character B may be written on the cathode ray tube by causing the sequence of 24 5-bit stroke writing commands to be applied to the respective X and Y counters and to the cathode ray tube beam on-off control.

While the deflection current is incremented in step fashion the relative size of the step as compared to the overall size of the character to be traced would be chosen such that the steps are for all practical purposes invisible to the observer's eye. It might further be appreciated that the cathode ray tube may advantageously employ electromagnetic deflection yokes the inductance of which, when considered with the clock rate employed, tend to smooth out the step-current commands.

Reference is made to FIG. 3 which illustrates the general line drawing technique as employed in the present invention.

GENERAL VARIABLE SLOPE STROKING TECHNIQUE

FIG. 3 depicts the general manner in accordance with the present invention by which line segments of various slopes may be traced on the cathode ray tube. The left-hand portion of FIG. 3 depicts equal X and Y clock rates, assumed to be 2 MHz. The slope of the line when ΔX and ΔY , each are 2 MHz becomes unity, thus defining a 45° slope. The actual 45° slope line traced is depicted as the step-like trace in the corresponding lower portion of FIG. 3.

Now, should the X clock rate be chosen as 2 MHz and the Y clock rate be chosen as one-half the X clock rate, or 1 MHz, the slope of the line is seen to be one-half as depicted in the center portion of FIG. 3. Similarly should the Y clock rate be chosen as 2 MHz and the X clock rate be chosen as one-half the Y clock rate or 1 MHz the slope becomes one-fourth, as depicted in the right-hand portion of FIG. 3. Thus by judicious choice of relative clock rates, lines may be displayed at any angle without the need for variable gain or variable slope analogue ramp generators, by digitally controlling the vertical and horizontal clock rates according to the slope $m = \pm \Delta X / \Delta Y$ or the slope $m = \pm \Delta Y / \Delta X$, where the denominator of the slope expression is the base clock frequency. Accordingly while the detailed embodiment of the present invention as herein defined

relates to an alphanumeric display wherein only 45° slopes are necessary to define characters and thus the X and Y clock rates may be one and the same, in general, the present invention provides a means for digitally effecting stroke writing of any predetermined symbol or representation by dividing the symbol into predetermined line segments each of which may be defined by a particular slope in terms of ΔX and ΔY and effecting control of clock rates accordingly. Thus for example a map might be traced out by defining the map display in terms of a sequence of strokes each one of which defines a straight line segment of predetermined length and slope. Thus although the present invention will be described in detail as an alpha-numeric character display embodiment wherein a common clock rate is used and the system is synchronous in nature, it is not to be so limited in that the technique is extendable in the general case to generating moving digital commands in the form of counts in X and Y deflection clocks which in turn may be applied to digital to analogue converters to develop beam deflection signal sequences to accomplish stroke writing of any desired symbology on the face of a cathode ray tube.

GENERAL DESCRIPTION OF ALPHANUMERIC DISPLAY EMBODIMENT

In the alphanumeric display to be described wherein only $\pm 45^\circ$ slope segments are employed, each of 64 characters to be displayed are preassigned a number of sequential strokes (not exceeding 24) whereby the beam is caused to deflect vertically, horizontally and at 45° slopes to complete the tracing of the character. As will be further described a digital base clock controlled master timing system may cause the beam to be affixed or positioned to predetermined successive start positions for each one of successive characters to be displayed. From each character start position the X and Y counters may be commanded to cause the beam to follow the particular stroke segments assigned to the character. The digital master timing system may further effect necessary video blanking between characters, between the end of one line of characters and the beginning of a succeeding line of characters, and between the last character of the last line of the display and the repeat of the display sequence at the first character position of the first line of the display. The embodiment to be described in detail is a specific application of the general operational concept of the invention of controlling X and Y deflection counters from which analogue X and Y deflection signals may be established for beam deflection along with a control of the beam current per se (on/off) under the control of a digital stroke defining words read out of a display data memory such that the cathode ray beam deflection is caused to follow or trace out a predetermined alphanumeric character or other type of display which may be defined as a time position sequence of line segments having predetermined slopes.

DETAILED DESCRIPTION OF ALPHANUMERIC DISPLAY EMBODIMENT (FIG. 4)

An embodiment of the present invention in the form of a digitally controlled stroke writing system for the display of 64 distinctly different alphanumeric characters is depicted in FIG. 4. The system of FIG. 4 operates on the basis of each of 64 different display characters each being defined by a maximum of 24 sequential

beam stroke commands. Each of the 24 beam strokes is in turn defined by the count carried in each of X and Y counters the outputs of which are converted to analogous beam deflection signals. The system of FIG. 4 includes a read-only memory which may be addressed to supply the 24 stroke segments stored therein for a selected one of the 64 possible characters. The X and Y counters are supplied inputs at a common system clock rate and caused to count up, count down, or maintain status quo by $\pm\Delta X$ and $\pm\Delta Y$ input commands defined by the 24 segment storage for a selected character. The system further comprises a master timing means comprised of digital dividers operated in cascade fashion under control of the master system clock to provide X and Y beam position signals necessary to move the beam to a new starting point for each successive character to be written on a given line, and to cause the sequential characters to be conventionally displayed line by line.

It is to be emphasized that the embodiment to be described is entirely digital in nature to the extent that it develops, within X and Y counters, moving digital deflection codes. These moving digital deflection codes developed in the X and Y counters are then converted to corresponding beam deflection currents to cause the beam to trace out the symbology on the cathode ray tube.

With reference to FIG. 4 an alphanumeric digitally controlled stroke writing system embodiment is depicted wherein any one of 64 characters may be displayed in any one of 16 character positions on any one of 13 display lines. The display thus consists of a "page" comprised of 13 lines with provision for 16 selected characters per line. For purpose of description of the embodiment, a memory 8 is depicted as supplying an input 9 to a character buffer register 10.

Memory 8 might comprise any one of a number of memory implementations by means of which a predetermined "page" to be displayed is stored along with timing and control means to synchronize readout of the stored page of information with the character and line positions on the CRT display. Thus memory 8 might comprise an input keyboard along with a read-in and read-out control circuitry to control a line memory with associated input and output controls and a line memory clock control. The output 9 from the memory 8 may, for purposes of the present description, be considered to be comprised of a source of sequential parallel 6-bit character addressing words time-synchronous with character and line positions of the display. Thus, the output 9 from memory 8 for any given character would comprise 6 parallel binary bits effective in addressing 2^6 or 64 different character words in the ensuing character memory portion of the display circuitry. The output 11 from character buffer register 10 is thus comprised of a sequence of paralleled 6-bit character address words related to the sequence of characters to be displayed.

The display data decoder of FIG. 1 is embodied in the alphanumeric 64 character writer embodiment of FIG. 4 as a read-only memory means which, in response to each 6-bit character address and further address sequencing from the system master timing means, provides 24 sequential output character stroke words each stroke of which is comprised of 5 bits in terms of $\pm X$ and $\pm Y$ deflection and video on/off control as previously described.

For a 64 character repertoire in a system employing 24 strokes per character, the read-only memory requirement becomes 1,536 stroke words. Each character word would be comprised of 24 stroke words of 5 bits each to accomplish the cathode ray tube beam deflection. While the read-only memory portion of the embodiment of FIG. 4 might then be comprised of a single memory containing 1,536 words of 5 bits each (64×24), the read-only memory in the embodiment of FIG. 4 is embodied as three separate read-only memories of 512 words each, which, under the addressing control of the 6-bit input addressing from character buffer register 10 and additional sequencing address control from the system master timer (to be further described in detail), generate the 24 stroke sequence of 5-bit code words to effect writing of a particular one of the 64 words in the character repertoire of the system.

Thus, in the writing of the above exemplified character B, the output 49 from the trio of read-only memories 43, 44, and 45, under the control of the character addressing from buffer register 10 and timing input controls from the master timer, provide a sequence of 24 stroke words of 5-bits each as previously described with reference to FIG. 5. The outputs 46, 47, and 48 from ROM's 43, 44, and 45 are depicted as being OR'd as a common output 49 supplied to a stroke buffer register 50, the latter acting as a high speed interface between the low frequency characteristics of MOS-ROM's which might be employed and the high speed up/down counters to which the 5-bit character stroke words are applied as controlling inputs. Thus stroke buffer register 50 supplied outputs 51 and 52 as respective count-up ($+\Delta Y$) and count-down ($-\Delta Y$) control inputs to a ΔY up/down counter 16. Stroke buffer register 50 also supplies outputs 53 and 54 as respective count-up ($+\Delta X$) and count-down ($-\Delta X$) inputs to a ΔX up/down counter 15. The clock input 57 to each of the ΔY and ΔX counters is provided as the output from an AND gate 56 through which 2 MHz clock pulses 14 from master clock 13 are gated under control of stroke counter output from the system master timing means.

The counters 15 and 16, under the control of the $\pm\Delta X$ and $\pm\Delta Y$ input pairs thereto, develop counts which are digital representations of respective X and Y beam deflection signals effective to write the sequential strokes assigned to a particular character. The count outputs 20 and 21 from the counters 15 and 16 are applied to associated ΔX and ΔY digital-to-analogue converters 17 and 18 such that the output 63 from ΔY converter 18 comprises an analogue deflection current for amplification by ΔY amplifier 64 and application to the ΔY -write yoke winding 65 of the cathode ray tube 58 of the system. Similarly the output 66 of the ΔX digital-to-analogue converter 17 is a current analogue of the count contained within the counter at any instant and is applied for amplification in ΔX amplifier 67 for application to the ΔX -write yoke winding 68 of the cathode ray tube 58.

Since the page format input information from memory 8 is in the form of sequential 6-bit character addresses which in turn are sequenced as to line-position and line to define a "page" to be displayed on the cathode ray tube 58, the system of FIG. 4 includes a unique master timing sequence which provides the timing control for character addressing, buffer register loading, and clock gating to the counters as well as developing digital counter outputs which, after application to asso-

ciated digital-to-analogue converters, provide Y-position and X-position analogue currents for the CRT beam. The X-position and Y-position outputs are utilized for character selection and character position on a given line, and for line positioning per se while the outputs from the ΔX and ΔY up/down counters effect the actual 24 stroke sequence to write a given character. Thus the X-position and Y-position deflection current outputs place the beam in a given reference or "start" position from which the ΔX and ΔY deflection current sequences trace out the stroke sequence to display the character.

MASTER TIMING WAVEFORMS — (FIGS. 6-9)

The operation of the system may best be comprehended by an analysis of the master timing sequence under the control of the master 2-MHz clock 13 of the system, in which certain timing waveforms are digitally developed to complete the necessary character address sequencing in the read-only memory along with synchronized video retrace blanking to arrive at a continuous "page" display.

With reference to FIG. 4, a 2-MHz output 14 from 2-MHz master clock 13 is applied to a $\div 3$ "sub-stroke" counter 22. The output 23 from sub-stroke counter 22 is applied as input to a further $\div 3$ counter 24. The output from $\div 3$ counter 24 is applied as input to a $\div 10$ counter 27. Counters 24 and 27 operate collectively as a "stroke" counter. The Q output 29 of $\div 10$ counter 27 is applied to a delay flip-flop 31 which provides an output 32 as input to a subsequent $\div 18$ "character" counter. The output from $\div 18$ counter 34 is applied as input to a $\div 14$ "line" counter 37. As will further be described, certain significant bit outputs from the above defined counter chain provide all necessary timing arrangements to effect character addressing in the system along with character position control, line control of the write-out, and the necessary retrace video blanking in the system.

MASTER TIMING ADDRESSING (FIGS. 6-7)

With reference to the character ROM addressing of FIG. 4 and operational waveforms of FIG. 6, the manner in which the three read-only memories are table addressed and word sequenced to provide 24 5-bit stroke output words to write a given character will first be discussed.

FIG. 6 depicts the 2-MHz clock output 14 being divided by three to provide the output waveform 23 from "sub-stroke" counter 22. The subsequent $\div 3$ counter 24 would be embodied as a 2-bit counter with appropriate logic so as to develop or provide the time sequential outputs 25a, 25b, and 25c depicted in FIG. 6. Output 25a from counter 24 is developed from appropriate logic circuitry in response to the first binary count of 1-0. Output 25b from the counter is developed in response to a counter count of 0-1, while counter output 25c is developed in response to a count of 1-1 in the two-bit counter 24.

Now, with reference to FIG. 4, output 25a of counter 24 is applied as an addressing input to a first character ROM 43. Output 25b from counter 24 is applied as a character addressing input to the second ROM 44. Output 25c from counter 24 is applied as a character addressing input to the third character ROM 45. All three of the character ROM's 43, 44, and 45 are simultaneously addressed by the 6-bit parallel addressing word

11 applied from character buffer register 10. A sequencing input 28 is also applied simultaneously to each of the three character ROM's 43, 44 and 45. The sequencing input 28 is comprised of paralleled inputs corresponding to the three least-significant bits of the $\div 10$ counter 27 to which the output 25c of the $\div 3$ counter 24 is applied as input. Reference is made to FIG. 7 which depicts binary output waveforms of the $\div 10$ counter 27 and identifies the three least-significant bits of the available output therefrom which define eight distinct binary counts (1-7) utilized for character ROM addressing (addressing input 28 to the ROM's 43, 44, and 45 of FIG. 4).

It might be noted here that the time base for the waveforms of FIG. 7 is reconstructed as is the time base of the successive operational waveforms of FIGS. 8 and 9, since the timing waveforms are based on successive cumulative divisions of the master 2 MHz clock and therefore cannot be readily displayed on the same time base for illustration purposes.

Now considering the outputs 25a, 25b and 25c from the $\div 3$ counter 22, as depicted in FIG. 6, along with the three least-significant bit outputs from the $\div 10$ counter 27 as depicted in FIG. 7, we shall consider the manner in which the ROM's are addressed.

Each of the three ROM's 43, 44 and 45 may be designed to be comprised of 64 addressable tables or groups of 8 stroke words each. Each of the 64 groups of 8 stroke words is associated with a particular one of the 64 characters in the system repertoire. Thus the character address (the 6-bit output 11 from the character buffer register 10) may be applied simultaneously to each of the character ROM's 43, 44 and 45 to address (alert) a particular table of 8 stroke words in each of the ROM's. The character addressed tables of 8 in each of the three ROM's collectively define the format of the character to be displayed in terms of $\pm X$ deflection, $\pm Y$ deflection and video (CRT write/blank). Once the ROM's are character addressed (an 8-word group in each ROM) the $\div 3$ and $\div 10$ counters, within the master timer, sequence through the ROM's to call up 24 sequential character segments (stroke words) for display. The segments are defined by two ROM addressing bits from the $\div 3$ counter and three ROM addressing bits (the three least-significant bits) from the $\div 10$ counter. The two addressing bits from the $\div 3$ counter allow up to three distinct ROM groups to be addressed and the three addressing bits from the 10 counter allow up to eight distinct ROM words within each group to be sequentially addressed, thereby allowing up to 24 ROM words to be addressed for each symbol work loaded into the character buffer register from page format memory 8.

To illustrate the manner in which this addressing is accomplished, reference is made to Table 1 below which represents a truth table for the above-referenced character B by means of which the 8-word groups in the three ROM's assigned to the character B may be definitized. Table 2 illustrates the 24 sequential strokes by means of which the character B will be written along with the corresponding ROM group address, the ROM word within the group address and the 5-bit stroke word which must be read out of the composite read-only memory system for application to the counters and the video control of the cathode ray tube. Reference is made again to FIG. 2 and FIG. 5 of the drawings wherein the 5-bit ROM words are defined for the 24

stroke sequence for writing the character B. Now considering the operational waveforms of FIGS. 6 and 7 along with the truth table of Table 1 and the graphics concerning the writing of the character B in FIGS. 2 and 5, it may be seen that the 6-bit character address from the character buffer register 10 addresses a predetermined group of eight stroke words in each of the three ROM's, which in Table 2 are depicted as 1, 2 and 3, respectively corresponding to ROM registers 43, 44 and 45 in FIG. 4. Each of the

plication to the stroke buffer register, one may rewrite the truth table as concerns the character letter B in the form depicted in Table 2 to illustrate the 8-word group in each of the ROM's assigned to the character B. The sequential readout as concerns Table 2 is seen to be the first word from ROM 1 followed respectively by the first words from ROM's 2 and 3, followed by the second word in sequence from each of the ROM tables, followed by the third word in sequence from each of the ROM tables, etc. It is to be realized that Tables 1

TABLE 1.—TRUTH TABLE FOR CHARACTER "B" FOR 8 WORD GROUPS IN ROM'S ASSIGNED "B"

Stroke No.	ROM address	ROM word group	Stroke word (5-bits)				
			$+\Delta Y$	$-\Delta Y$	$+\Delta X$	$-\Delta X$	V
		Address	Up	Down	Right	Left	On
1	1	1	1	0	0	0	1
2	2	1	1	0	0	0	1
3	3	1	1	0	0	0	1
4	1	2	1	0	0	0	1
5	2	2	1	0	0	0	1
6	3	2	1	0	0	0	1
7	1	3	0	0	1	0	1
8	2	3	0	0	1	0	1
9	3	3	0	0	1	0	1
10	1	4	0	1	1	0	1
11	2	4	0	1	0	0	1
12	3	4	0	1	0	1	1
13	1	5	0	0	0	1	1
14	2	5	0	0	0	1	1
15	3	5	0	0	0	1	1
16	1	6	0	0	1	0	0
17	2	6	0	0	1	0	0
18	3	6	0	0	1	0	0
Blank for 16-18 retrace requirement							
19	1	7	0	1	1	0	1
20	2	7	0	1	0	0	1
21	3	7	0	1	0	1	1
22	1	8	0	0	0	1	1
23	3	8	0	0	0	1	1
24	3	8	0	0	0	1	1
$\div 3$ counter addressing (sequential)			3-LSB of $\div 10$ counter addressing (sequential)				

ROM's would have sixty-four groups of eight stroke words each, with one particular group of the 64 in each of the ROM's being assigned to the character B and simultaneously addressable by the 6-bit address from character buffer register 10. Like positioned words (i.e., word 1, word 2, word 3, etc.) of each of the eight words in the selected groups are sequentially addressed by the three least significant outputs from the $\div 10$ counter. For this purpose, although not specifically depicted, it is to be understood that the ROM's 43, 44 and 45 would have addressing logic circuitry responsive to the binary output defined by the three least significant bits of the $\div 10$ counter to effect a sequencing address of the eight words within the group as a function of the count contained in the $\div 10$ counter. During each of the sequential addresses of the eight words within the group assigned to the addressed character, a stroke readout of five bits is sequentially read from each of the three ROM's under control of the sequential gating waveforms 25a, 25b and 25c from the $\div 3$ counter 24. Table 1 depicts eight groups (of three read-outs each) to define the 24 strokes for the addressed character B.

Now considering the 24-stroke sequence truth table of Table 1 as concerns the 5-bit memory output for ap-

and 2 depict the truth tables of 5-bit words stored in the read-only memories for only the character B, and that each of the ROM's would include 64 groups of eight 5-bit words each, with a first one of the groups in each of the ROM's being assigned a

TABLE 2

ROM 1 — Group "B" Table

ΔY	$-\Delta Y$	ΔX	$-\Delta X$	V
1	0	0	0	1
1	0	0	0	1
0	0	1	0	1
0	1	1	0	1
0	0	0	1	1
0	0	1	0	0
1	1	1	0	1
0	0	0	1	1

ROM 2 — Group "B" Table

ΔY	$-\Delta Y$	ΔX	$-\Delta X$	V
1	0	0	0	1
1	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	0	0	1	1
0	0	1	0	0
0	1	0	0	1
0	0	0	1	1

ROM 3 — Group "B" Table

ΔY	$-\Delta Y$	ΔX	$-\Delta X$	V
1	0	0	0	1
1	0	0	0	1
0	0	1	0	1
0	1	0	1	1
0	0	0	1	1
0	0	1	0	0
0	1	0	1	1
0	0	0	1	1

first character, the second one of each of the eight word groups in the three ROM's being assigned a second character, etc. In this manner it is seen that eight groups of three readouts to define 24 sequential strokes for any one of 64 addressed characters may be provided from the read-only memory system.

With further reference to FIG. 7, the most-significant bit output 29 from the $\div 10$ counter 27 defines a 36-microsecond character writing time followed by a 9-microsecond beam position time. As will be further described, a beam position time is necessary to effect a positioning of the beam to the starting point of a successive character to be written on the cathode ray tube. The 36-microsecond character writing time is seen to be defined as eight 4.5 microsecond periods each of which corresponds to three 1.5 microsecond stroke periods. Reference to FIG. 6 illustrates that each stroke period or stroke time of 1.5 microseconds comprises three clock periods of 0.5 microsecond. Thus the output 29 (the most-significant bit output) from the $\div 10$ counter 27 uniquely provides a timing base for character writing time as well as an ensuing 9-microsecond period of time during which the beam may be repositioned for the start position of a succeeding character to be written. FIG. 7 further illustrates that the time period for a particular character may be defined as the sum of the 36-microsecond character writing time and the 9-microsecond beam position time.

The most-significant bit output 29 from the $\div 10$ counter is applied through a delay flip-flop 31 with the output 32 therefrom feeding the succeeding character counter 34. The output 32 from the delay flip-flop is delayed one stroke (1.5 microseconds) to allow the last stroke of a character to be written before the beam is repositioned to the start of the next character.

CHARACTER POSITIONING WITHIN LINE AND HORIZONTAL RETRACE (FIG. 8)

The master timing to establish the 16 character per line capability of the display along with provision for horizontal retrace between successive lines is illustrated in FIG. 8. Again the time base has been condensed to permit the illustration of a complete line sequence. Waveform 32 of FIG. 8 illustrates the bottom waveform 32 of FIG. 7 on a condensed time basis to show a succession of 16 45-microsecond character periods followed by two 45-microsecond periods which are utilized for horizontal retrace. Note, with reference to FIG. 6, that the delayed output from the most significant bit portion of the $\div 10$ counter 27 is taken as output 32 from the delay flip-flop 31 and applied as input to the $\div 18$ character counter 34. FIG. 8 illustrates the outputs from the five stages embodying the $\div 18$ counter as waveforms 36a, 36b, 36c, 36d, and 36e, respectively.

FIG. 4 illustrates the collective waveforms 36a - 36d of FIG. 8 being applied to an X-position digital-to-analogue converter 59 the output 60 of which may be a current analogue proportional to the binary number

held in the $\div 18$ counter. Binary outputs corresponding to 0 through 15 are utilized to develop step-current increases in the X-position CRT yoke winding 62 so that the beam is positioned successively at starting points for successive characters to be written. The binary outputs from the $\div 18$ counter corresponding to binary 16 and 17 are utilized as horizontal retrace and it is noted for this purpose that the most-significant bit output 36e of the $\div 18$ counter provides a blanking waveform for this purpose. Reference to FIG. 4 illustrates that output 36e (designated binary 16 + 17) is applied as a beam blanking input to video amplifier 56.

A further output 35 from the divide by 18 counter 34 (designated binary 15 + 16) is utilized as a blanking control for input to the memory 8 such that the character address applied to the read-only memory of the system is read in on one count and the character displayed during the succeeding count. Further reference to the waveform of FIG. 8 illustrates binary counts 15 and 16 from the $\div 18$ counter being employed for line memory clock blanking purposes. It is to be realized that either the $\div 18$ counter 34 or the memory 8 would include appropriate logic circuitry to develop a blanking waveform in response to these two particular binary numbers being held in the $\div 18$ counter.

LINE COUNTER PAGE FORMAT CONTROL AND VERTICAL RETRACE (FIG. 9)

FIG. 9 reillustrates the most-significant bit output 36e from the divide by 18 line counter on a reduced time basis to permit showing the 810-microsecond line period defined by the system which is comprised of 720 microseconds for writing time per line along with two 45-microsecond character periods (totaling 90 microseconds) utilized for horizontal retrace as the beam is positioned from the end of one line to the beginning of a succeeding line. The most-significant bit output 36e (corresponding to the time occurrence of binary numbers 16 and 17 in the $\div 18$ counter) is applied as input to a $\div 14$ line counter and FIG. 9 illustrates the waveforms from successively more-significant bit sections of the $\div 14$ counter as providing successive counts of 13 to define 13 lines per page, along with a fourteenth count the time occurrence of which is utilized for vertical retrace.

With reference to FIG. 4, an output 39 from the line counter 37 is designated binary 13 to define a blanking pulse developed in response to a count of 13 by logic circuitry (not illustrated). This blanking pulse output 39 is applied as a further blanking input to the video amplifier 56 to effect beam turn-off during the period when vertical retrace is effected and line counter starts a successive count sequence with a binary zero count.

As previously described, the delay flip-flop 31 provides a delayed output waveform 33 (the complement of the delayed output 32 depicted in the waveforms of FIG. 7) which is utilized for loading the character buffer register 10, controlling the line memory clock within the memory 8, and effecting a clearing of the ΔX and ΔY up/down counters 15 and 16 at the conclusion of each 36-microsecond character writing time. The clearing function as concerns the counters might in accordance with a particular design implementation constitute setting the counters to 0 or in a more preferred manner setting the counters to a predetermined count corresponding to the center of the character format such that if no character is to be written in a character

position no ΔX , ΔY deflection yoke current flows, and thus a saving in system power requirement is realized.

ALPHANUMERIC DISPLAY OPERATION SUMMARY

In summary, the alphanumeric stroke writing system of FIG. 4 may be operationally defined as follows:

The next one of a successive number of characters to be displayed is loaded into the character buffer register 10 by the beam position time delayed most-significant bit of the $\div 10$ counter 27 in the master timing chain. This same loading signal 33 (Q output of delay flip-flop 31) sets or clears the ΔX and ΔY up/down counters 20 and 21 to a fixed display address.

For the embodiment illustrated in FIG. 4, a 64 character repertoire was utilized which requires six bits of address from the character buffer register 10.

The character buffer register 10 applies table addressing to the three character ROM's 43, 44, and 45, which tables collectively define the format of the character to be displayed in terms of $\pm \Delta X$ deflection, $\pm \Delta Y$ deflection, and video (CRT write/blank). Once the ROM's are character addressed, the $\div 3$ and $\div 10$ counters 24 and 27 in the master timer, sequence through the ROM's to call up the 24-character segments for display. These segments are defined by two ROM addressing bits from the $\div 3$ counter and three ROM addressing bits (the three least-significant bits) from the $\div 10$ counter. The two addressing bits from the $\div 3$ counter allow up to three distinct ROM groups to be addressed, and the three addressing bits from the $\div 10$ counter allow up to eight distinct ROM words within each group to be addressed, thereby allowing up to 24 ROM words to be addressed for each character word loaded into the character buffer register 10.

The stroke buffer register receives the outputs from the character ROM and acts as a high speed interface between the ROM's and the high speed up/down counters.

The outputs from the stroke buffer register 50 provides the counting control for the ΔX and ΔY up/down counters 15 and 16 and the video control 55 for selectively blanking the cathode ray tube 58. The ΔX and ΔY clock rates are derived from the master 2-MHz clock 13 and cause the counters to count up or down, or hold, depending on the counting control derived from the 5-bit stroke words from stroke buffer register 50.

The digital words derived from the ΔX and ΔY counters 15 and 16 are converted to analogue deflection signals (FIG. 5) by their respective digital-to-analogue converters 17 and 18. The analogue deflection signals provide the impetus for the linear ΔY and ΔX deflection amplifiers 64 and 67 to deflect the beam and, in conjunction with the video control signal 55, trace the symbology to be displayed.

The positioning of the CRT beam required to properly locate the symbology on the CRT screen is performed by X and Y deflection signals derived digitally from the respective counts held in the $\div 18$ character counter 34 and the $\div 14$ line counter 37. The binary outputs from these counters are applied to digital-to-analogue converters 26 and 59 and associated deflection amplifiers 41 and 61 provide position deflection current steps line position and character within line position, respectively, in the same manner as described for writing symbology on the cathode ray tube.

The present invention is thus seen to provide a means for displaying symbology utilizing digitally controlled stroke writing which inherently allows brighter images to be displayed at lower cathode ray beam currents than conventional raster scan displays. Because the beam traces the symbology being displayed, the symbology displayed is more readable than conventional dot matrix symbology. The digital stroke writing technique described herein does not require precision analogue ramp generators as do conventional stroke writing displays and thus obviates the attendant instability problems of analogue ramp and function generators.

Although described particularly as an embodiment for displaying alphanumeric characters, the present invention is not to be so limited, since, in a general sense, lines (strokes) may be displayed at any angle (slope) without the need for variable gain or variable slope analogue ramp generators by digitally controlling the relative vertical and horizontal clock rates according to a desired slope, and any configuration may be defined as a series of line segments for sequential write-out by stroke commands.

Thus, although the present invention has been described as a specific embodiment thereof, it is not to be so limited, as changes might be made therein which fall within the scope of the invention as defined in the appended claims.

I claim:

1. A digitally controlled stroke writing system for writing a selected display format on a cathode ray tube, said format being predefined as a sequential plurality of straight line strokes each of an individually predetermined length and line slope, comprising, means for defining each of said straight line strokes as a five-bit binary command word, the binary state of first and second bits of said command word defining respective cathode ray tube beam deflection command increments of left and right, the binary state of second and third bits of said command word defining respective cathode ray tube beam deflection command increments of up and down, the binary state of the fifth bit of said command word defining cathode ray tube beam on-off command; a master clock source of predetermined repetition rate, first and second binary up/down counting means, means for gating a clock defined pulse train to said first binary up/down counter under control of said first and second bits of sequential ones of said five-bit stroke command words, means for gating a clock defined pulse train to said second binary up/down counter under control of said third and fourth bits of said five-bit stroke command words, means for controlling the generation of said cathode ray tube beam as a function of said fifth bit of said five-bit binary stroke command words, means converting the binary count in each of said up/down counters to respective horizontal and vertical analog beam deflection signals, means effecting cathode ray tube beam deflection in response to said analogue deflection signals; the slope of successive ones of said straight line strokes being established by means establishing said clock defined pulse train repetition rates to define a predetermined ratio of the repetition rate of the clock defined pulses applied to said respective ones of said binary up/down counters to the repetition rate of said master clock source.

2. A digitally controlled stroke writing system for writing a selected display format on a cathode ray tube,

said format being predefined as a sequential plurality of straight line strokes each of an individually predetermined length and line slope, comprising, means for defining each of said straight line strokes as a five-bit binary command word, the binary state of first and second bits of said command word defining respective cathode ray tube beam deflection command increments of left and right, the binary state of second and third bits of said command word defining respective cathode ray tube beam deflection command increments of up and down, the binary state of the fifth bit of said command word defining cathode ray tube beam on-off command; a master clock source of predetermined repetition rate, first and second binary up/down counting means, means for gating a clock defined pulse train to said first binary up/down counter under control of said first and second bits of sequential ones of said five-bit stroke command words, means for gating a clock defined pulse train to said second binary up/down counter under control of said third and fourth bits of said five-bit stroke command words, means for controlling the generation of said cathode ray tube beam as a function of said fifth bit of said five-bit binary stroke command words, means converting the binary count in each of said up/down counters to respective horizontal and vertical analog beam deflection signals, means effecting cathode ray tube beam deflection in response to said analogue deflection signals; master timing means receiving said master clock source signal and including binary counting means responsive to said master clock signal to develop a first binary output predetermined least significant bits of which comprise a moving digital deflection code definitive of a horizontal deflection command for effecting successive character positions on one of a plurality of character lines, and a second binary output predetermined successive least significant bits of which comprise a moving digital deflection code definitive of a vertical deflection command for effecting line position, further digital-to-analogue conversion means receiving said first and second said binary count outputs from said master timing means and developing respective further analogue horizontal position and vertical position deflection signals, and means for controlling the horizontal and vertical deflection of said cathode ray tube beam in accordance with said further horizontal and vertical position deflection signals; whereby successive ones of said characters are written in a line-page format.

3. A digitally controlled stroke writing system for displaying a selected imagery on a cathode ray tube, said imagery being predefined as a sequential plurality of straight line strokes each of predetermined length and slope, comprising, a master clock source, digital memory means including addressable binary stroke word storage for each of said predetermined number of strokes, means under control of said clock source to address for sequential read-out of each of said predetermined number of binary stroke words; each said stroke word being defined as a five-bit binary word, the binary state of first and second bits of each said stroke word defining respective cathode ray tube beam deflection command increments of left and right, the binary state of second and third bits of each said stroke word defining respective cathode ray tube beam deflection command increments of up and down, and the binary state of the fifth bit of each said stroke word defining cathode ray tube beam on-off command, each of said

stroke word bits being of a time duration defined by a predetermined number of pulses the repetition rate of which is a predetermined function of said clock source repetition rate; a first binary up/down counter, means for controlling the application of first ones of said time duration defining pulses to said first binary counter as a function of said first and second bits of said binary stroke words; a second binary up/down counter, means for controlling the application of second ones of said time duration defining pulses to said second binary counter as a function of said third and fourth bits of said binary stroke words; digital-to-analogue converter means responsive to the count in each of said binary counters to develop respective horizontal and vertical cathode ray tube deflection signals; and video blanking means responsive to the binary state of said fifth bit of said binary stroke words to effect cathode ray tube beam on-off control; said selected imagery comprising a plurality of *m* alphanumeric characters in a display format defined by a predetermined number of character positions on each of a predetermined number of display lines; said system further comprising a master clock timing means, said master clock timing means receiving the output of said master clock source as a control input thereto and being comprised of a plurality of cascaded binary dividing means successive ones of which produce operational output wave forms to effect said sequential readout from said digital memory means of stored sequential strokes for each of successive ones of said plurality of alphanumeric characters to be displayed and binary outputs defining character and line position; further horizontal and vertical beam positioning means responsive to said character and line position master timing means outputs to effect beam positioning for the start of sequential stroke sequences defining successive characters to be written and successive lines upon which predetermined sequences of characters are to be written; and said master timing means further comprising outputs for application to said cathode ray tube to effect blanking of said cathode ray tube beam during beam positioning between successive characters on a line, between successive lines of said display, and during beam retrace between the last of said plurality of lines to be displayed and the initial starting position for a subsequent stroke writing sequence.

4. A stroke writing system as defined in claim 3 wherein said timing pulses as applied to said first and second binary up/down counters comprise pulse trains of like repetition rate, said sequential strokes defining each of said alphanumeric characters to be displayed comprised of a predetermined sequence of vertical, horizontal and 45° inclined straight line strokes.

5. A stroke writing system as defined in claim 4 wherein said master timing means comprises means to effect predetermined delay of said timing pulses as applied to said first and second binary up/down counters, said delay being effective to permit the final stroke of a character to be displayed prior to said cathode ray beam being repositioned to a position defining the start of a succeeding character to be displayed.

6. A stroke writing system as defined in claim 5 wherein said system has a character writing capability of 64 characters, each of said characters being defined by a stroke sequence not in excess of 24 strokes, each stroke comprising a time duration defined by three of said timing pulses, said digital memory means including

address means to define each successive character to be written as one of 64 6-bit binary character address words, said display including provision for 16 character writing spaces per line on each of 13 lines, said binary memory means including read-only memory means, means for collectively addressing said read-only memory means by said 6 bit character addressing words and a sequencing control readout from said master timing means, whereby 24 5-bit stroke segment command words are sequentially read out from said read-only memory means in a predetermined sequence individually defined by each one of said 6-bit character addressing words applied thereto, said read-only memory having a storage requirement of 1,536 5-bit stroke command words addressable in selected sequences of 24 words each, said master timing means comprising a first divide-by-three substroke binary counter receiving the output from said master clock, a second divide-by-three binary counter receiving the output from said first divide-by-three counter and including logic means for developing first, second and third time multiplexed sequential outputs for addressing said read-only memory, the most significant bit output of said second divide-by-three counter being applied to a divide-by-10 counter, the three least significant bit outputs of said divide-by-10 counter being applied as addressing inputs to said read-only memory, means for delaying the most significant bit output of said divide-by-10 counter by said predetermined delay, means for gating said clock pulses to said first and second binary up/down counters under control of the output of said means for delaying, a divide-by-18 counter receiving the output from said means for delaying the four least significant bit outputs from said divide-by-10 counter being applied to a further digital-to-analogue conversion means the output of which develops a horizontal position beam deflection signal for beam positioning between successive characters to be displayed, the most significant bit output of said divide-by-18 counter being applied to a divide-by-14 counter, respective successive significant bit outputs from said divide-by-14 counter including the least significant bit output thereof being applied to a still further digital-to-analogue conversion means the output of which develops a vertical position beam de-

flection signal for beam position between successive lines of characters to be displayed, the respective bit outputs from said divide-by-14 counter being additionally applied to said memory means to effect a display synchronized line memory output control therein, means utilizing the most significant bit output from said divide-by-18 counter to effect horizontal retrace blanking of said cathode ray tube, and means responsive to the most significant bit output of said divide-by-14 counter to effect vertical retrace blanking of said cathode ray tube beam.

7. A method of digitally controlling cathode ray tube stroke writing comprising the steps of:

defining the format to be displayed on said cathode ray tube as a sequence of straight line strokes of n increments each of a preassigned line slope,

storing each of said straight line strokes as a 5-bit binary command word individual bits of which define respective plus or minus vertical deflection increments, plus or minus horizontal deflection increments, and beam on-off control in accordance with a predetermined binary state of respective individual ones of said 5 bits,

reading out said plus or minus vertical deflection increment bits and said plus or minus horizontal deflection increment bits to respective first and second binary up/down counters to establish count up, count down, and count hold commands thereto, causing said binary up/down counters to count when so commanded at respective count rates derived from a master clock, which clock defines said n increments per straight line stroke, with an associated ratio of said respective count rates defining said preassigned line slopes for each successive line stroke,

converting the binary count in each of said up/down counters to respective analogue cathode ray tube beam deflection signals, and

applying said respective analogue cathode ray tube beam deflection signals, and said beam on/off command signals to said cathode ray tube to control the generation and deflection of said cathode ray tube beam as a composite function thereof.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,775,760

Dated November 27, 1973

Inventor(s) Lyle R. Strathman

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Col. 10, line 11, "(1-7" should read --(0-7)--.

Col. 12, the first column of the ROM1-group "B" Table should read:

ΔY

1
1
0
0
0
0
0
0

Col. 12, the third column of the ROM2-group "B" Table should read:

ΔX

0
0
1
0
0
1
0
0

Signed and sealed this 14th day of May 1974.

(SEAL)
Attest:

EDWARD M. FLETCHER, JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents