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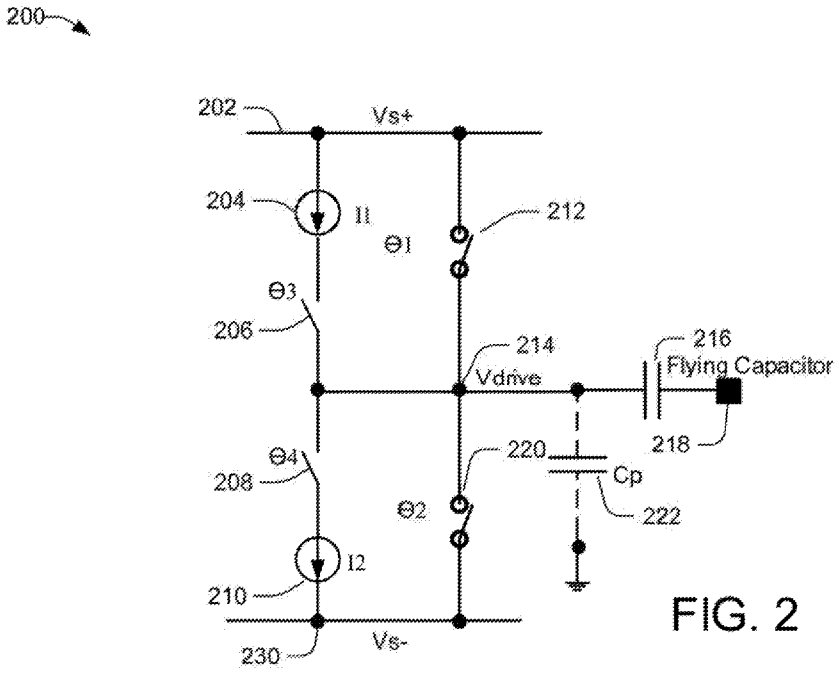


FIG. 2

(57) Abstract: Methods and systems of reducing a substrate noise in a charge pump having a flying capacitor are provided. An input node of the flying capacitor is precharged at a first slew rate. The input node of the flying capacitor is charged at a second slew rate that is faster than the first slew rate. The input node of the flying capacitor is pre-discharged at a third slew rate. The input node of the flying capacitor is discharged at a fourth slew rate that is faster than the first slew rate.

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[Continued on next page]

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METHODS AND SYSTEMS OF REDUCING CHARGE PUMP SUBSTRATE NOISE

BACKGROUND

TECHNICAL FIELD

[0001] This disclosure generally relates to charge pumps, and more particularly, to charge pumps with reduced substrate noise.

DESCRIPTION OF RELATED ART

[0002] In recent years, there has been a constant effort to improve performance, add additional features, reduce cost, and occupy less real estate in semiconductor integrated circuits (ICs). Consequently, the speed of circuits is progressively increasing, ICs are becoming more densely packed, and more circuit blocks are introduced that share a common substrate.

[0003] One challenge with these advanced digital, mixed signal, or analog ICs is to minimize noise coupling between various parts of the system to avoid degraded performance or even malfunctioning. Coupling caused by parasitics can lead to unreliable performance of the IC. For example, in mixed-signal circuits, both sensitive analog circuits and high frequency digital circuits that are a source of noise may be present on a same IC, leading to undesired signal coupling between these two types of circuits via the conductive substrate. The more densely packed these circuits are, the more pronounced the substrate noise issue becomes.

[0004] An example high frequency and high power circuit is a charge pump, which is a DC to DC converter that uses capacitors as energy storage elements to

provide a lower or higher voltage level from a reference input. A charge pump can introduce mixed-signal noise coupling via a common node, such as the substrate. The high frequency switching operations of a charge pump cause fluctuations in the underlying substrate voltage, which spreads through the common substrate causing variations in the substrate potential, affecting various components of the IC, including the sensitive analog section.

BRIEF DESCRIPTION OF DRAWINGS

[0005] The drawings are of illustrative embodiments. They do not illustrate all embodiments. Other embodiments may be used in addition or instead. Details that may be apparent or unnecessary may be omitted to save space or for more effective illustration. Some embodiments may be practiced with additional components or steps and/or without all of the components or steps that are illustrated. When the same numeral appears in different drawings, it refers to the same or like components or steps.

[0006] FIG. 1A illustrates a typical charge pump stage.

[0007] FIG. 1B illustrates several waveforms related to the operation of the charge pump stage of FIG. 1A.

[0008] FIG. 2 illustrates a charge pump stage 200, consistent with an illustrative embodiment.

[0009] FIG. 3 illustrates several waveforms related to the operation of the charge pump stage of FIG. 2, consistent with an illustrative embodiment.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

Overview

[0010] In the following detailed description, numerous specific details are set forth by way of examples in order to provide a thorough understanding of the relevant teachings. However, it should be apparent that the present teachings may be practiced without such details. In other instances, well-known methods, procedures, components, and/or circuitry have been described at a relatively high-level, without detail, in order to avoid unnecessarily obscuring aspects of the present teachings. Some embodiments may be practiced with additional components or steps and/or without all of the components or steps that are described.

[0011] The methods and circuits disclosed herein generally relate to methods and circuits of providing low noise charge pumps. More particularly, the present disclosure describes active charge pumps that have a reduced substrate noise. A charge pump uses switching devices to control a voltage across a capacitor. In this regard, multiple stages may be used to progressively increase a reference voltage from stage to stage. The capacitor used in each stage is sometimes referred to as a "flying capacitor," which is cycled between a first supply (e.g., Vin) and a second supply (e.g., ground). Flying capacitors generally have parasitic capacitance to ground (e.g., when used as an external device) or to the substrate (e.g., when integrated on a chip). This parasitic capacitance acts as a conduit for coupling noise to other circuit components that share the same ground and/or substrate.

[0012] Reference now is made to FIG. 1A, which illustrates a charge pump stage 100 as may be found in various typical charge pumps. Charge pump stage

100 includes a flying capacitor 116, which has a first node (V_{drive}) 114. There is a first switch Θ1 (112) coupled between the first voltage supply (V_S+) at node 102 and V_{drive} 114, and a second switch Θ2 (120) coupled between the second voltage supply (V_S-) at node 130 and V_{drive} 114. There is a parasitic capacitance C_p 122 between V_{drive} 114 and the substrate terminal. The substrate terminal is generally connected to ground or an external supply. The parasitic capacitance C_p 122 represents the total parasitic capacitance at the V_{drive} node 114, which may include the parasitic capacitance of the flying capacitor 116, the first switch 112, the second switch 120, wiring parasitics at node 114, etc., as well as any parasitic at node 118. In one estimate, the parasitic capacitance 122 may be 1/10 to 1/5 that of the actual flying capacitor 116, which may be in the nano-farad range.

[0013] Reference now is made to FIG. 1B, which illustrates several waveforms related to the operation of the charge pump stage 100 of FIG. 1A. The V_{drive} node 114 is cycled between a first voltage supply (V_S+) at node 102 and a second voltage supply (V_S-) at node 130, as illustrated by waveform 142. To that end, when switch Θ1 112 is ON, a path is created between Vs+ at node 102 and V_{drive} 114 to charge the flying capacitor 116, as illustrated by waveform 144. The flying capacitor 116 is discharged through the switch Θ2 120. Thus, when the switch Θ2 120 is ON, a path is created between the second voltage supply Vs- at node 130 and the V_{drive} node 114, as illustrated in waveform 146. The voltage transitions on the flying capacitor 116 are usually very fast, one nanosecond risetime or less. Accordingly, the transient currents driven by the switches Θ1 112 and Θ2 120 are also very fast. The resulting di/dt creates large voltage transients through the substrate connecting wire inductance. The resulting noise current is illustrated in waveform 148 and provided by equation 1 below:

[0014] $$I_{Noise} = Cp\frac{dv}{dt}$$ [Eq. 1]

[0015] Accordingly, the noise current I_{Noise} is a function of the parasitic capacitance C_p 122 and the change in voltage dv at the V_{drive} node 114. The current spikes 148 due to the sharp voltage edges of the flying capacitor 116 are generally difficult to suppress.

[0016] The applicant has identified that by using a configuration and a timing sequence discussed herein, the rush of current to/from the substrate during a charge/discharge operation can be actively controlled, thereby reducing the noise floor of the substrate of a charge pump stage. To that end, an input node of the flying capacitor is pre-charged at a first slew rate. The input node of the flying capacitor is charged at a second slew rate that is faster than the first slew rate but has a small voltage change at Vdrive. The input node of the flying capacitor is pre-discharged at a third slew rate. The input node of the flying capacitor is discharged at a fourth slew rate that is faster than the first slew rate but also of small magnitude. By virtue of the methods and architectures discussed herein, the substrate noise in a charge pump having a flying capacitor is reduced.

Example Implementation

[0017] FIG. 2 illustrates a charge pump stage 200, consistent with an illustrative embodiment. Charge pump stage 200 includes a flying capacitor 216, which is coupled between the V_{drive} node 214 and an output 218. In various embodiments, the output node 218 may be coupled to one or more charge pump stages to achieve a desired output voltage.

[0018] There is a first switch Θ1 (212), sometimes referred to herein as the drive switch, coupled between the first voltage supply (V_S+) at node 202 and the

V_{drive} node 214, and a second switch Θ2 (120), sometimes referred to herein as the discharge switch, coupled between the second voltage supply (V_S-) at node 230 and the V_{drive} 214. The first switch Θ1 (212) is configured to quickly charge the V_{drive} node 214, whereas the second switch Θ2 (220) is configured to quickly discharge the V_{drive} node 214.

[0019] In one embodiment, there is a first current source 204 coupled to the first voltage supply (Vs+) at node 202 and a second current source 210 coupled to the second voltage supply (Vs-). A third switch Θ3 (206) is coupled between the first current source I_1 (204) and the V_{drive} node 214. A fourth switch Θ4 (208) is coupled between the V_{drive} node 214 and the second current source I_2 (210).

[0020] The third switch Θ3 (206) is configured to pre-charge the V_{drive} node 214 at a slew rate that is substantially slower than that caused by the first switch Θ1. For instance, the Θ3 period can be one-fourth the clock period. If the clock frequency were 1MHz, the Θ3 period would be 250nsec, much slower than a 1nsec uncontrolled edge. The fourth switch Θ4 (208) is configured to pre-discharge the V_{drive} node 214 at a slew rate that is substantially slower than that caused by the second switch Θ2 (220). In one embodiment, the slew rate of the third switch Θ3 (206) and the fourth switch Θ4 (208) are substantially similar. Equation 2 below provides the guidelines for the first current source 204 and the second current source 210, for an example embodiment.

[0021] $$I_1 and\ I_2 \geq 4 \times C_p(V_{S+} - V_{S-}) \times F_{osc} \qquad \text{[Eq. 2]}$$

Where:

I_1 is the current through the first current source 204;

I_2 is the current through the second current source 210;

C_p is the parasitic capacitance 222; and

F_{OSC} is the inverse of the period of switches Θ1 (212) and Θ2 (220).

[0022] By virtue of the relationship in equation 2 above, the charge pump stage 200 provides a pre-charge and a pre-discharge having a slew rate that is substantially slower than the slew rate of the charge switch Θ1 (212) and the discharge switch Θ2 (220), respectively.

[0023] In one embodiment, a separate current source I_1 204 and/or I_2 208 are not necessary. For example, the switch Θ3 (204) may be configured such that it provides a reduced current between the first voltage supply Vs+ and the Vdrive node 214 that is consistent with equation 2 above. Similarly, the switch Θ4 (208) may be configured such that it provides a reduced current between the second voltage supply Vs- and the Vdrive node 214 consistent with equation 2 above. For example, if a field effect transistor is used as a switch, the width/length of the transistor may be adjusted to achieve the desired current through the transistor. It is believed that those skilled in the art are knowledgeable about the sizing of the different types of switches to achieve the desired current. Accordingly, the sizing of the switches is not discussed herein for brevity.

[0024] As discussed previously, there is a parasitic capacitance C_p 222 between V_{drive} node 214 and the substrate terminal. While the parasitic capacitance C_p 222 has been illustrated by way of example only and not by way of limitation to ground, in various scenarios, the parasitic capacitance C_p 222 may be to any other node, such as the substrate, the first supply (Vs+), the second supply (Vs-), or any other node of the charge pump stage 200.

[0025] The parasitic capacitance C_p 222 represents the total parasitic capacitance at the V_{drive} node 214, which may include the parasitic capacitance of the flying capacitor 216, the first switch 212, the second switch 220, wiring parasitics at node 214, wiring parasitics at node 218, etc.

[0026] Reference now is made to FIG. 3, which illustrates several waveforms related to the operation of the charge pump stage 200 of FIG. 2, consistent with an illustrative embodiment. The V_{drive} node 214 is cycled between a level provided by a first voltage supply (V_S+) at node 202 and a second voltage supply (V_S-) at node 230, as illustrated by waveform 310. Significantly, the charge pump stage 200 is configured in such a way to prevent a current spike to the ground or substrate. To that end, each hard charge by the switch Θ1 (212) is preceded by a pre-charge via switch Θ3 (206). Similarly, each hard discharge by switch Θ2 (220) is preceded by a pre-discharge by switch Θ4 (208). Put differently, each charge cycle includes a pre-charge and a hard charge, and every discharge cycle includes a pre-discharge and a hard discharge.

[0027] For example, the V_{drive} node 214 is pre-charged to a predetermined voltage level at a first slew rate by turning ON switch Θ3 (206), as indicated by waveform 340. Accordingly, a path is created between the first current source 204 and the V_{drive} node 214, thereby pre-charging the V_{drive} node 214, having a parasitic capacitance C_p 222, to a predetermined voltage, which may be at or slightly below Vs+, due to the effective resistance drop of the switch Θ3 (206), which in turn is due to flying capacitor 216 charge current, as indicated by level 362.

[0028] In various embodiments, during the charge cycle, the switch Θ3 (206) is turned ON before the switch Θ1 (212) is turned ON. The switch Θ1 may be kept

ON while switch Θ3 is ON (*see* dotted line of waveform 340 and its relationship to waveform 320) with little change in waveform 310. Thus, at T_0, the switch Θ3 (206) is ON until T_1 to T_3. At T_2, the switch Θ1 is turned ON and kept ON until T_3. Thus, the pre-charge may have a time window that overlaps with the hard charge.

[0029] Similarly, during a discharge cycle, the V_{drive} node 214 is pre-discharged to a second predetermined voltage (at or below Vs-) at a second slew rate, by turning ON switch Θ4 (208), as indicated by waveform 350. Accordingly, a path is created between the second current source 210 and the V_{drive} node 214, thereby pre-discharging the V_{drive} node 214 to a second predetermined voltage, which may be at or slightly above Vs-, as indicated by level 364. Thus, at T_3 the switch Θ4 (208) is turned ON. In various embodiments, the switch Θ4 (208) is kept ON until T_4 to T_6. Put differently, the switch Θ4 (208) is turned OFF before the second switch Θ2 (220) is turned ON, or kept ON until the next pre-charge cycle begins at T_6 (*see* dotted line in waveform 350).

[0030] The slew rate during a pre-charge is provided by equation 3 below.

[0031]
$$\frac{dv}{dt} = {}^{I1}/_{Cp} \qquad \text{[Eq. 3]}$$

Where:

dv is the change in voltage at the V_{drive} node 214;

dt is the time for the voltage change at the V_{drive} node 214;

I_1 is the current through the first current source 204; and

C_p is the parasitic capacitance 222.

[0032] In one embodiment, the pre-charge current provided by the first current source 204 is relatively small (e.g., in the order μA or tens of μA), thereby providing a slow slew rate). In contrast, the current provided through the first

switch Θ1 (212) may be up to a thousand times larger, providing a second slew rate that may be largely uncontrolled and significantly faster than that of the pre-charge. Accordingly, by using the pre-charge, the injected substrate current is not only smaller (*see* a relatively small bump 366 during a hard charge) but also spread over time, as indicated by waveform 360. The pre-discharge operation is similar to the above and therefore not repeated here for brevity. By virtue of the pre-charge and the pre-discharge discussed herein, the substrate noise floor is reduced.

[0033] It should be noted that, in one embodiment, due to the slow slew rate, much charge is not transferred to the flying capacitor 216 via the third switch Θ3 (206) during a pre-charge operation. Thus, the switch Θ1 (212) performs the charge transfer to the flying capacitor 216 during a charge operation via switch Θ1 (212). In this regard, since the V_{drive} node 214 almost arrived (*see* level 362 in waveform 310) at Vs+ level, the voltage at the V_{drive} node 214 jumps to the Vs+ level when the switch Θ1 is turned ON at T_2. Switches Θ4 and Θ2 provide similar waveforms during a discharge cycle.

CONCLUSION

[0034] The components, steps, features, objects, benefits, and advantages that have been discussed are merely illustrative. None of them, nor the discussions relating to them, are intended to limit the scope of protection in any way. Numerous other embodiments are also contemplated. These include embodiments that have fewer, additional, and/or different components, steps, features, objects, benefits, and/or advantages. These also include embodiments in which the components and/or steps are arranged and/or ordered differently.

[0035] For example, in various embodiments, a switch may be in the form of a field effect transistor (FET, such as a PFET, NFET, and/or JFET), bipolar device (e.g., NPN and/or PNP), any combination thereof, or any other suitable active or passive device based on the particular implementation. It is believed that those skilled in the art are familiar with the structure and general operation and implementation of a switch based on different technologies.

[0036] Unless otherwise stated, all measurements, values, ratings, positions, magnitudes, sizes, and other specifications that are set forth in this specification, are approximate, not exact. They are intended to have a reasonable range that is consistent with the functions to which they relate and with what is customary in the art to which they pertain.

[0037] Except as stated immediately above, nothing that has been stated or illustrated is intended or should be interpreted to cause a dedication of any component, step, feature, object, benefit, advantage, or equivalent to the public, regardless of whether it is or is not recited in the claims.

[0038] It will be understood that the terms and expressions used herein have the ordinary meaning as is accorded to such terms and expressions with respect to their corresponding respective areas of inquiry and study except where specific meanings have otherwise been set forth herein. Relational terms such as “first” and “second” and the like may be used solely to distinguish one entity or action from another, without necessarily requiring or implying any actual relationship or order between them. The terms “comprises,” “comprising,” and any other variation thereof when used in connection with a list of elements in the specification or claims are intended to indicate that the list is not exclusive and that other elements may be included. Similarly, an element preceded by an “a” or an “an”

does not, without further constraints, preclude the existence of additional elements of the identical type.

[0039] The Abstract of the Disclosure is provided to allow the reader to quickly ascertain the nature of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims. In addition, in the foregoing Detailed Description, it can be seen that various features are grouped together in various embodiments for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the claimed embodiments require more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter lies in less than all features of a single disclosed embodiment. Thus the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separately claimed subject matter.

CLAIMS:

What is claimed is:

1. A charge pump, comprising:

a flying capacitor coupled between a drive node and an output;

a first drive switch coupled between a first supply and the drive node and operative to charge the flying capacitor;

a second drive switch coupled between a second supply and the drive node and operative to discharge the flying capacitor;

a third switch coupled between the first supply and the drive node and operative to pre-charge the drive node;

a fourth switch coupled between the second supply and the drive node and operative to pre-discharge the drive node.

2. The charge pump of claim 1, wherein the third switch is configured to be turned ON before the first switch is turned ON.

3. The charge pump of claim 2, wherein the third switch is configured to be kept ON while the first switch is ON.

4. The charge pump of claim 1, wherein the fourth switch is configured to be turned ON before the second switch is turned ON.

5. The charge pump of claim 4, wherein the fourth switch is configured to be kept ON while the second switch is ON.

6. The charge pump of claim 1, further comprising:

a first current source coupled between the first supply and the drive node; and

a second current source coupled between the second supply and the fourth switch.

7. The charge pump of claim 1, wherein a slew rate of the third switch is slower than a slew rate of the first switch.

8. The charge pump of claim 1, wherein a slew rate of the fourth switch is slower than a slew rate of the second switch.

9. The charge pump of claim 1, wherein a current I_1 through the third switch and a current I_2 through the second switch is based on:

a parasitic capacitance C_p at the drive node;

the first supply Vs+;

the second supply Vs-; and

an inverse of a period of the first and second drive switches, wherein,

$$I_1 and\ I_2 \geq 4 \times C_p(V_{S+} - V_{S-})XF_{osc}$$

10. A method of reducing a substrate noise in a charge pump having a flying capacitor, the method comprising:

pre-charging an input node of the flying capacitor at a first slew rate;

charging the input node of the flying capacitor at a second slew rate that is faster than the first slew rate;

pre-discharging the input node of the flying capacitor at a third slew rate; and

discharging the input node of the flying capacitor at a fourth slew rate that is faster than the first slew rate.

11. The method of claim 10, wherein:

the pre-charging the input node of the flying capacitor is to a first predetermined voltage level;

the charging the input node of the flying capacitor is to a second predetermined voltage level that is above the first predetermined voltage level;

the pre-discharging the input node of the flying capacitor is to a third predetermined voltage level; and

the discharging the input node of the flying capacitor is to a fourth predetermined voltage level that is below the third predetermined voltage level.

12. The method of claim 10, wherein:

the first and third slew rates are substantially similar; and

the second and fourth slew rates are substantially similar.

13. The method of claim 10, wherein:

the charging the input node of the flying capacitor comprises turning ON a first switch, thereby creating a path between a first voltage supply and the input node of the flying capacitor; and

the discharging the input node of the flying capacitor comprises turning ON a second switch, thereby creating a path between a second voltage supply and the input node of the flying capacitor.

14. The method of claim 13, wherein:

the pre-charging the input node of the flying capacitor comprises turning ON a third switch, thereby creating a path between a first current source and the input node of the flying capacitor; and

the pre-discharging the input node of the flying capacitor comprises turning ON a fourth switch, thereby creating a path between a second current source and the input node of the flying capacitor.

15. The method of claim 14, further comprising, for each charge cycle, turning ON the third switch before turning ON the first switch.

16. The method of claim 15, further comprising keeping the third switch ON while the first switch is ON.

17. The method of claim 14, further comprising, for each discharge cycle, turning ON the fourth switch before turning ON the second switch.

18. The method of claim 17, further comprising keeping the fourth switch ON while the second switch is ON.

19. The method of claim 14, wherein a slew rate of the third switch is slower than a slew rate of the first switch.

20. The method of claim 14, wherein a slew rate of the fourth switch is slower than a slew rate of the second switch.

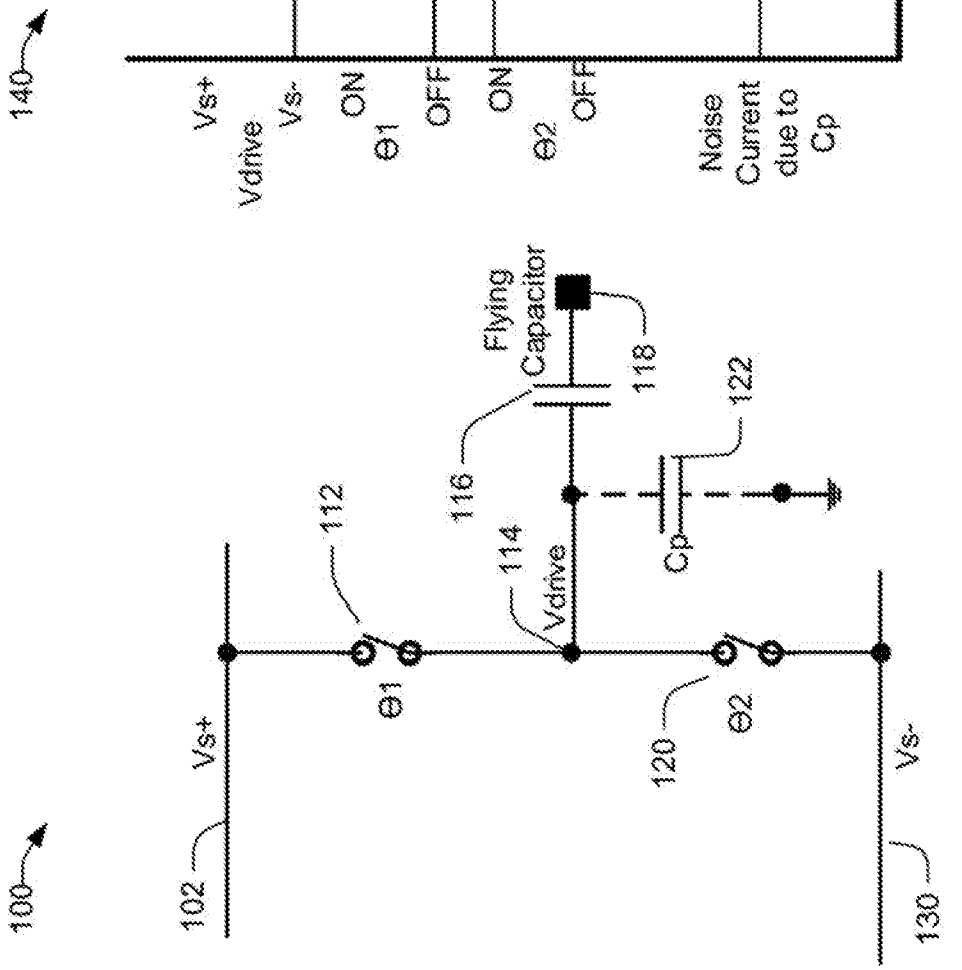


FIG. 1A Prior Art

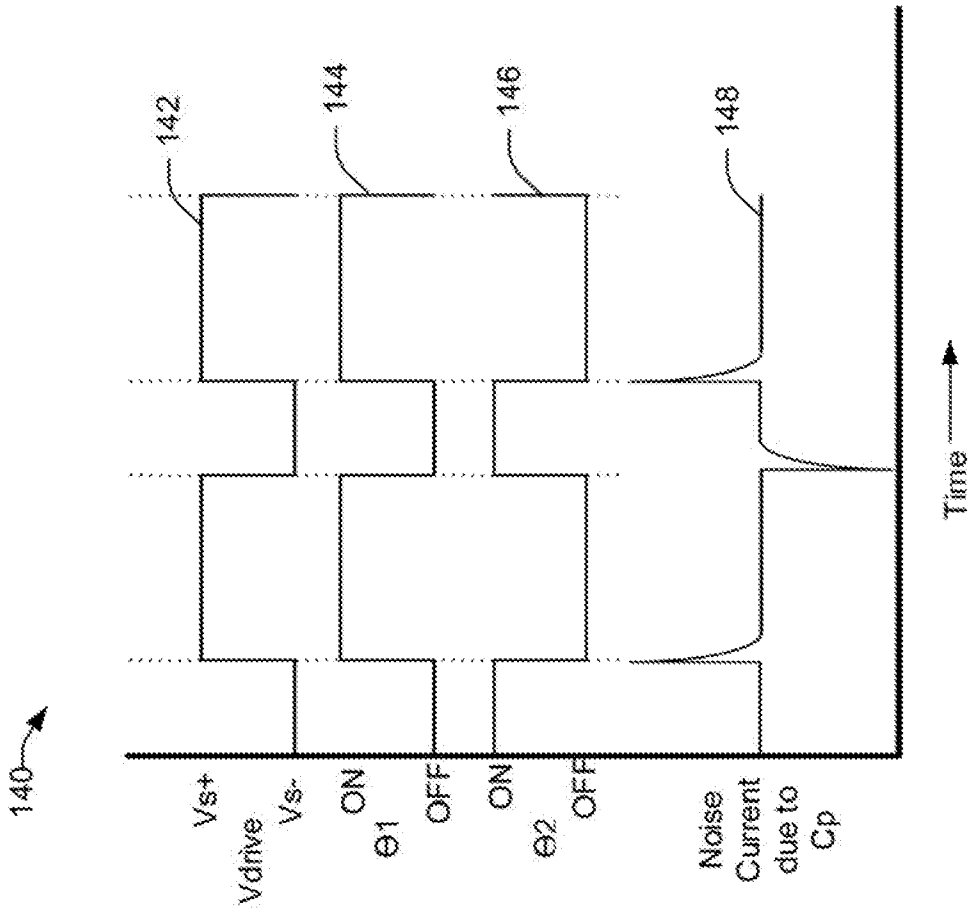


FIG. 1B Prior Art

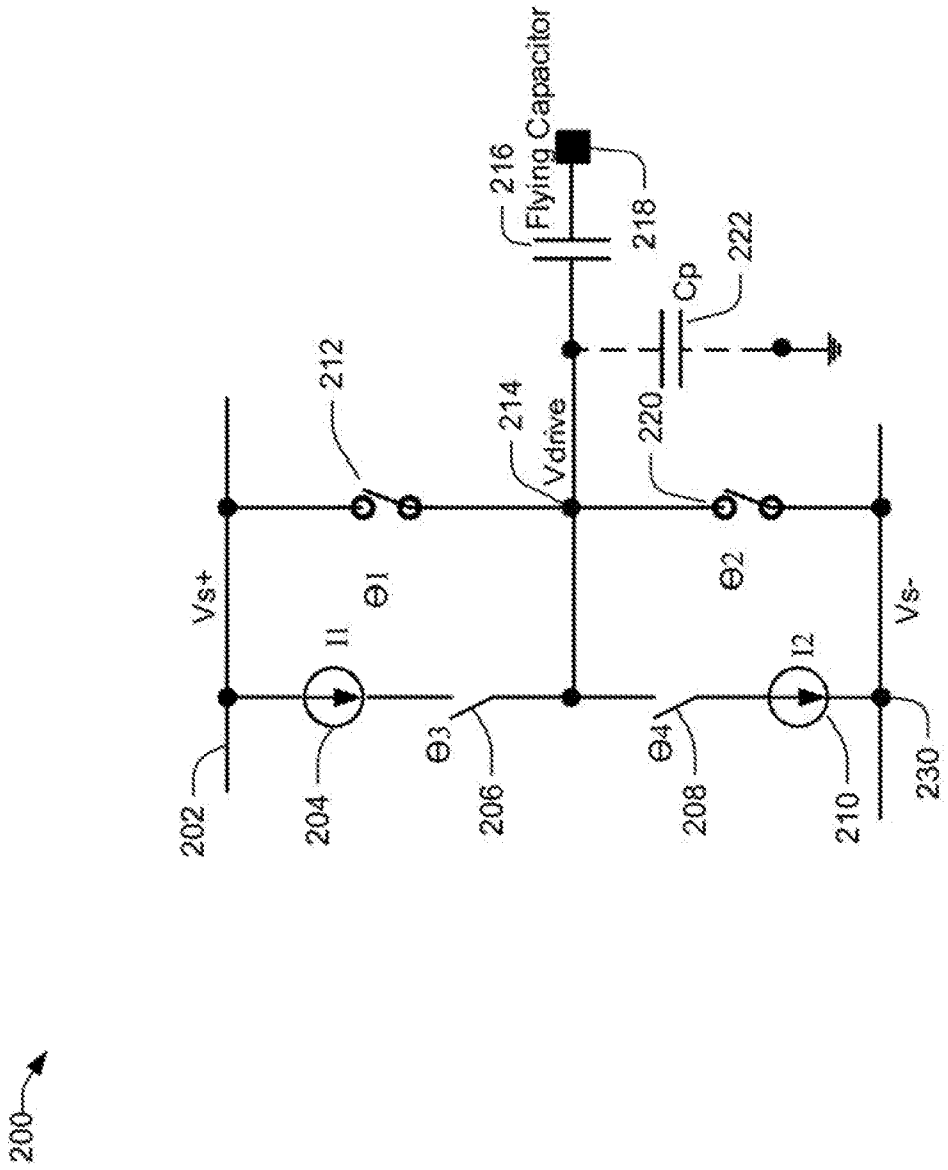

200
202
204
206
208
210
212
214
216
218
220
222
230
Vs+
Vs-
Vdrive
Flying Capacitor
Cp
I1
I2
Θ1
Θ2
Θ3
Θ4

FIG. 2

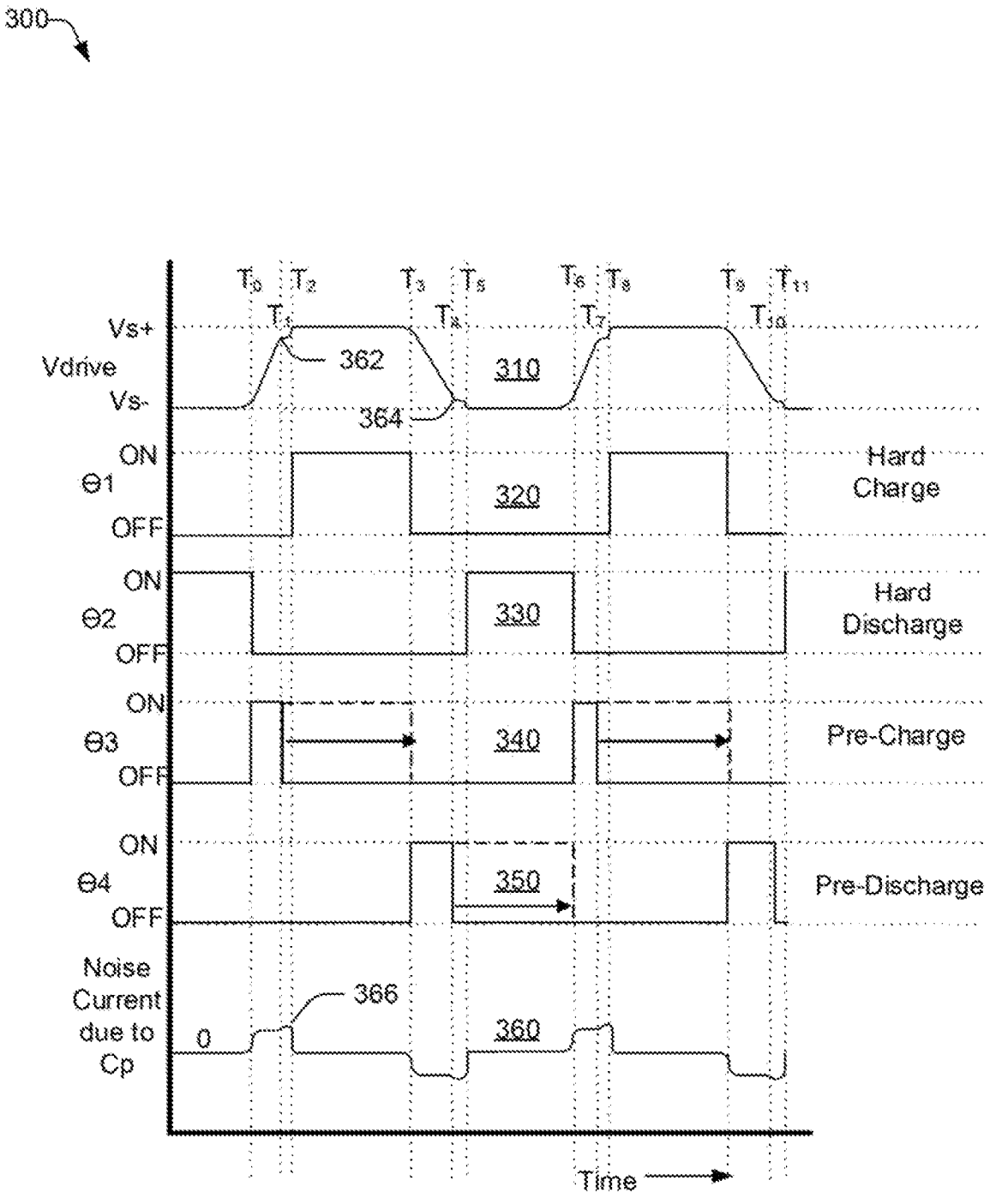

300
T0
T2
T3
T5
T6
T8
T9
T11
T1
T4
T7
T10
Vs+
Vdrive
Vs-
362
364
310
ON
Θ1
OFF
320
Hard Charge
ON
Θ2
OFF
330
Hard Discharge
ON
Θ3
OFF
340
Pre-Charge
ON
Θ4
OFF
350
Pre-Discharge
Noise Current due to Cp
0
366
360
Time

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/023409

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H02M 3/18; G05F 1/10; G05F 3/02; H02M 7/00 (2017.01)
CPC - H02M 3/07; G11C 5/145; H02M 3/073; H03K 17/16 (2017.02)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC - 327/382; 327/384; 327/534; 327/536; 327/537; 363/59 (keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 9,184,623 B1 (XILINX, INC.) 10 November 2015 (10.11.2015) entire document	1-9
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"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 June 2017	10 JUL 2017
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 Facsimile No. 571-273-8300	Authorized officer Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/023409

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
See extra sheet(s).

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-9

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/023409

Continued from Box No. III Observations where unity of invention is lacking

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I, claims 1-9, drawn to a charge pump.
Group II, claims 10-20, drawn to a method of reducing a substrate noise in a charge pump having a flying capacitor.

The inventions listed as Groups I-II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: the special technical feature of the Group I invention: a second drive switch coupled between a second supply and the drive node and operative to discharge the flying capacitor; a third switch coupled between the first supply and the drive node and operative to pre-charge the drive node; a fourth switch coupled between the second supply and the drive node and operative to pre-discharge the drive node as claimed therein is not present in the invention of Group II. The special technical feature of the Group II invention: pre-charging an input node of the flying capacitor at a first slew rate; charging the input node of the flying capacitor at a second slew rate that is faster than the first slew rate; pre-discharging the input node of the flying capacitor at a third slew rate; and discharging the input node of the flying capacitor at a fourth slew rate that is faster than the first slew rate as claimed therein is not present in the invention of Group I.

Groups I and II lack unity of invention because even though the inventions of these groups require the technical feature of charging the flying capacitor, this technical feature is not a special technical feature as it does not make a contribution over the prior art.

Specifically, US 2009/0039947 A1 (WILLIAMS) 12 February 2009 (12.02.2009) teaches charging the flying capacitor (Paras. 19-20).

Since none of the special technical features of the Group I or II inventions are found in more than one of the inventions, unity of invention is lacking.