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(71) Applicants: **APPLIED MATERIALS, INC.** [US/US];
3050 Bowers Avenue, Santa Clara, California 95054 (US).
NATIONAL UNIVERSITY OF SINGAPORE [SG/SG];
21 Lower Kent Ridge Road, Singapore 119077 (SG).

(72) Inventors: **WANG, Xinke**; Applied Materials Singapore
Technology Pte Ltd, 10 Science Park Road, #02-03, The Alpha
Science Park II, Singapore 117684 (SG). **LIU, Long**; 21
Lower Kent Ridge Road, Singapore 119077 (SG). **SALY,
Mark**; 3050 Bowers Avenue, Santa Clara, California 95054
(US). **BHUYAN, Bhaskar Jyoti**; 3050 Bowers Avenue,
Santa Clara, California 95054 (US). **TANG, Jiecong**; Ap-
plied Materials Singapore Technology Pte Ltd, 10 Science

Park Road, #02-03, The Alpha Science Park II, Singapore
117684 (SG). **SUDIJONO, John**; Applied Materials Sin-
gapore Technology Pte Ltd, 10 Science Park Road, #02-03,
The Alpha Science Park II, Singapore 117684 (SG).

(74) Agent: **SMIRK, Rebecca A.**; Servilla Whitney LLC, 33
Wood Avenue South, Suite 830, Iselin, New Jersey 08830
(US).

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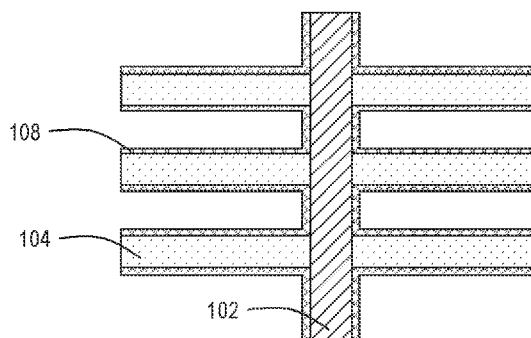


FIG. 4

(57) Abstract: Molecular layer deposition (MLD) is used to provide conformal and uniform doping technology for HAR and reentrant structures. MLD is used to deposit a conformal carbon-based film that contains a doping element. Thermal annealing is then used to make the doping element diffuse into the semiconductor material. For HAR structures, a conformal layer is used with low temperature doping, precise control, and the carbon-based film can be easily removed during doping or after doping. The amount of doping can be controlled by changing the thickness of MLD carbon-based film.

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DOPING BY MOLECULAR LAYER DEPOSITION

TECHNICAL FIELD

[0001] Embodiments of the disclosure relate to doping technologies. In particular, 5
embodiments of the disclosure are directed to methods of semiconductor doping by
molecular layer deposition (MLD) of a conformal film containing a doping element.

BACKGROUND

[0002] Semiconductor technology relies on the capability for tuning the electrical
10 properties of the substrate through the controlled introduction of substitutional
impurities (doping) in the crystal lattice of the semiconductor host material, in order to
tailor its electronic, optical and/or magnetic properties. The present ex situ doping
strategies, however, cannot be easily extended to the nanoscale. As the size of
semiconductor devices shrinks to the nanoscale, the standard random distribution of
15 the individual atoms within the semiconductor becomes critical since the assumption
of uniform doping distribution does not hold anymore. Currently there is a significant
effort by the scientific community for the development of a new technology to
demonstrate deterministic doping of semiconductor structures at the nanoscale.

[0003] Conventional doping techniques are mainly based on ion implantation which
20 implies the bombardment of the target semiconductor with high energy dopant-
containing ions that, subsequently, are induced to replace atoms in the lattice using a
high temperature thermal treatment. The main advantage of this technique is the
independent control of the dopant dose and depth distribution of the impurity atoms
within the semiconductor host. This approach has been widely explored, and has
25 become the workhorse in microelectronics, since it guarantees excellent doping
uniformity over large areas.

[0004] There are a number of drawbacks that are associated with ion implantation
technology, however, including damage to the crystal lattice during ion bombardment
and subsequent transient enhanced diffusion caused by defects during the thermal
30 treatment. Moreover, most of the source gases, commonly used in ion implantation,
are hazardous from a health and environmental perspective. Additionally, this
technique is incompatible with 3D nanostructured materials since it does not provide

conformal dopant incorporation for non-planar nanostructures. Accordingly, there is a need in the art for improved doping technologies to be able to precisely control the element doping into a high aspect ratio (HAR) semiconductor structure such as 3D-DRAM, gate-all-around, and the like.

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SUMMARY

[0005] One or more embodiments of the disclosure are directed to a method of semiconductor doping, the method comprising: flowing a first precursor over a substrate comprising a semiconductor surface and a dielectric surface to form a first portion of a doped carbon-containing layer on the semiconductor surface and on the dielectric surface, the first precursor comprising a first reactive group; removing a first precursor effluent comprising the first precursor from the substrate; flowing a second precursor comprising one or more of phosphorus (P), boron (B), aluminum (Al), arsenic (As), gallium (Ga), indium (In), or zinc (Zn) over the substrate to react with the first reactive group to form the doped carbon-containing layer on the semiconductor surface and on the dielectric surface; and removing a second precursor effluent comprising the second precursor from the substrate.

[0006] Another embodiment of the disclosure is directed to method of semiconductor doping, the method comprising: flowing a first precursor over a substrate comprising a semiconductor surface and a dielectric surface, the first precursor having a general formula $R^1-(X)_n$ wherein R^1 comprises one or more of alkyl group, an alkenyl group, an aryl, or aromatic group, and a cycloalkyl group, X_n comprises one or more of a hydroxide group, an aldehyde group, a ketone group, an acid group, an amino group, an isocyanate group, a thiocyanate group, and an acyl chloride group, and n is an integer in a range of from 1 to 6, wherein the first precursor reacts with a reactive group on one or more of the semiconductor surface and the dielectric surface to form a first portion of a doped carbon-containing layer on one or more of the semiconductor surface and the dielectric surface; removing a first precursor effluent comprising the first precursor from the substrate; flowing a second precursor over the substrate, the second precursor comprising one or more of phosphorus (P), boron (B), aluminum (Al), arsenic (As), gallium (Ga), indium (In), and zinc (Zn), wherein the second precursor reacts with the first portion to form a doped

carbon-containing layer; and removing a second precursor effluent comprising the second precursor from the substrate.

BRIEF DESCRIPTION OF THE DRAWING

5 [0007] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this disclosure and are
10 therefore not to be considered limiting of its scope, for the disclosure may admit to other equally effective embodiments. The embodiments as described herein are illustrated by way of example and not limitation in the figures of the accompanying drawings in which like references indicate similar elements.

[0008] FIG. 1 illustrates a process flow diagram of a method of semiconductor
15 doping by molecular layer deposition (MLD) of a conformal film containing a doping element according to one or more embodiments;

[0009] FIG. 2 illustrates cross-section view of a substrate according to one or more embodiments;

[0010] FIGS. 3A and 3B illustrate cross-section views of a substrate according to
20 one or more embodiments;

[0011] FIG. 4 illustrates cross-section view of a substrate according to one or more embodiments; and

[0012] FIG. 5 illustrates cross-section view of a substrate according to one or more
25 embodiments.

DETAILED DESCRIPTION

[0013] Before describing several exemplary embodiments of the invention, it is to be understood that the invention is not limited to the details of construction or process steps set forth in the following description. The invention is capable of other
30 embodiments and of being practiced or being carried out in various ways.

[0014] The term "about" as used herein means approximately or nearly and in the context of a numerical value or range set forth means a variation of $\pm 15\%$, or less, of

the numerical value. For example, a value differing by $\pm 14\%$, $\pm 10\%$, $\pm 5\%$, $\pm 2\%$, or $\pm 1\%$, would satisfy the definition of about.

[0015] As used in this specification and the appended claims, the term "substrate" or "wafer" refers to a surface, or portion of a surface, upon which a process acts. It will also be understood by those skilled in the art that reference to a substrate can refer to only a portion of the substrate unless the context clearly indicates otherwise. Additionally, reference to depositing on a substrate can mean both a bare substrate and a substrate with one or more films or features deposited or formed thereon.

[0016] A "substrate" or "substrate surface", as used herein, refers to any portion of a substrate or portion of a material surface formed on a substrate upon which film processing is performed. For example, a substrate surface on which processing can be performed includes materials such as silicon, silicon oxide, silicon nitride, doped silicon, germanium, gallium arsenide, glass, sapphire, and any other materials such as metals, metal nitrides, metal alloys, and other conductive materials, depending on the application. Substrates include, without limitation, semiconductor wafers. Substrates may be exposed to a pretreatment process to polish, etch, reduce, oxidize, hydroxylate, anneal, UV cure, e-beam cure and/or bake the substrate surface. In addition to film processing directly on the surface of the substrate itself, in the present disclosure, any of the film processing steps disclosed may also be performed on an underlayer formed on the substrate as disclosed in more detail below, and the term "substrate surface" is intended to include such underlayer as the context indicates. Thus, for example, where a film/layer or partial film/layer has been deposited onto a substrate surface, the exposed surface of the newly deposited film/layer becomes the substrate. Substrates may have various dimensions, such as 200 mm or 300 mm diameter wafers, as well as rectangular or square panes. In some embodiments, the substrate comprises a rigid discrete material.

[0017] The term "on" indicates that there is direct contact between elements. The term "directly on" indicates that there is direct contact between elements with no intervening elements.

[0018] As used in this specification and the appended claims, the terms "precursor," "reactant," "reactive gas" and the like are used interchangeably to refer to any gaseous species that can react with the substrate surface.

[0019] As used in this specification and the appended claims, the terms "reactive compound", "reactive gas", "reactive species", "precursor", "process gas" and the like are used interchangeably to mean a substance with a species capable of reacting with the substrate or material on the substrate in a surface reaction (e.g., chemisorption, oxidation, reduction, cycloaddition). The substrate, or portion of the substrate, is exposed sequentially to the two or more reactive compounds which are introduced into a reaction zone of a processing chamber.

[0020] Carbon-containing materials may be used in semiconductor device manufacturing for a number of structures and processes, including as a mask material, an etch resistant material, and a trench fill material, among other applications. More specific examples of applications for carbon-containing materials include the formation of hot implant hard masks, metal gate (MG)-cut hard masks, metal gate fabrication, and reverse tone patterning, self-aligned patterning, among others.

[0021] In one or more embodiments, molecular layer deposition (MLD) is used to provide conformal and uniform doping technology for HAR and reentrant structures. MLD is used to deposit a conformal carbon-based film that contains a doping element. Thermal annealing is then used to make the doping element diffuse into the semiconductor material. For HAR structures, a conformal layer is used with low temperature doping, precise control, and the carbon-based film can be easily removed during doping or after doping. In one or more embodiments, the amount of doping can be controlled by changing the thickness of MLD carbon-based film.

[0022] In specific embodiments, a carbon-containing film is deposited using molecular layer deposition (MLD). The methods may include flowing a first deposition precursor into a substrate processing region to form a first portion of an initial compound layer. The first deposition precursor may have a general formula $R^1-(X)_n$

wherein n is an integer in a range of from 1 to 6, and R^1 comprises one or more of an aryl, or aromatic group, and a cycloalkyl group. X_n comprises one or more of a hydroxide group, an aldehyde group, a ketone group, an acid group, an amino group, an isocyanate group, a thiocyanate group, and an acyl chloride group. Specific first
5 deposition precursors include terephthalaldehyde, phenylenediamine, ethylenediamine, hexamethylenediamine, terephthaloyl chloride, 1,3,5-benzenetricarbonyl trichloride, pyromellitic dianhydride.

[0023] The methods may include removing a first deposition effluent including the first deposition precursor from the substrate processing region. The methods may
10 include flowing a second precursor into the substrate processing region. The second precursor containing one or more of phosphorus (P), boron (B), aluminum (Al), arsenic (As), gallium (Ga), indium (In), or zinc (Zn). Specific second precursors may be selected from Tris(dimethylamino)phosphine, Phosphorus trichloride, Phosphorus(V) oxychloride, Tris(hydroxymethyl)phosphine, Boron trichloride, Trimethylaluminum,
15 Tris(dimethylamino)arsine, Trimethylindium, Diethylzinc, etc.

[0024] The second precursor may react with the reactive group of the first precursor to form a second portion of the initial compound layer. The methods may include removing a second deposition effluent including the second precursor from the substrate processing region. The methods may include annealing the initial compound
20 layer to form an annealed doped-carbon-containing material on the surface of the substrate.

[0025] In some embodiments, the methods may include one or more of etching the MLD film at an untargeted area, removing the MLD carbon film, thermal annealing to drive the dopant into the semiconductor layer, removing the residual MLD layer using
25 a wet etch or plasma etch.

[0026] Embodiments of the present technology include molecular layer deposition (MLD) methods and systems to deposit a doped carbon-based film. Exemplary MLD methods may include providing a first deposition precursor to a surface of a semiconductor substrate, where the precursor forms a first layer (e.g., a first
30 monolayer) on surfaces. During or after the formation of the first layer, unbound deposition effluents, which may include unbound molecules of the first deposition precursor, are removed from a processing region in which the semiconductor

substrate is exposed. A second deposition precursor may then be introduced to the semiconductor substrate, where molecules of the second deposition precursor bind to reactive moieties on the first layer to form a second layer (e.g., a second monolayer) on the surface. The second precursor contains one or more of phosphorus (P), boron (B), aluminum (Al), arsenic (As), gallium (Ga), indium (In), or zinc (Zn). During or after the formation of the second layer, unbound deposition effluent, which may include unbound molecules of the second deposition precursor, are removed from the processing region. The semiconductor substrate now has a doped carbon containing material layer bound to the surface of the semiconductor substrate. Additional compound layers of first and second layers may be built up on the deposited layers until the number of built-up compound layers reaches a desired thickness of doped carbon-containing material on the surface of the semiconductor substrate. The compound layers may then be annealed to drive one or more of phosphorus (P), boron (B), aluminum (Al), arsenic (As), gallium (Ga), indium (In), or zinc (Zn) into the semiconductor.

[0027] One or more embodiments advantageously provides solutions to problems with conventional doping methods. For example, the present technology avoids damage to the crystal lattice caused by ion implantation during ion bombardment and subsequent transient enhanced diffusion caused by defects during the thermal treatment. Plasma immersion ion implantation also leads to crystal damage and challenges for high aspect ratio (HAR) structures and can be avoided with the technology of one or more embodiments. Gas phase doping has fundamental limits in controlling dopant concentration near the surface and a lack of uniformity. Solid phase diffusion is challenging in HAR structure, residual film removal, and thermal budget. One or more embodiments, therefore, advantageously provides conformal and uniform doping for high aspect ratio (HAR) structures, especially for deep and reentrant features like 3D-DRAM. In some embodiments, a low thermal budget (≤ 800 °C) is possible, and any residue is easily removed after doping.

[0028] The embodiments of the disclosure are described by way of the Figures, which illustrate devices (e.g., transistors) and processes for forming semiconductor structures in accordance with one or more embodiments of the disclosure. The processes shown are merely illustrative possible uses for the disclosed processes,

and the skilled artisan will recognize that the disclosed processes are not limited to the illustrated applications.

[0029] FIG. 1 illustrates a process flow diagram of a method 10 of semiconductor doping by molecular layer deposition (MLD) of a conformal film containing a doping element according to one or more embodiments. FIGS. 2-5 illustrate cross-sectional views of a semiconductor substrate being processed according to the method of one or more embodiments. Referring to FIG. 1 and FIGS. 2-5, in one or more embodiments, at operation 12, a substrate is provided. As used in this specification and the appended claims, the term "provided" means that the substrate is made available for processing (e.g., positioned in a processing chamber).

[0030] Referring to FIG. 2, in one or more embodiments, a substrate includes a semiconductor surface 102 and a dielectric surface 104. The semiconductor surface 102 may comprise any suitable semiconductor material known to the skilled artisan. In one or more embodiments, the semiconductor surface 102 comprises one or more of silicon (Si), silicon germanium (SiGe), germanium (Ge), silicon carbide (SiC), indium gallium zinc oxide (InGaZnO), and the like.

[0031] In one or more embodiments, the dielectric surface 104 may comprise any suitable dielectric material known to the skilled artisan. A "dielectric surface," as used herein, refers to any portion of a substrate or portion of a material surface formed with the dielectric material. Non-limiting examples of dielectric material include silicon oxide (SiO_x), silicon nitride (Si_xN_y), silicon (Si), silicon oxynitride (SiON), carbides, oxycarbides, nitrides, oxynitrides, oxycarbonitrides, polymers, phosphosilicate glass, fluorosilicate (SiOF) glass, organosilicate glass (SiOCH), aluminum oxide (AlO_x), hafnium oxide (HfO_x), zirconium oxide (ZrO_2), titanium oxide (TiO_x), titanium nitride (TiN), tantalum oxide (Ta_xO_5), yttrium oxide (Y_2O_3), lanthanum oxide (La_2O_3), aluminum nitride (AlN), magnesium oxide (MgO), calcium fluoride (CaF_2), lithium fluoride (LiF), strontium oxide (SrO), barium oxide (BaO), hafnium silicate (HfSiO_4), lanthanum aluminate (LaAlO_3), niobium pentoxide (Nb_2O_5), barium titanate (BaTiO_3), strontium titanate (SrTiO_3), bismuth titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$), lead zirconium titanate ($\text{Pb}(\text{Zr}, \text{Ti})\text{O}_3$), calcium copper titanate ($\text{CaCu}_3\text{Ti}_4\text{O}_{12}$), lithium niobate (LiNbO_3), barium titanate (BaTiO_3), and potassium niobate (KNbO_3). In one or more specific embodiments, the dielectric surface 104 comprises one or more of silicon oxide

(SiO_x), silicon oxycarbide (SiOC), silicon oxycarbonitride (SiOCN), silicon nitride (SiN), silicon oxynitride (SiON), aluminum oxide (AlO_x), aluminum nitride (AlN), and hafnium oxide (HfO_x).

[0032] In one or more embodiments, the substrate on which the carbon-containing material is formed may include a material in which one or more features 103 may be formed. The substrate features 103 may be characterized by any shape or configuration according to the present technology. In some embodiments, the features 103 may be or include a trench structure, a via structure, or aperture formed within the substrate. Although the substrate features 103 may be characterized by any shapes or sizes, in some embodiments the substrate features may be characterized by higher aspect ratios, or a ratio of a depth of the feature 103 to a width across the feature 103. For example, in some embodiments substrate features 103 may be characterized by aspect ratios greater than or equal to 5:1, and may be characterized by aspect ratios greater than or equal to 10:1, greater than or equal to 15:1, greater than or equal to 20:1, greater than or equal to 25:1, greater than or equal to 30:1, greater than or equal to 40:1, greater than or equal to 50:1, or greater. Additionally, the features 103 may be characterized by narrow widths or diameters across the feature 103 including between two sidewalls, such as a critical dimension less than or equal to 100 nm, or less than or equal to 90 nm, or less than or equal to 80 nm, or less than or equal to 70 nm, or less than or equal to 60 nm or less than or equal to 50 nm or less than or equal to 40 nm or less than or equal to 30 nm, or less than or equal to 20 nm, or less than or equal to 10 nm.

[0033] In one or more embodiments, at operation 14, the one or more of the semiconductor surface 102 and the dielectric surface 104 may optionally be pre-cleaned. In addition to the pre-cleaning the semiconductor surface 102 and/or the dielectric surface 104 itself, in the present disclosure, any of the treatments or pre-treatments disclosed may also be performed on an underlayer metal surface as, and the term "dielectric surface" is intended to include such underlayer as the context indicates.

[0034] In one or more embodiments, the substrate is pre-cleaned with one or more of high temperature annealing, plasma treatment, and gas annealing. Plasma treatment may include treatment with a plasma selected from one or more of

hydrogen (H₂), oxygen (O₂), ammonia (NH₃), nitrogen (N₂), carbon dioxide (CO₂), nitrous oxide (N₂O), argon (Ar), and the like. Gas annealing may include annealing in an atmosphere of one or more of hydrogen (H₂), oxygen (O₂), ozone (O₃), nitrous oxide (N₂O), water (H₂O), hydrogen peroxide (H₂O₂), and the like. In one or more
5 embodiments, the pre-cleaning process of operation 14 removes layers from substrate.

[0035] In some embodiments, the semiconductor surface 102 is cleaned/pre-cleaned with a plasma. In some embodiments, the plasma is a conductively coupled plasma (CCP). In some embodiments, the plasma is an inductively coupled plasma
10 (ICP).

[0036] With reference to FIG. 1 and FIG. 3, at operation 16, a first type of precursor is introduced/flowed into the substrate processing region of a processing chamber and over the substrate surface. The first precursor binds strongly to the semiconductor surface 102 and to the dielectric surface 104.

15 [0037] In one or more embodiments, the first precursor may be a carbon-containing precursor that has at least two reactive groups that can form a bond with a group attached to the semiconductor surface 102 and the dielectric surface 104 of a substrate. Molecules of the first precursor react with the surface groups of the semiconductor surface 102 and the dielectric surface 104 to form bonds linking the
20 first precursor molecule to the semiconductor surface 102 and the dielectric surface 104 of the substrate. The reactions between the first precursor molecules and the groups on the semiconductor surface 102 and the dielectric surface 104 of the substrate continue until most or all the surface groups are bonded to a reactive group on the first precursor molecules. A first portion 105a of a doped carbon-containing
25 layer 106 is formed that blocks further reaction between first precursor molecules in the first precursor effluent and the substrate.

[0038] The first precursor may comprise any suitable precursor known to the skilled artisan. In one or more embodiments, first deposition precursor may have a general formula R¹-(X)_n wherein n is an integer in a range of from 1 to 6, and R¹ comprises
30 one or more of an aryl, or aromatic group, and a cycloalkyl group. X_n comprises one or more of a hydroxide group, an aldehyde group, a ketone group, an acid group, an amino group, an isocyanate group, a thiocyanate group, and an acyl chloride group.

[0039] Unless otherwise indicated, the term "lower alkyl," "alkyl," or "alk" as used herein alone or as part of another group includes both straight and branched chain hydrocarbons, containing 1 to 20 carbons, or 1 to 10 carbon atoms, in the normal chain, such as methyl, ethyl, propyl, isopropyl, butyl, t-butyl, isobutyl, pentyl, hexyl, 5 isohexyl, heptyl, 4,4-dimethylpentyl, octyl, 2,2,4-trimethyl-pentyl, nonyl, decyl, undecyl, dodecyl, the various branched chain isomers thereof, and the like. Such groups may optionally include up to 1 to 4 substituents. The alkyl may be substituted or unsubstituted.

[0040] Such alkyl groups may optionally include up to 1 to 4 substituents such as 10 halo, for example F, Br, Cl, or I, or CF₃, alkyl, alkoxy, aryl, aryloxy, aryl(aryl) or diaryl, arylalkyl, arylalkyloxy, alkenyl, cycloalkyl, cycloalkylalkyl, cycloalkylalkyloxy, amino, hydroxy, hydroxyalkyl, acyl, heteroaryl, heteroaryloxy, heteroarylalkyl, heteroarylalkoxy, aryloxyalkyl, alkylthio, arylalkylthio, aryloxyaryl, alkylamido, alkanoylamino, arylcarbonylamino, nitro, cyano, thiol, haloalkyl, trihaloalkyl, and/or 15 alkylthio, and the like. In one or more embodiments, R¹ is independently selected from C₁₋₂₀ alkyl. In other embodiments, R¹ is from C₁₋₁₂ alkyl.

[0041] As used herein, the term "alkene" or "alkenyl" or "lower alkenyl" refers to straight or branched chain radicals of 2 to 20 carbons, or 2 to 12 carbons, and 1 to 8 20 carbons in the normal chain, which include one to six double bonds in the normal chain, such as vinyl, 2-propenyl, 3-butenyl, 2-butenyl, 4-pentenyl, 3-pentenyl, 2-hexenyl, 3-hexenyl, 2-heptenyl, 3-heptenyl, 4-heptenyl, 3-octenyl, 3-nonenyl, 4-decenyl, 3-undecenyl, 4-dodecenyl, 4,8,12-tetradecatrienyl, and the like, and which may be optionally substituted with 1 to 4 substituents, namely, halogen, haloalkyl, alkyl, alkoxy, alkenyl, alkynyl, aryl, arylalkyl, cycloalkyl, amino, hydroxy, heteroaryl, 25 cycloheteroalkyl, alkanoylamino, alkylamido, arylcarbonyl-amino, nitro, cyano, thiol, alkylthio, and/or any of the alkyl substituents set out herein.

[0042] As used herein, the term "alkynyl" or "lower alkynyl" refers to straight or branched chain radicals of 2 to 20 carbons, or 2 to 12 carbons, or 2 to 8 carbons in the normal chain, which include one triple bond in the normal chain, such as 2- 30 propynyl, 3-butylnyl, 2-butylnyl, 4-pentylnyl, 3-pentylnyl, 2-hexynyl, 3-hexynyl, 2-heptylnyl, 3-heptylnyl, 4-heptylnyl, 3-octynyl, 3-nonylnyl, 4-decynyl, 3-undecynyl, 4-dodecynyl, and the like, and which may be optionally substituted with 1 to 4

substituents, namely, halogen, haloalkyl, alkyl, alkoxy, alkenyl, alkynyl, aryl, arylalkyl, cycloalkyl, amino, heteroaryl, cycloheteroalkyl, hydroxy, alkanoylamino, alkylamido, arylcarbonylamino, nitro, cyano, thiol, and/or alkylthio, and/or any of the alkyl substituents set out herein.

5 **[0043]** The term "halogen" or "halo" as used herein alone or as part of another group refers to chlorine, bromine, fluorine, and iodine as well as CF₃.

10 **[0044]** As used herein, the term "aryl" refers to monocyclic and bicyclic aromatic groups containing 6 to 10 carbons in the ring portion (such as phenyl, biphenyl or naphthyl, including 1-naphthyl and 2-naphthyl) and may optionally include 1 to 3 additional rings fused to a carbocyclic ring or a heterocyclic ring (such as aryl, cycloalkyl, heteroaryl, or cycloheteroalkyl rings). The aryl group may be optionally substituted through available carbon atoms with 1, 2, or 3 substituents, for example, hydrogen, halo, haloalkyl, alkyl, haloalkyl, alkoxy, haloalkoxy, alkenyl, trifluoromethyl, trifluoromethoxy, alkynyl, and the like.

15 **[0045]** Specific examples of first precursor include, but are not limited to, one or more of terephthaldehyde, phenylenediamine, ethylenediamine, hexamethylenediamine, terephthaloyl chloride, 1,3,5-benzenetricarbonyl trichloride, pyromellitic dianhydride, and the like.

20 **[0046]** In one or more embodiments, the formation rate of the first portion 105a of the doped carbon-containing layer 106 may depend on the temperature of the substrate as well as the temperature of the deposition precursors that flow into the substrate processing region. Exemplary substrate temperatures during the formation operations may be greater than or equal to 50 °C, greater than or equal to 60 °C, greater than or equal to 70 °C, greater than or equal to 80 °C, greater than or equal to 90 °C, greater than or equal to 100 °C, greater than or equal to 110 °C, greater than or equal to 120 °C, greater than or equal to 130 °C, greater than or equal to 140 °C, greater than or equal to 150 °C, or higher. By maintaining the substrate temperature elevated, such as above or about 100 °C in some embodiments, an increased number of nucleation sites may be available along the semiconductor surface 102 of the substrate, which may improve formation and reduce void formation by improving coverage at each location.

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[0047] The first precursor effluent may remain in the substrate processing region for a period of time to nearly, or completely, form the first portion 105a of the doped carbon-containing layer 106. The precursors may be delivered in alternating pulses to grow the material. In some embodiments, the pulse times of either or both of the first precursor and the second precursor may be greater than or equal to 0.1 seconds, greater than or equal to 1 second, greater than or equal to 2 seconds, greater than or equal to 3 seconds, greater than or equal to 4 seconds, greater than or equal to 5 seconds, greater than or equal to 10 seconds, greater than or equal to 20 seconds, greater than or equal to 40 seconds, greater than or equal to 60 seconds, greater than or equal to 80 seconds, greater than or equal to 100 seconds, or more.

[0048] With reference to FIG. 1, at operation 18, the first precursor is purged or removed from the substrate processing region following formation of the first portion 105a of the doped carbon-containing layer 106. The effluents of the first precursor may be removed by pumping them out of the substrate deposition region for a period of time ranging from about 10 seconds to about 100 seconds. Additional exemplary time ranges may include about 20 seconds to about 50 seconds, and 25 seconds to about 45 seconds, among other exemplary time ranges. In some embodiments, however, increased purge time may begin to remove reactive sites, which may reduce uniform formation. Accordingly, in some embodiments the purge may be performed for less than or equal to 60 seconds and may be performed for less than or equal to 50 seconds, less than or equal to 40 seconds, less than or equal to 30 seconds, or less. In some embodiments, a purge gas may be introduced to the substrate processing region to assist in the removal of the effluents. Exemplary purge gases include argon (Ar), helium (He), and nitrogen (N₂), among other purge gases.

[0049] Referring to FIG. 1 and FIG. 3B, at operation 20, a second type of precursor reacts with the first precursor to form a second portion 105b of doped carbon-containing layer 106. The second precursor advantageously contains one or more of phosphorus (P), boron (B), aluminum (Al), arsenic (As), gallium (Ga), indium (In), or zinc (Zn). Specific second precursors may be selected from tris(dimethylamino)phosphine, phosphorus trichloride, phosphorus(V) oxychloride, tris(hydroxymethyl)phosphine, boron trichloride, trimethylaluminum, tris(dimethylamino)arsine, trimethylindium, diethylzinc, and the like.

[0050] In one or more embodiments, the second precursor can form bonds with unreacted reactive groups of the first precursor that formed the first portion 105a of the doped carbon-containing layer 106. Molecules of the second precursor react with the unreacted reactive groups of the first precursor to form bonds linking the second precursor molecules to the first precursor molecules. The reactions between the second and first precursor molecules continue until most or all the unreacted reactive groups on the first precursor molecules have reacted with second precursor molecules. A second portion 105b of a doped carbon-containing layer 106 of the deposition precursors is formed that blocks further reaction between second precursor molecules in the second precursor effluent and the first portion 105a of the doped carbon-containing layer 106.

[0051] Referring to FIG. 1, in one or more embodiments, the method 10 also includes an operation 22 to purge or remove the second precursor effluents from the substrate processing region following the formation of the second portion of the doped carbon-containing layer 106. The effluents may be removed by pumping them out of the substrate deposition region for a period of time ranging from about 1 second to about 100 seconds. Additional exemplary time ranges may include about 20 seconds to about 50 seconds, and 25 seconds to about 45 seconds, among other exemplary time ranges. In some embodiments, a purge gas may be introduced to the substrate processing region to assist in the removal of the effluents. Exemplary purge gases include argon, helium, and nitrogen, among other purge gases.

[0052] In one or more embodiments, the formation rate of the second portion of the doped carbon-containing layer 106 may also depend on the pressure of the second precursor effluent in the substrate processing region. Exemplary effluent pressures in the substrate processing region may range from about 1 mTorr to about 20 Torr. Additional exemplary ranges include 5 Torr to 15 Torr, and 9 Torr to 12 Torr, among other exemplary ranges.

[0053] With reference to FIG. 1, in one or more embodiments of the method 10 there is a determination/decision point 24 of whether a target thickness of the as-deposited doped carbon-containing layer 106 on the semiconductor surface 102 and on the dielectric surface of the substrate has been achieved following one or more cycles of forming a doped carbon-containing layer 106 (e.g., following the formation of

the first and second portions of a compound layer). If a target thickness of as-deposited doped carbon-containing layer 106 has not been achieved, another cycle of forming first and second portions of a doped carbon-containing layer 106 is performed. If a target thickness of as-deposited doped carbon-containing layer 106 has been achieved, another cycle to form another doped carbon-containing layer 106 is not started. Exemplary numbers of cycles for the formation of carbon-containing layers may include 1 cycle to 2000 cycles. Additional exemplary ranges for the number of cycles may include 50 cycles to 1000 cycles, and 100 cycles to 750 cycles, among other exemplary ranges.

10 **[0054]** Accordingly, in one or more embodiments, the method 10 further includes depositing at least one additional doped carbon-containing layer on the initial doped carbon-containing layer, where the initial doped carbon-containing layer and the at least one additional doped carbon-containing layer form the doped carbon-containing layer 106 on the semiconductor and dielectric surfaces of the substrate.

15 **[0055]** In one or more embodiments, the doped carbon-containing layer 106 may have any suitable thickness. In one or more embodiments, the thickness of at least 1 nm, or at least 10 nm, or at least 100 nm, or at least 200 nm, or at least 500 nm, or at least 1000 nm. Exemplary ranges of target thickness to discontinue further cycles of forming compound layers include about 10 nm to about 500 nm. Additional exemplary thickness ranges may include about 50 nm to about 300 nm, and 100 nm to about 200 nm, among other exemplary thickness ranges.

20 **[0056]** In the embodiment shown in method 10 of FIG. 1, the as-deposited doped carbon-containing layer 106 on the semiconductor surface 102 and on the dielectric surface 104 of the substrate may be etched from the untargeted area 102, 104 at operation 26. In one or more embodiments, the targeted area is the target doping surface.

25 **[0057]** In the embodiment shown in method 10 of FIG. 1 and FIG. 4, the doped carbon-containing layer 106 is thermally annealed at operation 28. In one or more embodiments, thermal annealing is used to drive in/diffuse the dopant (one or more of phosphorus (P), boron (B), aluminum (Al), arsenic (As), gallium (Ga), indium (In), or zinc (Zn)) into the substrate. In one or more embodiments, the annealing is a thermal annealing at a temperature greater than 400 °C. In some embodiments, the annealing

is a thermal annealing process at a temperature in a range of from 400 °C to 1200 °C, or at a temperature in a range of from 600 °C to 800 °C. In one or more embodiments, the thermal annealing process is a one-step annealing process. In other embodiments, the thermal annealing process is two or more steps at different
5 temperatures. The annealing environment of some embodiments comprises one or more of an inert gas (e.g., molecular nitrogen (N₂), argon (Ar)) or a reducing gas (e.g., molecular hydrogen (H₂) or ammonia (NH₃)) or an oxidant, such as, but not limited to, oxygen (O₂), ozone (O₃), or peroxides. Annealing can be performed for any suitable length of time. In some embodiments, the carbon-containing layer is annealed for a
10 predetermined time in the range of about 1 second to about 90 minutes, or in the range of about 1 minute to about 60 minutes.

[0058] In the embodiment shown in method 10 of FIG. 1 and FIG. 5, the doped carbon-containing layer 106 is then subjected to a plasma treatment process at operation 30 to remove the doped carbon-containing layer 106. The plasma may
15 comprise one or more of hydrogen (H₂), argon (Ar), ammonia (NH₃), or oxygen (O₂).

[0059] In some embodiments, the processing region is in a modular system comprising multiple chambers which perform various functions including substrate center-finding and orientation, degassing, annealing, deposition and/or etching. According to one or more embodiments, the modular system includes at least a first
20 processing chamber and a central transfer chamber. The central transfer chamber may house a robot that can shuttle substrates between and among processing chambers and load lock chambers. The transfer chamber is typically maintained at a vacuum condition and provides an intermediate stage for shuttling substrates from one chamber to another and/or to a load lock chamber positioned at a front end of the
25 cluster tool. Any suitable modular system known to the skilled artisan may be adapted for the present disclosure. However, the exact arrangement and combination of chambers may be altered for purposes of performing specific steps of a process as described herein. Other processing chambers which may be used include, but are not limited to, cyclical layer deposition (CLD), atomic layer deposition (ALD), chemical
30 vapor deposition (CVD), physical vapor deposition (PVD), etch, pre-clean, chemical clean, thermal treatment such as RTP, plasma nitridation, degas, orientation, hydroxylation, and other substrate processes. By carrying out processes in the

processing chamber of modular system, surface contamination of the substrate with atmospheric impurities can be avoided without oxidation prior to depositing a subsequent film.

[0060] According to one or more embodiments, the substrate is continuously under vacuum or "load lock" conditions and is not exposed to ambient air when being moved from one chamber to the next. The transfer chambers are thus under vacuum and are "pumped down" under vacuum pressure. Inert gases may be present in the processing chambers or the transfer chambers. In some embodiments, the inert gas is used to purge or remove some or all of the reactants (e.g., reactant). According to one or more embodiments, the inert gas is injected at the exit of the processing chamber to prevent reactants (e.g., reactant) from moving from the processing chamber to the transfer chamber and/or additional processing chamber. Thus, the flow of inert gas forms a curtain at the exit of the chamber.

[0061] The substrate can be processed in single substrate deposition chambers, where a single substrate is loaded, processed, and unloaded before another substrate is processed. The substrate can also be processed in a continuous manner, similar to a conveyer system, in which multiple substrates are individually loaded into a first part of the chamber, move through the chamber, and are unloaded from a second part of the chamber. The shape of the chamber and associated conveyer system can form a straight path or curved path. Additionally, the processing chamber may be a carousel in which multiple substrates are moved about a central axis and are exposed to deposition, etch, annealing, cleaning, etc. processes throughout the carousel path.

[0062] During processing, the substrate can be heated or cooled. Such heating or cooling can be accomplished by any suitable means including, but not limited to, changing the temperature of the substrate support, and flowing heated or cooled gases to the substrate surface. In some embodiments, the substrate support includes a heater/cooler which can be controlled to change the substrate temperature conductively. In one or more embodiments, the gases (either reactive gases or inert gases) being employed are heated or cooled to locally change the substrate temperature. In some embodiments, a heater/cooler is positioned within the chamber adjacent the substrate surface to convectively change the substrate temperature.

[0063] The substrate can also be stationary or rotated during processing. A rotating substrate can be rotated (about the substrate axis) continuously or in discrete steps. For example, a substrate may be rotated throughout the entire process, or the substrate can be rotated by a small amount between exposures to different reactive or
5 purge gases. Rotating the substrate during processing (either continuously or in steps) may help produce a more uniform deposition or etch by minimizing the effect of, for example, local variability in gas flow geometries.

[0064] In a spatial ALD process, the reactive gases are flowed into different processing regions within a processing chamber. The different processing regions are
10 separated from adjacent processing regions so that the reactive gases do not mix. The substrate can be moved between the processing regions to separately expose the substrate to the reactive gases. During substrate movement, different portions of the substrate surface, or material on the substrate surface, are exposed to the two or more reactive gases so that any given point on the substrate is substantially not
15 exposed to more than one reactive gas simultaneously. As will be understood by those skilled in the art, there is a possibility that a small portion of the substrate may be exposed to multiple reactive gases simultaneously due to diffusion of the gases within the processing chamber, and that the simultaneous exposure is unintended, unless otherwise specified.

[0065] In another aspect of the spatial ALD process, the reactive gases are delivered simultaneously to the reaction zone but are separated by an inert gas curtain and/or a vacuum curtain. The gas curtain can be combination of inert gas
20 flows into the processing chamber and vacuum stream flows out of the processing chamber. The substrate is moved relative to the gas delivery apparatus so that any given point on the substrate is exposed to only one reactive gas.

[0066] A "pulse" or "dose" as used herein refers to a quantity of a source gas that is intermittently or non-continuously introduced into the process chamber. The quantity of a particular compound within each pulse may vary over time, depending on the duration of the pulse. A particular process gas may include a single compound or a
30 mixture/combination of two or more compounds.

[0067] In a time-domain ALD process in some embodiments, exposure to each reactive gas, which includes but not limited to the metal and dielectric material to be

used for the ALD film, is separated by a time delay to allow each compound to adhere and/or react on the substrate surface and then be purged from the processing chamber. The reactive gases are prevented from mixing by the purging of the processing chamber between subsequent exposures.

5 [0068] In another aspect of a time-domain ALD process of some embodiments, a time delay exists between pulses of reactive gases. During each time delay, a purge gas, such as argon, is introduced into the processing chamber to purge the reaction zone or otherwise remove any residual reactive gas or reaction products or by-products from the reaction zone. Alternatively, the purge gas may flow continuously
10 throughout the deposition process so that only the purge gas flows during the time delay between pulses of reactive gases. The reactive gases are alternatively pulsed with a pulse of purge gas there between multiple times. The purge may also be achieved with a vacuum pump with or without an inert gas.

[0069] The durations for each pulse/dose are variable and may be adjusted to
15 accommodate, for example, the volume capacity of the processing chamber as well as the capabilities of a vacuum system coupled thereto. Additionally, the dose time of a reactive gas may vary according to the flow rate of the reactive gas, the temperature of the process gas, the type of control valve, the type of process chamber employed, as well as the ability of the components of the process gas to adsorb onto the
20 substrate. Dose times may also vary based upon the type of layer being formed and the geometry of the device being formed. A dose time should be long enough to provide a volume of compound sufficient to adsorb/chemisorb onto substantially the entire surface of the substrate and form a layer of a process gas component thereon.

[0070] Once the carbon-containing layer is deposited, the method may optionally
25 include further processing (e.g., bulk deposition of a dielectric film). In some embodiments, the further processing may be an ALD process.

[0071] The disclosure provides that the processes may generally be stored in the memory as a software routine that, when executed by the processor, causes the process chamber to perform processes of the present disclosure. The software
30 routine may also be stored and/or executed by a second processor (not shown) that is remotely located from the hardware being controlled by the processor. Some or all of the method of the present disclosure may also be performed in hardware. As such,

the process may be implemented in software and executed using a computer system, in hardware as, e.g., an application specific integrated circuit or other type of hardware implementation, or as a combination of software and hardware. The software routine, when executed by the processor or controller, transforms the general-purpose computer into a specific purpose computer (controller) that controls the chamber operation such that the processes are performed. The process can be stored on non-transitory computer readable medium including instructions, that, when executed by a controller of a substrate processing chamber, causes the substrate processing chamber to perform the operations of: flow a first precursor over a substrate comprising a semiconductor surface and a dielectric surface to form a first portion of a doped carbon-containing film on the semiconductor surface and on the dielectric surface, the first precursor comprising a first reactive group; remove a first precursor effluent comprising the first precursor from the substrate; flow a second precursor comprising a second reactive group over the substrate to react with the first reactive group to form a second portion of the doped carbon-containing film on the semiconductor surface and on the dielectric surface; remove a second precursor effluent comprising the second precursor from the substrate; and anneal the doped carbon-containing film to form an annealed doped carbon-containing layer on the semiconductor surface and on the dielectric surface.

[0072] Reference throughout this specification to "one embodiment," "certain embodiments," "one or more embodiments" or "an embodiment" means that a particular feature, structure, material, or characteristic described in connection with the embodiment is included in at least one embodiment of the disclosure. Thus, the appearances of the phrases such as "in one or more embodiments," "in certain embodiments," "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily referring to the same embodiment of the disclosure. Furthermore, the particular features, structures, materials, or characteristics may be combined in any suitable manner in one or more embodiments.

[0073] Although the disclosure herein has been described with reference to particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present disclosure. It will be apparent to those skilled in the art that various modifications and variations can be

made to the method and apparatus of the present disclosure without departing from the spirit and scope of the disclosure. Thus, it is intended that the present disclosure include modifications and variations that are within the scope of the appended claims and their equivalents.

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What is claimed is:

1. A method of semiconductor doping, the method comprising:
flowing a first precursor over a substrate comprising a semiconductor surface
5 and a dielectric surface to form a first portion of a doped carbon-containing layer on
the semiconductor surface and on the dielectric surface, the first precursor comprising
a first reactive group;
removing a first precursor effluent comprising the first precursor from the
substrate;
10 flowing a second precursor comprising one or more of phosphorus (P), boron
(B), aluminum (Al), arsenic (As), gallium (Ga), indium (In), or zinc (Zn) over the
substrate to react with the first reactive group to form the doped carbon-containing
layer on the semiconductor surface and on the dielectric surface; and
removing a second precursor effluent comprising the second precursor from
15 the substrate.
2. The method of claim 1, wherein the first precursor has a general formula R^1-
 $(X)_n$
wherein R^1 comprises one or more of an alkyl group, an alkenyl group, an
20 aryl, or aromatic group, and a cycloalkyl group, $(X)_n$ comprises one or more of a
hydroxide group, an aldehyde group, a ketone group, an acid group, an amino group,
an isocyanate group, a thiocyanate group, and an acyl chloride group, and n is an
integer in a range of from 1 to 6.
- 25 3. The method of claim 1, wherein the first precursor is selected from one or more
terephthalaldehyde, phenylenediamine, ethylenediamine, hexamethylenediamine,
terephthaloyl chloride, 1,3,5-benzenetricarbonyl trichloride, and pyromellitic
dianhydride.
- 30 4. The method of claim 1, wherein the second precursor is selected from one or
more of Tris(dimethylamino)phosphine, Phosphorus trichloride, Phosphorus(V)

oxychloride, Tris(hydroxymethyl)phosphine, Boron trichloride, Trimethylaluminum, Tris(dimethylamino)arsine, Trimethylindium, and Diethylzinc.

5 5. The method of claim 1, further comprising pre-cleaning the semiconductor surface and the dielectric surface.

6. The method of claim 1, further comprising depositing at least one additional doped carbon-containing layer on the doped carbon-containing layer.

10 7. The method of claim 1, wherein removing the first precursor comprises:
flowing a purge gas over the substrate; and
removing a mixture of the first precursor effluent and the purge gas from the substrate.

15 8. The method of claim 7, wherein the purge gas is selected from argon (Ar), helium (He), and nitrogen (N₂).

9. The method of claim 1, further comprising annealing the doped carbon-containing layer at a temperature in a range of from 400 °C to 1200 °C.

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10. The method of claim 9, wherein the doped carbon-containing layer is annealed at a temperature in a range of from 600 °C to 800 °C.

11. The method of claim 1, further comprising exposing the doped carbon-containing layer to a plasma treatment to remove the doped carbon-containing layer from the semiconductor surface and from the dielectric surface.

25

12. The method of claim 1, further comprising etching the doped carbon-containing layer at an untargeted area.

30

13. A method of semiconductor doping, the method comprising:

flowing a first precursor over a substrate comprising a semiconductor surface and a dielectric surface, the first precursor having a general formula $R^1-(X)_n$

5 wherein R^1 comprises one or more of alkyl group, an alkenyl group, an aryl, or aromatic group, and a cycloalkyl group, X_n comprises one or more of a hydroxide group, an aldehyde group, a ketone group, an acid group, an amino group, an isocyanate group, a thiocyanate group, and an acyl chloride group, and n is an integer in a range of from 1 to 6,

10 wherein the first precursor reacts with a reactive group on one or more of the semiconductor surface and the dielectric surface to form a first portion of a doped carbon-containing layer on one or more of the semiconductor surface and the dielectric surface;

removing a first precursor effluent comprising the first precursor from the substrate;

15 flowing a second precursor over the substrate, the second precursor comprising one or more of phosphorus (P), boron (B), aluminum (Al), arsenic (As), gallium (Ga), indium (In), and zinc (Zn),

wherein the second precursor reacts with the first portion to form a doped carbon-containing layer; and

20 removing a second precursor effluent comprising the second precursor from the substrate.

14. The method of claim 13, wherein the first precursor and the second precursor are independently selected from one or more of terephthalaldehyde, phenylenediamine, ethylenediamine, hexamethylenediamine, terephthaloyl chloride, 1,3,5-
25 benzenetricarbonyl trichloride, pyromellitic dianhydride, tris(dimethylamino)phosphine, phosphorus trichloride, phosphorus(V) oxychloride, tris(hydroxymethyl)phosphine, boron trichloride, trimethylaluminum, tris(dimethylamino)arsine, trimethylindium, and diethylzinc.

30 15. The method of claim 13, further comprising pre-cleaning one or more of the semiconductor surface and the dielectric surface.

16. The method of claim 13, further comprising depositing at least one additional doped carbon-containing layer on the doped carbon-containing layer.
17. The method of claim 13, wherein removing the first precursor comprises:
5 flowing a purge gas over the substrate; and
 removing a mixture of the first precursor effluent and the purge gas from the substrate.
18. The method of claim 17, wherein the purge gas is selected from argon (Ar),
10 helium (He), and nitrogen (N₂).
19. The method of claim 13, further comprising annealing the doped carbon-containing layer at a temperature in a range of from 400 °C to 1200 °C.
- 15 20. The method of claim 13, further comprising exposing the doped carbon-containing layer to a plasma treatment to remove the doped carbon-containing layer from one or more of the semiconductor surface and the dielectric surface.

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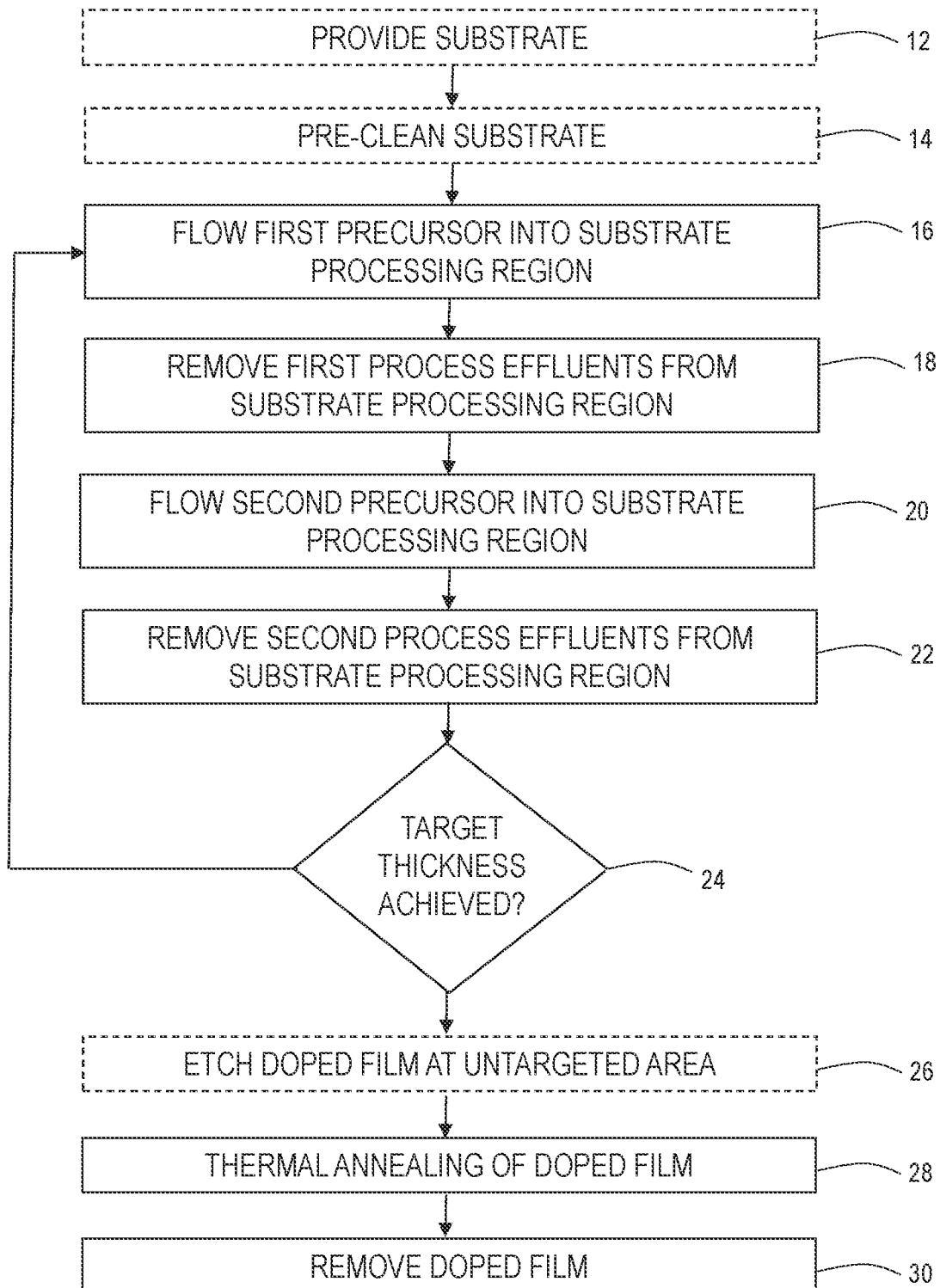


FIG. 1

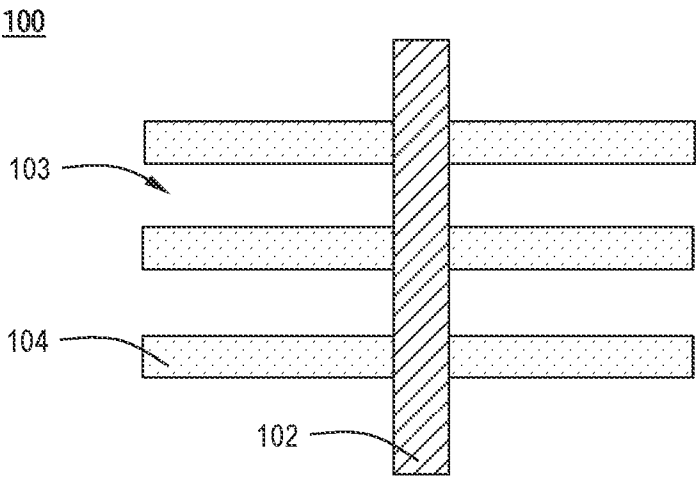


FIG. 2

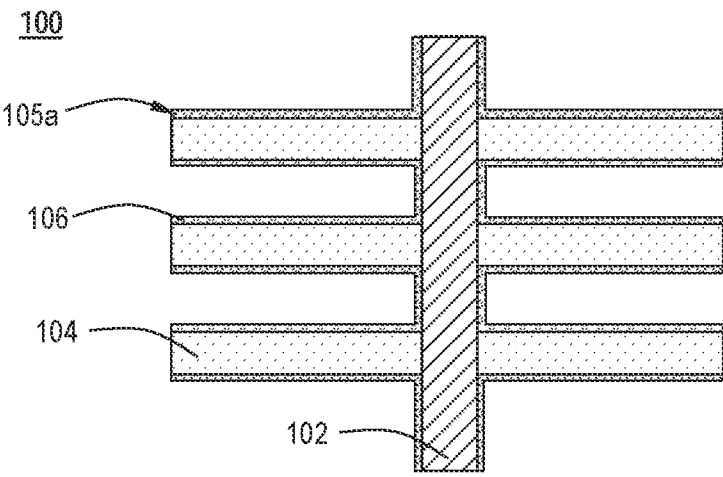


FIG. 3A

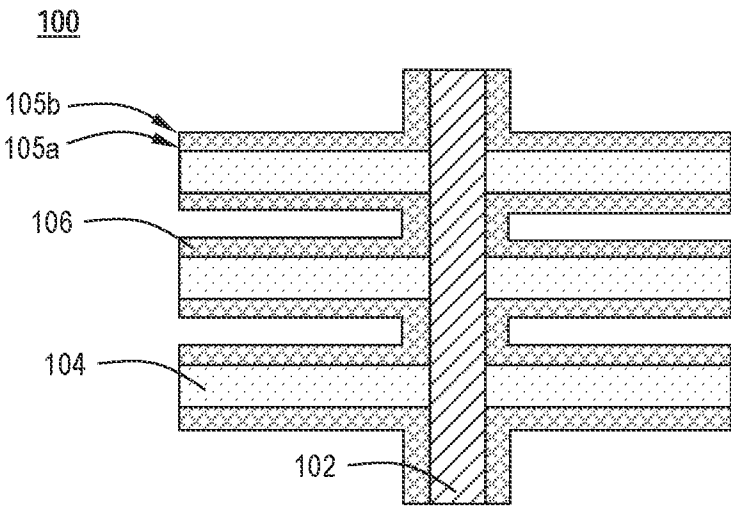


FIG. 3B

100

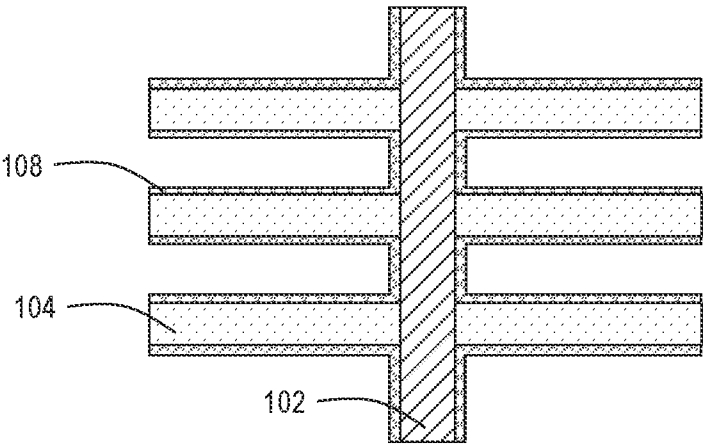


FIG. 4

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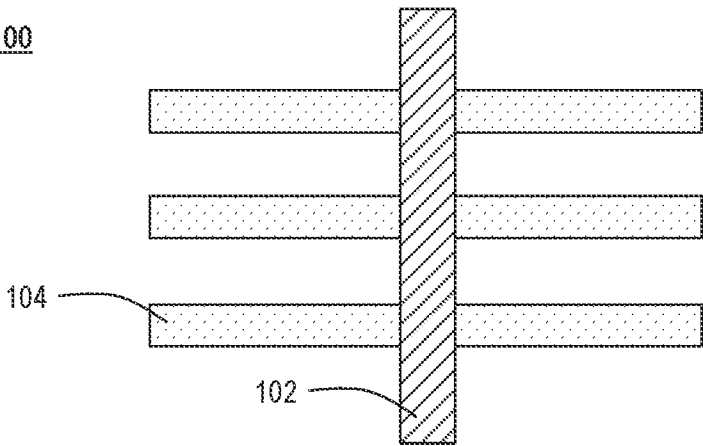


FIG. 5