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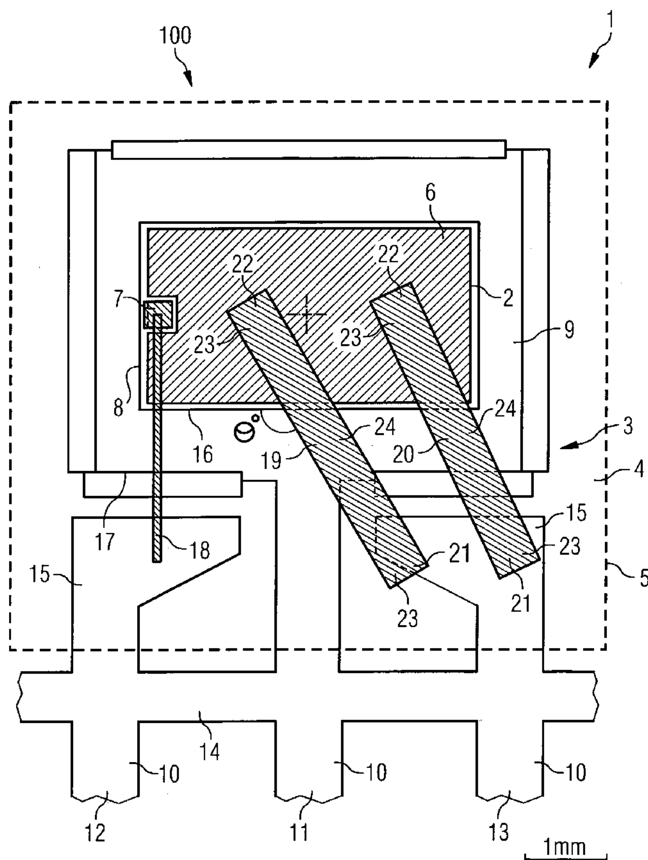

(57) Abstract: A method is provided by which the current carrying capacity of a semiconductor component (1; 25; 31; 35) having a standard package outline and a standard pin arrangement may be increased. The semiconductor component (1; 25; 31; 35) comprises a semiconductor device (2; 27) and a leadframe (3). A package layout (100) is defined and the orientation of the electrically conductive means (19, 20) with respect to a semiconductor device (2; 27) and inner contact area (15) of the leadframe (3) is altered so as to maximise the interfacial bonding area (23). The constraints of the standard package dimensions and the component assembly method are taken into account.

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Description

WIRE-BONDED SEMICONDUCTOR COMPONENT AND MANUFACTURING METHOD THEREOF

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The invention relates to methods for increasing the current carrying capacity of a semiconductor component and to semiconductor components with increased current carrying capacity.

10 High power semiconductor components such as diodes and transistors, e.g MOSFETs and IGBTs, are normally provided to the customer as a packaged semiconductor component. The packaged semiconductor component, typically, has one of a number of standard package outlines which conforms to agreed industry
15 standards regarding the outer form and dimensions of the plastic package as well as the number, dimensions and spacing of the pins. A standard package outline has the advantage that the component can be simply mounted on standardised printed circuit boards.

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However, the packages suffer from the disadvantage that the current carrying capacity is limited. In order to increase the current carrying capacity, it is known, for example from US 2003/0011051, to provide two or more bonding wires which are
25 connected in parallel between the power electrode of the semiconductor die and the source lead of the leadframe.

The leadframe and package outline are also modified in order to further increase the current carrying capacity. The pin se-
30 quence of the package is changed in order to increase the size of the source post, or inner contact area of the source pin. Additionally, the cross-sectional area of the external por-

tions of the pins is increased to increase the current carrying capacity of the package.

However, although the current carrying capacity may be increased by modifying the package and pins, the advantages offered to the user of a standard package outline and a standard pin arrangement are lost. The user, therefore, has to modify the board in order to be able to mount the modified package. This increases the complexity for the user and increases the costs which can outweigh the benefit of a higher current carrying capacity.

It is, therefore, an object of the invention to provide methods by which the current carrying capacity of a semiconductor component with a standard package outline and a standard pin arrangement may be increased.

It is a further object of the invention to provide a semiconductor component with an increased current carrying capacity which retains the advantages of a standard package outline and a standard pin arrangement.

These objects are achieved with the subject matter of the independent claims.

Further advantageous developments are the subject matter of the dependent claims.

According to the invention, a method for increasing the current carrying capacity of a semiconductor component having a standard package outline and a standard pin arrangement comprises the following steps.

Firstly, a package layout is defined. The package layout comprises a die pad having an edge defining a first line and lateral dimensions. The package layout also comprises a plurality of leads disposed on one side of the die pad. Each lead has an inner portion and an outer portion. At least one drain lead extends from the die pad in a direction defining a second line. The inner portion of each of the remaining leads comprises an inner contact area which is spaced at a distance from the die pad. Each of the remaining leads extends in a direction parallel to the second line. The inner contact area of each remaining lead has maximum allowable dimensions. The package layout further comprises a semiconductor device, which has lateral dimensions which are equal to or less than the lateral dimensions of the die pad, and a plurality of electrically conductive connecting means.

In the next step of the method, the area of the inner contact area is defined and the cross-sectional area of the electrically conductive connecting means is defined. When the electrically conductive connecting means is bonded to a surface an interfacial bonding area is created between the electrically conductive connecting means and the surface. The interfacial bonding area of the electrically conductive connecting means having the defined cross-sectional area after it is bonded to a surface is calculated. The following optimisation method is then performed:

(a) a first end of the electrically conductive connecting means is orientated with respect to the second line to maximise the interfacial bonding area between the electri-

cally conductive connecting means and the inner contact area;

(b) a second end of the electrically conductive connecting means is orientated with respect to the first line to maximise the interfacial bonding area between the electrically conductive connecting means and the upper surface of the semiconductor device;

(c) the semiconductor device is orientated with respect to the first line so that the central portion of the electrically conductive connecting means has an orientation with respect to the edge of the semiconductor device which is as close to 90° as possible and so that the semiconductor device remains within the area of the die pad;

(d) the unoccupied area of the inner contact area is determined;

(e) it is then determined if the unoccupied area is equal to or larger than a predetermined value. The predetermined value is the area required by the bonding tool clamps. If the unoccupied area is not equal to or larger than a predetermined value step (f) is performed. If the unoccupied area is equal to or larger than a predetermined value step (g) is performed,

(f) the relationship between the area of the inner contact area and the cross-sectional area of the electrically conductive connecting means is changed by increasing the area of the inner contact area and/or decreasing the cross-sectional area of the electrically conductive connecting

means. The interfacial bonding area is calculated and steps a to e of the method are repeated;

(g) it is then determined if the unoccupied area is larger than a second predetermined value. The second predetermined value defining a non-optimum interfacial area. If the unoccupied area is larger than the second predetermined value, the cross-sectional area of the electrically conductive connecting means is increased, the interfacial bonding area is calculated and steps a to e are repeated. If the unoccupied area is not larger than a second predetermined value, the determined values are output.

The values which may be determined by the method according to the invention are: the area of the inner contact area; the cross-sectional area of the electrically conductive connecting means; the orientation of the first end of the electrically conductive means with respect to the second line; the orientation of the second end of the electrically conductive means with respect to the first line, and the orientation of the semiconductor device on the die pad. The interfacial bonding area and the unoccupied area of the inner contact area may also be output.

These values are used in the assembly of the semiconductor component in order that the resulting component has an increased current carrying capacity.

A semiconductor component may then be assembled by firstly providing a lead frame in which the inner contact area has lateral dimensions and an area as determined by the method according to the invention.

The semiconductor device is then mounted on the die pad with an orientation with respect to the first line, defined by an edge of the die pad, as determined by the method according to
5 the invention.

The semiconductor device is electrically connected to the inner contact area by electrically conductive connecting means having a cross-sectional area according to the invention. The
10 electrically conductive connecting means is orientated of with respect to the semiconductor device and to the inner contact area as determined by the method according to the invention.

In a further step of the assembly, further electrical connec-
15 tions may be provided between control contacts, such as the gate contact, and the lead frame. The semiconductor device, die pad, electrically conductive connecting means and the inner portions of the leads are then encapsulated in a plastic molding compound. This is performed, typically, by a transfer
20 molding process in which the mold provides the component with a plastic housing mass with outer surfaces which correspond to the desired standard package outline.

The method according to the invention provides a method by
25 which the current carrying capacity of a semiconductor component may be increased without modifications to the package outline or to the pin arrangement. The method provides a means by which the internal layout of the package is improved, and may be optimised, so as to increase the current carrying ca-
30 pacity.

In this context, the pin arrangement is used to denote the external portions of the pins which are seen by the customer or user. The pin arrangement refers to the size of the individual pins, their spacing from each other and their arrangement with respect to the plastic package housing of the component.

This optimisation of the internal layout of the package has the further advantage that a semiconductor device with a particular current demand may be accommodated in a component having a smaller package outline. This is particularly desirable as the miniaturisation of microelectronic systems without a loss in power or functionality is, in general, one of the driving forces behind developments in this technical field.

The method according to the invention provides a method by which the interfacial area between the semiconductor device and the electrically conductive connecting means and between the inner contact area of the lead of the leadframe and the electrically conductive connecting means is optimised within the confines of the standard package outline.

Therefore, the method also provides the maximum interfacial bonding area allowable for an inner contact area which itself has maximum allowable dimensions due to the standard package outline. An increased interfacial bonding area reduces the resistance of the electrically conductive connecting means and enables a larger current to be carried.

Additionally, the method according to the invention takes the assembly process into account. The electrically conductive connecting means is typically attached to the semiconductor device to the inner contact area using a bonding tool. For

electrically conductive connecting means in the form of bond wires among this is performed by a wire bonder. The bonding tool, typically, has clamps which are in contact with the lead frame, and, in particular, the inner contact area during the
5 bonding process. This prevents movement of the leads and the lead frame during the bonding process.

The method according to the invention provides a method by which the interfacial bonding area is maximised while leaving
10 sufficient area of unoccupied that the bonding tool can be placed on the inner contact area. The bonding process can, therefore, be reliably carried out.

The method also includes the feature that the electrically
15 conductive connecting means is orientated with respect to the semiconductor device so that the central portion of the electrically conductive connecting means has an orientation which is as close to 90° as possible to the edge of the semiconductor device. This orientational relationship increases the in-
20 terfacial bonding area and enables the length of the connection to be reduced. This reduces the inductance of the wire which further improves the functionality of the component. This feature of the method also further improves the reliability of the bonding process as well as the reliability of the
25 electrical connection after it has been formed.

Furthermore, the method also includes a step by which the orientation of the semiconductor device on the die pad is altered under the constraint that the semiconductor device remains
30 within the area of the die pad. Therefore, the outline of the package is not changed. The semiconductor device is orientated with respect to the edge of the die pad so that the central

portion of the electrically conductive connecting means has an orientation with respect to the edge of the semiconductor device which is as close to 90° as possible. This reduces the length of the electrically conducting connecting means which reduces resistive losses and increases the current carrying capacity of the component.

In an embodiment, the cross-sectional area of the electrically conductive connecting means is selected from a plurality of pre-defined values. This embodiment takes into account that electrically conductive connecting means, such as bond wires, are typically provided by a manufacturer which provides the material in a limited range of standard sizes. This material is cheaper than material made specifically for a customer order. Therefore, this embodiment of the method allows for the optimisation of standard sized electrically conductive connecting means within the standard package housing. This optimises the current carrying capacity of the component while keeping the cost of the component as low as possible.

In an embodiment, the electrically conductive connecting means is provided by a bond wire with an essentially circular cross-section. In an alternative embodiment, the electrically conductive connecting means is provided by a foil with an essentially rectangular cross-section.

In an embodiment, the first end of the electrically conductive connecting means is orientated approximately perpendicular to the second line. This arrangement maximises the interfacial bonding area between the bond formed at the first end of the electrically conductive connecting means and the inner contact area. The further embodiment, the second end of the electri-

cally conductive connecting means is orientated approximately parallel to the first line. In this embodiment, the interfacial bonding area is maximised between the bond at the second end of the electrically conductive connecting means and the semiconductor device.

In a further embodiment, both the first end and the second end are orientated approximately perpendicular to the edge of the inner contact area and semiconductor device respectively. The edge of the inner contact area is essentially parallel to the first line defined by the edge of the die pad and essentially perpendicular to the second line defined by the drain lead. This type of bond is commonly referred to as an S bond.

In a further embodiment of the invention, the first predetermined value defining the unoccupied area of the inner contact area required by the bonding tool clamps is the area required by the bonding tool clamps in a single pass bonding process.

In a single pass bonding process, all of the bonds connecting the semiconductor device to the inner contact area are performed with the bonding tool clamps in one position. Two or more physically isolated electrically conductive connecting means may be connected in parallel between the semiconductor device and the inner contact area without re-positioning the bonding tool clamps. This embodiment has the advantage that the provision of two or more electrically conductive connecting means connected in parallel further reduces the resistance of the current carrying pass within the package outline. As all of the bonds are formed using one position of the bonding tool clamps, the bonding process can be carried out efficiently.

In an alternative embodiment, the first predetermined value defining the unoccupied area of the inner contact area required by the bonding tool clamps is the area required by the bonding tool clamps in a two pass bonding process.

In a two pass bonding process, the bonding tool clamps are placed on the inner contact area and/or lead frame in a first position while a first electrically conductive connecting means is electrically connected between the semiconductor device and the inner contact area. After the first electrically conductive connecting means is bonded, the bonding tool clamps are moved to a second position. A second electrically conductive connecting means is then provided between the semiconductor device and the inner contact area. The first and second electrically conductive connecting means are connected in parallel between the semiconductor device and the inner contact area so as to reduce the resistance of the current path.

A two pass bonding process has the advantage that the area of the inner contact, which will be later occupied by the second electrically conductive connecting means, can be used by the bonding tool clamp while attaching the first electrically conductive connecting means. This can provide a more reliable clamping of the bonding tool on the lead frame during the first pass.

In a further embodiment, it is also possible that the wire bonding tool clamps are outside of the inner contact area during the second pass, i.e. when the second electrically conductive conducting means is produced between the semiconductor device and the inner contact area. This is possible due to the

stability provided to the lead frame and inner contact area by the first electrically conductive connecting means. This embodiment has the advantage that the area, which is unoccupied by the interfacial bonding areas, is reduced. Therefore, the interfacial bonding area may be increased. This further reduces the resistance of the current path and can also enable the current carrying capacity of the component to be increased.

Their further embodiment, the following additional steps may be carried out after step (d) of the optimisation process outlined above.

The area required by each bonding tool clamp within the area of the inner contact area is defined and the lateral position of the bonding tool clamp within the area of the inner contact area is defined. The lateral position of the unoccupied area of the inner contact area is determined. A comparison of the lateral position of the unoccupied area and the defined lateral position of the bonding tool clamp and the defined area required by the bonding tool clamp is carried out. If the defined lateral position of the bonding tool clamp and the defined area required by the bonding tool clamp lie outside the lateral position of the unoccupied area, step (f) of the method described above is performed. If the defined lateral position of the bonding tool clamp and the defined area required by the bonding tool clamp lie within the lateral position of the unoccupied area step (g) of the method described above is performed.

This embodiment of the invention takes into account the lateral position of each bonding clamp within the area of the in-

ner contact area. Therefore, the different area requirements for a single pass and a two pass bonding process can be taken into account and the interfacial bonding area maximised accordingly.

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The invention also provides a semiconductor component having a standard package outline and a standard pin arrangement which comprises a die pad having an edge defining a first line and having a lateral dimensions. The component also comprises a
10 plurality of leads disposed on one side of the die pad. Each lead has an inner portion and an outer portion. At least one drain lead extends from the die pad in a direction defining a second line. The inner portion of each of the remaining leads comprises an inner contact area which is spaced at a distance
15 from the die pad. Each lead extends in a direction parallel to the second line. The semiconductor component also comprises a semiconductor device having lateral dimensions which are equal to or less than the lateral dimensions of the die pad and a plurality of electrically conductive connecting means. The
20 standard package outline is a TO252 package outline and the electrically conductive connecting means comprise bond wires with a diameter of greater than approximately 350 µm.

The semiconductor component, therefore, comprises bond wires
25 with a larger diameter than can be conventionally used in component with a TO252 package outline. Therefore, the current carrying capacity of the component can be increased by using the method of the invention to optimise the internal layout of the component so that the diameter of the bond wires may be
30 increased and the component can be reliably assembled. In an embodiment, the component comprises two bond wires with a diameter of 350 µm which stretch between the semiconductor de-

vice and a single inner contact pad. In this embodiment, the component also has a TO252 package outline.

In further embodiment, the component comprises two or more bond wires with a diameter of approximately 500 µm. The two or more bond wires reach between the semiconductor device and a single inner contact area. The provision of two bond wires with a diameter of approximately 500 µm further increases the current carrying capacity of a component with a TO252 package outline.

In a further embodiment, the semiconductor device is orientated with respect to the first line, defined by an edge of the die pad, by an angle θ, where $0° < \theta < 90°$. The semiconductor device is orientated so that the angle formed between the central portion of the bond wire and the edge of the semiconductor device is as close to 90° as possible under the constraint that the semiconductor device is located within the lateral dimensions of the die pad. The semiconductor device can be mounted inside the standard package outline which avoids modifying the standard dimensions of the package.

As the angle formed between the central portion of the bond wires and the edge of the semiconductor device is as close to 90° as possible, the length of the bond wire between the semiconductor device and the inner contact area can be reduced and may be chosen to be as short as possible. This reduces inductance and improves the functionality of the device. In addition, the heat dissipated by the component is reduced which further improves the functionality of the component, for example the switching speed of a transistor.

In an embodiment, the semiconductor device is a high power semiconductor device. The high power semiconductor device may be a power switching device such as a MOSFET, a IGBT, a BJT or a diode. The power switching device may also be a vertical power device.

In the description, the semiconductor power switch is described as having at least one source electrode, at least one drain electrode and at least one gate electrode as is used for MOSFET switches. However, this nomenclature is not intended to limit the semiconductor power switch to a MOSFET. For other types of semiconductor power switch, this nomenclature refers to the corresponding feature. For a BJT, gate corresponds to base, source corresponds to emitter and drain corresponds to collector. For a IGBT, source corresponds to emitter and drain corresponds to collector.

In summary, the invention provides a method by which the current carrying capacity of a semiconductor component with a standard package outline and a standard pin arrangement can be increased. In one embodiment of the invention, a semiconductor component is provided which has a TO252 outline, also known as a Dpak 3 package, which includes two bond wires with a diameter of 350 µm. The bond wires comprise aluminium and provide two parallel electrical connections between the source inner contact area or source lead post and a semiconductor MOSFET device.

In a further embodiment, a component with a TO252 package outline comprises two aluminium source leads connected in parallel between the source contact of the semiconductor device and the inner contact area of the source lead which each have a

diameter of 500 μm. The current carrying capacity of the package is increased to around 90 Amps.

The invention, therefore, provides a Dpak 3 package which is suitable for applications requiring 90 Amps. In conventional packages, this capacity is provided only by Dpak5 packages which have 5 pins and are much larger. The invention, therefore, provides a package without redundant leads and removes the design constraints of the PCB layout which arise as a result of the use of a Dpak5 package for the MOSFET device.

Embodiments of the invention will now be described with reference to the diagrams.

Figure 1 illustrates a semiconductor component assembled after a first iteration of the method of the invention;

Figure 2 shows a semiconductor component assembled after a second iteration of the method according to the invention is performed on the component of Figure 1,

Figure 3 illustrates the assembly of a semiconductor component according to a second embodiment of the invention,

Figure 4 shows the first position of the wire bond clamps when assembling a semiconductor component according to a third embodiment of the invention,

Figure 5 depicts the second position of the wire bond clamps when assembling the semiconductor component of Figure 4, and

5 Figure 6 shows the assembly a semiconductor component according to a fourth embodiment of the invention.

Figure 1 shows a plan view of a semiconductor component 1 assembled after a first iteration of the method of the invention. The semiconductor component 1 comprises a semiconductor device 2, a lead frame 3 and a plastic housing 4 having a TO252 package outline 5. The semiconductor device 2 is a vertical MOSFET device. The upper surface of the MOSFET device comprises a source contact 6 and a gate contact 7. The lower surface of the MOSFET device comprises the drain contact 8 which cannot be seen in figure 1.

According to the method of the invention a package layout 100 is defined. The package layout was defined as conforming to the TO252 standard. Therefore, and the lateral dimensions of the leadframe 3, including a die pad 9, the number, position and dimensions of the outer portions leads 10 and the maximum lateral dimensions of a semiconductor device which will fit within the lateral dimensions of the die pad 9 are defined by this standard.

In the package layout 100, the lead frame 3 comprises a die pad 9, which is essentially rectangular, and three leads, or pins 10 which are arranged adjacent the long side 17 of the die pad 9 which defines a first line. The outer portion of each of the three leads 10 extends in a direction which is essentially perpendicular to the long edge 17 of the rectangular

die pad 9. Each lead 10 extends in a direction essentially parallel to each of the other leads 10 of the component 1. the direction of the leads defines a second line.

5 The central lead 11 extends from and is mechanically and electrically connected to the die pad 9 and provides the drain lead 11 of the package 1. The lead 12 positioned to one side (the left in the orientation of the component shown in Figure 1) of the drain lead 11 comprises the gate lead of the component 1. The lead 13 positioned on the opposite side (on the 10 right in the orientation of the component shown in Figure 1) of the drain lead 11 comprises the source lead 13 of the semiconductor component 1. The three leads 10 each comprise an inner portion and an outer portion. The three leads 10 are joined by support bar 14 which is disposed approximately per- 15 pendicular to the three leads 10. The support bar 14 holds the leadframe 3 within a lead frame strip which comprises a plurality of essentially identical leadframes 3 arranged in rows and columns which are not shown in figure 1 for clarity. The support bar 14 is removed after the component assembly process 20 is complete to electrically isolate the three leads 11, 12, and 13.

The inner portion of the gate lead 12 and the source lead 13 includes an inner bonding area or lead post 15. The inner con- 25 tact areas 15 are positioned at a short distance from the edge of the die pad 3 and are, therefore, not directly mechanically attached to, or electrically connected to, the die pad 9. According to the method of the invention, an area is defined for the inner bonding area 15. This area is, in this embodi- 30 ment of the invention defined as A. The inner bonding area 15 extends, in each case, inwardly towards the central drain lead

11. The portion of the inner contact area 15 adjacent to the edge 17 of the die pad 9 is essentially rectangular. The portion of the inner die pad 15 from which the source lead 13 extends is approximately triangular. The form of the inner contact areas 15 can be considered as a rectangle in which the corner adjacent the drain lead 11 which faces away from the die pad 9 has been removed.

The gate electrode 7 positioned on the upper surface of the semiconductor device 2 is connected to the inner contact area 15 of the gate lead 12 by a single gold bond wire 18 which has a diameter of 75 μm.

According to the method of the invention, the cross-sectional area of the connecting means which electrically connect the source contact 6 to the leadframe 3 is then defined. In this embodiment of the invention, the source electrode 6 is electrically connected to the inner contact area 15 of the source lead 13 by two bond wires 19 and 20 which each has a defined diameter of 350 μm.

The interfacial bonding area 21, which defines the area of the bond formed between the bond wires 19 and 20 and the upper surface of the source contact 6 and the upper surface of the inner contact area 15 was calculated. This can be done based on the known bond process parameters such temperature and pressure of the bond process for a bond wire with a diameter of 350 μm. The optimisation method of the invention was then carried out.

The first end 21 of each source bond wire 19, 20 was orientated with respect to the inner contact area 15 so as to maximise the interfacial bonding area.

5 The second end 22 of each bond wire 19,20 was orientated with respect to the edge of the die pad to maximise the interfacial bonding area between the second end 22 of each bond wire 19,20 and the upper surface of the semiconductor device 2. As can be seen in figure 1, the semiconductor device 2 was orientated
10 such that the bond wires 19, 20 form an angle of 45° to the edge of the semiconductor chip.

The semiconductor device 2 is, in this embodiment of the invention, also essentially rectangular and is positioned ap-
15 proximately concentrically on the rectangular die pad 9. Therefore, the long edge 16 of the semiconductor device 2 lies in a plane which is essentially parallel to the long edge 17 of the die pad 9. The angle between the long edge 16 of the semiconductor device 2 and the long edge 17 of the die pad 9
20 is, therefore, approximately 0°.

With the restrictions of the size of the semiconductor device and lateral dimensions of the inner contact area 15, according to the further conditions regarding the area required by the
25 bonding tool clamps, an angle of 45° between the second end 22 of the bond wires 19, 20 and the edge 16 of the semiconductor device 2 is as close as possible to an angle of 90°.

As can be seen in Figure 1, the area A of the inner contact
30 area 15 is insufficient to accommodate the bond wires 19, 20. Therefore, according to the method of the invention, the area of the inner contact area was increased to a value B and the

optimisation method repeated. The result of the second iteration of the optimisation method is shown in Figure 2.

Features which are essentially the same as those shown in Figure 1 are indicated by the same reference number in the following Figures and are not necessarily described in detail again.

The semiconductor component of Figure 2 differs from that of Figure 1 in that the inner contact areas 15 are rectangular and have a larger area than the inner contact areas shown in Figure 1. In the second iteration, the interfacial bonding areas were maximised and the orientation of the semiconductor chip with respect to the bond wires 19, 20 was chosen so as to provide an angle as close to 90° as possible.

A comparison of the area of the inner contact area 15 occupied by the interfacial bonding areas 23 and the unoccupied area shows that an inner contact area with an area of B is sufficiently large to accommodate two bond wires 19, 20 with a diameter of 350 µm within a TO252 package outline. Sufficient space also remains for the wire bonding clamps. The component as shown in Figure 2, therefore, fulfils the criteria of the method of the invention.

After the semiconductor component 1 has been assembled according to the method of the invention, the semiconductor device 2, the die pad 9, the inner portions of the leads 10 including the inner contact areas 15, and the bond wires 18, 19, and 20 are encapsulated in a plastic mold material 4. The outer surfaces of the mold material 4 provide the outer surfaces of the semiconductor component 1. The outline of the package provided

by these outer surfaces is indicated in figure 1 by the dashed line 5. In this embodiment of the invention, the semiconductor component 1 has a package outline 5 which corresponds to the dimensions of a TO252 package outline.

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The position of the bonding tool clamps used to assemble a component according to various embodiments of the method according to the invention, are shown in relation to Figures 3 to 6.

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Figure 3 shows the assembly of a semiconductor component 25 according to a second embodiment of the invention and shows a component position 26 of a leadframe strip. The component position 26 is sued to assemble a semiconductor component 25
15 with the TO252 package outline. Since Figures 3 to 6 illustrate the production method for the fabrication of the source wire bonds 19, 20, the package outline is not shown in the figures for clarity.

20 The semiconductor component 25, according to a second embodiment of the invention, differs from the semiconductor component 1 depicted in Figure 2, in that the semiconductor device 27 has smaller lateral dimensions than the semiconductor device 2 of the first embodiment. The inner contact areas 15
25 have an area B as in the embodiment of Figure 2.

The semiconductor device 27 is also a MOSFET device and its upper surface comprises a source contact 6 and a drain contact 7. The drain contact 8 is positioned on its rear surface and
30 is electrically connected to the die pad 9 and, therefore, the drain lead 11. The semiconductor component 25 was also assembled according to the method of the invention.

Since the lateral dimensions of the semiconductor device 27 are smaller, the semiconductor device 27 is orientated on the die pad so that the long edge 16 of the semiconductor device 27 lies at an angle of around 20° to the long edge 17 of the die pad 9. The source contact 6 is electrically connected to the inner contact that 15 of the source lead 13 by two wires 19, 20. The inner contact area 15 has essentially the same lateral dimensions as the inner contact area 15 shown in Figure 2. The two bond wires 19, 20 also comprise aluminium and have a diameter of approximately 350 µm.

The central portion 24 of the bond wires 19, 20 lies at an angle of approximately 85° to the long edge 16 of the semiconductor device 27. The semiconductor component 25 was assembled using an embodiment of the method of the invention in which the position of the bonding tool clamps 28, 29, and 30 required to form the two source wires 19, 20 in a single bonding pass process, is taken into account. The position of the bonding tool clamps in indicated in the figures by rectangles.

As can be seen in Figure 3, the bonding tool clamp 28 is positioned so that it clamps the drain lead 11 and the bottom left hand corner of the essentially rectangular inner contact area 15 of the source lead 13. The two remaining bonding tool clamps 29, 30 placed in contact with the support bar 14 either side of the source lead 13. This arrangement provides a stable clamping of the lead frame 3 during the wire bonding process while also requiring that only a small area or the inner contact area 15 is occupied by the clamp 28 and is unavailable for use by the interfacial bonds 20.

The method according to the invention was used to determined an optimum combination of the area and position required by the bonding clamp 28, the available area of the inner contact area 15, the diameter of the wires 19, 20 and orientation of 5 the semiconductor device 27 on the die pad 9. This combination of features results in an increased current carrying capacity of the semiconductor component 25 within a T0252 package outline. This package can carry up to 90 Amps.

10 Figures 4 and 5 show two stages in a method according to a third embodiment of the invention for the assembly of a semiconductor component 31 using a two-pass wire bonding method.

The semiconductor component 31 comprises a MOSFET semiconduc-15 tor device 27 and the lead frame 3. The lead frame 3 comprises a rectangular die pad 9 and three leads 10 disposed on one of the long sides of the die pad 3. Similarly to the embodiments of figures 1 and 2, the lead frame 3 of the semiconductor component 31 includes a central drain lead 11, a gate lead 12 and 20 a source lead 13. The source lead 13 and the gate lead 12 include inner contact areas 15. Each inner contact area 15 is essentially rectangular, has an area B and extends from the innermost end of the inner portion of the respective gate lead 12 and source lead 13 towards the central drain lead 11. The 25 lateral dimensions of the inner contact area 15 is approximately the same as in the embodiments shown in Figures 2 and 3.

The MOSFET device 27 is mounted with its rear surface on the 30 upper surface of the die pad 9 so that the long side 16 of the MOSFET device 27 dies at an angle of approximately 20° to the long side 17 of the die pad 9. The gate electrode 7 is con-

nected by a first bond wire 18 which comprises gold and has a diameter of approximately 75 μm to the inner contact area 15 of the gate electrode 12.

5 The MOSFET device 27 will be electrically connected by two bond wires which reach between the source contact 6 and the inner contact area 15 of the source lead 13.

In this embodiment of the invention, the wire bonding of the
10 source contact 6 to the source lead 13 occurs in two passes. In the first stage, shown in Figure 4, the wire bonding tool clamps 32 and 33 are positioned on the lead frame 3 so as to simplify the production of a first bond wire 19 between the source electrode 6 and the inner contact area 15 of the source
15 lead 13. As can be seen in Figure 4, a wire bonding clamp 32 is positioned towards one side (the right side for the orientation of the component shown in Figure 4) of the inner contact area 15 in approximately the lateral centre of the short side. A second wire bonding clamp 33 is positioned on the sup-
20 port bar 14 to the right of the source lead 13. This provides a stable clamping of the lead frame 3 while leaving the majority of the inner contact area 15 (the central and left hand regions for the orientation shown in Figure 4) unoccupied so as to simplify the bonding of the first bond wire 19 to the
25 inner contact area 15.

The lead frame 3 represents a single component position of a leadframe strip having a plurality of similar component positions, which are not shown in the Figure for clarity. In the
30 first pass of the wire bond, a first wire bond 19 is produced between the source contact 6 of the MOSFET device 27 and the inner contact area 15 of the source lead 13 in each of the

component positions. In the second pass of the wire bond tool over the lead frame strip, a second bond wire 20 will be produced in each of the component positions.

5 The production of the second bond wire 20 between the source electrode 6 disposed on the upper surface of the MOSFET device 27 and the inner contact area 15 of the source lead 13 is illustrated in connection with Figure 5.

10 As can be seen in Figure 5, the second bond wire 20 extends form the source electrode 6 to the inner contact area 15 in a direction which is essentially parallel to that of the first bond wire 19. Since the inner contact area 15 is already mechanically secured to the die pad via the first bond wire 19
15 and the mounted semiconductor device 27, the positioning of a bond wire clamp on the inner contact area in the second pass can be avoided. As can be seen in figure 4, the two clamps 32 and 33 are positioned on the support bar 14 either side of the source lead 13. This arrangement maximises the area available
20 for bonding within the inner contact area 15.

Figure 6 shows a semiconductor component 35 assembled using a method according to the invention.

25 Similarly to the embodiments shown in Figures 3, 4 and 5, the semiconductor component 35 comprises a MOSFET device 27 and a lead frame 3 comprising a die pad 9 and three leads 10. The MOSFET device 27 is orientated on the die pad 9 so that the long side 16 of the MOSFET device 27 dies at an angle of ap-
30 proximately 20° to the long side 17 of the die pad 9. The inner contact areas 15 have an area B and dimensions essentially the same as the embodiments of Figures 3, 4 and 5.

The embodiment of Figure 6 differs from the embodiments of Figures 3 and 5 in that the source electrode 6 is electrically connected to the inner contact area 15 of the source lead 13 by two bond wires 19, 20 which include a kink or bend 36. The first end 21 of each of the source bond wires 19, is positioned so as to be approximately perpendicular to the long side of the inner contact area 15 and approximately parallel to the drain lead 11. The second end 22 of each of the source wires 19,20 is positioned on the source contact 6 of the semiconductor device 27 so as to form an angle of approximately 85° with the long side 16 of the MOSFET device 27. Therefore, the central portion 24 of each of the bond wires 19, 20 lies at an angle of approximately 160° to the direction of the first end 21 of the bond wires 19,20 which is attached to the inner contact area 15 of the source lead 13.

As can be seen in figure 6, this arrangement allows the interfacial bonding area 20 between the two source wires 19, 20 and inner contact area 15 to have an approximately square or rectangular form. This enables bond wires with a larger diameter to be accommodated on an inner contact area with the same lateral dimensions as in the embodiments illustrated in Figures 1, 2 and 4. In this embodiment, the bond wires 19, 20 have a diameter of 500 µm.

Furthermore, the interfacial bonding areas 20 can be positioned towards the lateral centre of the inner contact area 15. This has the advantage, that regions of the inner contact area 15 towards the two short sides remains unoccupied by the bond wires 19, 20. This enables the wire bond clampers 32 and 33 to be positioned so as to clamp the outer regions of the

two short sides of the inner contact area 15. This arrangement provides a more stable clamping of the inner contact area as the inner contact area is directly clamped by the two bond wire clamps 32, 33.

5

Reference numbers

1 semiconductor component
2 MOSFET device
3 leadframe
4 mold material
5 package outline
6 source contact
7 gate contact
8 drain contact
9 die pad
10 leads
11 drain lead
12 gate lead
13 source lead
14 support bar
15 inner contact area
16 long edge of MOSFET
17 long edge of die pad
18 first bond wire
19 first source bond wire
20 second source bond wire
21 first end of bond wire
22 second end of bond wire
23 interfacial bond
24 central portion of bond wire
25 second semiconductor component
26 component position
27 second MOSFET device
28 first wire bond clamp
29 second wire bond clamp
30 third wire bond clamp
31 third semiconductor component
32 first wire bond clamp
33 second wire bond clamp
35 fourth semiconductor component
36 kink in bond wire
100 package layout

Patent claims

1. Method for increasing the current carrying capacity of a semiconductor component (1; 25; 31; 35) having a standard package outline and a standard pin arrangement, the method comprising:
   - defining a package layout (100), the package layout (100) comprising:
     - a die pad (9) having an edge (17) defining a first line and having a lateral dimensions;
     - a plurality of leads (10) disposed on one side of the die pad (9), each lead (10) having an inner portion and an outer portion, wherein at least one drain lead (11) extends from the die pad (9) in a direction defining a second line and the inner portion of each of the remaining leads (12, 13) comprises an inner contact area (15) which is spaced at a distance from the die pad (9), each lead (10) extending in a direction parallel to the second line, the inner contact area (15) having maximum allowable dimensions;
     - a semiconductor device (2; 27) having lateral dimensions which are equal to or less than the lateral dimensions of the die pad (9); and
     - a plurality of electrically conductive connecting means (19, 20),
   - defining the area of the inner contact area (15);
   - defining the cross-sectional area of the electrically conductive connecting means (19, 20);
   - calculating the interfacial bonding area (23) of the electrically conductive connecting means (19, 20) having said cross-sectional area after the electrically

conductive connecting means (19, 20) is bonded to a surface;

- performing the following optimisation method:

(a) orientating a first end (21) of the electrically conductive connecting means (19, 20) with respect to the second line to maximise the interfacial bonding area (23) between the electrically conductive connecting means (19, 20) and the inner contact area (15);

(b) orientating a second end (22) of the electrically conductive connecting means (19, 20) with respect to the first line to maximise the interfacial bonding area (23) between the electrically conductive connecting means (19, 20) and the upper surface of the semiconductor device (2; 27);

(c) orientating the semiconductor device (2; 27) with respect to the first line so that the central portion (24) of the electrically conductive connecting means (19, 20) has an orientation with respect to the edge (16) of the semiconductor device (2; 27) which is as close to 90° as possible and so that the semiconductor device (2; 27) remains within the area of the die pad (9);

(d) determining the unoccupied area of the inner contact area (15);

(e) determining if the unoccupied area is equal to or larger than a predetermined value, the predetermined value being the area required by the bonding tool clamps (28); if no performing step (f), if yes performing step (g),

(f) changing the relationship between the area of the inner contact area (15) and the cross-sectional area of the electrically conductive connecting means (19, 20) by increasing the area of the inner contact area (15)

and/or decreasing the cross-sectional area of the electrically conductive connecting means (19, 20) and calculating the interfacial bonding area (23) and repeating steps a to e,

5 (g) determining if the unoccupied area is larger than a second predetermined value, the second predetermined value defining a non-optimum interfacial area; if yes, increasing the cross-sectional area of the electrically conductive connecting means (19, 20), calculating the

10 interfacial bonding area (23) and repeating steps a to e; if no, outputting the determined values.

2. Method according to claim 1
characterised in that

15 the cross-sectional area of the electrically conductive connecting means (19, 20) is selected from a plurality of pre-defined values.

3. Method according to claim 1 or claim 2

20 characterised in that
the electrically conductive connecting means (19, 20) is provided by a bond wire with an essentially circular cross-section.

25 4. Method according to claim 1 or claim 2
characterised in that
the electrically conductive connecting means (19, 20) is provided by a foil with an essentially rectangular cross-section.

30

5. Method according to one of the previous claims
characterised in that

the first end (21) of the electrically conductive connecting means (19, 20) is orientated approximately parallel to the second line.

5 6. Method according to one of the previous claims characterised in that the second end (22) of the electrically conductive connecting means (19, 20) is orientated approximately perpendicular to the first line (17).

10

7. Method according to one of the previous claims characterised in that the first predetermined value defining the unoccupied area of the inner contact area (15) required by the bonding
15 tool clamps (28) is the area required by the bonding tool clamps (28) in a single pass bonding process.

8. Method according to one of claims 1 to 6 characterised in that
20 the first predetermined value defining the unoccupied area of the inner contact area (15) required by the bonding tool clamps (32) is the area required by the bonding tool clamps (32)in a two pass bonding process.

25 9. Method according to one of the previous claims characterised in that the following additional steps after step (d) are performed:

- defining the area required by each bonding tool clamp (28; 32) within the area of the inner contact area
30 (15);

- defining the lateral position of the bonding tool clamp (28; 32) within the area of the inner contact area (15);
- determining the lateral position of the unoccupied area
5 of the inner contact area (15);
- comparing the lateral position of the unoccupied area with the defined lateral position of the bonding tool clamp (28; 32) and the defined area required by the bonding tool clamp (28; 32); if the defined lateral po-
10 sition of the bonding tool clamp (28; 32) and the defined area required by the bonding tool clamp (28; 32) lies outside the lateral position of the unoccupied area, performing step (f), if the defined lateral position of the bonding tool clamp (28; 32) and the defined
15 area required by the bonding tool clamp (28; 32) lies within the lateral position of the unoccupied area, performing step (g).

10. A semiconductor component (1; 25; 31; 35) having a stan-
20 dard package outline and a standard pin arrangement comprising:
- a die pad (9) having an edge defining a first line (17) and having a lateral dimensions;
- a plurality of leads (10) disposed on one side of the
25 die pad (9), each lead (10) having an inner portion and an outer portion, wherein at least one drain lead (11) extends from the die pad in a direction defining a second line and the inner portion of each of the remaining leads (12, 13) comprises an inner contact area (15)
30 which is spaced at a distance from the die pad (9), each lead (10) extending in a direction parallel to the second line;

- a semiconductor device (2; 27) having lateral dimensions which are equal to or less than the lateral dimensions of the die pad (9); and
- a plurality of electrically conductive connecting means (19, 20),

wherein the standard package outline is a TO252 package outline and the electrically conductive connecting means (19, 20) comprise bond wires with a diameter of greater than approximately 350 µm.

11. Semiconductor component (1; 25; 31; 35) according to claim 10
characterised in that
the bond wires (19, 20) have a diameter of approximately 500 µm.

12. Semiconductor component (1; 25; 31; 35) according to claim 10 or claim 11
characterised in that
the semiconductor device (2; 27) is orientated with respect to the first line (17) by an angle θ, where $0° < \theta < 90°$.

13. Semiconductor component (1; 25; 31; 35) according to one of claims 10 to 12
characterised in that
the semiconductor device (2; 27) is orientated with respect to the first line (17) so that the central portion (24) of the electrically conductive connecting means (19, 20) has an orientation with respect to the edge (16) of the semiconductor device (2; 27) which is as close to 90°

as possible and so that the semiconductor device (2; 27) remains within the area of the die pad (9).

14. Semiconductor component (1; 25; 31; 35) according to one of claims 10 to 13
characterised in that
the semiconductor device (2; 27) is a high power semiconductor device.

15. Semiconductor component (1; 25; 31; 35) according to claim 14
characterised in that
the semiconductor device (2; 27) is a MOSFET, a IGBT, a BJT or a diode.

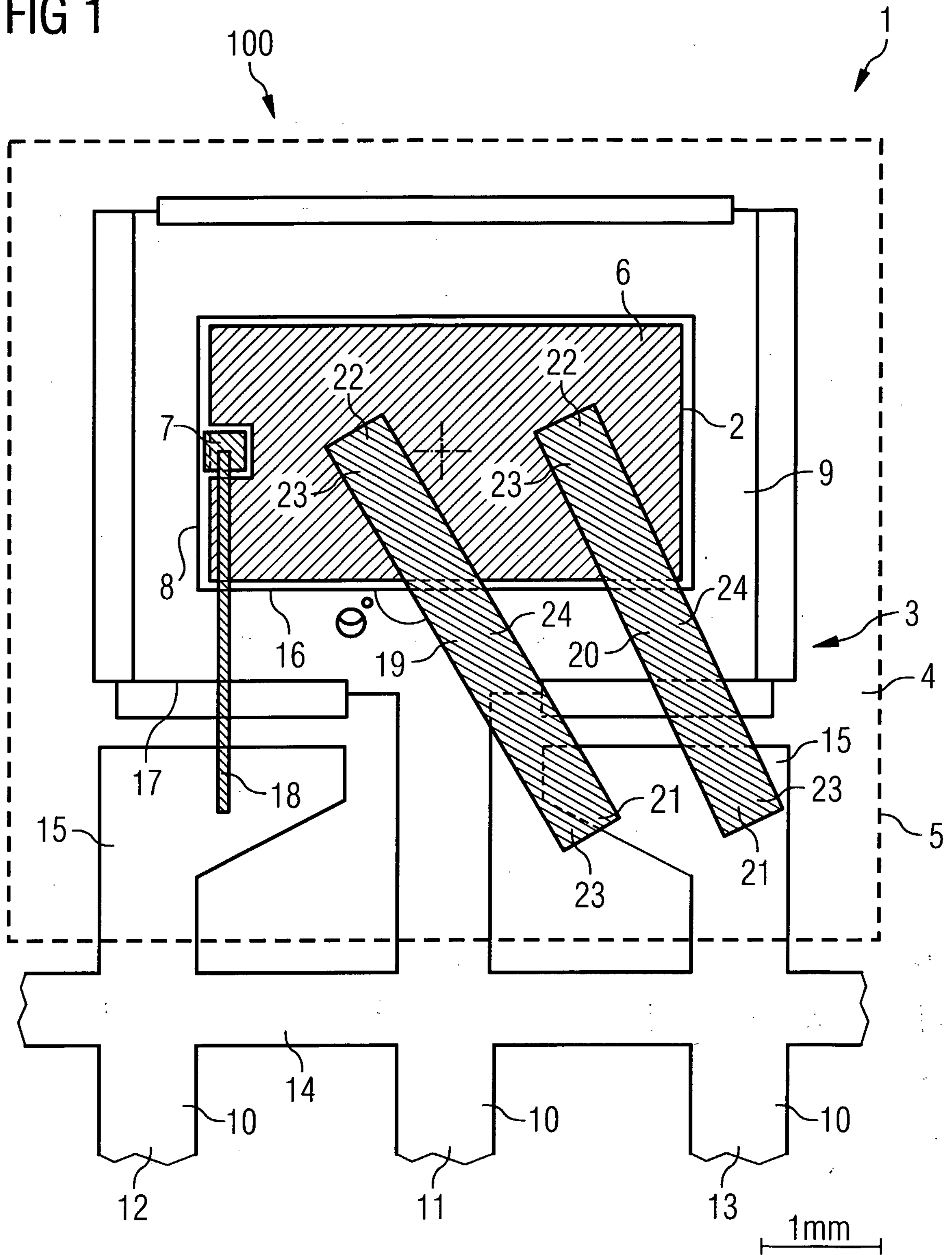
FIG 1
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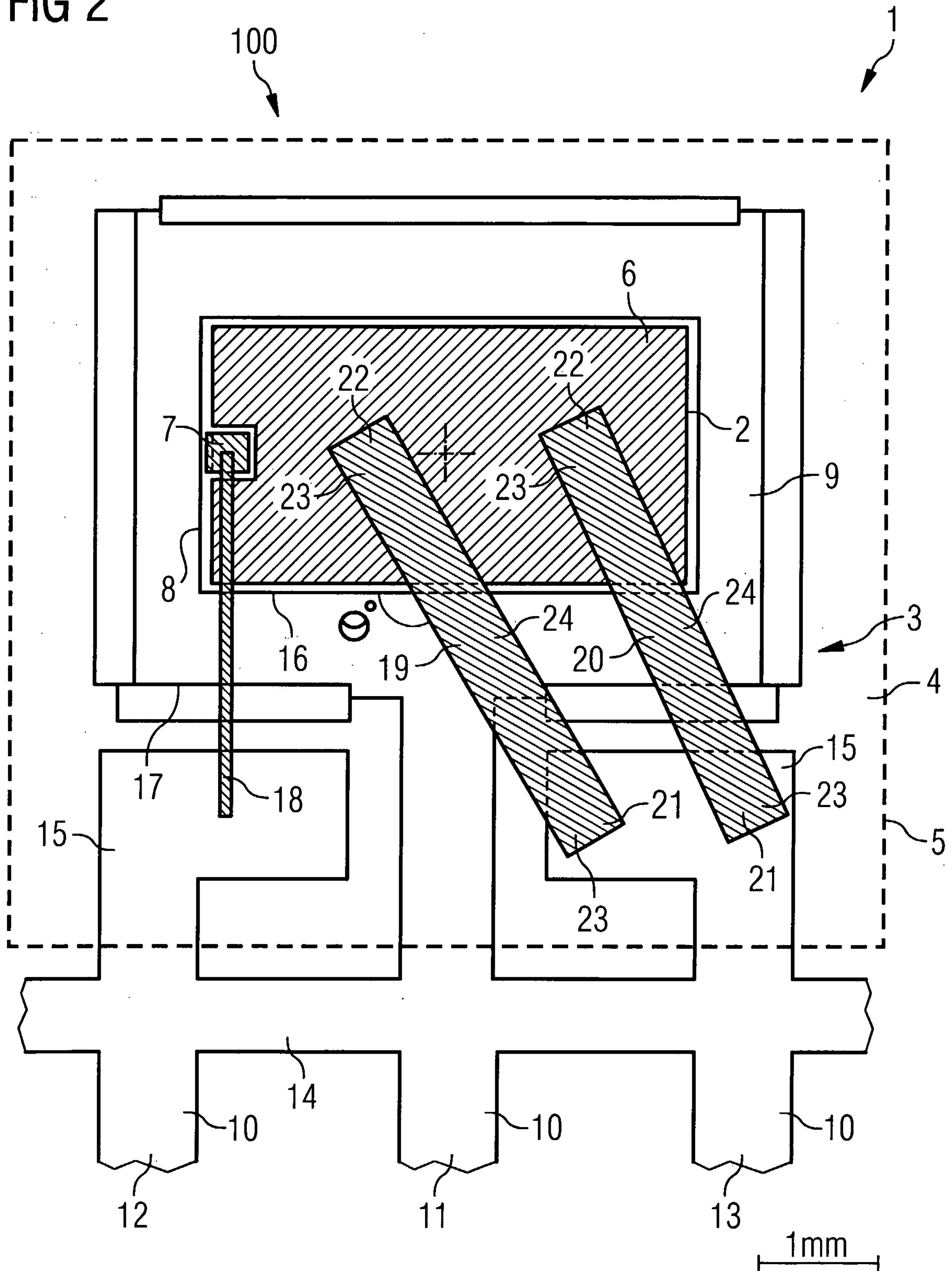
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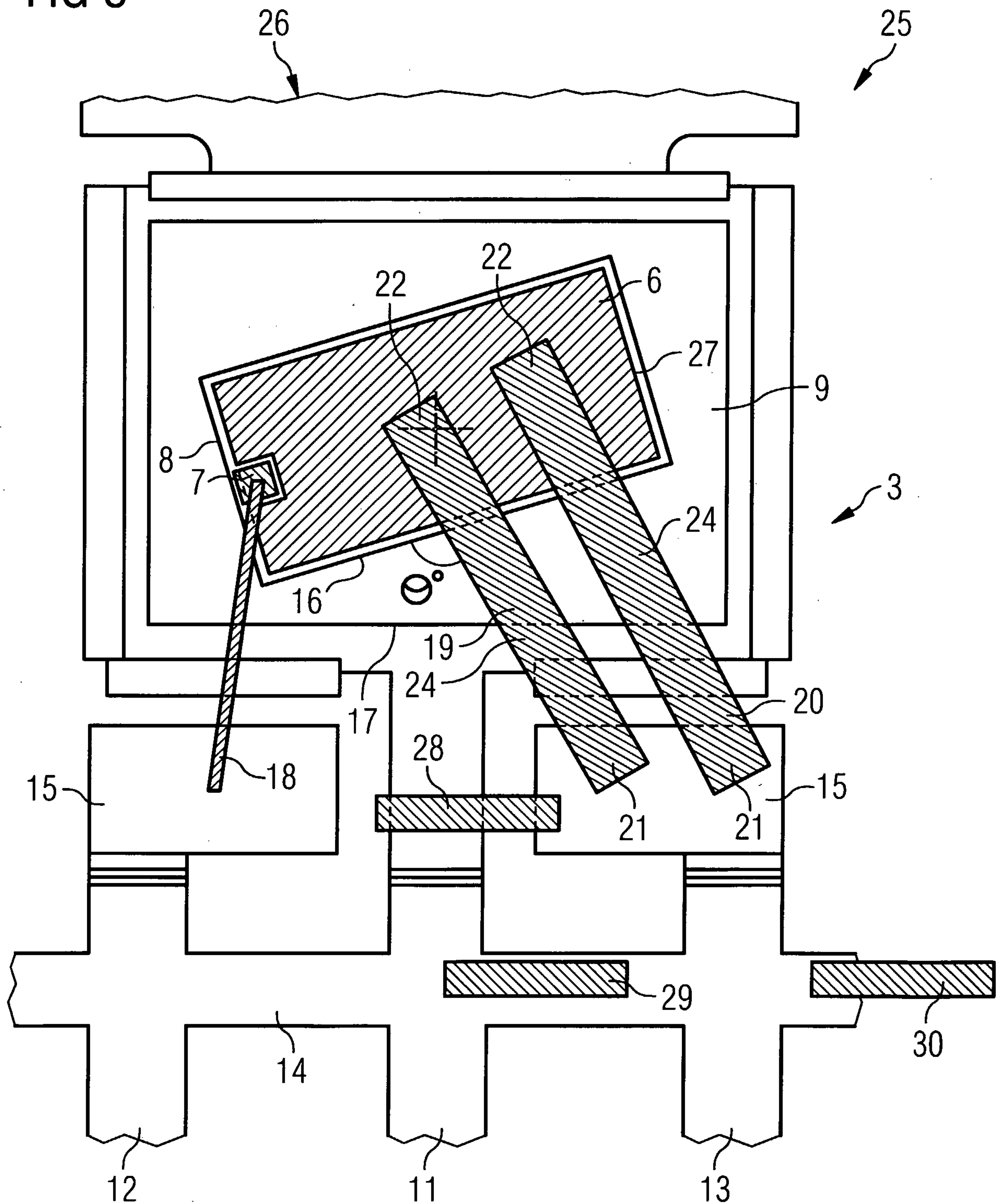
FIG 3
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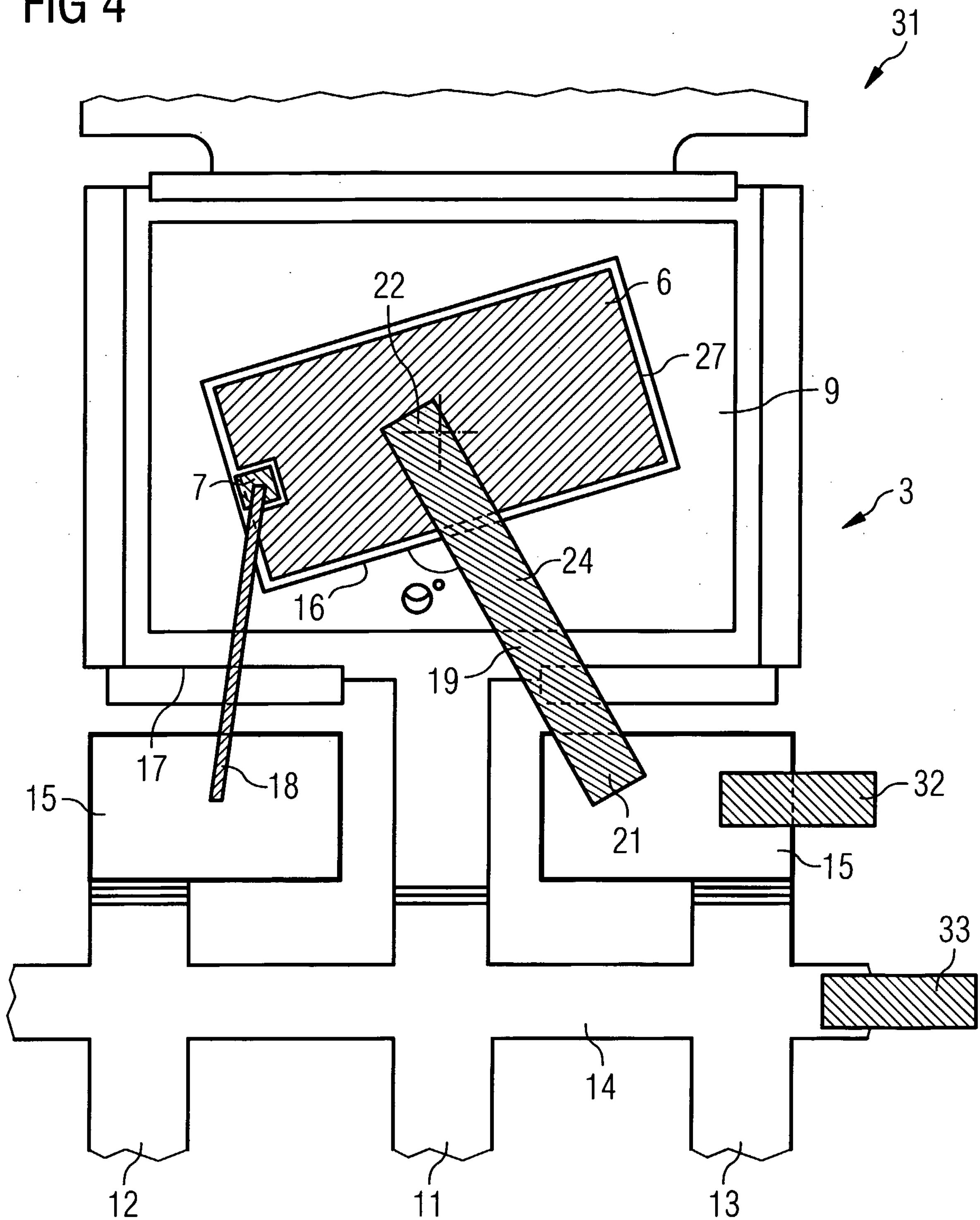
FIG 4
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FIG 5

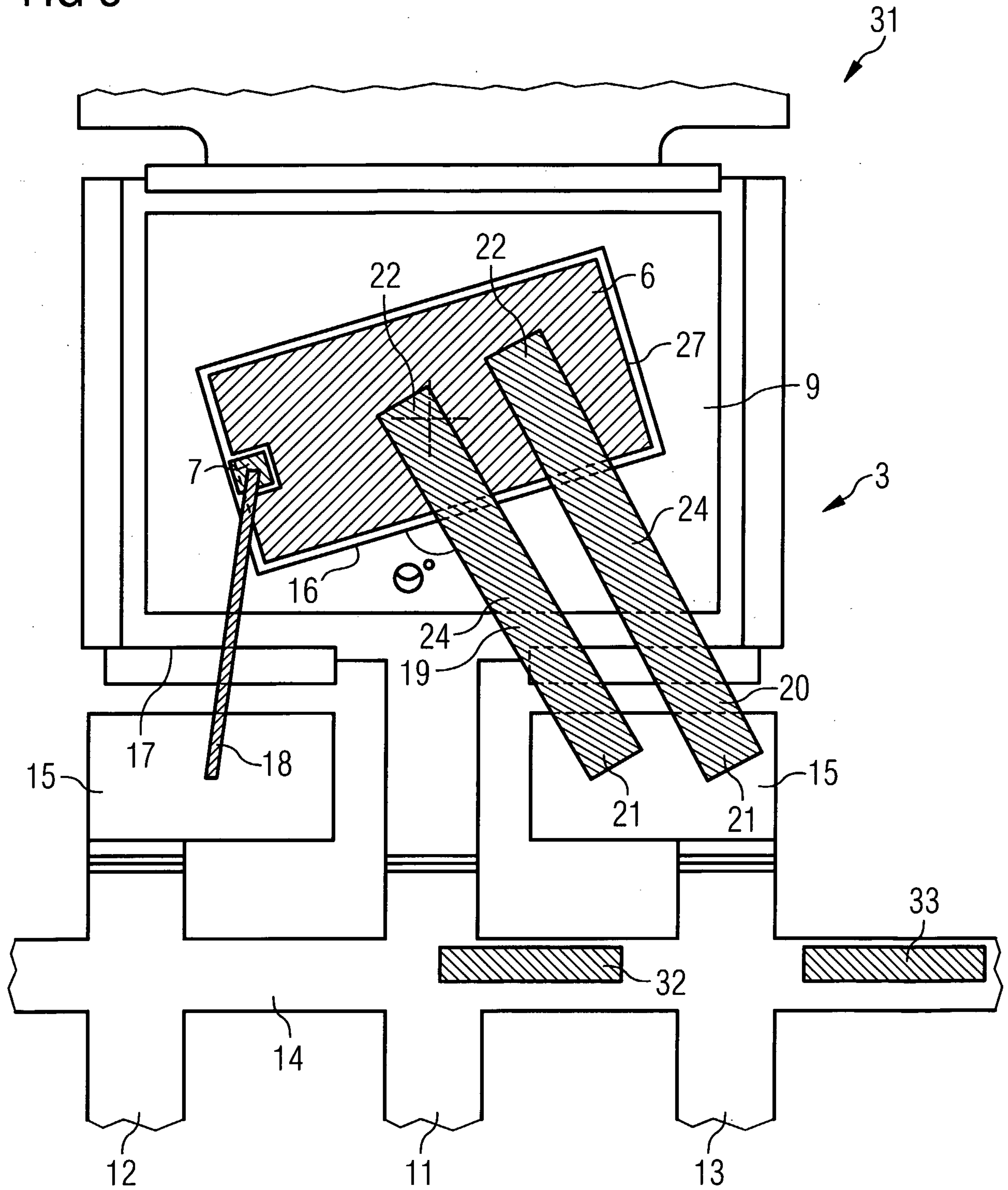
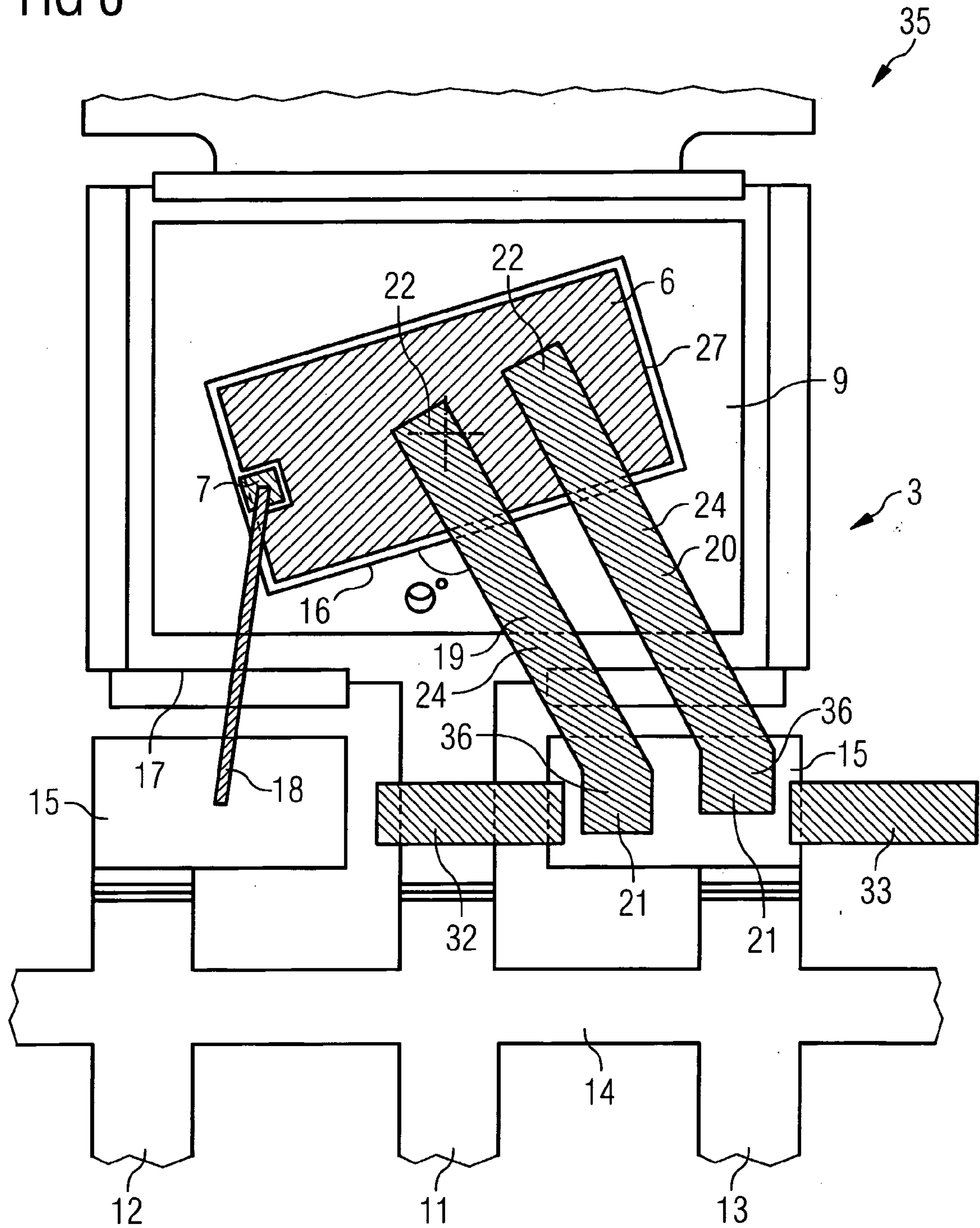


FIG 6



INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2005/002893

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/495 H01L21/60

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 756 658 B1 (GILLETT BLAKE A ET AL) 29 June 2004 (2004-06-29) column 1, line 1 - column 2, line 20; figures 1-3	1-15
A	PATENT ABSTRACTS OF JAPAN vol. 014, no. 278 (E-0941), 15 June 1990 (1990-06-15) -& JP 02 087535 A (HITACHI LTD), 28 March 1990 (1990-03-28) abstract	1-15
A	US 2003/011051 A1 (WOODWORTH ARTHUR ET AL) 16 January 2003 (2003-01-16) cited in the application paragraphs [0036] - [0039]; figure 4	1-15

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 July 2006	19/07/2006
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Authorized officer Edmeades, M

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2005/002893

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	US 5 300 815 A (ROSTOKER ET AL) 5 April 1994 (1994-04-05) figures 3A-C -----	1

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Information on patent family members

International application No
PCT/IB2005/002893

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