Title: DEVICE AND METHOD FOR FABRICATING DOUBLE-SIDED SOI WAFER SCALE PACKAGE WITH THROUGH VIA CONNECTIONS

Abstract: A semiconductor package includes an SOI wafer having a first side including an integrated circuit system, and a second side, opposite the first side, forming at least one cavity. At least one chip or component is placed in the cavity. A through buried oxide via connects the chip(s) to the integrated circuit system.
DEVICE AND METHOD FOR FABRICATING DOUBLE-SIDED SOI WAFER SCALE PACKAGE WITH THROUGH VIA CONNECTIONS

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to semiconductor processing and devices, and more particularly to devices and methods, which employ silicon-on-insulator (SOI) technology to provide a double-sided chip structure.

Description of the Related Art

As the relentless scaling of complementary metal oxide semiconductor (CMOS) technology approaches its physical limit, the integration of very large-scale integrated circuit (VLSI) systems on a package (SoP) becomes increasingly important. The integration of many different chips on a package is often not cost effective, due to the incompatibility between various chip technologies. For example, non-volatile random access memory (NVRAM) with floating gate devices and dynamic random access memory (DRAM) with deep trenches require additional masks and processing steps to fabricate. High-speed Gallium Arsenide (GaAs) chips are manufactured on a different substrate than a silicon chip.

An efficient method to integrate different chips on a two-dimensional (2-D) or three-dimensional (3-D) package can not only enhance circuit performance but also reduce manufacturing cost. If the chips are stacked vertically, the through vias should also be used to further reduce the interconnect delay and maximize circuit performance.

Advanced three-dimensional wafer-to-wafer vertical stack integration technology has recently been developed to improve system performance. In U.S. Patent No. 6,645,832, entitled "Etch stop layer for silicon via etch in three-dimensional wafer-to-wafer vertical stack", a method of using nickel silicide (NiSi) as an etch stop layer for the silicon via etch is described. In a 3-D package, a dielectric layer is used to bond the two vertically stacked wafers, and a silicon via etch is required to provide electrical conductivity between the wafers.
The vias are formed by selectively etching through the silicon of the top wafer until stopped by the etch stop layer. The sidewalls of the silicon vias are coated with a layer of insulating material, forming a barrier layer. The vias are then filled with conductive material to provide electrical connection.

In U.S. Patent No. 6,762,076, entitled "Process of vertically stacking multiple wafers supporting different active integrated circuit devices", a metal-to-metal bonding method is used to bond adjacent wafers and provide electrical connections.

In U.S. Patent No. 6,355,501, entitled "Three-dimensional chip stacking assembly", multiple silicon-on-insulator (SOI) chips are stacked together and interconnects between chips are accomplished by aligning prefabricated contacts at the top and bottom surfaces of the chips. Each chip is thinned down significantly by backside chemical-mechanical-polishing (CMP) to remove all the material behind the buried oxide layer. In the 3-D assembly, each SOI chip includes a handler making mechanical contact to a first metallization pattern, the first metallization pattern making electrical contact to a semiconductor device, and the semiconductor device making electrical contact to a second metallization pattern on the opposite surface of the semiconductor device.

In U.S. Patent No. 6,737,297, entitled "Process for making fine pitch connections between devices and structure made by the process", a method is disclosed to join two or more chips together on a temporary substrate with prefabricated global wirings by aligning the stud on the chip surface and the via on the temporary alignment substrate. The two-dimensional chip assembly is then transferred to a permanent support carrier with heat-sink devices, and the transparent plate of the temporary alignment structure is ablated and detached from the assembly.

In U.S. Patent No. 6,607,938, entitled "Wafer level stack chip package and method for manufacturing same", the semiconductor chips are stacked on the redistribution substrate. After multiple thin chips on the corresponding wafers are stacked together, the stack-chip structures are cut out from the stack-wafer assembly and the carrier material is then stripped away.

In U.S. Patent No. 6,730,541, entitled "Wafer-scale assembly of chip-size packages", a polymer film carrying solder balls for each of the contact pads is aligned with the wafer. Infrared energy is applied to the
backside of the wafer to uniformly heat the wafer. The process is then repeated to sequentially assemble an interposer and a second polymer film carrying solder balls.

SUMMARY OF THE INVENTION

A semiconductor device or package includes a wafer having a first side including an electronic component, and a second side, opposite the first side, forming a cavity. A chip or component is placed in the cavity. A through via connects the chip to the electronic component through a portion of the wafer.

These and other objects, features and advantages of the present invention will become apparent from the following detailed description of illustrative embodiments thereof, which is to be read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

Preferred embodiments of the present invention will now be described, by way of example only, with reference to the accompanying drawings in which:

FIG. 1 is a cross-sectional view of a silicon-on-insulator structure/wafer showing electronic components formed thereon;

FIG. 2 is a cross-sectional view showing through vias etched, dielectric liners formed and filled with a conductive material in accordance with one embodiment of the present invention;

FIG. 3 is a cross-sectional view showing a protective coating formed on a first side of the wafer in accordance with the present invention;

FIG. 4 is a cross-sectional view showing polishing/etching of a silicon substrate portion of the wafer in preparation for etching in accordance with the present invention;

FIG. 5 is a cross-sectional view showing silicon substrate (backside) photolithography patterning in accordance with the present invention;
FIG. 6 is a cross-sectional view showing backside etching to form a cavity in accordance with the present invention;

FIG. 7 is a cross-sectional view showing pockets opened around through vias within the cavity in accordance with the present invention;

FIG. 8 is a cross-sectional view showing selective deposition of solder on through vias in accordance with the present invention;

FIG. 9 is a cross-sectional view showing the placement of sub-chips into the backside cavity and aligning the sub-chips with the through vias in accordance with the present invention;

FIG. 10 is a cross-sectional view showing soldering and bonding of the sub-chips to the through vias to permit the sub-chips and components of the original to coact to perform a function in accordance with the present invention;

FIG. 11 is a cross-sectional view showing a thermally conductive underfill and deposition of a thermally conductive layer in accordance with the present invention;

FIG. 12 is a cross-sectional view showing the protective coating being removed from the front side of the wafer in accordance with the present invention;

FIG. 13 is a cross-sectional view showing front side global interconnect formation and C4 formation in accordance with the present invention;

FIG. 14 is a cross-sectional view showing the formation of a backside heat sink in accordance with the present invention;

FIG. 15 is a perspective view showing a plurality of sub-chips placed and connected by through vias to a mother chip in accordance with one embodiment of the present invention; and

FIG. 16 is a top schematic view of a mother chip with daughter (sub-chips) placed therein showing through via placement and function in accordance with one embodiment of the present invention.
DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention provides a low-cost and high-yield double-sided wafer scale package preferably on a silicon-on-insulator (SOI) wafer. A mother chip is formed on the front side of the SOI wafer with a fully or partially depleted body to achieve high performance. A plurality of thinned daughter chips are then mounted inside the cavities on the backside of the SOI wafer, opposite the mother chip. Through silicon and buried oxide, metal studs are fabricated to facilitate interconnection between the mother and daughter chips.

Advantageously, the present methods do not need the chips to be transferred from a temporary carrier to a permanent carrier, which reduces the cost. Accordingly, by employing through via connections and cavity formation, sub-chips (daughter chips) can be directly diced out of a wafer and mounted on the backside of the mother chip. The method further avoids the use of vertical stacking in a 3-D package to facilitate heat dissipation. In addition, multiple chips manufactured in different technologies can be integrated on the same package.

The double-sided package protocol adopts two-dimensional chip packaging schemes on both sides of the wafer. In the thin silicon layer on the front side of the SOI wafer, mother chips such as central processing units and serializer/deserializer (SerDes) chips are fabricated. The performance of these chips is boosted by the floating body effect as well as low junction capacitance.

The floating body effect is an inherent characteristic of SOI MOSFETs. Since the potential of the body is not fixed, the holes that are injected into the body cause the potential in the body to rise, resulting in lower threshold voltage, higher drain current and faster gate. The buried oxide layer also eliminates the area junction capacitance between the source/drain diffusion and the substrate, which allows the transistor to operate faster with less capacitance to charge and discharge. With secondary components placed on the backside of the wafer, the mother chips will have smaller dimensions and higher yield than equivalent system-on-chip (SoC) designs.

The remaining area on the front side of the SOI wafer can be used to form decoupling capacitors and other discrete devices. The backside of the SOI wafer may have thicker material that can be thinned down before etching to form the cavities for the daughter chips. The daughter chips
that can be embedded in the cavities may include high-speed radio
frequency (RF) input/output (I/O) chips, memory chips such as non-volatile
random access memory (NVRAM), magnetic RAM (MRAM), ferroelectric RAM
(FRAM), and embedded dynamic RAM (eDRAM) whose deep trench capacitor
process is not fully compatible with conventional CMOS processes,
decoupling capacitors, high-Q semiconductor inductors, and
micro-electromechanical systems (MEMS).

The present invention may form deep vias from the pads of the mother
chips on the front side of the SOI wafer, through the buried oxide layer,
to the pads of the daughter chips on the backside of the SOI wafer. These
through vias not only provide the power supplies, signals and controls,
but also enable the communication, testing, and monitoring of the mother
and daughter chips. To fabricate the through vias, no devices or
interconnects should be formed underneath the designated pads of the
mother chip. Since the total thickness of the top silicon layer and the
buried oxide layer is within a few hundred microns, the size of these
through vias can be much smaller than a traditional multi-chip package.

It is to be understood that the present invention will be described
in terms of a given illustrative architecture having a SOI wafer; however,
other architectures, structures, substrate materials and process features
and steps may be varied within the scope of the present invention.

Referring now in detail to the figures in which like numerals
represent the same or similar elements and initially to FIG. 1, a
silicon-on-insulator (SOI) wafer 10 with a top silicon layer 43, a buried
dielectric (e.g., oxide) layer 42, and a bottom substrate 40 (e.g.,
silicon) are illustratively shown. An integrated circuit system 11
includes active devices 44, metal interconnects 45, and discrete devices
48 formed on the silicon wafer 10. The buried oxide layer 42 on SOI wafer
10 may include a thickness of say, 5 micrometers or less.

Referring to FIG. 2, trenches 50 may be formed. In one embodiment,
high-density plasma reactive ion etching (RIE) can be used to create
trenches 50 down to the silicon substrate 40 through layers 32, 42 and 43
for forming through vias 51, which permit other chips to be mounted on the
backside of the wafer 10, and will be described herein.

Through vias 51 are formed through a top silicon layer 43 after
lithographic patterning, etching, sidewall dielectric coating 52, and
metal or conductive filling 53. In one embodiment, the ratio of via depth
to via size (e.g., trench width) may range from between about 1 to about 5. To etch a back end of line (BEOL) insulating material 32, the silicon layer 43, and the buried oxide layer 42, respectively, CF₄, Cl₂ and/or CF₆ based plasma etching may be employed successively, with a proper end-point detection method. Such detection methods are known in the art.

To ensure that vias 51 are extended below the buried oxide layer 42, it may be necessary to over-etch the buried oxide layer 42. Insulating materials 52, such as the oxide/nitride sidewall spacers, are preferably employed to prevent the vias 51 from being shorted to any adjacent conductive layers, well regions, or the substrate layer. The vias 51 can then be filled with conductive metal 53, such as copper, tungsten, aluminum, doped polycrystalline material, alloys and/or any other conductive material. A conformal chemical vapor deposition (CVD) deep-etch technique can be used to eliminate any void formation inside the vias 51 during the filling process.

Referring to FIG. 3, a layer of protective coating 60 such as oxide, nitride, oxy-nitride, or glass is formed on a top surface of the wafer 10 to protect it from being damaged during the backside processing. Other materials or protection schemes may also be employed.

Referring to FIG. 4, the silicon substrate 40 on the backside of the wafer is thinned, by for example, chemical-mechanical polishing (CMP) or high-density plasma etching (e.g., RIE) to a proper thickness “d”. It is preferable that “d” may be a few microns thicker than the thickest chip to be mounted on the backside.

Referring to FIGS. 5 and 6, a photolithography pattern 64 is generated by applying a photoresist 66 and patterning the resist 66 using known methods. Resist 66 is then employed as a mask in an etching process to form a backside cavity or cavities 68. The size of the cavity 68 should be slightly larger than the chip to be mounted inside (below the open surface) and margins should be provided in case of misalignment. Multiple chips may be placed inside the same cavity 68.

The cavities 68 are formed after etching and the conductive material 53 of through vias 51 is exposed at the surface of the buried oxide layer 42. The resist 66 is removed from substrate 40.

Referring to FIG. 7, an extra etching step may be employed to open a pocket 70 on top of each via 51 by thin photoresist patterning and
exposure at the surface of the buried oxide 42. The pocket 70 formation is preferable during the ensuing bonding and soldering reflow steps, to provide the space for solder to flow and thus form better contacts.

Referring to FIG. 8, a selective plating process may be employed to form solder balls 74 on exposed studs 53 in vias 51 and inside the pockets 70. The process selectively forms metal on studs 53. Low melting-temperature material is preferable in forming the solder balls 74. Solder balls 74 may include tin or lead alloys and may employ a process similar to a controlled collapse chip connection (C4) bonding method.

Referring to FIG. 9, chips (sub-chips) 80 and 82 are illustratively shown making contact with studs 53 of vias 51. Chips 80 and 82 may include thinned chips (referred to earlier as daughter chips), which are flipped upside down, placed inside the cavity 68, and bonded to the mother chip (wafer 10). The depth (d) of the cavities 68 is preferably deeper than the thickness of all the daughter chips (80 and 82). Chips 80 and 82 may be formed in a separate processing step and may themselves include a cavity therein with even smaller sub-chips connected thereto in accordance with the present invention.

Chips 80 and 82 may be placed in cavity 68 having gaps 84 therebetween and between walls 86 and chips 80 and 82. Alternately, chips 80 and 82 may include spacers or layers of material to ensure a proper fit and automatically align studs 53 with contacts 88 and 90 of each chip 80 and 82. These chips 80 and 82 may also be aligned using tooling or other gapping methods. In one embodiment, chips 80 and 82 are connected or attached to one another prior to placing them into cavity 68.

A bonding process may include a temperature of about 400°C to be carried out to join solder balls for contacts 88 and 90 of the daughter chips 80 and 82 with the solder balls 74 for through vias 51 for the mother chip 10.

Referring to FIG. 10, collection of excessive bonding material 94 is shown inside the pocket areas 70. Chips 80 and 82 are now bonded to vias 51.

Referring to FIG. 11, an under-fill process is employed to fill the gaps 84 and 86 and any other locations between chips 80 and 82 and wafer 10 with a thermally conductive agent 98, such as a thermal paste, or standard filling polymer or other fillers. It is preferred that the agent
be thermally conductive to promote heat dissipation, but act as an electrical insulator. The top surface of the cavity 68 may further be filled with a more thermally conductive material 102 such as, for example, chemical vapor deposited (CVD) diamond. A metal film 104 may also be formed on the backside of wafer 10 to seal the daughter chips inside the cavities 68.

Referring to FIG. 12, after the daughter chips 80 and 82 are mounted on the backside, the top protective layer 60 of a mother chip 120 (on wafer 10) can be stripped. This may be in preparation for further processing on the system such as global or local interconnects and vias, attaching other components or forming additional layers or features, etc.

Referring to FIG. 13, more metal layers 106, contact pads 108, and C4 balls 110 can be formed on the front side of the wafer 10 of mother chip 120. Further processing may be performed to form additional structures or to provide packaging for system 100.

A final double-side chip assembly 100 can be cut from the wafer 10 (e.g., dicing the wafer to form chip packages), where each assembly has a mother chip 120 on the front side and a plurality of daughter chips (e.g., 80 and 82) mounted on the backside. The buried oxide layer 42 of the SOI wafer 10 is used as the holding plate for through via interconnection between the mother chip 120 and daughter chips 80 and 82.

A heat sink 111 can be mounted on the backside of the chip as illustratively shown in FIG. 14. Heat sink 111 may be attached, e.g., using a thermal adhesive material, or may be formed by depositing materials and etching the material into a predetermined shape (e.g., fins and troughs).

Referring to FIG. 15, a SOI wafer scale package 200 includes one mother chip 202, such as a processor (or memory device or combination thereof) formed on a top silicon layer (e.g., 43 of FIG. 1) to achieve high performance, and several daughter chips 204, 206, 208, 210 and 212. These chips may include for example, SRAM cache, eDRAM, NVRAM, FPGA, and high-speed RF interface chips mounted on the backside of the assembly 200. Through via connections 251 are illustratively shown in one area between the mother chip 202 and daughter chips 204-212. Vias and the chip placement and alignment need to be performed after appropriate planning. It is preferably that the mother and daughter chips be co-designed for the
package 200 to ensure coaction, proper alignment/placement and proper functioning.

Referring to FIG. 16, one example of a package 300 where the mother chip 302 includes 3 macros M1, M2, and M3 (sub-chips). Package 300 indicates aspects to be considered during co-design of mother and daughter chips in a system. In this embodiment, through via connections 351 are only permitted in the empty space between the adjacent macros (M1, M2, M3) and edges of the mother chips' substrate 340. Through vias 351 may be designated for different tasks, such as carrying power Vdd, or Vss or signals (Signal) as illustratively indicated in FIG. 16. In an alternate embodiment, motherchip 302 may be comprised of multiple chips C1, C2, C3 and C4 and connected using macros, structures or subchips.

Having described preferred embodiments of a device and method for fabricating double-sided SOI wafer scale package with buried oxide through via connections (which are intended to be illustrative and not limiting), it is noted that modifications and variations can be made by persons skilled in the art in light of the above teachings. It is therefore to be understood that changes may be made in the particular embodiments of the invention disclosed which are within the scope of the invention as outlined by the appended claims.
CLAIMS

1. A semiconductor package, comprising:
a wafer having a first side including at least one electronic
component, and a second side opposite the first side and forming a cavity;
at least one chip placed in the cavity; and
a through via connecting the at least one chip to the at least one
electronic component through a portion of the wafer.

2. The package as recited in claim 1, wherein the wafer includes a
silicon-on-insulator wafer.

3. The package as recited in claim 2, wherein the first side includes a
top silicon layer and the second side includes a silicon substrate wherein
the top silicon layer is separated from the silicon substrate by a buried
dielectric layer.

4. The package as recited in claim 3, wherein the through via is formed
through the buried dielectric layer to form a connection between the
electronic component and the at least one chip.

5. The package as recited in claim 1, wherein the first side includes
one of a processor and a memory device and the at least one chip includes
one of a memory device, and a processor.

6. The package as recited in claim 1, wherein the at least one chip
includes contacts and the contacts are connectable to the through vias.

7. The package as recited in claim 1, further comprising a thermally
conductive fill material at least partially surrounding the at least one
chip.

8. The package as recited in claim 1, further comprising a thermally
conductive layer formed over at least a portion of the at least one chip.

9. The package as recited in claim 8, further comprising a heat sink
formed on the thermally conductive layer.

10. The package as recited in claim 1, wherein the cavity includes a
depth below an open surface into which the at least one chip is placed,
and the at least one chip fits into the depth below the open surface.
11. A semiconductor package, comprising:
   at least one mother chip having a cavity on one side;
   at least one a daughter chip mounted in the cavity and being
   connected to the at least one mother chip by a through via extending
   through at least a portion of the at least one mother chip such that the
   at least one mother chip and the at least one daughter chip electrically
   coact to perform a function.

12. The package as recited in claim 11, wherein the at least one mother
    chip is formed in a silicon-on-insulator (SOI) wafer, which includes a top
    silicon layer and a silicon substrate where the top silicon layer is
    separated from the silicon substrate by a buried dielectric layer.

13. The package as recited in claim 12, wherein the through via is
    formed through the buried dielectric layer to form a connection between an
    electronic component on the at least one mother chip and an electronic
    component on the at least one daughter chip.

14. The package as recited in claim 11, wherein the at least one mother
    chip and the at least one daughter chip include one of a memory device and
    a processor.

15. The package as recited in claim 11, wherein the through vias of the
    at least one mother chip are soldered to contacts of the at least one
    daughter chip.

16. The package as recited in claim 11, further comprising a thermally
    conductive fill material at least partially surrounding the at least one
    daughter chip.

17. The package as recited in claim 11, further comprising a thermally
    conductive layer formed over at least a portion of the at least one
    daughter chip.

18. The package as recited in claim 17, further comprising a heat sink
    formed on the thermally conductive layer.

19. The package as recited in claim 11, wherein the cavity includes a
    depth below an open surface into which the at least one daughter chip is
    placed, and the at least one daughter chip fits into the depth below the
    open surface.
20. A method for forming a semiconductor package, comprising the steps of:
   forming a through via through a first side of a wafer;
   forming a cavity on a second side of the wafer exposing a portion of the through via;
   placing at least one sub-chip in the cavity and connecting the sub-chip to the through via.

21. The method as recited in claim 20, wherein the wafer includes a silicon-on-insulator wafer and the step of forming a through via through a first side of a wafer includes etching a via hole through a top silicon layer and a buried dielectric layer and filling the via hole with a conductor.

22. The method as recited in claim 21, wherein the step of forming a cavity on a second side of the wafer exposing a portion of the through via includes etching a silicon substrate of the wafer to expose the portion of the through via.

23. The method as recited in claim 20, wherein exposing a portion of the through via includes opening a pocket around the through via in the cavity.

24. The method as recited in claim 20, further comprising the step of selectively depositing solder to the exposed portion of the through via.

25. The method as recited in claim 20, wherein the step of placing at least one sub-chip in the cavity and connecting the sub-chip to the through via includes the step of soldering a contact of the sub-chip to the through via.

26. The method as recited in claim 20, further comprising the step of underfilling the sub-chip with a thermally conductive material.

27. The method as recited in claim 20, further comprising the step of depositing a thermally conductive layer over the sub-chip.

28. The method as recited in claim 20, further comprising the step of providing a heat sink for heat dissipation from the sub chip.

29. The method as recited in claim 20, wherein connecting the sub-chip to the through via includes aligning and contacting contacts of the
sub-chip with a soldered through via and applying heat to bond the contacts to the through via.
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

- H01L23/48
- H01L25/065
- H01L25/18
- H01L21/768
- H01L29/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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<tr>
<td>X</td>
<td>US 6 175 160 B1 (PANNICIA MARIO ET AL) 16 January 2001 (2001-01-16)</td>
<td>1,5-11, 14-20, 24-29</td>
</tr>
<tr>
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<td>column 3, lines 46-67; figure 4</td>
<td>2-4,12, 13,21,22</td>
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<td>column 3, lines 40-55</td>
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Further documents are listed in the continuation of Box C. See patent family annex.

* "A" document defining the general state of the art which is not considered to be of particular relevance
* "E" earlier document published on or after the International filing date
* "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
* "O" document referring to an oral disclosure, use, exhibition or other means
* "P" document published prior to the International filing date but later than the priority date claimed

"I" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, each contribution being obvious when read in the art.

"&" document member of the same patent family

Date of the actual completion of the international search: 2 February 2006

Date of mailing of the international search report: 13/02/2006

Name and mailing address of the ISA

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Authorized officer: Cousins, D
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<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
</table>
| A        | US 6 448 174 B1 (RAMM PETER)  
10 September 2002 (2002-09-10)  
the whole document | 20                   |
<table>
<thead>
<tr>
<th>Patent document cited in search report</th>
<th>Publication date</th>
<th>Patent family member(s)</th>
<th>Publication date</th>
</tr>
</thead>
<tbody>
<tr>
<td>US 6175160 B1</td>
<td>16-01-2001</td>
<td>NONE</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>WO 0074134 A1</td>
<td>07-12-2000</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EP 1171912 A1</td>
<td>16-01-2002</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 2003501804 T</td>
<td>14-01-2003</td>
</tr>
<tr>
<td>EP 0926726 A</td>
<td>30-06-1999</td>
<td>NONE</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>DE 19813239 C1</td>
<td>23-12-1999</td>
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<td></td>
<td>EP 1064680 A1</td>
<td>03-01-2001</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 2002508590 T</td>
<td>19-03-2002</td>
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