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(71) Applicant *(for all designated States except US)*: **LAM RESEARCH CORPORATION** [US/US]; 4650 Cushing Parkway, Fremont, California 94538 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **YASSERI, Amir A.** [US/US]; 930 Schoolhouse Road, San Jose, California 95138 (US). **ZHU, Ji** [CN/US]; 3101 Carlson Boulevard #4, El Cerrito, California 94530 (US). **YUN, Seokmin** [KR/US]; 2749 Foxglove Court, Pleasanton, California 94588 (US). **MUI, David S.L.** [US/US]; 48472 Arkansas Place, Fremont, California 94539 (US). **MIKHAYLICHENKO, Katrina** [RU/US]; 1818 Fumia Place, San Jose, California 95131 (US).

(74) Agents: **LEE, Michael B.K. Lee** et al.; Beyer Law Group LLP, P.O. Box 1687, Cupertino, California 95015-1687 (US).

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[Continued on next page]

(54) Title: METHOD OF REDUCING PATTERN COLLAPSE IN HIGH ASPECT RATIO NANOSTRUCTURES

(57) Abstract: A method is provided for treating the surface of high aspect ratio nanostructures to help protect the delicate nanostructures during some of the rigorous processing involved in fabrication of semiconductor devices. A wafer containing high aspect ratio nanostructures is treated to make the surfaces of the nanostructures more hydrophobic. The treatment may include the application of a primer that chemically alters the surfaces of the nanostructures preventing them from getting damaged during subsequent wet clean processes.. The wafer may then be further processed, for example a wet cleaning process followed by a drying process. The increased hydrophobicity of the nanostructures helps to reduce or prevent collapse of the nanostructures.

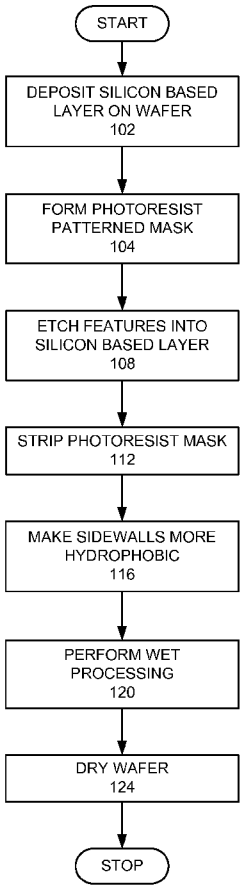

FIG. 1A

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METHOD OF REDUCING PATTERN COLLAPSE IN HIGH ASPECT RATIO NANOSTRUCTURES

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The invention relates to semiconductor devices. More specifically, the present invention relates to the production of semiconductor devices where wet chemical treatments are used on a wafer with high aspect ratio nanostructures that are sensitive to pattern collapse during processing.

Description of the related art

[0002] Semiconductor devices are fabricated using a long complex procedure. One portion of the procedure involves etching features into a stack of materials on a silicon wafer. The stack of materials may comprise a single layer of silicon based material such as SiO or SiN, or the stack may comprise multiple layers of materials such as SiO, SiN, TEOS, polysilicon or silicon in different orders within the stack. The stack may be formed by a number of methods, including physical vapor deposition, chemical vapor deposition, electrochemical deposition and molecular beam epitaxy, for example. Once the stack of materials is created, a photoresist layer is applied. This photoresist layer is used as a mask for etching. Many methods of etching may be used including methods of wet etching and dry etching. After the etching, the photoresist layer is usually removed, often by a plasma ashing procedure.

[0003] During the fabrication, the wafers are subjected to wet processing such as wet cleaning. Wet cleaning is helpful to prepare the surfaces and to remove residue left behind by some of the other processing. The cleaning process usually consists of chemical treatment in combination with megasonics, jets and/or other particle removal techniques followed by rinsing and drying. The drying may include bulk liquid removal from the surface by spin off, vacuum suction, Marangoni effect with isopropyl alcohol or combination of these commonly known techniques

[0004] A wafer may go through multiple occurrences of these steps during the entire fabrication process. Hence, as device features shrink on a wafer and as much liquid is used in the processing, strong capillary forces may exert enough force to collapse the structures during drying steps.

SUMMARY OF THE INVENTION

[0005] To achieve the foregoing and in accordance with the purpose of the present invention, a method of processing a wafer used in fabricating semiconductor devices is provided. The method teaches processing the wafer in such a way as to reduce or eliminate collapse of high aspect ratio features on the wafer. High aspect ratio features are formed in a silicon based layer that has been produced on the wafer. The sidewalls of the features are treated to make them more hydrophobic. A wet processing of the wafer is performed on the wafer and then the wafer is dried.

[0006] In another embodiment, a method of processing a wafer used in fabricating semiconductor devices is provided. High aspect ratio features are formed in a silicon based layer on the wafer. A wet processing of the wafer is performed. The wet processing includes wet cleaning the wafer, depositing a primer on the wafer that modifies surface properties of the features so as to increase the hydophobicity of the surfaces of the features and rinsing the wafer. After the wet processing, the wafer is then dried.

[0007] These and other features of the present invention will be described in more details below in the detailed description of the invention and in conjunction with the following figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

[0009] FIGS. 1A and 1B show high level flow charts of some embodiments of the invention.

[0010] FIGS. 2A-2C show an exemplary wafer undergoing a damaging wet processing and drying.

[0011] FIGS. 3A-3G show an exemplary wafer undergoing select steps of an embodiment of the invention.

[0012] FIGS. 4A-4G show an exemplary wafer undergoing select steps of an embodiment of the invention.

[0013] FIGS. 5A-5H show an exemplary wafer undergoing select steps of an embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0014] The present invention will now be described in detail with reference to a few preferred embodiments thereof as illustrated in the accompanying drawings. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process steps and/or structures have not been described in detail in order to not unnecessarily obscure the present invention.

[0015] Oxides and nitrides of silicon grown by low-temperature oxidation (LTO), chemical vapor deposition (CVD) and implantation have been traditionally used in front-end-of-the-line (FEOL) processing for electrical and thermal isolation, masking and encapsulation in high aspect ratio nanostructures. The use of such materials in FEOL applications has continued to offer the selectivity to reduce feature sizes and increase aspect ratios to achieve the desired densities of devices for 32 nm integrated circuit (IC) fabrication and beyond. Aspect ratios are now commonly in the range of 10:1 to 25:1 and possibly higher. However, as the critical dimensions continue to shrink and aspect ratios continue to increase in FEOL applications, problems associated with processing such densely fabricated nanostructures have surfaced and are anticipated to pose tremendous challenges for wet clean processes. One commonly observed problem has been the collapse of densely packed high aspect ratio nanostructures used for shallow trench isolation.

[0016] Fig. 2A shows a wafer 201 together with a set of nanostructures 202. Feature collapse occurs during wet cleaning and subsequent drying. Fig. 2B shows the nanostructures 202 of Fig. 2A during a wet cleaning where the fluid 204 has gathered between the nanostructures 202. Fluid enters the features during wet processing and strong capillary forces may exert sufficient force to damage the delicate nanostructures. In addition, the surface tension forces of the drying liquid tend to pull surfaces of adjacent nanostructures into contact. These forces are often exacerbated by the lack of balance of pressures across the many features due to non-uniformity of the fluid amounts gathered in the features, as well as non-uniformity in drying. These forces often lead to the collapse of the features individually or also through bridging. Bridging occurs when at least two adjacent nanostructures collapse

against one another and become adhered together. The sidewalls of adjacent nanostructures themselves may adhere together, or a residue material may gather between the nanostructures, joining them together. Fig. 2C shows two examples of feature collapse. One example is the single collapse of a nanostructure 206. The other example shows a bridging of two nanostructures 205. Other types of feature collapse are possible as well. Feature collapse can be a significant problem in semiconductor fabrication and can lead to defects in the circuits produced.

[0017] Some methods of reducing feature collapse have been explored. Examples include rinsing with ultra-low surface tension liquids such as 2-propanaol $\gamma = 22$ dynes /cm, use of fluorinated organic surfactants (HFE, $\gamma = 14$ dynes/cm) supercritical carbon dioxide drying, and drying using similar approaches at elevated temperatures. Some of these techniques have met with limited success; however, such techniques are costly and often require elaborate setups. For example, supercritical carbon dioxide requires high pressures to go to the critical point.

[0018] A wafer may go through multiple occurrences of wet processing and drying during the entire fabrication process. As device features shrink on a wafer, strong capillary forces may exert enough force to collapse the structures during drying steps. A cost-effective and simple method of processing the wafers is needed that reduces the occurrence of the collapsing of high aspect ratio nanostructures during sequential wet processing. In light of this notion, the present invention outlines a methodology that can be used during single wafer wet cleaning of high aspect ratio nanostructures on a wafer to avoid collapse and sticking.

[0019] Fig. 1A is a high level overview of an embodiment of the invention. At the start of the method, at least one silicon based layer is deposited upon a wafer (step 102). A photoresist patterned mask is formed over the silicon based layer (step 104) and features are etched into the silicon based layer using the photoresist as a mask (step 108). The photoresist mask is then stripped away (step 112). A procedure is then used to make the sidewalls of the features more hydrophobic (step 116). In one embodiment, this procedure may include depositing a primer on the wafer that chemically alters the surface of the features as a first step in the process flow without needing to wet the features. This step can be carried out by exposing the surface of interest to the vapor of the modifying agent prior to the wet processing. Wet

processing is then performed on the wafer (step 120), which may include a sequential series of wet cleaning steps to clean the features of common residues left behind after etch. The wafer is then dried (step 124).

[0020] Fig. 1B is a high level overview of another embodiment of the invention. In this embodiment, the steps of making the sidewalls more hydrophobic (step 116) and the wet processing (step 120) are combined into one step of making the sidewalls more hydrophobic during the wet processing (step 124). For example this step can be carried out by exposing the surface of interest to a liquid solution that contains the modifying agent prior to or after the wet clean sequence. The liquid solution that contains the surface modifying agent can be derived from solvents that are miscible with the agent such as n-Hexane, Toluene, NPM, DMSO, Acetone, DMF, DMAC, or HFEs. The other steps may be left unchanged.

[0021] Figs. 3A – 3G show an example of a wafer with high aspect nanostructures at selected steps of an embodiment of the disclosed method. Fig. 3A shows the result after step 102 has been performed. A layer of silicon based material 306 has been formed on the wafer 301. There are many processes that may be used to form the silicon based layer 306. For example, the layer may be formed by physical vapor deposition, chemical vapor deposition, electrochemical deposition or molecular beam epitaxy. While Fig. 3A shows a single uniform silicon based layer 306, it is important to note that multiple layers of materials may be used depending on many factors, such as the intended use of the circuit being fabricated or the specific fabrication process being used. Examples of multilayer structures include a common shallow trench isolation (STI) stack consisting of TEOS at the top followed by SiN, then PolySi, and then Si at the bottom, or a stack consisting of SiN at the top followed by TEOS, then another layer of SiN, then PolySi, and then Si at the bottom. In another embodiment, a silicon based layer 306 is not formed on the wafer 301. Instead, the silicon wafer 301 is etched.

[0022] Fig. 3B shows the wafer 301 with the layer of silicon based material 306 and a photoresist layer 305 that has been patterned. A photoresist layer 305 is deposited on the silicon based material, often using a spin coating process and the photoresist is patterned using photolithography (step 104). The photoresist layer 305 is used as a mask to determine what silicon based material to remove and what to

leave behind during the etching process. A wet or dry etching process (step 108) is used to remove the material not covered by the photoresist 305.

[0023] Fig. 3C shows the wafer 301 after the etching, showing the nanostructures 302 formed by the etching (step 108). At this point the photoresist 305 is still present. After the etching, the photoresist material may then be removed (step 112). The photoresist may be removed by a chemical stripping process or by an ashing process.

[0024] Fig. 3D shows a wafer 301 and four columns of the silicon based material that remains after etching and photoresist removal. The columns of the silicon based material make up the nanostructures 302. It is important to note that while the figures show a particular example of features that may be etched on the wafer 301, other numbers and types of features are possible.

[0025] Fig. 3E shows the wafer 301 and nanostructures 302 after a layer of primer 303 has been deposited on the nanostructures 302 (step 116). The primer 303 may be a monolayer formed by self-assembly or any other known deposition process. Alternatively, the primer layer 303 may be thicker, such as a film. Some examples of possible surface modifying agents include hexamethyldisiloxane (HMDS), and various alkoxysilanes and alkysilanes. More specifically, fluorinated or long chain hydrocarbon based trichlorosilane, dichlorosilane, monochlorosilane, trimethoxysilane, dimethoxysilane, methoxysilane, triethoxysilane, diethoxysilane, and ethoxysilane to name a few examples.

[0026] Adding the primer 303 to the nanostructures 302 helps reduce feature collapse by modifying the surface properties of the nanostructures 302. The surface of the nanostructures 302 is chemically altered such that the stiction force between two adjacent surfaces is reduced or preferably eliminated by making the surfaces of the nanostructures 302 more hydrophobic. One example of a chemical modification that would modulate stiction would be substituting polar hydroxyl groups of a nanostructure surface (for example Si-O or Si-N, often used to fabricate high aspect ratio nanostructures) with nonpolar groups, such as Si-CH3, Si-R or Si-RF (where R is a hydrocarbon or fluoro substituted chain of n-length). The Si-CH3 groups may be provided, for example, by HDMS ($C_6H_{18}OSi_2$). Another example of chemical modifier is 1H, 1H, 2H, 2H-perfluorooctyltrichlorosilane (FOTS, $C_8F_{13}H_4SiCl_3$). The presence of nonpolar groups provides a stable modified surface with DI water contact

angles varying from 70-130° where development of excessive forces due to liquid meniscus formation can be prevented.

[0027] The primer 303 may be added before the wet phase of processing via reaction of the surface with its vapor. When added before the wet phase, the primer 303 additionally acts to minimize or prevent the excessive stictional forces that are often exerted by the adsorption of water on surfaces that are in close proximity. A sample process flow using FOTS is first generating a stock solution of chemical modifier by mixing a solution of 0.1-50% FOTS by weight with anhydrous n-hexane, then co-heating one drop of the stock solution with the sample to be modified in an oven at a temperature of 40-200°C. After approximately 2-300 seconds, the stock solution evaporates completely and FOTS molecule reacts with the sample surface. A surface prepared this way has DI water contact angle larger than 120°.

[0028] Alternatively, the primer may be added during the wet phase processing (step 126) by use of suitable solvents containing the modifying agent. This step could be applied either before or after the wet clean steps in the sequential process flow. A sample process using FOTS is immersing the sample into 0.01-50% by weight of FOTS in HFE-7100 (3M, Minneapolis, MN), Toluene, n-hexane, chloroform, or acetone for approximately 10 seconds up to 1 hour under nitrogen, followed by rinsing ultrasonically with fresh HFE-7100, then drying with nitrogen.

[0029] Fig. 3F shows the wafer 301 undergoing a wet processing (step 120) such as a wet cleaning after having the primer 303 applied. The liquid 304 from the wet processing is gathered within the nanostructures 302 and is repelled by the now more hydrophobic sidewalls of the nanostructures 302. The increased hydrophobicity of the sidewalls of the nanostructures 302 reduces the capillary forces present between the nanostructures 302 and prevents the formation of a concave meniscus in the fluid gathered within the features. Fig. 3G shows the wafer 301 after it has been dried from a DI water rinse (step 124). Optionally, the primer 303 may be removed after the drying, for example by an oxygen or carbon dioxide flash process. This would return the wafer 301 and nanostructures 302 to the state shown in Fig. 3D, but with any processing residue greatly reduced or removed.

[0030] Figs. 4A – 4G show an example of a wafer 301 with high aspect ratio nanostructures 302 at selected steps of another embodiment of the disclosed invention. Fig. 4A shows the result after step 102 has been performed. A layer of

silicon based material 306 has been formed on the wafer 301. There are many processes that may be used to form the silicon based layer 306. For example, the layer may be formed by physical vapor deposition, chemical vapor deposition, electrochemical deposition or molecular beam epitaxy. While Fig. 4A shows a single uniform silicon based layer 306, it is important to note that multiple layers of materials may be used depending on many factors, such as the intended use of the circuit being fabricated or the specific fabrication process being used. Examples of multilayer structures include a stack consisting of TEOS at the top followed by SiN, then PolySi, and then Si at the bottom, or a stack consisting of SiN at the top followed by TEOS, then another layer of SiN, then PolySi, and then Si at the bottom.

[0031] Fig. 4B shows the wafer 301 with the layer of silicon based material 306 and a photoresist layer 305 that has been patterned. A photoresist layer 305 is deposited on the silicon based material, often using a spin coating process and the photoresist is patterned using photolithography (step 104). The photoresist layer 305 is used as a mask to determine what silicon based material to remove and what to leave behind during the etching process. A wet or dry etching process (step 108) may be used to remove the material not covered by the photoresist 305.

[0032] Fig. 4C shows the wafer 301 after the etching, showing the nanostructures 302 formed by the etching (step 108). At this point the photoresist 305 is still present. After the etching, the photoresist material 305 may then be removed (step 112). The photoresist 305 may be removed by a chemical stripping process or by an ashing process.

[0033] Fig. 4D shows a wafer 301 and four columns of the silicon based material that remain after etching and photoresist removal (step 112). The columns of the silicon based material make up the nanostructures 302. It is important to note that while the figures show a particular example of features that may be etched on the wafer 301, other numbers and types of features are possible.

[0034] In this embodiment, the sidewalls of the nanostructures 302 are made more hydrophobic (step 116) by a roughening process. The surface of the nanostructures 302 can be reacted with a chemical substituent such that the surface morphology of the nanostructures 302 is changed. For example, while the photoresist 305 is spin-coated on the silicon based layer 306 the polymer resist can be exposed to a fluorine (F) and oxygen (O) mixture plasma to induce polymer re-deposition on the

substrate. The re-deposited polymer generated by the plasma reaction is not a smooth thin film hence it can be used as a mask to etch the underlying substrate. An alternating deposition and etch process can be used to vary the surface roughness and achieve the required topography to produce a super-hydrophobic surface via a subsequent C_4F_8 plasma thin film coating process. The change results in rough interfaces 401, as shown in Fig. 4E, with increased surface area for subsequent reactions with surface modifiers such that the surface becomes more hydrophobic. Roughening may be implemented by RIE texturing using polymerzing plasma and dry or vapor phase fluoride etching at increased temperature, for example.

[0035] Fig. 4F shows the wafer 301 undergoing a wet processing (step 120) such as a wet cleaning after having surfaces of the nanostructures roughened to increase surface area for subsequent surface modification reactions. The liquid 304 from the wet processing is gathered within the nanostructures 302 and is repelled by the now more hydrophobic sidewalls of the nanostructures 302. The increased hydrophobicity of the sidewalls of the nanostructures 302 reduces the capillary forces present between the nanostructures 302 and prevents the formation of a concave meniscus in the fluid gathered within the features. Fig. 4G shows the wafer 301 after it has been dried (step 124) and showing no signs of feature collapse.

[0036] Figs. 5A – 5H show an example of a wafer 301 with high aspect ratio nanostructures 302 at selected steps of another embodiment of the disclosed invention. Fig. 5A shows the result after step 102 has been performed. A layer of silicon based material 306 has been formed on the wafer 301. There are many processes that may be used to form the silicon based layer 306. For example, the layer may be formed by physical vapor deposition, chemical vapor deposition, electrochemical deposition or molecular beam epitaxy. While Fig. 5A shows a single uniform silicon based layer 306, it is important to note that multiple layers of materials may be used depending on many factors, such as the intended use of the circuit being fabricated or the specific fabrication process being used. Examples of multilayer structures include a stack consisting of TEOS at the top followed by SiN, then PolySi, and then Si at the bottom, or a stack consisting of SiN at the top followed by TEOS, then another layer of SiN, then PolySi, and then Si at the bottom.

[0037] Fig. 5B shows the wafer 301 with the layer of silicon based material 306 and a photoresist layer 305 that has been patterned. A photoresist layer 305 is

deposited on the silicon based material, often using a spin coating process and the photoresist is patterned using photolithography (step 104). The photoresist layer 305 is used as a mask to determine what silicon based material to remove and what to leave behind during the etching process. A wet or dry etching process (step 108) may be used to remove the material not covered by the photoresist 305.

[0038] Fig. 5C shows the wafer 301 after the etching, showing the nanostructures 302 formed by the etching (step 108). At this point the photoresist 305 is still present. After the etching, the photoresist material 305 may then be removed (step 112). The photoresist 305 may be removed by a chemical stripping process or by an ashing process.

[0039] Fig. 5D shows a wafer 301 and four columns of the silicon based material that remain after etching and photoresist removal (step 112). The columns of the silicon based material make up the nanostructures 302. It is important to note that while the figures show a particular example of features that may be etched on the wafer 301, other numbers and types of features are possible.

[0040] Fig. 5E shows the wafer 301 undergoing a wet cleaning during wet processing to clean etch or ash residue from previous processes. The wet cleaning chemicals 501 may include: aqueous, semi-aqueous or organic solutions of chemicals or combination of chemicals including HCl, HF, NH_4F, NH_3 aqueous solution, H_2SO_4, H_2O_2, for example.

[0041] Fig. 5F shows the surfaces of the nanostructures 302 being made more hydrophobic by depositing surface modifying agents 303 during wet processing (step 126) after the wet cleaning shown in Fig. 5E. One particular example of a procedure to make the surfaces of the nanostructures 302 more hydrophobic is: 1) rinsing away the wet cleaning chemicals 501 with DI water, 2) replacing DI water with isopropyl alcohol, 3) replacing isopropyl alcohol with HFEs, 4) immersing the wafer into 0.01-50% by weight of FOTS in HFE for approximately 2 seconds - 10 minutes, and 5) rinsing with HFE. An alternative example is: 1) rinsing away the wet cleaning chemicals 501 with DI water, 2) replacing DI water with organic solvents that don't contain an –OH group, but are also miscible with DI water (Examples of solvents having such properties include: DMF, DMAC, acetone, NMP.), 3) immersing the wafer into 0.01-50% by weight of FOTS in the organic solvent solution for approximately 2 seconds - 10minutes, and 4) rinsing with the organic solvent. Item

502 of Fig. 5F represents the chemicals used during the procedure of making the surfaces of the nanostructures 302 more hydrophobic.

[0042] Fig 5G shows the step to re-introduce DI water 304 into the hydrophobic nanostructures 302 after Fig. 5F to exploit the high Laplace pressure generated by convex water meniscus inside the hydrophobic nanostructures 302 to prevent the nanostructures 302 from collapse during the drying process. One particular example of doing so is: 1) replacing the HFE with isopropyl alcohol, and 2) replacing isopropyl alcohol with DI water. Since isopropyl alcohol has a lower surface tension than DI water and is miscible with DI water, immersion in isopropyl alcohol first then in DI water can introduce DI water into the hydrophobic nanostructures 302 through diffusion process. Alternatively, if the step represented by Fig. 5F ends with an organic solvent that does not contain –OH group, but miscible with water, a simple DI water wash step can be applied here.

[0043] Fig 5H shows intact high density high aspect ratio nanostructures 302 after drying.

[0044] While this invention has been described in terms of several preferred embodiments, there are alterations, permutations, modifications and various substitute equivalents, which fall within the scope of this invention. It should also be noted that there are many alternative ways of implementing the methods and apparatuses of the present invention. It is therefore intended that the following appended claims be interpreted as including all such alterations, permutations, modifications, and various substitute equivalents as fall within the true spirit and scope of the present invention.

CLAIMS

What is claimed is:

1. A method of processing a wafer used in fabricating semiconductor devices, said method comprising:

forming high aspect ratio features in a silicon based layer on the wafer;

making sidewalls of the features more hydrophobic;

performing wet processing of the wafer; and

subsequently drying the wafer.

2. The method of claim 1, wherein the making the sidewalls of the features more hydrophobic is accomplished by depositing a primer on the wafer, wherein the primer makes the sidewalls more hydrophobic by chemically altering the surface of the features.

3. The method of claim 2, wherein the primer is deposited on the wafer by way of vapor deposition prior to the performing wet processing of the wafer.

4. The method of claim 3, wherein the depositing of the primer on the wafer prior to the wet processing comprises:

generating a primer solution by mixing a solution of 0.1-50% by weight of $C_8F_{13}H_4SiCl_3$ (FOTS) with anhydrous n-hexane; and

co-heating a portion of the primer solution with the wafer such that the primer solution evaporates and the FOTS molecule reacts with the sidewalls of the nanostructures.

5. The method of claim 2, wherein the primer is deposited on the wafer by way of liquid deposition during the wet processing of the wafer.

6. The method of claim 5, wherein the performing wet processing of the wafer includes rinsing the wafer subsequent to the depositing the primer on the wafer during the wet processing.

7. The method of claim 2, wherein the primer comprises a self-assembled monolayer.

8. The method of claim 2, wherein the primer comprises a film, and wherein the film comprises at least one of: hexamethyldisiloxane, an alkoxysilane or an alkysilane.

9. The method of claim 1, wherein the making the sidewalls more hydrophobic is accomplished by roughening the sidewalls.

10. The method of claim 9, wherein the roughening of the sidewalls is accomplished by way of exposing the wafer to at least one of: polymerizing plasma, hydrogen fluoride vapor or fluoride based plasma etch.

11. The method of claim 9, wherein the roughening of the sidewalls is accomplished by reactive-ion etching.

12. The method of any of claims 1-11, wherein the forming the high aspect ratio features comprises:

forming a photoresist patterned mask over the silicon based layer; and

etching the high aspect ratio features into the silicon based layer.

13. The method of claim 12, wherein the forming the high aspect ratio features further comprises stripping the photoresist patterned mask.

14. A method of processing a wafer used in fabricating semiconductor devices, said method comprising:

forming high aspect ratio features in a silicon based layer on the wafer;

performing a wet processing of the wafer, wherein the wet processing comprises:

wet cleaning the wafer;

depositing a primer on the wafer that modifies surface properties of the features so as to increase the hydrophobicity of the surfaces of the features; and

replacing organic solvent used in primer deposition with DI water; and subsequently drying the wafer

15. The method of claim 14, wherein the primer comprises a self-assembled monolayer.

16. The method of claim 14, wherein the primer comprises a film, and wherein the film comprises at least one of: hexamethyldisiloxane, an alkoxysilane or an alkysilane.

17. The method of claim 14 wherein the depositing the primer on the wafer comprises:

immersing the wafer in a solution of 0.01-50% by weight $C_8F_{13}H_4SiCl_3$ (FOTS) in at least one of HFE, Toluene, n-hexane, chloroform or acetone, under a nitrogen atmosphere; and

rinsing with HFE;

18. The method of any of claims14 -17 wherein the replacing of organic solvent comprises:

rinsing the wafer with an organic solvent miscible with water; and

rinsing the wafer with DI water.

19. The method of any of claims 14-18 wherein a solution used in the wet cleaning of the wafer comprises one or more of: HCl, HF, NH_4F, NH_3 aqueous solution, H_2SO_4 or H_2O_2.

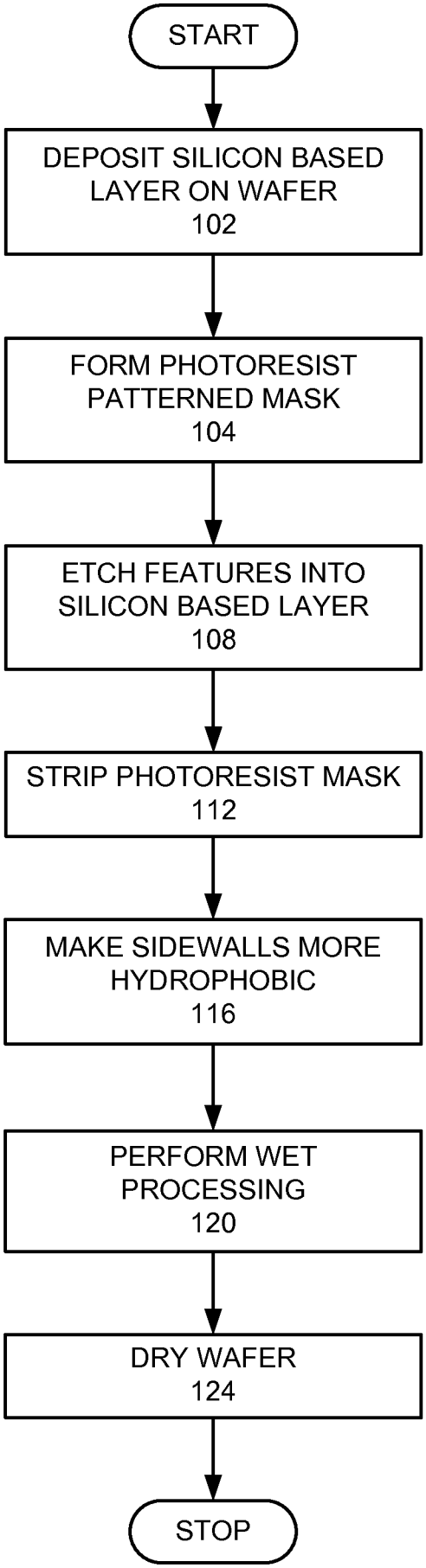
START
DEPOSIT SILICON BASED LAYER ON WAFER 102
FORM PHOTORESIST PATTERNED MASK 104
ETCH FEATURES INTO SILICON BASED LAYER 108
STRIP PHOTORESIST MASK 112
MAKE SIDEWALLS MORE HYDROPHOBIC 116
PERFORM WET PROCESSING 120
DRY WAFER 124
STOP

FIG. 1A

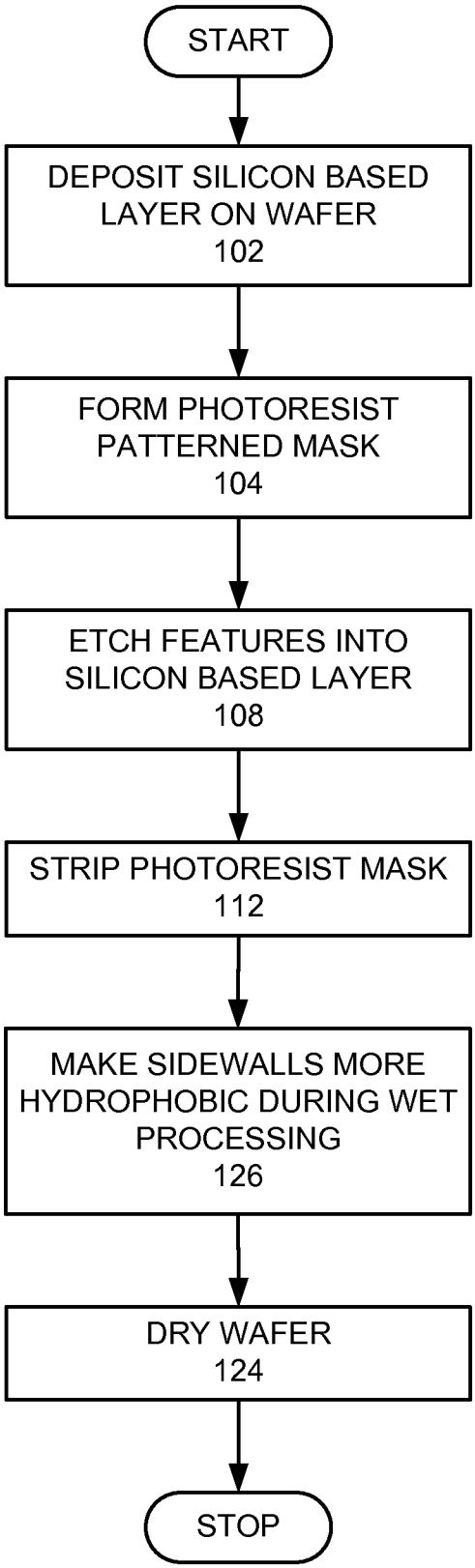
START
DEPOSIT SILICON BASED LAYER ON WAFER 102
FORM PHOTORESIST PATTERNED MASK 104
ETCH FEATURES INTO SILICON BASED LAYER 108
STRIP PHOTORESIST MASK 112
MAKE SIDEWALLS MORE HYDROPHOBIC DURING WET PROCESSING 126
DRY WAFER 124
STOP

FIG. 1B

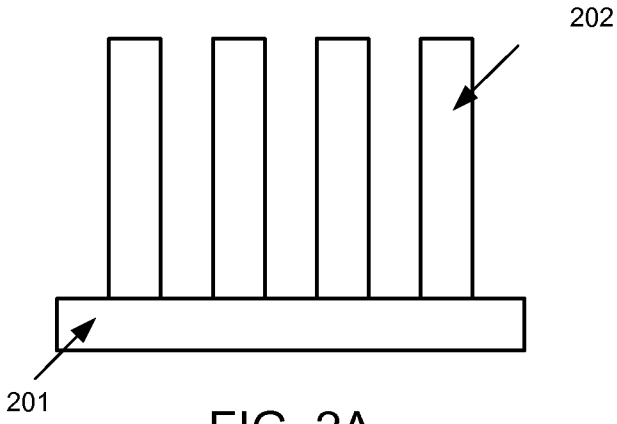

FIG. 2A

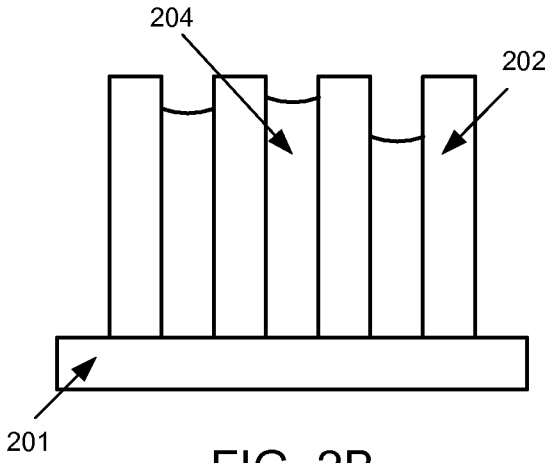

FIG. 2B

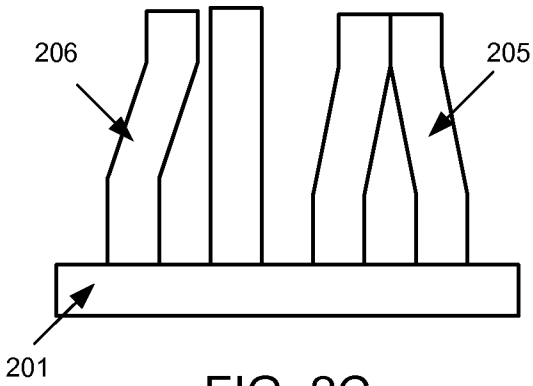

FIG. 2C

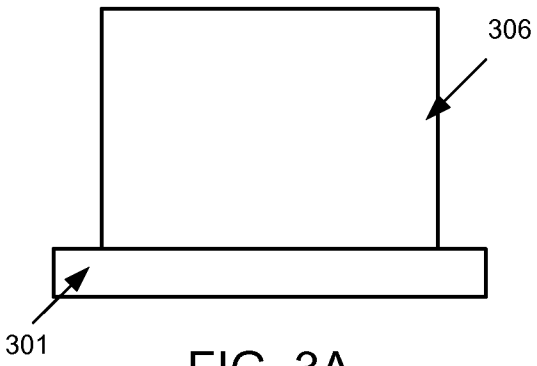

FIG. 3A

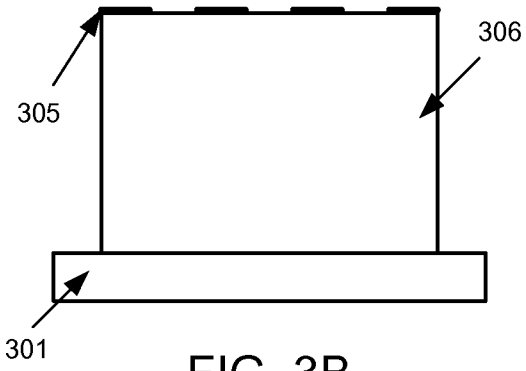

FIG. 3B

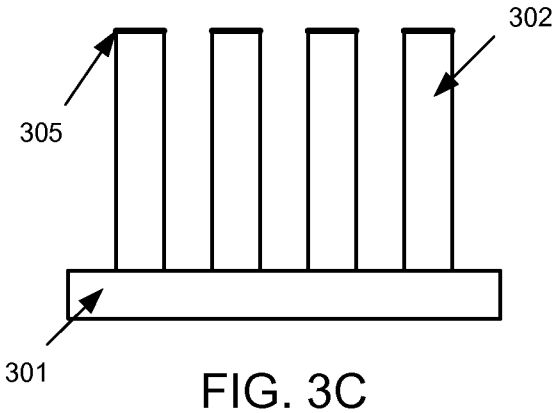

FIG. 3C

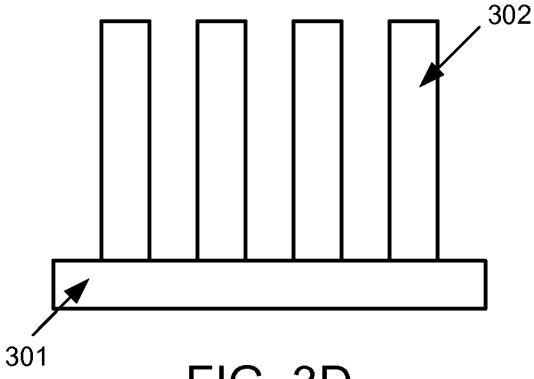

FIG. 3D

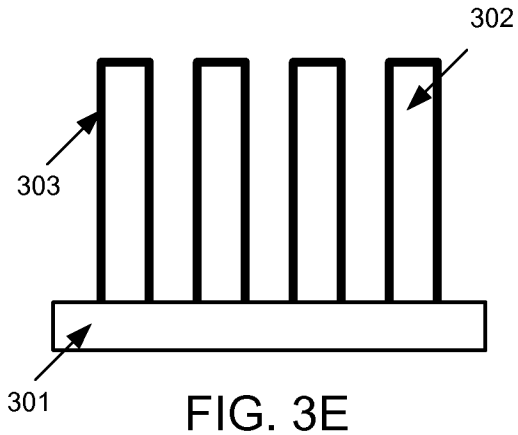

FIG. 3E

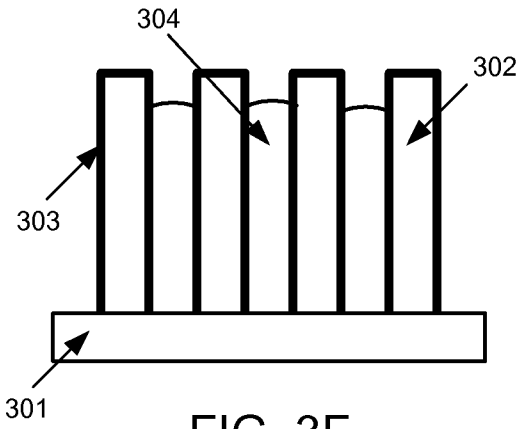

FIG. 3F

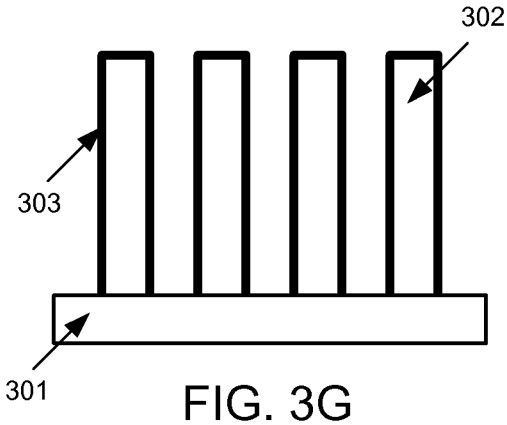

FIG. 3G

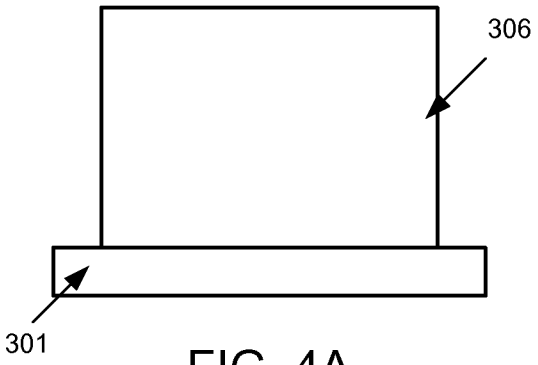

FIG. 4A

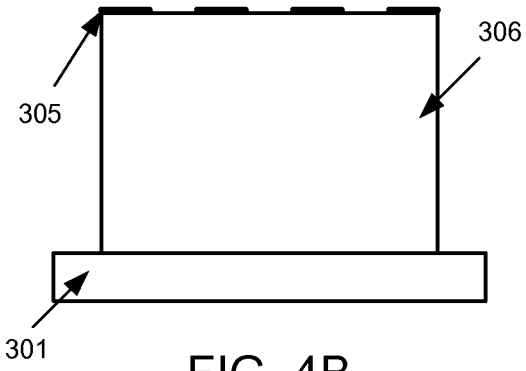

FIG. 4B

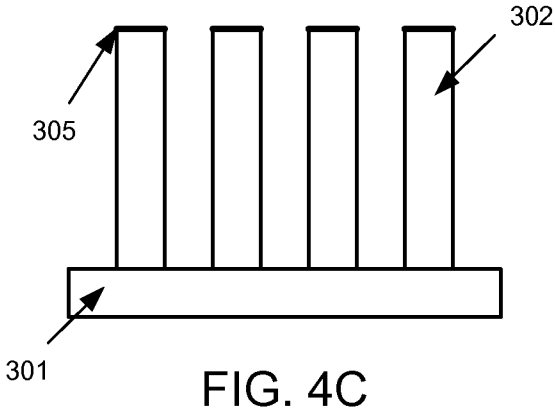

FIG. 4C

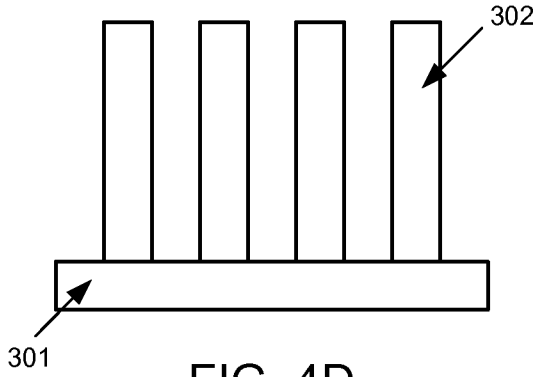

FIG. 4D

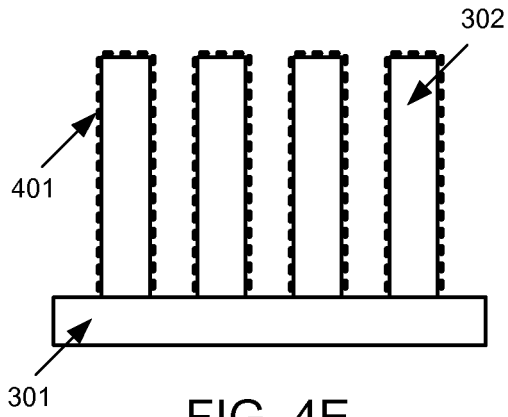

FIG. 4E

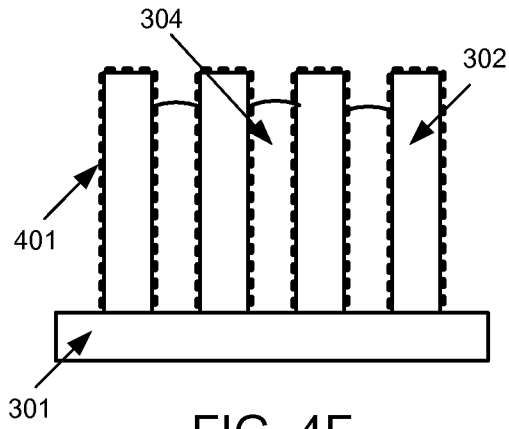

FIG. 4F

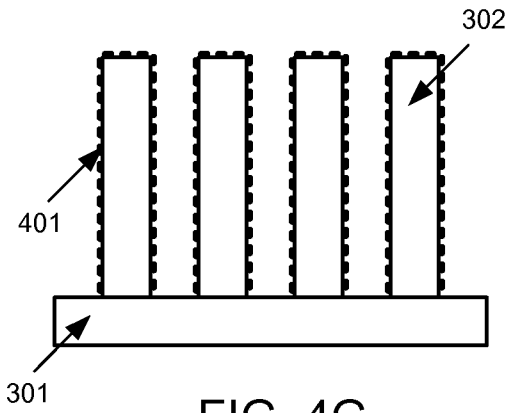

FIG. 4G

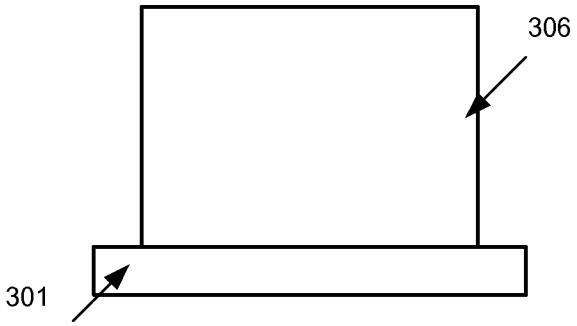

FIG. 5A

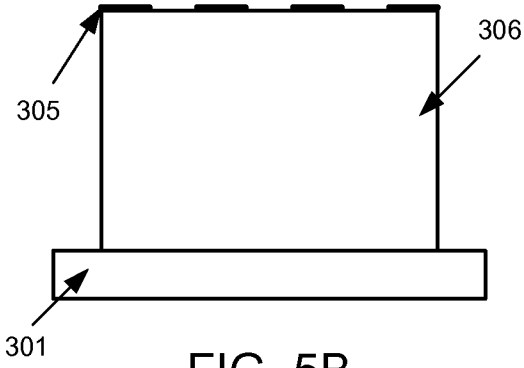

FIG. 5B

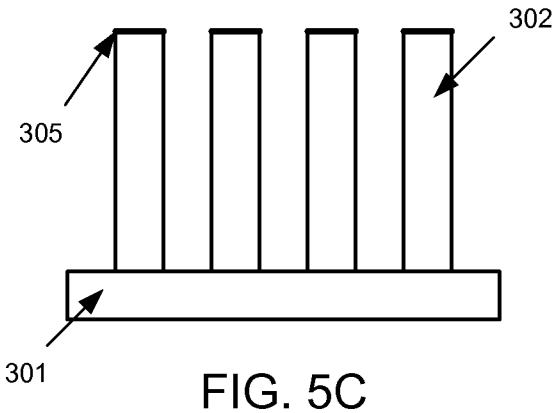

FIG. 5C

FIG. 5D

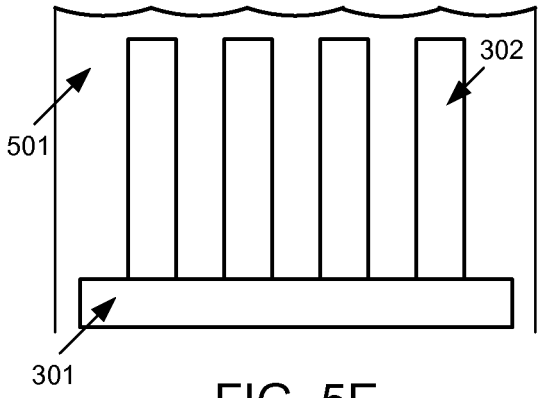

FIG. 5E

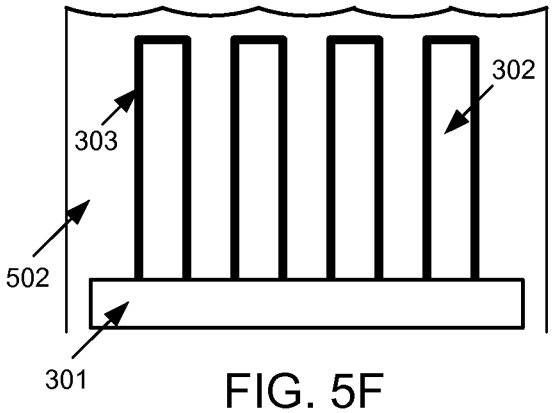

FIG. 5F

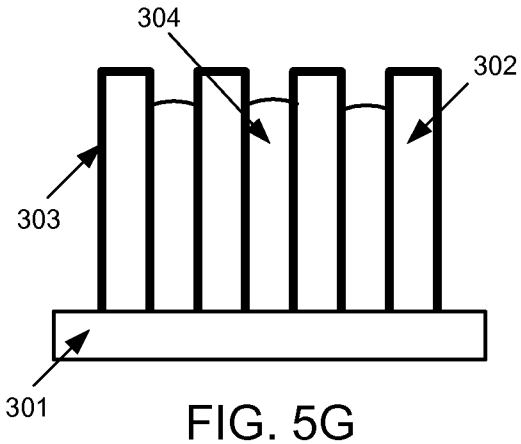

FIG. 5G

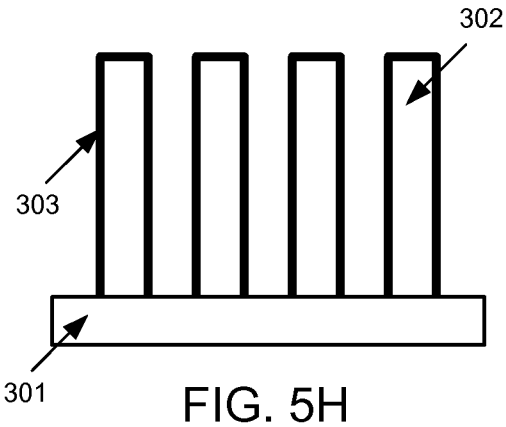

FIG. 5H