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(54) Title: IN-SITU TRANSISTOR RECOVERY SYSTEMS AND METHODS

(57) Abstract: An embodiment includes a method comprising: determining the system, which includes a hardware processor comprising a transistor, is operating in a first system power state; determining the transistor is operating in a first transistor power state; and in response to determining the first system and first transistor power states, elevating a temperature of the transistor for a predetermined period of time. Other embodiments are described herein.

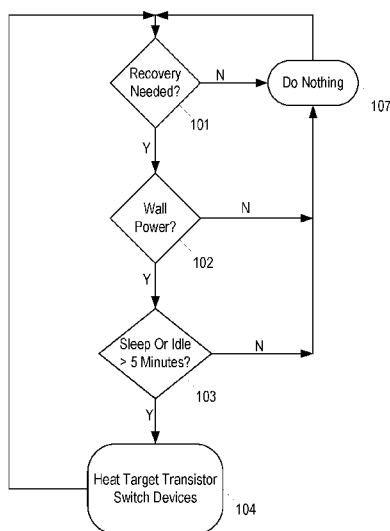


Figure 1



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IN-SITU TRANSISTOR RECOVERY SYSTEMS AND METHODS

Technical Field

[0001] Embodiments of the invention are in the field of semiconductor devices and, in particular, transistors.

Background

[0002] As integrated circuit fabrication technology improves, semiconductor manufacturers are able to integrate additional functionality onto a single silicon substrate and/or include more transistors in the same area (Moore's law). As transistor density and functionalities increase so too does the probability of having circuits operating at marginal voltage specifications increase. Consequently, some burn-in (BI) process is often applied to products and extra voltage "guardbanding" is applied to help ensure aging does not affect processor performance until the end of targeted life for the processor. However, transistor aging removes part of the initial voltage guardband.

[0003] Furthermore, additional components and the use of more transistors may increase signal switching that, in turn, generates more heat and more operating time at higher voltages. The additional heat and high voltage may damage various components of a chip. For example, memory devices that utilize p-channel metal-oxide semiconductor (P-MOS) transistors may be affected by the additional heat when the transistors are negatively biased over time (e.g., due to negative bias temperature instability (BTI)). Another example of possible failures is that oxide degradation may also damage the transistors over time. This can be generalized for processor failure mechanisms dependent on temperature and voltage.

[0004] As processor memory devices degrade their functionality may suffer due to, for example, a shift in their gate threshold voltage (V_{th}). Designs may include voltage margins to reduce the impact by such degradations, but the additional design margins may reduce processor performance, increase processor power consumptions, and/or increase the requisite area to provide to the processor and memory devices.

Brief Description of the Drawings

[0005] Features and advantages of embodiments of the present invention will become apparent from the appended claims, the following detailed description of one or more example embodiments, and the corresponding figures. Where considered appropriate, reference labels have been repeated among the figures to indicate corresponding or analogous elements.

Figure 1 includes a process in an embodiment.

Figure 2 includes a process in an embodiment.

Figure 3 includes a system that further includes a BTI threshold voltage restoration system.

Figure 4 includes a system that further includes a BTI threshold voltage system.

Figure 5 includes a system that further includes a BTI threshold voltage system.

Detailed Description

[0006] Reference will now be made to the drawings wherein like structures may be provided with like suffix reference designations. In order to show the structures of various embodiments more clearly, the drawings included herein are diagrammatic representations of structures. The drawings may only show the structures useful to understand the illustrated embodiments. Additional structures known in the art may not have been included to maintain the clarity of the drawings. For example, not every layer of a semiconductor device is necessarily shown. "An embodiment", "various embodiments" and the like indicate embodiment(s) so described may include particular features, structures, or characteristics, but not every embodiment necessarily includes the particular features, structures, or characteristics. Some embodiments may have some, all, or none of the features described for other embodiments. "First", "second", "third" and the like describe a common object and indicate different instances of like objects are being referred to. Such adjectives do not imply objects so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner. "Connected" may indicate elements are in direct physical or electrical contact with each other and "coupled" may indicate

elements co-operate or interact with each other, but they may or may not be in direct physical or electrical contact.

[0007] As mentioned above, transistors may be affected by aging. For example, long operation of the transistor at high voltage(s) introduces degradation of the transistor threshold voltage ($V_{\min}$) for a group of transistors (where $V_{\min}$ is the maximum V_{th} for the group of transistors). Increasing $V_{\min}$ in turn increases the target values for the minimum fused voltage (e.g., the minimum voltage a processor requires). The voltage increase generates more transistor degradation (due to the effect of the sustained use of higher voltages) and more power consumption (again due to the effect of the sustained use of higher voltages).

[0008] However, a transistor can recover some V_{th} if it is exposed to higher temperatures. An embodiment leverages this effect and provides an in-situ transistor recovery application (i.e., available in the end product at the consumer level and not, for example, only available during testing of a transistor at a fabrication (fab) facility). Such an embodiment provides, in situ (e.g., in a computing node such as a desktop, laptop, Smartphone, wearable, thermostat, spectacles) transistor recovery as follows.

[0009] After the transistor is subject to stress degradation and a change in $V_{\min}$ occurs. A portion of this voltage degradation is recovered by exposing the device to high temperatures while at lower voltages. For example, the embodiment generates high temperatures (e.g., above 80-90 C) while the computing node is charging (e.g., when a user charges a Smartphone overnight) or in sleep (when a node on the Internet of Things (IoT) is not active) or hibernate modes. The high temperatures and higher voltages may affect transistors in the processor including transistors with elevated $V_{\min}$.

[0010] Embodiments may employ different methods to achieve high temperatures. One embodiment uses logic (e.g., hardware, software, firmware) to determine when a computing node has an active screen saver or when the node is hibernation. Upon such a determination the logic triggers the generation of higher temperatures. The embodiment may use a power virus application, scan function, and the like to

generate the higher temperature for a short period of time (e.g., 10, 20, 30, 40, 50, 60 seconds or more), although other embodiments are not so limited (e.g., some embodiments may include a time span of 10-30, 30-60, 60-90 seconds or more).

[0011] A power virus is logic that executes specific machine code in order to reach the maximum processor power dissipation (e.g., total thermal energy output for the central processing units). Computer cooling apparatuses are designed to dissipate power up to the thermal design power, rather than maximum power. A power virus may be included in test logic used for integration testing and thermal testing of computer components during the design phase of a product, or for product benchmarking. Stability test applications are similar logic that have the same effect as power viruses (i.e., high CPU usage) but stay under the user's control. They are used for testing CPUs, for example, when overclocking. Different micro-architectures typically require different logic to hit their maximum power.

[0012] Other embodiments may use dedicated test circuitry or other circuitry to generate the extra heat for short periods of time (e.g., 10, 20, 30, 40, 50 or 60 seconds).

[0013] Such "test circuitry" may include, for example, Joint Test Action Group (JTAG) boundary scan (scan function) technology that provides access to many logic signals of a complex integrated circuit, including the device pins. The signals are represented in the boundary scan register (BSR) accessible via a test access port. This permits testing as well as controlling the states of the signals for testing and debugging. Therefore, both software and hardware (manufacturing) faults may be located and an operating device may be monitored. When combined with built-in self-test (BIST), the JTAG scan chain enables a low overhead, embedded solution to testing a circuit for certain static faults (shorts, opens, and logic errors). The ability to perform such testing on finished boards may be considered a part of Design for Test in a product. The boundary scan test circuitry (which executes scan functions) may generate elevated heat when operated.

[0014] Such "other circuitry" may include neighboring circuitry, such as a baseband processor (see 905 of Figure 3), which may be used to expose transistors within

registers of an application processor (see 910 of Figure 3) to elevated temperatures. A baseband processor (also known as baseband radio processor, BP, or BBP) is a device (a chip or part of a chip) in a network interface that manages all the radio functions (all functions that require an antenna); however, this term is generally not used in reference to Wi-Fi and Bluetooth radios. A baseband processor typically uses its own RAM and firmware. The application processor may include a CPU.

[0015] While transistor threshold voltage is being recovered, the transistor may be in a relatively low voltage state such as the “low frequency mode” described immediately below.

[0016] For example, Enhanced Intel® SpeedStep® Technology provides thermal and power management by giving application software control over the processor's operating frequency and input voltage. Systems can manage power consumption dynamically. The technology allows the processor performance and power consumption levels to be modified while a system is functioning. This is accomplished via application software, which changes the bus-to-core frequency ratio and the processor core voltage (V_{cc}). A variety of inputs such as system power source, processor thermal state, or operating system policy are used to determine the proper operating state. Frequency/Voltage power states may be provided as follows for a processor: 1.6 GHz (HFM)/1.484 V; 1.4 GHz/1.420 V; 1.2 GHz/1.276 V; 1.0 GHz/1.164 V; 800 MHz/1.036 V; 600 MHz (LFM)/0.956 V. The top and bottom modes may be referred to as high frequency mode (HFM) and low frequency mode (LFM). These frequency and voltage operating points are stored within a read-only processor model specific register (MSR). This MSR ensures BIOS will not allow transitions to invalid states above the HFM maximum or below the LFM minimum. The other four operating points are stored within BIOS code, as a drop in voltage table provided to BIOS vendors.

[0017] An embodiment provides transistor recovery at normal operating temperatures with most recovery at higher temperatures. 10 seconds may suffice for BTI recovery, however other embodiments may provide treatment for 20, 40, 60 seconds or more. Logic for running the recovery profile (e.g., elevating temperature while keeping target transistor at relatively low voltage) may be located in firmware in

the power control unit (PCU), which may be located in the CPU or power management integrated circuit (PMIC) 915 of Figure 3. The recover profile may be run on a daily schedule. A PCU may have other responsibilities such as, for example, if only two cores of a four-core machine are active the PCU may completely shut down the inactive cores and divert spare power to active ones. The unit can also moderate the speed and power consumption of each core independently.

[0018] Other operations may be performed to increase heat for the target transistor. For example, cooling fans may be turned off along with operation of a power virus to generate a short time interval (e.g., 10 seconds) of heat that has minimum impact on the user. Another option may include generating heat using a fully integrated voltage regulator (FIVR) that regulates voltage and is located on the same chip as a processor. The voltage regulator may generate significant heat that can be directed towards target transistors within a processor core or cache memory located on the same chip as the processor.

[0019] Thus, embodiments may arrest or reverse $V_{\min}$, thereby arresting or reversing or at least deterring transistor degradation (due to the effect of the sustained use of higher voltages) and lowering power consumption (again due to the effect of the sustained use of higher voltages).

[0020] Figure 1 includes a process 100 in an embodiment. Block 101 determines whether recovery is needed for a target transistor or group of transistors. The determination may be made based on various factors such as, for example, (1) whether a predetermined period of time has passed since the last recovery process has been performed, (2) whether a predetermined amount of usage has occurred for the transistor(s), (3) whether a predetermined amount of usage has occurred for the transistor(s) within a predetermined time period; (4) whether a “reliability meter” indicates a threshold level of hardware problems have occurred, and the like.

[0021] A reliability meter or monitor is a tool that measures hardware and software problems and other changes to a computing node. It provides a stability index that ranges from a first value (the least stable) to another value (the most stable).

[0022] If block 101 results in “no”, the process moves to block 107 and then resumes. If “yes”, block 102 determines whether the computing node is powered by battery or a source such as wired power from a municipal power grid. This may ensure a large amount of power is not drained from a battery in an effort to create redemptive high temperatures.

[0023] If “yes”, block 103 determines whether the computing node is in sleep mode.

[0024] Sleep mode (also known as “Stand By” or “Suspend to RAM”) is where machine state is held in RAM and, when placed in sleep mode, the computer lowers power to unneeded subsystems and places the RAM into a minimum power state, just sufficient to retain its data. A computer must consume some energy while sleeping in order to power the RAM and to be able to respond to a wake-up event. A sleeping PC is a case of a device on standby power. In addition to a wake-up press of the power button, PCs can also respond to other wake cues, such as from keyboard and mouse.

[0025] Hibernation, also called “Suspend to Disk”, saves all computer operational data on the hard disk before turning the computer off completely. On switching the computer back on, the computer is restored to its state prior to hibernation, with all programs and files open, and unsaved data intact. In standby mode, computer's state is saved in RAM; in hibernation mode, computer's state is saved on the hard disk.

[0026] “Hybrid sleep” allows for sleep mode and hibernation to be combined whereby the contents of RAM are first copied to non-volatile storage like for regular hibernation, but then, instead of powering down, the computer enters sleep mode. This approach combines the benefits of sleep mode and hibernation: The machine can resume instantaneously, but it can also be powered down completely (e.g. due to loss of power) without loss of data, because it is already effectively in a state of hibernation.

[0027] A processor is in “idle mode” when, for example, the CPU has completed its scheduled tasks. Processors use idle time to save power. Common methods are reducing the clock speed along with the CPU voltage and sending parts of the

processor into a sleep state. On processors that have a halt instruction that stops the CPU until an interrupt occurs, such as x86's HLT instruction, it may save significant amounts of power and heat if the idle task consists of a loop which repeatedly executes HLT instructions. Logic may include an idle task, which is a special task loaded by a scheduler only when there is nothing for the processor to do. The idle task can be hard-coded into the scheduler, or it can be implemented as a separate task with the lowest possible priority. The elevated heat generation for transistor rehabilitation may be based on an idle task. Thus, the transistor recover program makes use of CPU idle time by running at a low priority so as not to impact programs that run at normal priority. This allows the recovery program to run when it would not affect the performance of other applications.

[0028] While block 103 refers to “sleep” or “idle” mode, the block more generally relates to determining a general power state or user activity level. The power state need not be “sleep” mode but may include a mode described by an Advanced Configuration and Power Interface (ACPI) power specification, and the like. “Sleep mode” corresponds to ACPI mode S3.

[0029] If block 103 results in “yes”, then heating commences in block 104. The heating may occur as described herein using, for example, a power virus, Design for Test circuitry, circuitry neighboring the target transistor. The heat may keep the target transistor exposed to 90 degrees C for 10 seconds. Other embodiments may target 70, 80, 100, or more degrees C at different intervals of time.

[0030] Heating may occur again based on the process returning to block 101.

[0031] Referring now to Figure 3, shown is a block diagram of an example system with which embodiments can be used. As seen, system 900 may be a smartphone or other wireless communicator or any other IoT device. A baseband processor 905 is configured to perform various signal processing with regard to communication signals to be transmitted from or received by the system. In turn, baseband processor 905 is coupled to an application processor 910, which may be a main CPU of the system to execute an OS and other system software, in addition to user applications such as many well-known social media and multimedia apps.

Application processor 910 may further be configured to perform a variety of other computing operations for the device.

[0032] In turn, application processor 910 can couple to a user interface/display 920, e.g., a touch screen display. In addition, application processor 910 may couple to a memory system including a non-volatile memory, namely a flash memory 930 and a system memory, namely a DRAM 935. In some embodiments, flash memory 930 may include a secure portion 932 in which secrets and other sensitive information may be stored. As further seen, application processor 910 also couples to a capture device 945 such as one or more image capture devices that can record video and/or still images.

[0033] A universal integrated circuit card (UICC) 940 comprises a subscriber identity module, which in some embodiments includes a secure storage 942 to store secure user information. System 900 may further include a security processor 950 that may couple to application processor 910. A plurality of sensors 925, including one or more multi-axis accelerometers may couple to application processor 910 to enable input of a variety of sensed information such as motion and other environmental information. In addition, one or more authentication devices 995 may be used to receive, e.g., user biometric input for use in authentication operations.

[0034] As further illustrated, a near field communication (NFC) contactless interface 960 is provided that communicates in a NFC near field via an NFC antenna 965. While separate antennae are shown, understand that in some implementations one antenna or a different set of antennae may be provided to enable various wireless functionalities.

[0035] A power management integrated circuit (PMIC) 915 couples to application processor 910 to perform platform level power management. To this end, PMIC 915 may issue power management requests to application processor 910 to enter certain low power states as desired. Furthermore, based on platform constraints, PMIC 915 may also control the power level of other components of system 900.

[0036] To enable communications to be transmitted and received such as in one or more IoT networks, various circuitries may be coupled between baseband processor

905 and an antenna 990. Specifically, a radio frequency (RF) transceiver 970 and a wireless local area network (WLAN) transceiver 975 may be present. In general, RF transceiver 970 may be used to receive and transmit wireless data and calls according to a given wireless communication protocol such as 3G or 4G wireless communication protocol such as in accordance with a code division multiple access (CDMA), global system for mobile communication (GSM), long term evolution (LTE) or other protocol. In addition a GPS sensor 980 may be present, with location information being provided to security processor 950 for use as described herein when context information is to be used in a pairing process. Other wireless communications such as receipt or transmission of radio signals, e.g., AM/FM and other signals may also be provided. In addition, via WLAN transceiver 975, local wireless communications, such as according to a Bluetooth™ or IEEE 802.11 standard can also be realized.

[0037] Referring now to Figure 4, shown is a block diagram of a system in accordance with another embodiment of the present invention. Multiprocessor system 1000 is a point-to-point interconnect system such as a server system, and includes a first processor 1070 and a second processor 1080 coupled via a point-to-point interconnect 1050. Each of processors 1070 and 1080 may be multicore processors such as SoCs, including first and second processor cores (i.e., processor cores 1074a and 1074b and processor cores 1084a and 1084b), although potentially many more cores may be present in the processors.

[0038] First processor 1070 further includes a memory controller hub (MCH) 1072 and point-to-point (P-P) interfaces 1076 and 1078. Similarly, second processor 1080 includes a MCH 1082 and P-P interfaces 1086 and 1088. MCH's 1072 and 1082 couple the processors to respective memories, namely a memory 1032 and a memory 1034, which may be portions of main memory (e.g., a DRAM) locally attached to the respective processors. First processor 1070 and second processor 1080 may be coupled to a chipset 1090 via P-P interconnects 1052 and 1054, respectively. Chipset 1090 includes P-P interfaces 1094 and 1098.

[0039] Furthermore, chipset 1090 includes an interface 1092 to couple chipset 1090 with a high performance graphics engine 1038, by a P-P interconnect 1039. In

turn, chipset 1090 may be coupled to a first bus 1016 via an interface 1096. Various input/output (I/O) devices 1014 may be coupled to first bus 1016, along with a bus bridge 1018 which couples first bus 1016 to a second bus 1020. Various devices may be coupled to second bus 1020 including, for example, a keyboard/mouse 1022, communication devices 1026 and a data storage unit 1028 such as a non-volatile storage or other mass storage device. As seen, data storage unit 1028 may include code 1030, in one embodiment. As further seen, data storage unit 1028 also includes a trusted storage 1029 to store sensitive information to be protected. Further, an audio I/O 1024 may be coupled to second bus 1020.

[0040] Embodiments may be used in environments where IoT devices may include wearable devices or other small form factor IoT devices. Referring now to Figure 5, shown is a block diagram of a wearable module 1300 in accordance with another embodiment. In one particular implementation, module 1300 may be an Intel® Curie™ module that includes multiple components adapted within a single small module that can be implemented as all or part of a wearable device. As seen, module 1300 includes a core 1310 (of course in other embodiments more than one core may be present). Such core may be a relatively low complexity in-order core, such as based on an Intel Architecture® Quark™ design. Core 1310 couples to various components including a sensor hub 1320, which may be configured to interact with a plurality of sensors 1380, such as one or more biometric, motion environmental or other sensors. A power delivery circuit 1330 is present, along with a non-volatile storage 1340. In an embodiment, this circuit may include a rechargeable battery and a recharging circuit (as well as a PCU), which may in one embodiment receive charging power wirelessly. One or more input/output (IO) interfaces 1350, such as one or more interfaces compatible with one or more of USB/SPI/I2C/GPIO protocols, may be present. In addition, a wireless transceiver 1390, which may be a Bluetooth™ low energy or other short-range wireless transceiver is present to enable wireless communications as described herein. Understand that in different implementations a wearable module can take many other forms. Wearable and/or IoT devices have, in comparison with a typical general purpose CPU or a GPU, a small form factor, low power requirements, limited instruction sets, relatively slow computation throughput, or any of the above.

[0041] Embodiments may be used in many different types of systems. For example, in one embodiment a communication device can be arranged to perform the various methods and techniques described herein. Of course, the scope of the present invention is not limited to a communication device, and instead other embodiments can be directed to other types of apparatus for processing instructions, or one or more machine readable media including instructions that in response to being executed on a computing device, cause the device to carry out one or more of the methods and techniques described herein.

[0042] Embodiments may be implemented in code and may be stored on a non-transitory storage medium having stored thereon instructions which can be used to program a system to perform the instructions. Embodiments also may be implemented in data and may be stored on a non-transitory storage medium, which if used by at least one machine, causes the at least one machine to fabricate at least one integrated circuit to perform one or more operations. The storage medium may include, but is not limited to, any type of disk including floppy disks, optical disks, solid state drives (SSDs), compact disk read-only memories (CD-ROMs), compact disk rewritables (CD-RWs), and magneto-optical disks, semiconductor devices such as read-only memories (ROMs), random access memories (RAMs) such as dynamic random access memories (DRAMs), static random access memories (SRAMs), erasable programmable read-only memories (EPROMs), flash memories, electrically erasable programmable read-only memories (EEPROMs), magnetic or optical cards, or any other type of media suitable for storing electronic instructions.

[0043] As used herein a processor or controller may include control logic intended to represent any of a wide variety of control logic known in the art and, as such, may well be implemented as a microprocessor, a micro-controller, a field-programmable gate array (FPGA), application specific integrated circuit (ASIC), programmable logic device (PLD) and the like.

[0044] A module as used herein refers to any hardware, software, firmware, or a combination thereof. Often module boundaries that are illustrated as separate commonly vary and potentially overlap. For example, a first and a second module

may share hardware, software, firmware, or a combination thereof, while potentially retaining some independent hardware, software, or firmware.

[0045] In one embodiment, use of the term logic includes hardware, such as transistors, registers, or other hardware, such as programmable logic devices. However, in another embodiment, logic also includes software or code integrated with hardware, such as firmware or micro-code.

[0046] Figure 2 includes a process 200 in an embodiment. Block 201 includes determining a system, which includes a processor having a transistor, is not operating based on power from battery included in the system. Block 203 includes determining the system is operating in a first system power state. Block 205 includes determining the transistor is operating in a first transistor power state. Block 210 includes elevating a temperature of the transistor, for a predetermined period of time (e.g., < 60 seconds) and to a predetermined temperature (e.g., > 85 degrees Celsius), in response to at least one of: (a) executing a power virus, (b) executing a predetermined test routine for a hardware component included in the system, (c) executing a scan function, (d) operating a voltage regulator included in the system, and (e) operating an additional processor (e.g., baseband processor, graphics processor, security processor) included in the system.

[0047] Various embodiments include a semiconductive substrate. Such a substrate may be a bulk semiconductive material this is part of a wafer. In an embodiment, the semiconductive substrate is a bulk semiconductive material as part of a chip that has been singulated from a wafer. In an embodiment, the semiconductive substrate is a semiconductive material that is formed above an insulator such as a semiconductor on insulator (SOI) substrate. In an embodiment, the semiconductive substrate is a prominent structure such as a fin that extends above a bulk semiconductive material.

[0048] The following examples pertain to further embodiments.

[0049] Example 1 includes at least one storage medium having instructions stored thereon for causing a system to: determine the system, which includes a hardware processor comprising a transistor, is operating in a first system power state; determine the transistor is operating in a first transistor power state; and in response

to determining the first system and first transistor power states, elevate a temperature of the transistor for a predetermined period of time.

[0050] The transistor may be included in for example, components 905, 910, 950, 925, 935 (Figure 3), 1074a, 1074b, 1090, 1028, 1032 (Figure 4), 1310, 1340, 1350 (Figure 5), and the like.

[0051] In example 2 the subject matter of the Example 1 can optionally include wherein the elevating the temperature of the transistor comprises elevating the temperature of the transistor to a predetermined temperature.

[0052] That temperature may include 60, 65, 70, 75, 80, 85, 90, 95, 100 degrees Celsius or more.

[0053] In example 3 the subject matter of the Examples 1-2 can optionally include wherein the first system power state corresponds to at least one member selected from the group comprising: sleep mode, standby mode, suspend to RAM mode, hibernate mode, suspend to disk mode, hybrid sleep mode, idle mode, active screen saver mode, battery charging mode, and an Advanced Configuration and Power Interface (ACPI) power mode.

[0054] In example 4 the subject matter of the Examples 1-3 can optionally include wherein the processor is configured to operate in at least a high frequency mode (HFM) and a low frequency mode (LFM) and the first transistor power state corresponds to the LFM.

[0055] In example 5 the subject matter of the Examples 1-4 can optionally include wherein the processor is configured to operate in at least a high frequency mode (HFM) and a low frequency mode (LFM) and the first transistor power state corresponds to the LFM.

[0056] In example 6 the subject matter of the Examples 1-5 can optionally include wherein the elevating the temperature of the transistor comprises at least one member selected from the group comprising executing a power virus, executing a predetermined test routine for a hardware component included in the system, and executing a scan function.

[0057] The hardware component may include a subcomponent within the processor, a component on a SoC that includes a processor (i.e., on a shared substrate with the processor), or a component relatively nearby the processor but on a different substrate than the processor.

[0058] In example 7 the subject matter of the Examples 1-6 can optionally include wherein the system includes a battery for powering the processor and the at least one medium comprises instructions including determining the system is not operating based on power from the battery.

[0059] For example, the system may be receiving power via a wired or wireless (e.g., induction) coupling from a power grid.

[0060] In example 8 the subject matter of the Examples 1-7 can optionally include wherein the elevating the temperature of the transistor for the predetermined period of time is configured to at least partially offset bias temperature instability (BTI) of the transistor.

[0061] By “configured to” the temperature may be determined based on recovery rates (example a: change in mV/decade vs. change in temperature for a period of time, example b: change in V_{th} versus time that has transpired since the end of stressing the transistor at a certain temperature) determined for a transistor.

[0062] In example 9 the subject matter of the Examples 1-8 can optionally include wherein (a) the system is included in a computing node selected from the group comprising a laptop, desktop, Smartphone, and mobile computing node; and (b) the elevating the temperature of the transistor comprises elevating temperature adjacent the transistor but not within the transistor.

[0063] A mobile computing node includes, for example, the systems represented by Figures 3 and 5.

[0064] In example 10 the subject matter of the Examples 1-9 can optionally include wherein the predetermined temperature is greater than 85 degrees Celsius and the predetermined period of time is less than 60 seconds.

[0065] In an embodiment this is a critical range for temperature and time determined to offset BTI. Another example includes wherein the predetermined temperature is greater than 90 degrees Celsius and the predetermined period of time is less than 10 seconds. This is a critical range for temperature and time determined to offset BTI.

[0066] In another version of example 10 the subject matter of the Examples 1-9 can optionally include wherein the predetermined temperature is greater than 85 degrees Celsius.

[0067] In another version of example 10 the subject matter of the Examples 1-9 can optionally include wherein the predetermined period of time is less than 60 seconds.

[0068] In example 11 the subject matter of the Examples 1-10 can optionally include wherein the elevating the temperature of the transistor comprises elevating the temperature via operation of at least one member selected from the group comprising a voltage regulator included in the system and an additional processor included in the system.

[0069] The additional processor may include graphics, baseband, security processors and the like. Other components could include, for example, elements 970, PMIC 915 (Figure 3), 104, 1024 (Figure 4), 1350 (Figure 5).

[0070] In example 12 the subject matter of the Examples 1-11 can optionally include instructions to determine the transistor is in a condition corresponding to a V_{min} that exceeds a predetermined value.

[0071] In example 13 the subject matter of the Examples 1-12 can optionally include wherein determining the transistor is in the condition includes a member selected from the group comprising determining: (1) a predetermined period of time has passed since a previous bias temperature instability (BTI) recovery process was performed on the transistor, (2) a predetermined amount of usage has occurred for the transistor, (3) a predetermined amount of usage has occurred for the transistor within a predetermined time period; and (4) a reliability meter indicates a threshold level of hardware problems have occurred in the system.

[0072] Example 14 includes an apparatus comprising: at least one memory; at least one processor, coupled to the memory, to perform operations comprising: determining the system, which includes a hardware processor comprising a transistor, is operating in a first system power state; determining the transistor is operating in a first transistor power state; and in response to determining the first system and first transistor power states, elevating a temperature of the transistor for a predetermined period of time.

[0073] In example 15 the subject matter of Example 14 can optionally include wherein the elevating the temperature of the transistor comprises elevating the temperature of the transistor to a predetermined temperature.

[0074] In example 16 the subject matter of the Examples 14-15 can optionally include wherein the first system power state corresponds to at least one member selected from the group comprising: sleep mode, standby mode, suspend to RAM mode, hibernate mode, suspend to disk mode, hybrid sleep mode, idle mode, active screen saver mode, battery charging mode, and an Advanced Configuration and Power Interface (ACPI) power mode.

[0075] In example 17 the subject matter of the Examples 14-16 can optionally include wherein the processor is configured to operate in at least a high frequency mode (HFM) and a low frequency mode (LFM) and the first transistor power state corresponds to the LFM.

[0076] In example 18 the subject matter of the Examples 14-17 can optionally include wherein the elevating the temperature of the transistor comprises at least one member selected from the group comprising executing a power virus, executing a predetermined test routine for a hardware component included in the system, and executing a scan function.

[0077] In example 19 the subject matter of the Examples 14-18 can optionally include wherein the system includes a battery for powering the processor and the operations comprise determining the system is not operating based on power from the battery.

[0078] In example 20 the subject matter of the Examples 14-19 can optionally include wherein the elevating the temperature of the transistor for the predetermined period of time is configured to at least partially offset bias temperature instability (BTI) of the transistor.

[0079] In example 21 the subject matter of the Examples 14-20 can optionally include wherein the elevating the temperature of the transistor comprises elevating the temperature via operation of at least one member selected from the group comprising a voltage regulator included in the system and an additional processor included in the system.

[0080] In example 22 the subject matter of the Examples 14-21 can optionally include wherein the operations comprise determining the transistor is in a condition corresponding to a $V_{\min}$ that exceeds a predetermined value.

[0081] Example 23 includes a method comprising: determining the system, which includes a hardware processor comprising a transistor, is operating in a first system power state; determining the transistor is operating in a first transistor power state; and in response to determining the first system and first transistor power states, elevating a temperature of the transistor for a predetermined period of time.

[0082] In example 24 the subject matter of the Example 23 can optionally include wherein: the first system power state corresponds to at least one member selected from the group comprising: sleep mode, standby mode, suspend to RAM mode, hibernate mode, suspend to disk mode, hybrid sleep mode, idle mode, active screen saver mode, battery charging mode, and an Advanced Configuration and Power Interface (ACPI) power mode; and wherein the processor is configured to operate in at least a high frequency mode (HFM) and a low frequency mode (LFM) and the first transistor power state corresponds to the LFM.

[0083] In example 25 the subject matter of the Examples 23-24 can optionally include wherein the elevating the temperature of the transistor comprises at least one member selected from the group comprising executing a power virus, executing a predetermined test routine for a hardware component included in the system, and executing a scan function.

[0084] Example 26 includes a communications device arranged to carry out a method according to any one of examples 23 to 25.

[0085] Example 27 includes an apparatus comprising means for performing any one of examples 23 to 25.

[0086] Example 28 includes at least one machine readable medium comprising a plurality of instructions that in response to being executed on a computing device, cause the computing device to carry out a method according to any one of examples 23 to 25.

[0087] Example 1a includes a method executed by at least one hardware processor comprising: determining a system, which includes the at least one hardware processor that comprises a transistor, is operating in a first system power state; determining the transistor is operating in a first transistor power state; and in response to determining the first system and first transistor power states, elevate a temperature of the transistor for a predetermined period of time.

[0088] In example 2a the subject matter of the Example 1a can optionally include, wherein the elevating the temperature of the transistor comprises elevating the temperature of the transistor to a predetermined temperature.

[0089] In example 3a the subject matter of the Examples 1a-2a can optionally include wherein the first system power state corresponds to at least one member selected from the group comprising: sleep mode, standby mode, suspend to RAM mode, hibernate mode, suspend to disk mode, hybrid sleep mode, idle mode, active screen saver mode, battery charging mode, and an Advanced Configuration and Power Interface (ACPI) power mode.

[0090] In example 4a the subject matter of the Examples 1a-3a can optionally include wherein the processor is configured to operate in at least a high frequency mode (HFM) and a low frequency mode (LFM) and the first transistor power state corresponds to the LFM.

[0091] In example 5a the subject matter of the Examples 1a-4a can optionally include wherein the processor is configured to operate in at least a high frequency

mode (HFM) and a low frequency mode (LFM) and the first transistor power state corresponds to the LFM.

[0092] In example 6a the subject matter of the Examples 1a-5a can optionally include wherein the elevating the temperature of the transistor comprises at least one member selected from the group comprising executing a power virus, executing a predetermined test routine for a hardware component included in the system, and executing a scan function.

[0093] In example 7a the subject matter of the Examples 1a-6a can optionally include wherein the system includes a battery for powering the processor and the method comprises determining the system is not operating based on power from the battery.

[0094] In example 8a the subject matter of the Examples 1a-7a can optionally include wherein the elevating the temperature of the transistor for the predetermined period of time is configured to at least partially offset bias temperature instability (BTI) of the transistor.

[0095] In example 9a the subject matter of the Examples 1a-8a can optionally include wherein (a) the system is included in a computing node selected from the group comprising a laptop, desktop, Smartphone, and mobile computing node; and (b) the elevating the temperature of the transistor comprises elevating temperature adjacent the transistor but not within the transistor.

[0096] In example 10a the subject matter of the Examples 1a-9a can optionally include wherein the predetermined temperature is greater than 85 degrees Celsius and the predetermined period of time is less than 60 seconds.

[0097] In example 11a the subject matter of the Examples 1a-10a can optionally include wherein the elevating the temperature of the transistor comprises elevating the temperature via operation of at least one member selected from the group comprising a voltage regulator included in the system and an additional processor included in the system.

[0098] In example 12a the subject matter of the Examples 1a-11a can optionally include comprising determining the transistor is in a condition corresponding to a V_{min} that exceeds a predetermined value.

[0099] In example 13a the subject matter of the Examples 1a-12a can optionally include wherein determining the transistor is in the condition includes a member selected from the group comprising determining: (1) a predetermined period of time has passed since a previous bias temperature instability (BTI) recovery process was performed on the transistor, (2) a predetermined amount of usage has occurred for the transistor, (3) a predetermined amount of usage has occurred for the transistor within a predetermined time period; and (4) a reliability meter indicates a threshold level of hardware problems have occurred in the system.

[0100] In example 14a the subject matter of the Examples 1a-13a can optionally include at least one machine readable medium comprising a plurality of instructions that in response to being executed on a computing device, cause the computing device to carry out a method according to any one of examples 1a to 13a.

[0101] In example 15a the subject matter of the Examples 1a-14a can optionally include a communications device arranged to carry out a method according to any one of examples 1a to 13a.

[0102] In example 16a the subject matter of the Examples 1a-15a can optionally include an apparatus comprising means for performing any one of examples 1a to 13a.

[0103] The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Persons skilled in the relevant art can appreciate that many modifications and variations are possible in light of the above teaching. Persons skilled in the art will recognize various equivalent combinations and substitutions for various components shown in the Figures. It is therefore intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

What is claimed is:

- 1 1. At least one storage medium having instructions stored thereon for causing a
2 system to:
3 determine the system, which includes a hardware processor comprising a
4 transistor, is operating in a first system power state;
5 determine the transistor is operating in a first transistor power state; and
6 in response to determining the first system and first transistor power states,
7 elevate a temperature of the transistor for a predetermined period of time.
- 1 2. The at least one medium of claim 1, wherein the elevating the temperature of
2 the transistor comprises elevating the temperature of the transistor to a
3 predetermined temperature.
- 1 3. The at least one medium of claim 1, wherein the first system power state
2 corresponds to at least one member selected from the group comprising: sleep
3 mode, standby mode, suspend to RAM mode, hibernate mode, suspend to disk
4 mode, hybrid sleep mode, idle mode, active screen saver mode, battery charging
5 mode, and an Advanced Configuration and Power Interface (ACPI) power mode.
- 1 4. The at least one medium of claim 3, wherein the processor is configured to
2 operate in at least a high frequency mode (HFM) and a low frequency mode (LFM)
3 and the first transistor power state corresponds to the LFM.
- 1 5. The at least one medium of claim 1, wherein the processor is configured to
2 operate in at least a high frequency mode (HFM) and a low frequency mode (LFM)
3 and the first transistor power state corresponds to the LFM.
- 1 6. The at least one medium of claim 1, wherein the elevating the temperature of
2 the transistor comprises at least one member selected from the group comprising
3 executing a power virus, executing a predetermined test routine for a hardware
4 component included in the system, and executing a scan function.

- 1 7. The at least one medium of claim 1, wherein the system includes a battery for
2 powering the processor and the at least one medium comprising instructions
3 including determining the system is not operating based on power from the battery.
- 1 8. The at least one medium of claim 1, wherein the elevating the temperature of
2 the transistor for the predetermined period of time is configured to at least partially
3 offset bias temperature instability (BTI) of the transistor.
- 1 9. The at least one medium of claim 1, wherein (a) the system is included in a
2 computing node selected from the group comprising a laptop, desktop, Smartphone,
3 and mobile computing node; and (b) the elevating the temperature of the transistor
4 comprises elevating temperature adjacent the transistor but not within the transistor.
- 1 10. The at least one medium of claim 1, wherein the predetermined period of time
2 is less than 60 seconds.
- 1 11. The at least one medium of claim 1, wherein the elevating the temperature of
2 the transistor comprises elevating the temperature via operation of at least one
3 member selected from the group comprising a voltage regulator included in the
4 system and an additional processor included in the system.
- 1 12. The at least one medium of claim 1 comprising instructions to determine the
2 transistor is in a condition corresponding to a V_{min} that exceeds a predetermined
3 value.
- 1 13. The at least one medium of claim 12, wherein determining the transistor is in
2 the condition includes a member selected from the group comprising determining: (1)
3 a predetermined period of time has passed since a previous bias temperature
4 instability (BTI) recovery process was performed on the transistor, (2) a
5 predetermined amount of usage has occurred for the transistor, (3) a predetermined
6 amount of usage has occurred for the transistor within a predetermined time period;

7 and (4) a reliability meter indicates a threshold level of hardware problems have
8 occurred in the system.

1 14. An apparatus comprising:
2 at least one memory;
3 at least one processor, coupled to the memory, to perform operations
4 comprising:
5 determining the system, which includes a hardware processor
6 comprising a transistor, is operating in a first system power state;
7 determining the transistor is operating in a first transistor power state;
8 and
9 in response to determining the first system and first transistor power
10 states, elevating a temperature of the transistor for a predetermined period of time.

1 15. The apparatus of claim 14, wherein the elevating the temperature of the
2 transistor comprises elevating the temperature of the transistor to a predetermined
3 temperature.

1 16. The apparatus of claim 14, wherein the first system power state corresponds
2 to at least one member selected from the group comprising: sleep mode, standby
3 mode, suspend to RAM mode, hibernate mode, suspend to disk mode, hybrid sleep
4 mode, idle mode, active screen saver mode, battery charging mode, and an
5 Advanced Configuration and Power Interface (ACPI) power mode.

1 17. The apparatus of claim 14, wherein the processor is configured to operate in
2 at least a high frequency mode (HFM) and a low frequency mode (LFM) and the first
3 transistor power state corresponds to the LFM.

1 18. The apparatus of claim 14, wherein the elevating the temperature of the
2 transistor comprises at least one member selected from the group comprising
3 executing a power virus, executing a predetermined test routine for a hardware
4 component included in the system, and executing a scan function.

1 19. The apparatus of claim 14, wherein the system includes a battery for
2 powering the processor and the operations comprise determining the system is not
3 operating based on power from the battery.

1 20. The apparatus of claim 14, wherein the elevating the temperature of the
2 transistor for the predetermined period of time is configured to at least partially offset
3 bias temperature instability (BTI) of the transistor.

1 21. The apparatus of claim 14, wherein the elevating the temperature of the
2 transistor comprises elevating the temperature via operation of at least one member
3 selected from the group comprising a voltage regulator included in the system and
4 an additional processor included in the system.

1 22. The apparatus of claim 14, wherein the operations comprise determining the
2 transistor is in a condition corresponding to a $V_{\min}$ that exceeds a predetermined
3 value.

1 23. A method comprising:
2 determining the system, which includes a hardware processor comprising a
3 transistor, is operating in a first system power state;
4 determining the transistor is operating in a first transistor power state; and
5 in response to determining the first system and first transistor power states,
6 elevating a temperature of the transistor for a predetermined period of time.

1 24. The method of claim 23 wherein:
2 the first system power state corresponds to at least one member selected
3 from the group comprising: sleep mode, standby mode, suspend to RAM mode,
4 hibernate mode, suspend to disk mode, hybrid sleep mode, idle mode, active screen
5 saver mode, battery charging mode, and an Advanced Configuration and Power
6 Interface (ACPI) power mode;

7 the processor is configured to operate in at least a high frequency mode
8 (HFM) and a low frequency mode (LFM) and the first transistor power state
9 corresponds to the LFM.

1 25. The method of claim 21, wherein the elevating the temperature of the
2 transistor comprises at least one member selected from the group comprising
3 executing a power virus, executing a predetermined test routine for a hardware
4 component included in the system, and executing a scan function.

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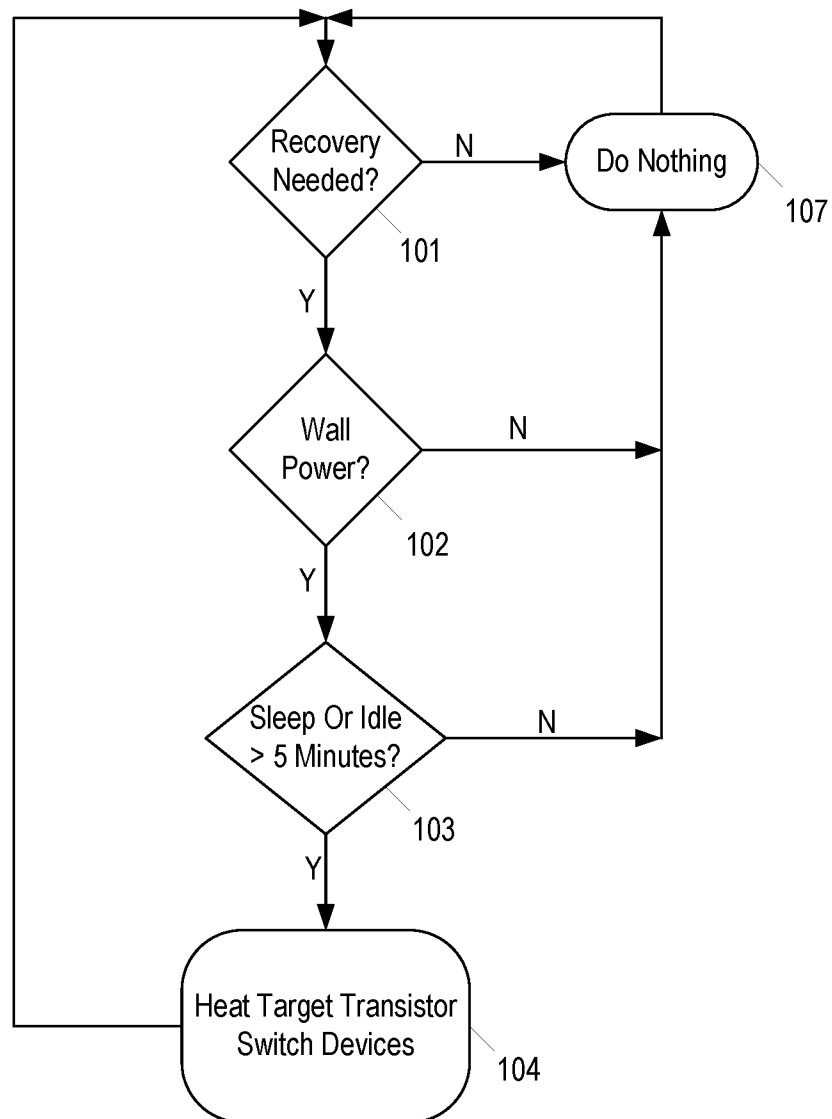


Figure 1

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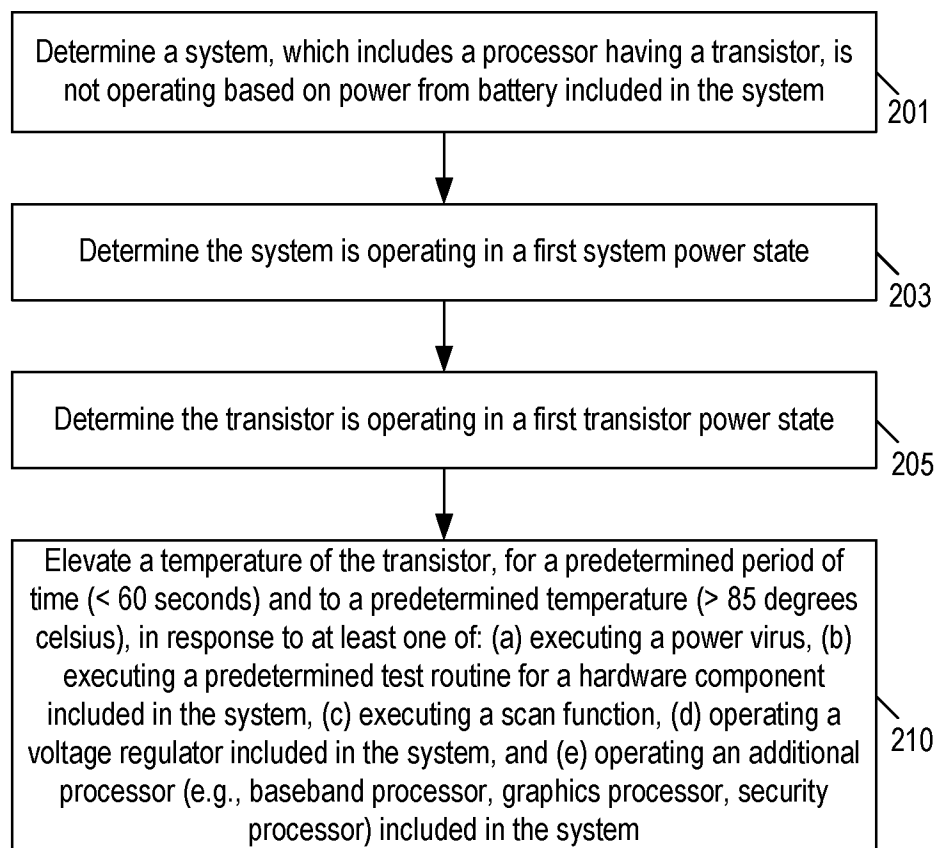
200

Figure 2

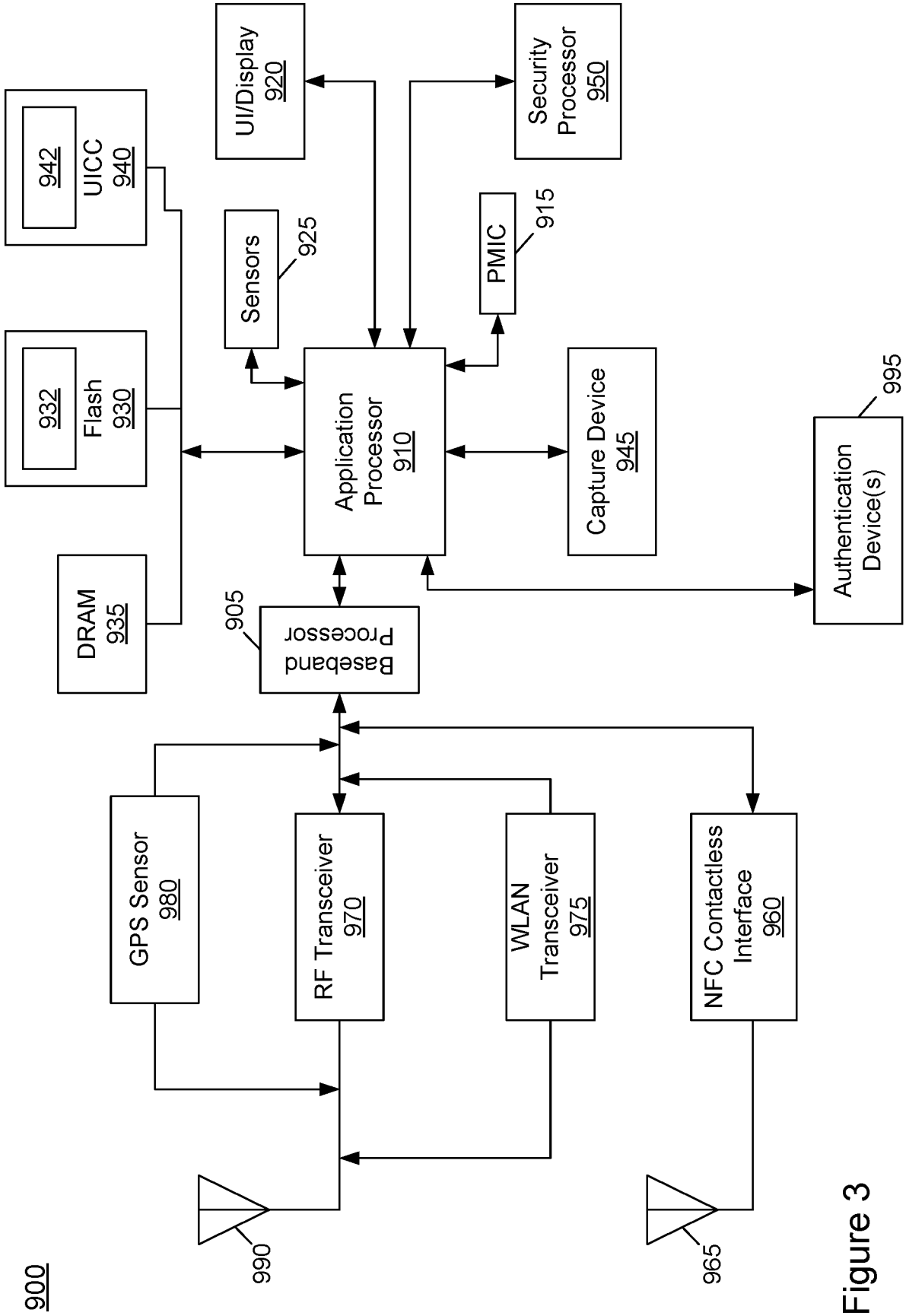


Figure 3

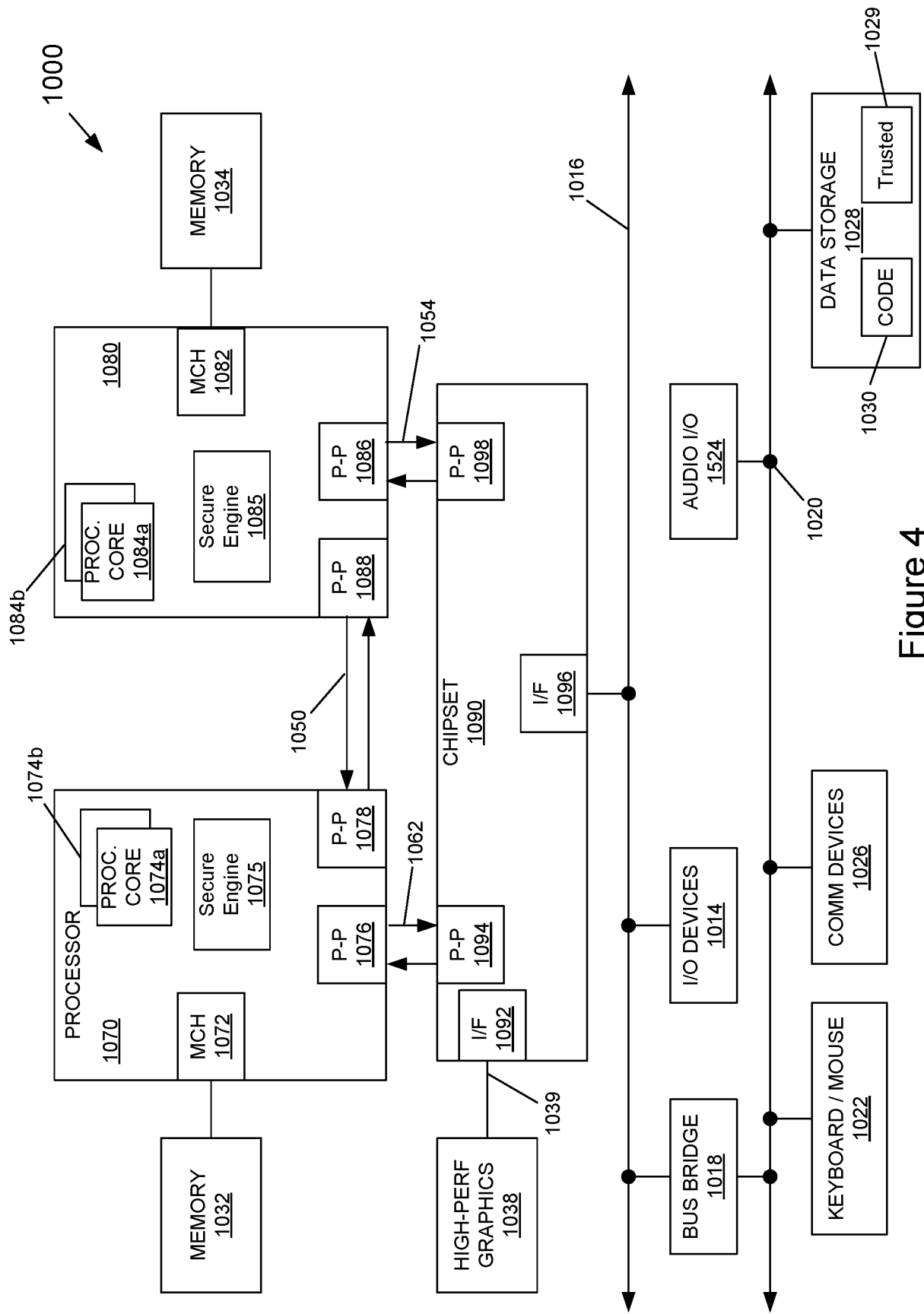


Figure 4

1300 →

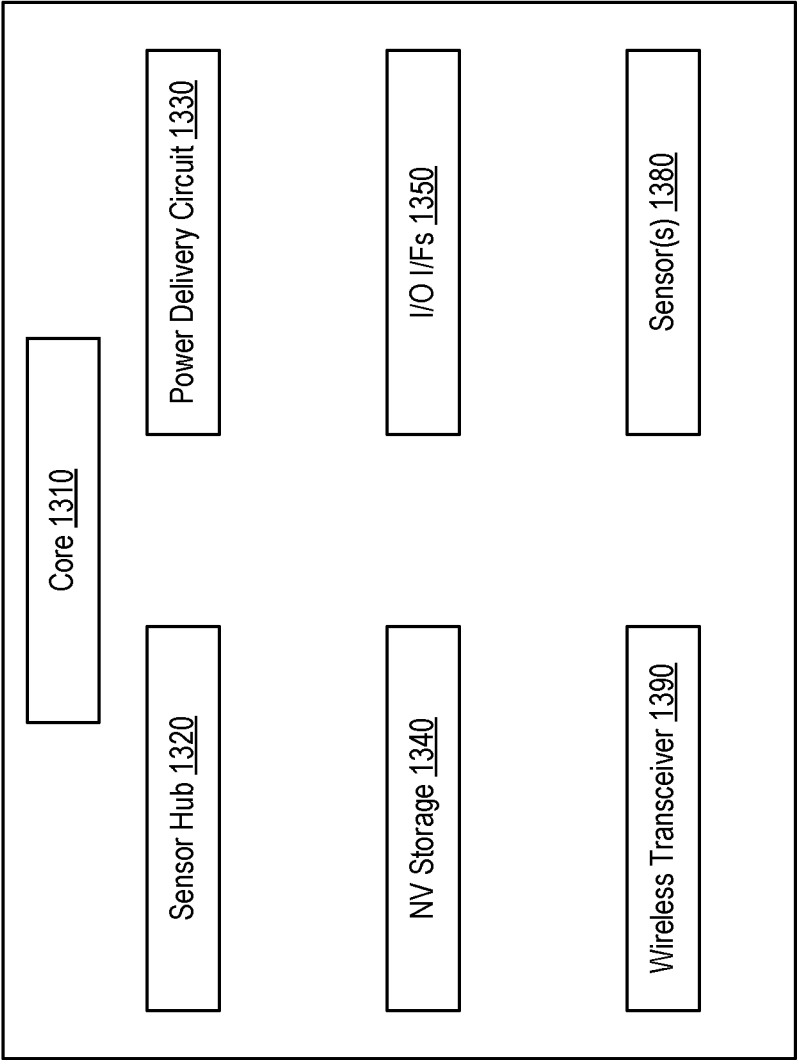


Figure 5

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/00(2006.01)i, H01L 21/336(2006.01)i, H01L 21/67(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/00; G01R 31/26; G01L 1/00; G01R 31/28; H03K 3/01; G06F 1/26; H01L 27/04; H01L 21/336; H01L 21/67

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: transistor, recover, threshold voltage, temperature, power mode

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2014-0013131 A1 (ADITYA BANSAL et al.) 09 January 2014 See abstract, paragraphs [0045]–[0050], claims 1–9 and figure 9.	1–25
A	US 2009-0319202 A1 (FADI H. GEBARA et al.) 24 December 2009 See abstract, paragraph [0035], claim 1 and figure 8.	1–25
A	US 2011-0128069 A1 (ZHIJIAN YANG et al.) 02 June 2011 See abstract, paragraphs [0073]–[0089], claims 1, 10 and figures 9–11.	1–25
A	JP 2011-191176 A (FUJITSU SEMICONDUCTOR LTD.) 29 September 2011 See paragraphs [0049], [0056], claim 9 and figure 6.	1–25
A	US 2009-0251167 A1 (KANAK B. AGARWAL et al.) 08 October 2009 See abstract, paragraph [0029], claim 1 and figure 4.	1–25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

26 December 2016 (26.12.2016)

Date of mailing of the international search report

26 December 2016 (26.12.2016)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/025413

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