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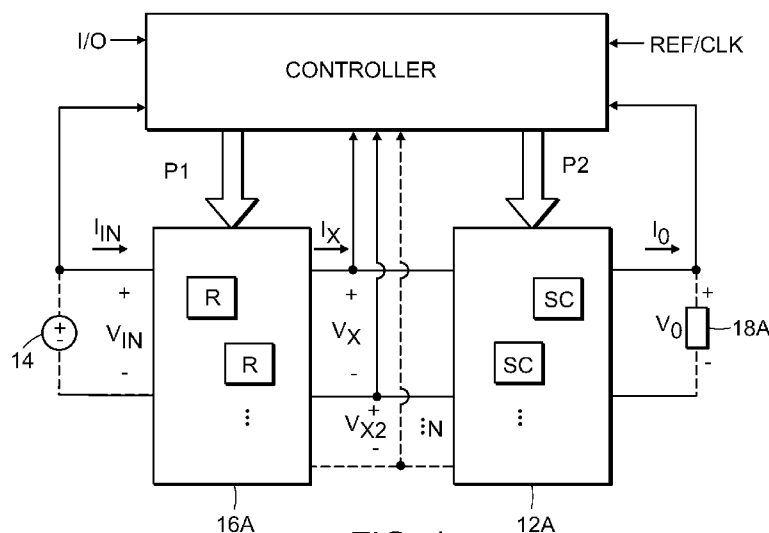


FIG. 1

(57) Abstract: An apparatus for providing electric power to a load includes a power converter that accepts electric power in a first form and provides electric power in a second form. The power converter comprises a control system, a first stage, and a second stage in series. The first stage accepts electric power in the first form. The control system controls operation of the first and second stage. The first stage is either a switching network or a regulating network. The second stage is a regulating circuit when the first stage is a switching network, and a switching network otherwise.

1 **SWITCHED-CAPACITOR POWER CONVERTERS**

2 **CROSS REFERENCE TO RELATED APPLICATION**

3 This application claims the benefit of the priority
4 date of U.S. Provisional Application No. 62/189,909, filed
5 on July 8, 2015, the contents of which are hereby
6 incorporated by reference in their entirety.

7 **FIELD OF INVENTION**

8 This invention relates to power converters, and in
9 particular, to dc-dc power converters.

10 **BACKGROUND**

11 It is known in the art that electrical devices require
12 electric power to operate. However, some electrical devices
13 are more omnivorous than others. For example, a tungsten
14 filament light bulb will operate over a wide range of
15 voltages. Although it may be dim at low voltages, and
16 although it may burn out prematurely at high voltages, it
17 does not simply stop operating.

18 Digital circuits, however, are more finicky in their
19 requirements. A digital circuit demands power with
20 particular characteristics. A processor that receives power
21 falling short of these characteristics will not just
22 compute more slowly. It will simply shut down.

23 Unfortunately, power is not always delivered in a form
24 that a microprocessor-based system will find acceptable.
25 For example, in a handheld device, the battery voltage
26 ranges from fully charged to almost zero. Thus, most such
27 systems require something that accepts power in raw form
28 and delivers it to the system in a form that the system
29 finds more palatable.

1 This critical but unglamorous task falls upon the
2 power converter.

3 A variety of power converters are known. These include
4 power converters described in U.S. Patent No. 8,860,396,
5 U.S. Patent No. 8,743,553, U.S. Patent No. 8,723,491, U.S.
6 Patent No. 8,503,203, U.S. Patent No. 8,693,224, U.S.
7 Patent No. 8,724,353, U.S. Patent No. 8,339,184, U.S.
8 Patent No. 8,619,445, U.S. Patent No. 8,817,501, U.S.
9 Patent Publ. 2015/0077175, and U.S. Patent No. 9,041,459.
10 The contents of all the foregoing patents are herein
11 incorporated by reference.

12 **SUMMARY**

13 In one aspect, the invention features an apparatus for
14 providing electric power to a load. Such an apparatus
15 includes a power converter that accepts electric power in a
16 first form and provides electric power in a second form.
17 The power converter includes a control system, and first
18 and second stages in series. The first stage accepts
19 electric power in the first form. The control system
20 controls operation of the first and second stages. The
21 first stage is either a switching network or a regulating
22 network. The second stage is a regulating network when the
23 first stage is a switching network. On the other hand, the
24 second stage is a switching network when the first stage is
25 a regulating network.

26 Among the embodiments are those in which the control
27 system controls at least in part based on a voltage
28 measured between the first and second stages.

29 Also among the embodiments are those in which the
30 first stage is a regulating network, those in which the

1 first stage is a switching network, and those in which it
2 is the second stage that is a switching network, such as a
3 cascade multiplier. In either case, the switching network
4 can be a cascade multiplier.

5 In some embodiments, at least one of the stages
6 includes a switching network having first and second
7 terminals. Among these are embodiments in which these
8 terminals are isolated, embodiments in which they have a
9 common ground, and embodiments in which they have separate
10 grounds.

11 In other embodiments, at least one of the stages
12 includes a switching network having a first and second
13 switching circuits, each of which has first and second
14 terminals. In these embodiments, the first terminal of the
15 second switching circuit connects to the second terminal of
16 the first switching circuit. Among these are embodiments in
17 which the two switching circuits have different voltage-
18 transformation ratios, and embodiments in which they have
19 the same voltage-transformation ratios.

20 In some embodiments, the switching network includes
21 first and second switching circuits in series, whereas in
22 others, it includes first and second switching circuits in
23 series-parallel.

24 Some embodiments of the power converter further
25 include a third stage in series with the first stage and
26 the second stage so that the second stage is between the
27 first stage and the third stage. These embodiments include
28 those in which the first and third stages are switching
29 networks, those in which the first and third stages are

1 regulating networks, and those in which the third stage is
2 operated with a duty cycle that causes the third stage to
3 become a magnetic filter.

4 In some embodiments, the switching network includes a
5 cascade multiplier. Among these are those embodiments in
6 which the cascade multiplier is a single-phase cascade
7 multiplier, those in which it is asymmetric, those in which
8 it is a step-down, multiplier, and any those in which it is
9 any combination thereof. Also among these embodiments are
10 those in which the cascade multiplier is a dual-phase
11 cascade multiplier. In this case, the cascade multiplier
12 could be a symmetric cascade multiplier, or one that
13 includes parallel pumped capacitors, or one that lacks DC
14 capacitors.

15 In some of the foregoing embodiments, the cascade
16 multiplier creates an auxiliary voltage to drive an
17 additional circuit. Among these are embodiments that
18 include a level shifter connected to be driven by the
19 auxiliary voltage, and those in which a gate driver is
20 connected to be driven by the auxiliary voltage.

21 In some embodiments, the switching network includes
22 first and second dual-phase cascade multipliers, and a
23 phase node shared by both cascade multipliers. In these
24 embodiments, the first cascade multiplier, which is stacked
25 on the second, is asynchronous and the second cascade
26 multiplier is synchronous. Among these embodiments are
27 those in which the first and second cascade multipliers
28 operate at the same frequency, and those in which the first
29 and second cascade multipliers operate at different
30 frequencies.

1 In some embodiments, the regulating network includes a
2 buck converter. Among these are embodiments in which the
3 buck converter includes first and second terminals with the
4 same reference voltage. Examples include those in which the
5 buck converter's first and second terminals are at
6 different reference voltages, those in which the buck
7 converter has three terminals, and those in which the buck
8 converter has a floating node at a floating voltage. In
9 embodiments that have a floating node, the floating node
10 can be between two loads or between two sources.

11 A variety of other regulating networks are
12 contemplated. These include a buck-boost converter, a boost
13 converter, and even a four-terminal non-inverting buck-
14 boost converter.

15 In some embodiments that use a boost converter as a
16 regulating network, the switching network includes a step-
17 down single-phase asymmetric cascade multiplier. In some of
18 these embodiments, selection switches connected to the
19 regulating network cause the switching network to output a
20 fraction of its normal output voltage. In others, switches
21 are oriented so that cathodes of parasitic diodes
22 corresponding to the switches connect to each other. Among
23 these embodiments are those in which the first stage is a
24 regulating network.

25 Embodiments include those in which those in which the
26 regulating network regulates plural wires, those in which
27 it regulates at most one wire, and those in which it
28 regulates a particular one of plural wires based on an
29 input voltage to the regulating network.

1 Also among the embodiments are those in which the
2 regulating network has plural output ports and those in
3 which it is a multi-tap boost converter. Among these are
4 embodiments in which the switching network includes a
5 single-phase step-down switched-capacitor circuit.

6 In yet other embodiments, the power converter floats
7 above ground.

8 In some embodiments, the switching network is
9 reconfigurable. In other embodiments, it is the regulating
10 network that is reconfigurable. In yet others, both are
11 reconfigurable. In either case, there are embodiments in
12 which a magnetic filter connects to whichever of the two
13 are reconfigurable. Thus, a magnetic filter could be
14 connected to either the reconfigurable switching network or
15 the reconfigurable regulating network.

16 In some embodiments, the switching network includes a
17 dual-phase switched capacitor circuit. Among these are
18 embodiments in which the switched capacitor circuit
19 includes pump capacitors in series and DC capacitors in
20 series.

21 In some embodiments, the switching network includes a
22 dual-phase switching circuit including DC capacitors that
23 store charge from the regulating network only during a
24 dead-time transition during which the switching network is
25 between states.

26 In yet other embodiments, the regulating network
27 includes an inductor that promotes adiabatic charge
28 transfer within the switching network.

1 Some embodiments also include a magnetic filter
2 connected to the switching network to promote adiabatic
3 charge transfer within the switching network. Among these
4 are embodiments in which the magnetic filter is connected
5 between the switching network and a load, those in which
6 the magnetic filter is connected between the switching
7 network and a source, and those in which the regulating
8 network and the magnetic filter cooperate to promote
9 adiabatic charge transfer within the switching network.

10 Embodiments further include those that have a circuit
11 connected to the switching network to constrain current
12 flow out of the switching network, and those that have a
13 circuit connected to the switching network to promote
14 adiabatic charge transfer within the switching network.

15 In some embodiments, the switching network includes a
16 two-phase step-down switching network and the regulating
17 network is a step-down network. Among these are embodiments
18 in which the switching network includes a cascade
19 multiplier. In those embodiments that include a cascade
20 multiplier, the regulating network can include a buck
21 converter. Also among these embodiments are those in which
22 regulating network promotes adiabatic charge transfer.

23 In still other embodiments, the switching network
24 includes a step-down single-phase asymmetric cascade
25 multiplier and the regulating network includes a converter
26 that causes voltage to step down. In some of these
27 embodiments, it is the first stage that is a switching
28 network.

1 In some embodiments, the regulating network includes a
2 multiple-tap buck converter configured to have two
3 operating modes. Among these are embodiments in which the
4 switching network provides first and second voltage rails
5 that, in operation, are maintained at different voltages.

6 Yet other embodiments are those in which the
7 regulating network includes a buck converter having
8 multiple taps and configured have three operating modes.
9 Among these are embodiments in which the switching network
10 provides first, second, and third voltage rails that, in
11 operation, are maintained at different voltages.

12 Other embodiments of the apparatus are those in which
13 the switching network includes a two-phase switched-
14 capacitor circuit and the regulating network is a buck
15 converter.

16 Also among the embodiments are those in which the
17 regulating network includes parallel first and second
18 regulating circuits.

19 In some embodiments, the power converter includes
20 first and second outputs. In operation, the first output
21 and second outputs being maintained at corresponding first
22 and second voltage differences. The first voltage different
23 is a difference between a first voltage and a second
24 voltage, and the second voltage difference is a difference
25 between a third voltage and the second voltage.

26 In some embodiments, the regulating network includes
27 first, second, and third regulating circuits in parallel.

1 In other embodiments, the power converter includes
2 first second, and third outputs. In operation, the first,
3 second, and third outputs are maintained at corresponding
4 first second, and third voltage differences. The first
5 voltage different is a difference between a first voltage
6 and a second voltage. The second voltage difference is a
7 difference between a third voltage and the second voltage.
8 And the third voltage difference is a difference between a
9 fourth voltage and the second voltage.

10 In some embodiments, the power converter has a first
11 terminal and a second terminal such that, in operation, a
12 first voltage different is maintained across the first
13 terminal and a second voltage difference is maintained
14 across the second terminal. The first voltage difference is
15 a difference between a first voltage and a second voltage,
16 and the second voltage difference is a difference between a
17 third voltage and the second voltage, with the second
18 voltage being variable. Some of these embodiments also have
19 a third stage that provides the second voltage. Also among
20 these are embodiments in which the third stage includes a
21 switched-mode power converter, a switched capacitor
22 converter, a buck converter, or a cascade multiplier.

23 In some embodiments, the power converter is configured
24 to provide AC output with a non-zero DC offset.

25 In other embodiments, the switching network includes a
26 reconfigurable asynchronous cascade multiplier, and the
27 regulating network is connected to the switching network to
28 enable the switching network to cause either a step up in
29 voltage or a step down in voltage. In some cases, the the

1 regulating network includes a four-switch buck-boost
2 converter.

3 In still other embodiments, the first stage is a
4 switching network that includes a reconfigurable cascade
5 multiplier that operates synchronously in a single-phase,
6 and the regulating network includes a four switch buck
7 boost converter. Among these are embodiments in which the
8 regulating network connects to the switching network at a
9 point that enables the switching network to step voltage up
10 or step voltage down.

11 Embodiments also include those in which the switching
12 network includes a cascade multiplier with a charge pump
13 embedded therein. The charge pump can have a variety of
14 characteristics. For example, the charge pump can be
15 reconfigurable, or it can be a fractional charge pump.
16 Alternatively, the embedded charge pump operates in
17 multiple modes, each of which corresponds to a voltage
18 transformation ratio. Or the cascade multiplier might
19 include a reconfigurable two-phase asynchronous step-down
20 cascade multiplier. In any of these embodiments, the
21 regulating network could include a two-phase boost
22 converter.

23 In still other embodiments, the power converter
24 further includes a third stage in series with the first
25 stage and the second stage, wherein the second stage is
26 between the first stage and the third stage, both of which
27 are switching networks. The regulating circuit includes a
28 buck converter, and both switching networks include a
29 single-phase asynchronous step-up cascade multiplier. These
30 embodiments include those in that further include a

1 stabilizing capacitor at an output of the regulating
2 network.

3 In still other embodiments, the power converter
4 further includes a third stage in series with the first
5 stage and the second stage, with the second stage being
6 between the first stage and the third stage. In these
7 embodiments, the first stage and the third stage are
8 switching networks, the regulating circuit includes a buck-
9 boost converter, the first switching network includes a
10 single-phase asynchronous step-up cascade multiplier, and
11 the second switching network includes a single-phase
12 synchronous step-up cascade multiplier. Among these
13 embodiments are those that also have a stabilizing
14 capacitor at an output of the regulating network.

15 In some embodiments, the power converter further
16 includes a third stage in series with the first and second
17 stage, with the second stage being between the first stage
18 and the third stage. The first and third stage are both
19 regulating networks. However, the first stage includes a
20 boost converter, and the third stage includes a buck
21 converter. The switching network includes first and second
22 cascade multipliers having equal numbers of stages. Some of
23 these embodiments also have a phase pump shared by the
24 first and second cascade multipliers. In others, the first
25 and second cascade multipliers operate 180 degrees out of
26 phase. And in yet others, the cascade multipliers comprise
27 corresponding first and second switch stacks, and an output
28 of the switching network is a voltage difference between a
29 top of the first switch stack and a top of the second
30 switch stack.

1 In some embodiments, the power converter further
2 includes a third stage in series with the first and second
3 stages, with the second stage being between the first stage
4 and the third stage. In these embodiments, the first stage
5 and the third stage are regulating networks, the first
6 stage includes a three-level boost converter, the third
7 stage includes a buck converter, and the switching network
8 includes first and second cascade multipliers having
9 unequal numbers of stages.

10 In other embodiments, the switching network receives
11 current that has a first portion and a second portion,
12 wherein the first portion comes from the regulating network,
13 and the second portion, which is greater than the first,
14 bypasses the regulating network.

15 In some embodiments, the power converter further
16 includes a third stage in series with the first stage and
17 the second stage, the second stage being between the first
18 stage and the third stage. The first stage is a first
19 regulating network, the third stage is a second regulating
20 network, and the first stage includes a boost converter.
21 The third stage includes a buck converter. The switching
22 network includes cascade multipliers having unequal numbers
23 of stages. Among these embodiments are those in which the
24 second stage includes an additional inductor connected to
25 the first stage.

26 Yet other embodiments include a third stage. In these
27 embodiments, the first stage includes a regulating network,
28 the third stage includes a regulating network, the power
29 converter provides a load with a first voltage difference,
30 the first stage provides a second voltage difference to the

1 second stage, the second stage provides a third voltage
2 difference to the third stage, the first voltage difference
3 is a voltage difference between a first voltage and a
4 second voltage, the second voltage difference is a voltage
5 difference between a third voltage and a fourth voltage,
6 the third voltage difference is a voltage difference
7 between a fifth voltage and a sixth voltage, the fourth
8 voltage differs from the second voltage, and the sixth
9 voltage differs from the second voltage. Among these
10 embodiments are those in which the second stage includes a
11 reconfigurable switching network.

12 In some embodiments, the first stage includes a
13 switching network having a reconfigurable dual phase
14 cascade multiplier with an embedded inductor configured to
15 promote adiabatic charge transfer between capacitors in the
16 cascade multiplier. In some embodiments, the inductor is
17 embedded at a location through which a constant current
18 passes. Also among these embodiments are those in which the
19 second stage includes a zeta converter, and those in which
20 the cascade multiplier includes a phase pump with the
21 inductor being embedded therein. In others of these
22 embodiments, the cascade multiplier includes pump
23 capacitors, and the inductor is embedded at a location that
24 maximizes the number of paths that pass between the
25 inductor and a pump capacitor.

26 In some embodiments, the switching network includes a
27 dual-phase cascade multiplier with pump capacitors in
28 series. Among these are embodiments in which the switching
29 network has a variable transfer function and embodiments in
30 which the switching network includes a phase pump that

1 includes an embedded charge pump. In this latter case, the
2 embedded charge pump includes switch sets, pump capacitors,
3 and a controller that operates the switch sets to cause
4 transitions between a first operating mode and a second
5 operating mode, each of which corresponds to a transfer
6 function for the cascade multiplier. Among these cases are
7 those in which the controller operates the switch sets so
8 that the embedded controller causes the cascade multiplier
9 to have a transfer function in which the cascade multiplier
10 provides either a voltage gain or a voltage attenuation.

11 In another aspect, the invention features an apparatus
12 for providing electric power to a load includes a power
13 converter that accepts electric power in a first form and
14 provides electric power in a second form. The power
15 converter includes a control system, a first stage, and a
16 second stage in series. The first stage accepts electric
17 power in the first form. The control system controls
18 operation of the first and second stage. The first stage is
19 either a switching network or a regulating network. The
20 second stage is a regulating circuit when the first stage
21 is a switching network, and a switching network otherwise.

22 These and other features will be apparent from the
23 following detailed description and the accompanying figures,
24 in which:

25 **BRIEF DESCRIPTION OF THE DRAWINGS**

26 FIG. 1 shows a power converter having a regulating circuit
27 and a switching network in series;

28 FIG. 2 shows a power converter that is the converse of that
29 shown in FIG. 1;

1 FIG. 3 shows a power converter having a switching network
2 with two switching circuits in series;

3 FIG. 4 shows a power converter having a switching network
4 with two switching circuits in series-parallel;

5 FIG. 5 shows a switching network between two regulating
6 networks;

7 FIG. 6 shows a regulating network between two switching
8 networks;

9 FIG. 7 shows an equivalent circuit for a switching network
10 in which the input and output are isolated;

11 FIG. 8 shows an equivalent circuit for a switching network
12 in which the input and output have a common ground;

13 FIG. 9 shown an equivalent circuit for a switching network
14 in which the input and output have a non-common
15 ground;

16 FIG. 10 shows a first implementation of the switching
17 network in FIG. 1;

18 FIG. 11 shows a second implementation of the switching
19 network in FIG. 1 in which the switching network is a
20 dual-phase symmetric cascade multiplier having
21 parallel pumped capacitors;

22 FIG. 12 shows a third implementation of the switching
23 network in FIG. 1 in which the switching network has a
24 dual-phase asymmetric cascade multiplier stacked on
25 top of dual-phase symmetric cascade multiplier with
26 shared phase nodes;

1 FIG. 13A shows a variant of the power converter in FIG. 10;

2 FIG. 13B shows a power converter similar to that shown in
3 FIG. 13A, but with the order of the regulating network
4 and the switching network having been reversed;

5 FIG. 14A shows a second implementation of the switching
6 network in FIG. 1;

7 FIGS. 14B and 14C show implementations of the phase pump
8 shown in FIG. 14A;

9 FIG. 15A shows a buck converter used to implement a
10 regulating network;

11 FIGS. 15B-15C show non-isolating variants of the buck
12 converter of FIG. 15A;

13 FIGS. 16A-16B show non-isolating buck-boost converters used
14 to implement a regulating network in any of the
15 foregoing power converters;

16 FIGS. 17A-17B show non-isolating boost converters used to
17 implement a regulating network in any of the foregoing
18 power converters;

19 FIGS. 18A-18B show four-terminal non-inverting buck-boost
20 converters;

21 FIG. 19 shows the power converter of FIG. 1 with a
22 reconfiguring switching network;

23 FIG. 20 shows the power converter of FIG. 1 with a
24 reconfiguring regulating network;

1 FIG. 21 shows a power converter in which the regulating
2 circuit has more than two output ports;

3 FIG. 22 shows a power converter similar to that shown in
4 FIG. 21, but with a dual-phase switched-capacitor
5 circuit instead of as a single-phase switched-
6 capacitor circuit;

7 FIG. 23 shows a power converter with a magnetic filter
8 between a switching network and a load;

9 FIG. 24 shows a power converter with a magnetic filter
10 between a switching network and a power source;

11 FIG. 25 shows the power converter of FIG. 22 modified to
12 include a magnetic filter between the switching
13 network and the load;

14 FIG. 26 shows a power converter that uses a two-phase step-
15 down switching network connected in series with a
16 step-down regulating network;

17 FIG. 27 shows a power converter similar to that shown in
18 FIG. 19 but with the order of the switching network
19 and the regulating network reversed;

20 FIG. 28 shows a power converter in which the regulating
21 network is a buck converter with multiple taps;

22 FIG. 29 shows a power converter similar to that shown in
23 FIG. 28, but with the buck converter having four
24 instead of three taps;

25 FIG. 30 shows the power converter of FIG. 26 with a two-
26 phase switched-capacitor circuit implementing the

switching network and a buck converter implementing
the regulating network;

FIG. 31 shows a power converter with two voltage outputs;

FIG. 32 shows a power converter with three voltage outputs;

FIG. 33 shows a power converter floating above ground;

FIG. 34 is an embodiment in which a 4-switch buck-boost
converter implements the regulating network and a
reconfigurable single-phase asymmetric cascade
multiplier implements the switching network;

FIG. 35 is a particular embodiment of the power converter
in FIG. 2 in which a dual-inductor buck converter
implements the regulating network and a reconfigurable
dual-phase asymmetric step-up cascade multiplier
implements the switching network;

FIG. 36 shows an implementation of a power converter in
which the switching network has a separate charge pump
embedded within a cascade multiplier;

FIG. 37 shows the embedded charge pump of FIG. 36;

FIG. 38 shows the power converter of FIG. 6 in which a buck
converter implements the regulating circuit, a single-
phase asymmetric step-up cascade multiplier implements
the first switching network, and a single-phase
symmetric step-up cascade multiplier implements the
second switching network;

FIG. 39 shows the power converter of FIG. 38 in which the buck converter is replaced with a buck-boost converter;

FIG. 40 shows a power converter in which two cascade multipliers with equal numbers of stages implements the switching network;

FIG. 41 shows a power converter in which two cascade multipliers with unequal numbers of stages implements the switching network;

FIG. 42 shows a power converter in which the bulk of the current into the switching network bypasses the boost converter;

FIG. 43 shows a power converter having floating regulating networks and a grounded switching network; and

FIG. 44 shows an implementation of FIG. 2 in which inductors embedded in the switching network promote adiabatic charge transfer within the switching network.

DETAILED DESCRIPTION

FIG. 1 shows a power converter having two stages in series. Depending on details of the circuitry within the two stages, and on the operation of the controller, the power converter will be a dc-dc converter, an ac-dc converter, a dc-ac converter, or an ac-ac converter.

Each stage is either a regulating network **16A** or a switching network **12A**. The illustrated power converter separates the function of voltage/current transformation from that of regulation. As shown in FIG. 1, it does so by providing a regulating network **16A** in series with a

1 switching network **12A**. The two stages can operate at the
2 same frequency, at different frequencies, in phase, and out
3 of phase.

4 A power source **14** and a load **18A** are shown only for
5 clarity. These components are not actually part of the
6 power converter. They merely represent the source of the
7 power to be converted, and the ultimate consumer of that
8 power. Dashed lines between these components and the power
9 converter indicate that they are optional. Other components
10 shown connected with dashed lines in this and other figures
11 are likewise optional. For example, a dashed wire between
12 the regulating network **16A** and the switching network **12A** is
13 also optional.

14 In FIG. 1, the power source **14** is a voltage source.
15 However, since power is the product of voltage and current,
16 the power source **14** could just as easily be a current
17 source. Examples of a suitable power source **14** include, but
18 are not limited to, a battery, a solar panel, a fuel-cell,
19 and a power supply.

20 The power source **14** need not deliver a constant stream
21 of power. In fact, if it did, the power converter would not
22 be nearly as necessary. After all, among the tasks of a
23 power converter is to deliver a constant stream of power
24 with specific characteristics to the load **18A**
25 notwithstanding variations in the power stream provided by
26 the power source **14**. The power source **14** is merely a source
27 of power, or equivalently, since power is the time-
28 derivative of energy, a source of energy.

1 The load **18A** can be any type of electrical load. What
2 is essential, is that it be a net energy consumer. Examples
3 of a load **18A** include a microprocessor, LED, RF PA, or a
4 DSP. In fact, the load **18A** might even be another power
5 converter.

6 The arrows shown in the figure represent power flow,
7 and not magnitude of power flow. Hence, each stage can be
8 bidirectional. In such cases, if the load **18A** supplies
9 power, then the load **18A** acts as a power source **14** and the
10 power source **14** acts as a load **18A**. However, in some
11 embodiments, one or more stages are unidirectional. In
12 addition, embodiments exist in which a stage can be a step-
13 up stage, a step-down stage or a step-up/down stage.

14 The illustrated regulating network **16A** can itself
15 comprise two or more constituent regulating circuits
16 operating as a combination in order to regulate some
17 electrical parameter. These regulating circuits can have
18 different voltage ratings and connect to each other in
19 different ways. In some embodiments, the regulating
20 circuits connect in series. In others, they connect in
21 parallel, in series-parallel, or in parallel-series.

22 The regulating circuits that comprise a regulating
23 network **16A** can be of different types. For example, a
24 regulating network **16A** may comprise a buck converter in
25 combination with a linear regulator. Examples of suitable
26 regulating circuits include a buck converter, a boost
27 converter, a buck-boost converter, a fly-back converter, a
28 push-pull converter, a forward converter, a full bridge
29 converter, a half-bridge converter, a multi-level converter

1 (buck or boost), a resonant converter, a Cuk converter, a
2 SEPIC converter, a Zeta converter, and a linear regulator.

3 Like the regulating network **16A**, the switching network
4 **12A** can also be made of a combination of cooperating
5 switching circuits. These individual switching circuits can
6 have different transformation ratios, the same
7 transformation ratios, and different voltage ratings. They
8 can also be different kinds of switching circuits, such as
9 series parallel or cascade multiplier circuits.

10 A cascade multipliers includes a switch stack, a phase
11 pump, pump capacitors, and, optionally, dc capacitors. The
12 phase pump comprises a pair of switches that cooperate to
13 create a pump signal V_{clk} . In general, the two states of the
14 clock are separated by a brief dead-time to allow
15 transients and the like to decay. In cascade multipliers
16 that require a complement to the clock signal, the phase
17 pump includes another pair of switches to generate the
18 complement. The switch stack is a series of switches
19 connected between the input and the output of the cascade
20 multiplier.

21 In those cases in which the switching circuit is a
22 cascade multiplier, it can be asymmetric, symmetric,
23 series-pumped, or parallel-pumped. Additional types of
24 switching circuits include series-parallel switching
25 circuits, parallel-series switching circuits, voltage-
26 doubling circuits, and Fibonacci circuits. These
27 constituent switching circuits can connect to each other in
28 series, in parallel, in series-parallel, or in parallel-
29 series. Some configurations of the illustrated power

1 converter permit adiabatic charge transfer into or out of a
2 capacitor in the switching network **12A**.

3 Other configurations feature a reconfigurable
4 switching network **12A** that transitions between two or more
5 states in the course of transferring charge. This charge
6 transfer depends on the voltage across the capacitor's
7 terminals. Reconfiguring the switching network **12A** involves
8 causing switches in the network to change state to cause
9 this voltage to change. Reconfiguration can occur, for
10 example, when the voltage or current transformation between
11 the ports of the switching network **12A** is to be changed.

12 FIG. 1 also shows a controller that controls the
13 operation of one or more stages in the power converter. The
14 controller operates in response to an I/O signal and a
15 clock signal. In some embodiments, the I/O signal is a
16 digital communication signal. The clock signal can be a
17 signal from a clock or it can be a signal from some analog
18 reference. This might be a signal set by the user.
19 Alternatively, another subsystem sets this signal and sends
20 it to the power converter.

21 In some embodiments, the controller receives multiple
22 sensor inputs from the power converter and provides control
23 signals along first and second paths **P1**, **P2**. Examples of
24 sensor signals provided to the sensor inputs are V_o , V_x , V_{IN} ,
25 I_{IN} , I_x , and I_o . Among the foregoing sensor inputs, the
26 negative terminals of V_{IN} , V_x , and V_o can be at ground, above
27 ground, or below ground depending upon their corresponding
28 regulating circuits and switching networks. In fact, since
29 voltage reflects a difference in potential energy between

1 two points, there is nothing particularly special about
2 ground.

3 The controller's function is to control both the
4 regulating network **16A** and the switching network **12A** in an
5 effort to control V_{IN} , I_{IN} , V_O , and I_O . In carrying this out,
6 the controller can use either feed-forward control or
7 feedback control. Feed-forward control involves choosing an
8 output control signal based on an input, whereas feedback
9 control involves choosing an output control signal based on
10 an output.

11 Additional control methods that are applicable include
12 voltage-mode control, current-mode control, hysteretic
13 control, PFM control, pulse-skipping control, and ripple-
14 based control. In embodiments that rely upon voltage-mode
15 control, control can be linear or non-linear. In
16 embodiments that rely upon current-mode control, current
17 can be based on both an average value of current or a peak
18 value of current.

19 It is possible to interconnect the regulating network
20 and the switching network in a variety of ways. FIGS. 1, 2
21 5, and 6 show four fundamental building blocks.

22 In particular, FIG. 1 shows a switching network **12A** in
23 series with a regulating network **16A**, with the load **18A**
24 connected to the switching network **12A** and the power source
25 **14** connected to the regulator network **16A**.

26 FIG. 2 is similar to FIG. 1 but with the power source
27 **14** and load **18A** having been swapped. Thus, in FIG. 2, the
28 power source **14** connects to the switching network **12A** and
29 the load **18A** connects to the regulating network **16A**. When

1 power is supplied from the load **18A** in the power converter
2 shown in FIG. 1, the result is a power converter that is
3 equivalent to that shown in FIG. 2.

4 As mentioned above, it is possible for a switching
5 network **12A** to comprise two or more switching circuits. FIG.
6 3 shows a particular example in which a switching network
7 **12A** has two switching circuits in series. Each switching
8 circuit is a stage. Assuming the same switched-capacitor
9 topology for each stage, the resulting switching network
10 **12A** achieves a larger transformation ratio with the same
11 number of switches and capacitors. Alternatively, the
12 switching network **12A** can achieve the same transformation
13 ratio, but with fewer switches and capacitors. On the other
14 hand, a disadvantage of the power converter shown in FIG. 3
15 is that the voltage stresses on the components in at least
16 one of the two stages increases when compared to the single
17 stage case.

18 FIG. 4 shows an embodiment in which the switching
19 network **12A** has first and second switching circuits
20 connected in series-parallel. The first switching circuit
21 achieves a 4:1 transformation ratio and the second
22 switching circuit achieves a 3:1 transformation ratio. As a
23 result, an intermediate voltage V_x between the regulating
24 network **16A** and the switching network **12A** can be any
25 fraction of the output voltage V_o . In the illustrated power
26 converter, the intermediate voltage V_x equals the output
27 voltage V_o . However, had the first switching circuit
28 provided a 4:1 transformation ratio and had the second
29 switching circuit provided a 2:1 transformation ratio, then
30 the intermediate voltage V_x would have been larger than the

1 output voltage V_o . Similarly, had the first switching
2 circuit provided a 4:1 transformation ratio and had the
3 second switching circuit provided a 7:2 transformation
4 ratio, then the intermediate voltage V_x would have been
5 smaller than the output voltage V_o .

6 FIG. 5 and FIG. 6 show representative three-stage
7 embodiments.

8 The embodiment of FIG. 5 is similar to that of FIG. 1,
9 but with the inclusion of an additional regulating network
10 **16B** connected to the switching network **12A**. As a result,
11 the switching network **12A** is between two regulating
12 networks **16A**, **16B**.

13 Conversely, the embodiment of FIG. 6 is similar to
14 that of FIG. 2, but with the inclusion of an additional
15 switching network **12B** connected to the regulating network
16 **16A**. As a result, the regulating network **16A** is between two
17 switching networks **12A**, **12B**.

18 The four building blocks described above combine in
19 various ways. For example, combining the building block in
20 FIG. 5 with that in FIG. 1 would result in a power
21 converter in which a first regulating network connects to
22 an input of a first switching network, the output of which
23 connects to an input of a second regulating network. The
24 output of this second regulating network leads to an input
25 of a second switching network. In the resulting power
26 converter, the power source **14** connects to an input of the
27 first regulating network and the load **18A** connects to an
28 output of the second switching network.

FIGS. 7-9 are circuits that are suitable for modeling the behavior of a switching network **12A**. In particular, a switching network **12A** provides a voltage transformation from a first voltage V_1 to a second voltage V_2 , with the second voltage V_2 and the first voltage V_1 being related by a ratio of integers. Commonly used ratios are 1:3, 1:2, 1:1, 2:1, and 3:1. The output resistor R_o accounts for voltage drops resulting from finite resistance of various components. For example, in a switching network **12A** that is intended to provide a 1:2 transformation ratio, it would not be uncommon to have an actual transformation ratio of around 1:1.9 instead of the ideal 1:2 ratio.

The model shown in FIG. 7 differs from that shown in FIGS. 8-9 because the second voltage V_2 can be isolated from the first voltage V_1 . In addition, it is possible to arbitrarily separate the negative terminal of the first voltage V_1 and the negative terminal of the second voltage V_2 . This can be achieved by combining a traditional switched-capacitor circuit with a capacitive isolation stage. However, this comes at the price of increased component cost, size, and a reduction of efficiency.

The model shown in FIG. 8 differs from that shown in FIG. 7 and FIG. 9 because of its common ground. A common ground is desirable in certain applications. For example, many devices that rely on a battery, such as cell-phones, tablets, and notebooks, use the same ground throughout the device.

The model shown in FIG. 9 has a non-common ground. In particular, an offset voltage V_{off} separates the negative terminal of the transformer winding on the first voltage V_1

1 side and the negative terminal of the transformer winding
2 on the second voltage V_2 side. The switched-capacitor
3 topology sets the extent of the offset voltage V_{off} . This
4 ability to set the offset voltage is advantageous in
5 certain applications.

6 FIG. 10 shows a particular implementation of the
7 switching network **12A** in FIG. 1. In the illustrated
8 embodiment, the switching network **12A** is a step-down
9 single-phase asymmetric cascade multiplier having first and
10 second sets of one or more switches. These sets of switches
11 will be herein referred to as first and second "switches" **1**,
12 **2** for convenience, with the understanding that each can be
13 implemented by multiple switches operating in unison. The
14 switching network **12A** further includes pump capacitors **C5-**
15 **C7**, and dc capacitors **C1-C4**. The pump capacitors **C5-C7** are
16 in parallel because their negative terminals all connect to
17 a pump signal V_{clk} . The dc capacitors **C1-C4** are in parallel
18 because their negative terminals connect to ground. In
19 operation, these dc capacitors **C1-C4** store charge from the
20 pump capacitors **C5-C7**.

21 During normal operation, the switching network **12A**
22 alternates between a first and second state at a specific
23 frequency and duty cycle, such as 50%.

24 During the first state, the first switch **1** is closed
25 and the second switch **2** is open. During the second state,
26 the first switch **1** is open and the second switch **2** is
27 closed. The frequency at which the first and second
28 switches **1**, **2** both transition between states can be the
29 same as or different from that at which the regulating
30 network **16A** switches between states. In cases where these

1 frequencies are the same, they can, but need not be in
2 phase.

3 The pump capacitors **C5-C7** swing up and down as the
4 pump signal V_{clk} alternates between zero volts and the
5 output voltage V_o . At each clock cycle, charge moves between
6 a pump capacitor **C5-C7** and a dc capacitor **C1-C4**. In the
7 particular embodiment shown, charge from a dc capacitor **C1**
8 makes its way to the last dc capacitor **C4** after three clock
9 cycles. Overall, the switching network **12A** can be modeled
10 using the circuit model shown in FIG. 9 with a
11 transformation ratio of 1:1 and an offset voltage V_{off} of $3V_o$.

12 In an alternative embodiment, shown in FIG. 11, the
13 switching network **12A** is a dual-phase symmetric cascade
14 multiplier having parallel pumped capacitors. All switches
15 operate in the same manner already described in connection
16 with FIG. 10. Cascade multipliers are described in
17 connection with the description of FIG. 15 in U.S. Patent
18 No. 8,860,396, the contents of which are herein
19 incorporated by reference.

20 A particular feature of the embodiment shown in
21 FIG. 11 is the absence of dc capacitors inside the cascade
22 multiplier (i.e., capacitors **C1**, **C2** are at the input and
23 output terminals). As a result, it is necessary to add a
24 first switch **1A**, a second switch **2A**, and a first dc
25 capacitor **C2**. The sole function of the first dc capacitor
26 **C2** is to keep the node voltage relatively constant. As a
27 result, the capacitance of the first dc capacitor **C2**
28 depends on the amount of charge that is expected to flow in
29 and out of the first dc capacitor **C2** as well as the voltage
30 ripple requirement of the node voltage.

1 In operation, the first switch **1A** and the second
2 switch **2A** are never in a closed state at the same time. To
3 as great an extent as is possible, the first switch **1A** is
4 synchronized with a first switch set **1** so that when the
5 first switch **1A** is open, so are all the switches in the
6 first switch set **1**, and when the first switch **1A** is closed,
7 so are all the switches in the first switch set **1**.
8 Similarly, to as great an extent as is possible, the second
9 switch **2A** is synchronized with the second switch set **2** so
10 that when the second switch **2A** is open, so are all the
11 switches in a second switch set **2**, and when the second
12 switch **2A** is closed, so are all the switches in the second
13 switch set **2**. As a result, when the pump signal V_{clk} is high,
14 a pump capacitor **C8** connects to the first dc capacitor **C2**.
15 When the pump signal V_{clk} is low, a pump capacitor **C5** is
16 connected to the first dc capacitor **C2**.

17 An advantage of the embodiment shown in FIG. 11 is
18 that it becomes possible to create additional dc voltages.
19 For example, it is possible to create an auxiliary voltage
20 across a second dc capacitor **C3**. This auxiliary voltage
21 thus becomes available to drive other circuits, included
22 such circuits as gate drivers and level shifters, or any
23 other circuit that would require, during its operation, a
24 voltage that falls between the input voltage V_{IN} and the
25 output voltage V_o of the power converter.

26 Yet another advantage is the possibility for using
27 charge that is stored in the second dc capacitor **C3** to
28 supply a linear regulator, thus creating a regulated
29 voltage.

1 In yet another embodiment, shown in FIG. 12, the
2 switching network **12A** features a dual-phase asymmetric
3 cascade multiplier stacked on top of dual-phase symmetric
4 cascade multiplier with shared phase pump nodes, i.e. the
5 pump signal V_{clk} and its complement. All switches operate in
6 the same manner already described in connection with FIG.
7 10.

8 Because the nodes are shared in the illustrated
9 embodiment, both cascade multipliers are operated at the
10 same frequency. However, sharing the phase pump is not
11 required.

12 Additionally, in the particular embodiment shown, the
13 transformation ratio of each stage is relatively low.
14 However, there is no special constraint on transformation
15 ratio. For example, it would be quite possible for the
16 dual-phase asymmetric cascade multiplier to have a
17 transformation ratio of 2:1, while the dual-phase symmetric
18 cascade multiplier has a transformation ratio of 10:1.

19 An advantage of the structure shown in FIG. 12 is that
20 the symmetric cascade multiplier lacks dc capacitors and
21 has fewer switches than a corresponding asymmetric cascade
22 multiplier. Thus, the combination of the two as shown in
23 the figure has fewer switches and fewer dc capacitors. On
24 the other hand, the first and second switches **S1**, **S2** block
25 twice the voltage as other switches.

26 FIG. 13A shows a power converter that is a variant of
27 that shown in FIG. 10. In the power converter shown in FIG.
28 13A, the intermediate voltage V_x is applied across the dc
29 capacitors **C1**, **C3** instead of across the dc capacitors **C1**,

1 **C2** as shown in FIG. 10. The corresponding circuit model
2 would be that shown in FIG. 9, but with a transformation
3 ratio of 2:1 and with an offset voltage V_{off} of $2V_o$. In some
4 cases, depending on the nature of the regulating network
5 **16A**, the configuration shown in FIG. 13A permits a wider
6 input voltage V_{IN} range, than the configuration in FIG. 10.

7 FIG. 13B shows a power converter similar to that shown
8 in FIG. 13A, but with the order of the regulating network
9 **16A** and the switching network **12A** having been reversed.
10 Unlike the configuration shown in FIG. 13A, in which the
11 switching network **12A** causes the voltage to step down, in
12 the configuration shown in FIG. 13B, the switching network
13 **12A** causes the voltage to step up.

14 FIG. 14A shows a power converter similar to that shown
15 in FIG. 10 with the exception that the cascade multiplier
16 is a two-phase cascade multiplier instead of a single-phase
17 cascade multiplier. In addition, the pump capacitors **C1-C3**
18 are in series instead of in parallel. As a result, the pump
19 capacitors **C1-C3** avoid having an excessively high voltage
20 across them. On the other hand, the capacitance required is
21 higher than that required in the switching network **12A**
22 shown in FIG. 10. Yet another disadvantage of connecting
23 pump capacitors **C1-C3** in series is that, when adiabatic
24 charge transfer occurs between such capacitors during
25 charge redistribution, the loss associated with such
26 redistribution is greater than it would be with the
27 switching network **12A** shown in FIG. 10.

28 The cascade multiplier includes a phase pump **32**. FIGS.
29 14B-14C show examples of suitable phase pumps. Unlike
30 conventional phase pumps, those shown in FIGS. 14B-14C

include embedded charge pumps. The resulting phase pumps can thus generate pump signals with variable gain. In particular, the phase pump **32** shown in FIG. 14B provides voltage attenuation; the phase pump **32** shown in FIG. 14C provides voltage gain.

The phase pump **32** shown in FIG. 14B includes a first pair of switches **1**, a second pair of switches **2**, a third pair of switches **3**, a fourth pair of switches **4**, a first pump capacitor **C1**, and a second pump capacitor **C2**. In response to receiving an output voltage V_o , the illustrated phase pump **32** produces a pump signal V_{clk} and its complement.

In operation, the phase pump **32** operates in either a first operating mode or a second operating mode. In the first operating mode, the pump signal V_{clk} alternates between 0 volts and $V_o/2$ volts. In the second operating mode, the pump signal V_{clk} alternates between 0 volts and V_o volts.

Operation in the first mode requires that the phase pump **32** transition between four states according to the following switching pattern in Table 1A:

State	V_{clk}	1	2	3	4
first	0 V	OFF	ON	ON	OFF
second	$V_o/2$	OFF	ON	OFF	ON
third	0 V	OFF	ON	ON	OFF
fourth	$V_o/2$	ON	OFF	ON	OFF

Table 1A

Operation in the second mode requires that the phase pump **32** transition between two states according to the following switching pattern in Table 1B:

State	V_{clk}	1	2	3	4
first	0 V	OFF	ON	ON	OFF
second	V_O	ON	OFF	OFF	ON

Table 1B

Switching between the first and second mode enables the phase pump **32** to change the transfer function of the cascade multiplier. For example, if the phase pump **32** in FIG. 14A were implemented as shown FIG. 14B, then in the first mode, the transformation ratio would be 1:2 with an offset voltage V_{off} of $2V_O$ volts, but in the second mode the transformation ratio would be 1:1 with an offset voltage V_{off} of $3V_O$ volts.

The phase pump **32** shown in FIG. 14C includes a first set of switches **1**, a second set of switches **2**, a first pump capacitor **C1**, and a second pump capacitor **C2**. In response to receiving an output voltage V_O , the illustrated phase pump **32** produces a pump signal V_{clk} and its complement.

In normal operation, the phase pump **32** transitions between a first and a second state. During the first state, the switches in the first set of switches **1** are closed while those in the second set of switches **2** are opened. During the second state, the switches in the first set of switches **1** are opened while those in the second set of switches **2** are closed.

Unlike the phase pump **32** shown in FIG. 14B, which provided an alternating signal with a peak below the output voltage V_O , this phase pump **32** provides an alternating signal with a peak above the output voltage V_O . Since the peak voltage of the pump signal V_{clk} is twice that of the output voltage V_O , the phase pump **32** shown in FIG. 14C

1 produces a higher transformation ratio and offset voltage
2 V_{off} than a standard phase pump that uses two pairs of
3 switches.

4 For example, if the phase pump **32** shown in FIG. 14A
5 were implemented as shown in FIG. 14C, the transformation
6 ratio would be 2:1 with an offset voltage V_{off} of $5V_0$ volts
7 compared to 1:1 with an offset voltage V_{off} of $3V_0$ volts for
8 a standard phase pump.

9 FIG. 15A shows a buck converter that can be used in
10 connection with implementing a regulating network **16A**. The
11 buck converter is similar to that shown as configuration
12 "A1" in the table in the appendix.

13 In FIG. 15A, the buck converter has an input terminal,
14 an output terminal, and a common negative terminal. The
15 common negative terminal is maintained at a common voltage
16 V_{com} . The input terminal is maintained at a first voltage V_1
17 that differs from the common voltage V_{com} by V_1 volts. The
18 output terminal is maintained at a second voltage V_2 that
19 differs from the common voltage by V_2 volts.

20 The buck converter includes a first switch **S1**, a
21 second switch **S2**, an inductor **L1**, and a driver circuit **20A**.
22 The driver circuit **20A** receives a control signal **VR** and
23 outputs suitable voltages for controlling the first and
24 second switches **S1**, **S2**.

25 It is not actually necessary for the input terminal
26 and the output terminal to share a common negative terminal.
27 In fact, there are six possible configurations of non-
28 isolated regulating circuits that have two switches **S1**, **S2**,
29 an inductor **L1**, and four terminals. Two of them are buck

1 converters. These are shown in FIGS. 15B-15C. Two are buck-
2 boost converters, which are shown in FIGS. 16A-16B. And the
3 remaining two are boost converters, which are shown in FIGS.
4 17A-17B. If one is willing to have four switches **S1**, **S2**, **S3**,
5 **S4**, additional possibilities emerge, two of which are shown
6 in FIGS. 18A-18B.

7 Examples of configurations other than those described
8 above for regulating circuits are shown in the appendix.
9 All of the exemplary regulating circuits shown in the
10 appendix can be used within the regulating network **16A**.

11 The buck converters shown in FIGS. 15B-15C each have a
12 positive input terminal and output terminal with their own
13 respective negative terminal. For ease of discussion,
14 voltages at each terminal of the buck converters in
15 FIGS. 15B-15C have been assigned names and practical values.
16 Each buck converter has first and second switches **S1**, **S2**,
17 an inductor **L1**, and a drive circuit **20A**. The drive circuit
18 **20A** receives a control signal **VR** and, in response, outputs
19 voltages that control the first and second switches **S1**, **S2**.
20 The drive circuit **20A** is referenced to a ground potential
21 (i.e., 0 V), which is the negative input terminal in FIG.
22 15B, and the negative output terminal in FIG. 15C. A level
23 shifter or a boot strap circuit might be required within
24 the driver circuit **20A** to provide appropriate voltage
25 signals to control the first and second switches **S1**, **S2**.

26 In operation, the buck converters in FIGS. 15B-15C
27 transition between a first state and a second state. In the
28 first state, the first switch **S1** is closed and the second
29 switch **S2** is open. In the second state, the first switch **S1**
30 is open and the second switch **S2** is closed. In a power

1 converter that uses this regulating network **16A**, the
2 voltage $+V_2$ at the positive output terminal is lower than
3 the voltage $+V_1$ at the positive input terminal.

4 In the buck converter shown in FIG. 15B, the negative
5 output terminal, which carries a floating voltage, $-V_2$, is
6 between two loads **18A**, **18B**. Meanwhile, the voltage $+V_2$ is
7 constrained to float between $+V_1$ and $-V_2$. In the buck
8 converter shown in FIG. 15C, the negative input terminal,
9 which carries a floating voltage, $-V_1$, is coupled between
10 two sources **14A**, **14B**. Meanwhile, the voltage $+V_2$ is
11 constrained to float between $+V_1$ and $-V_1$.

12 FIGS. 16A-16B show four-terminal buck-boost converters
13 that are used to implement the regulating network **16A**. In
14 FIG. 16A, the voltage $-V_2$ floats between $+V_1$ and $+V_2$. In
15 FIG. 16B, the voltage $-V_1$ floats between $+V_1$ and $+V_2$.

16 Each buck-boost converter has first and second
17 switches **S1**, **S2**, an inductor **L1**, and a driver circuit **20A**
18 that receives a control signal **VR** and, in response, outputs
19 voltage signals that control the switches **S1**, **S2**. The buck-
20 boost converters transition between first and second states.
21 In the first state, the first switch **S1** is closed and the
22 second switch **S2** is open. Conversely, in the second state,
23 the first switch **S1** is open and the second switch **S2** is
24 closed. In a power converter that uses this regulating
25 network **16A**, the voltage $+V_2$ at the positive output terminal
26 can be higher or lower than the voltage $+V_1$ at the positive
27 input terminal.

28 FIGS. 17A-17B show boost converters that are used to
29 implement the regulating network **16A**. In the boost

1 converter shown in FIG. 17A, the voltage $+V_1$ is between $+V_2$
2 and $-V_2$. In the boost converter shown in FIG. 17B, the
3 voltage $+V_1$ is between $+V_2$ and $-V_1$.

4 Each boost converter features first and second
5 switches **S1**, **S2**, an inductor **L1**, and a drive circuit **20A**
6 that receives a control signal **VR** and, in response, outputs
7 voltages suitable for driving the first and second switches
8 **S1**, **S2**.

9 In operation, each boost converter transitions between
10 first and second states. In the first state, the first
11 switch **S1** is closed and the second switch **S2** is open. In
12 contrast, in the second state, the first switch **S1** is open
13 and the second switch **S2** is closed. In the regulating
14 network **16A** implemented using the boost converter of FIGS.
15 17A or 17B, the voltage $+V_2$ at the positive output terminal
16 is higher than the voltage $+V_1$ at the positive input
17 terminal.

18 The regulating network **16A** can also be implemented
19 using non-isolating regulating circuits that have a first
20 switch **S1**, a second switch **S2**, a third switch **S3**, a fourth
21 switch **S4**, an inductor **L1**, and four ports. A variety of
22 configurations are shown in the table in the appendix.

23 FIGS. 18A-18B show two embodiments of such four-
24 terminal non-inverting buck-boost converters, each of which
25 can operate in buck mode or boost mode depending on the
26 switch configuration. In buck mode, the regulator causes
27 voltage to step down, whereas in boost mode, it causes
28 voltage to step up.

1 When operating in buck mode, the first switch **S1** is
2 closed and the second switch **S2** is opened. The remaining
3 switches are then operated to transition between first and
4 second states. In the first state, the third switch **S3** is
5 closed and the fourth switch **S4** is open. In the second
6 state, the third switch **S3** is open and the fourth switch **S4**
7 is closed. In buck mode, $+V_2 < +V_1$ while $-V_2 < +V_1$.

8 When operating in boost mode, the third switch **S3** is
9 closed while the fourth switch **S4** is open. The remaining
10 switches are then operated to transition between first and
11 second states. In the first state, the first switch **S1** is
12 closed and the second switch **S2** is opened. In the second
13 state, the first switch **S1** is open and the second switch **S2**
14 is closed. When operated in boost mode, $+V_2 > +V_1$ while $-V_2 < +V_1$.

15 A converter along the lines shown in FIGS. 18A-18B is
16 desirable because it widens acceptable voltage limits at
17 its terminals. However, it does so at the cost of increased
18 component cost and size, as well as a reduction in
19 efficiency.

20 A disadvantage of the power converters shown in
21 FIGS. 10-13 is that the offset voltage V_{off} is fixed to
22 specific fraction of the output voltage V_o . For example, in
23 the power converter shown in FIG. 10, the offset voltage
24 V_{off} is $4V_o$. In the power converter shown in FIG. 13 the
25 offset voltage V_{off} is $2V_o$. This is acceptable if the input
26 voltage V_{IN} or the output voltage V_o is constrained over a
27 narrow range. However, if the input voltage V_{IN} or output
28 voltage V_o varies over a range that is wider than this
29 narrow range, this can place the regulating network **16A**
30 outside acceptable voltage limits associated with its

1 specific implementation. This leads to gaps in the
2 operating range or over voltage of the switches.

3 The power converter shown in FIG. 19 overcomes the
4 foregoing disadvantages. The illustrated power converter is
5 a species of that shown in FIG. 1 with the switching
6 network **12A** implemented using a step-down single-phase
7 asymmetric cascade multiplier having selection switches **S3-**
8 **S10** and with the regulating network **16A** implemented using
9 the regulating circuit shown in FIG. 17A.

10 The illustrated switching network **12A** is an example of
11 a reconfigurable switched-capacitor network. There are many
12 ways to implement such a reconfigurable switched-capacitor
13 network. In fact, in principle, if one can add any number
14 of switches, there are an infinite number of ways to
15 implement such a reconfigurable switched-capacitor network.

16 The regulating network **16A** includes first and second
17 active switches **3, 4** and an inductor **L1**. The first and
18 second active switches **3, 4** cycle between first and second
19 states at a particular duty cycle and frequency.

20 Depending on the upon the required offset voltage V_{off} ,
21 which is set by input voltage V_{IN} and output voltage V_o , the
22 offset voltage V_{off} can be set to a fraction of the output
23 voltage V_o by selectively enabling and disabling the
24 selection switches **S3-S10**. In particular, the state of each
25 selection switch for the various offset voltages V_{off} is
26 shown in Table 2:

V_{LX}	V_{off}	S3	S4	S5	S6	S7	S8	S9	S10
V_1/V_2	$3V_4$	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF
V_2/V_3	$2V_4$	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF
V_3/V_4	$1V_4$	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
V_4/gnd	0 V	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON

Table 2

Some of the disabled switches (i.e., OFF) will see a higher voltage than the active switches in the regulating network **16A**.

For example, suppose V_4 equals one volt. Then V_3 equals two volts, V_2 equals three volts, and V_1 equals four volts. When operating in the mode described on the first line of Table 2, switches **S3** and **S7** are ON: switch **S6** has three volts across it and switch **S5** has two volts across it, while the active switches **3**, **4** only have one volt across them. In general, the selection switches **S3-S10** will either have to have a higher voltage rating than the active switches **3**, **4** or they will need to be implemented as cascaded low-voltage switches.

Another issue with this circuit is that the voltage across the selection switches **S3-S10** can change polarity. This poses a difficulty because a MOSFET has a parasitic diode in parallel with it, the polarity of which depends on where the body contact of the MOSFET is tied. For example, in one embodiment, the first active switch **3** of the regulating network **16A** is a MOSFET having a parasitic diode **D1** with its positive terminal connected to the inductor **L1**. As a result, the first active switch **3** can only block a voltage that is higher at the terminal on the output side of the active switch **3** than the voltage at the inductor side of the active switch **3**. Hence, the selection switches

1 **S3-S10** must be able to block in both directions. One way to
2 do this is to connect two switches back-to-back with their
3 bodies tied such that the cathodes (negative terminals) of
4 their corresponding parasitic diodes connect to each other.
5 Another way to do this is to provide circuitry for changing
6 polarity of the parasitic diode on the fly, for example by
7 providing a body-snatcher circuit.

8 The illustrated power converter further includes a
9 disconnect switch **S11** to protect the low voltage switches
10 in the power converter in the event of a fault (described
11 in U.S. Patent No. 8,619,445). The disconnect switch **S11**
12 must be a high-voltage switch to achieve this function.
13 Since this switch is not routinely operated, it can be made
14 large to reduce its resistance. However, doing so increases
15 die cost.

16 In some practices, because a boost converter is
17 practical only when its duty cycle is between about 5% and
18 95%, there will be gaps in the space of available output
19 voltages.

20 There are at least two ways to fill these gaps. A
21 first way is to press the disconnect switch **S11** into
22 service as a linear regulator at the input of the
23 regulating network **16A**. Another way is to place a linear
24 regulator at the output of the regulating network **16A**.
25 These both come at the cost of efficiency. Of the two,
26 placing the linear regulator at the input is preferable
27 because doing so impairs efficiency less than placing the
28 linear regulator at the output.

1 In principle, it is possible to reconfigure either the
2 regulating network **16A** or the switching network **12A**.

3 FIG. 20 shows a circuit in which the regulating network **16A**
4 is configured to accept or produce, depending upon
5 direction of power transfer, voltages V_1 - V_4 . In operation,
6 the regulating network **16A** regulates at least one wire.

7 However, in some embodiments, the regulating network **16A**
8 regulates more than one wire. In those embodiments in which
9 the regulating network **16A** regulates more than one wire, it
10 does so depending upon the value of the input voltage V_{IN} .
11 For example, if the input voltage V_{IN} is low, the regulating
12 network **16A** will regulate V_3 . If the input voltage V_{IN} is
13 high the regulating network **16A** will regulate V_1 . This
14 regulating network **16A** reconfigures instead of the
15 switching network **12A**.

16 Instead of using a series of selection switches to
17 present different voltages to a regulating network **16A** with
18 two output ports, as shown FIG. 19, it is also quite
19 possible to use a regulating network **16A** with more than two
20 output ports. FIG. 21 shows a power converter having such a
21 configuration.

22 The power converter shown in FIG. 21 includes both a
23 reconfigurable switching network **12A** and a reconfigurable
24 switching regulating network **16A**. Reconfiguration is
25 carried in both cases by reconfiguration switches. These
26 reconfiguration switches are not involved in actual
27 operation of the network. Their function is to select
28 different tap points on the network.

29 In the power converter shown in FIG. 21, the
30 reconfigurable switching network **12A** is a single-phase

step-down switched-capacitor circuit. The reconfigurable regulating network **16A** is a multi-tap boost converter having active switches **S1–S5**, a cascode switch **S6**, an inductor **L1**, and a disconnect switch **S11**.

During normal operation, only two of the active switches **S1–S5** are opening and closing at some specific frequency. The remaining active switches are disabled. The boost converter connected to multiple taps on the switching network **12A**. This allows the boost converter to regulate the voltage difference between two dc capacitors by controlling the time ratio of the enabled active switches. Such control results in a regulated output voltage V_o . Since the voltage difference between two dc capacitors is the output voltage V_o , the active switches **S1–S5** only need to support the output voltage V_o , which is low voltage. In the illustrated examples, each active switch **S1–S5** only has to support one volt. However, the disabled switches would normally have to see a higher voltage. Selection switches **S6–S10** within the switching network **12A** block this voltage, thereby sparing the disabled active switches from having to endure it.

Table 3 below shows the proper configuration of the switches to achieve a particular LX signal V_{LX} .

V_{LX}	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
V_1/V_2	3	4	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF
V_2/V_3	OFF	3	4	OFF	OFF	OFF	OFF	ON	ON	OFF
V_3/V_o	OFF	OFF	3	4	OFF	OFF	OFF	OFF	ON	ON
V_o/gnd	OFF	OFF	OFF	3	4	ON	OFF	OFF	OFF	ON

Table 3

1 The disconnect switch **S11** is rated to handle the
2 highest voltage. Its function is to disconnect the input
3 from the output. However, it can also be used during
4 startup, during a power to ground short, and to function as
5 a linear regulator in the manner already discussed in
6 connection with FIG. 19.

7 The power converter of FIG. 21 has the same number of
8 switches as that shown in FIG. 19. However, it has fewer
9 high-voltage switches. In particular, the power converter
10 shown in FIG. 19 has eight high-voltage switches, whereas
11 the power converter in FIG. 21 has only five. On the other
12 hand, the power converter shown in FIG. 19 has only two
13 active switches instead of five for the power converter of
14 FIG. 21. This means that the power converter shown in FIG.
15 19 requires smaller gate drivers and fewer level shifters.

16 In both cases, selection switches must be able to
17 block in both directions. Thus, both the power converter of
18 FIG. 19 and that of FIG. 21 include bidirectional switches
19 or body-snatchers.

20 One disadvantage of the power converter of FIG. 21 is
21 that the active switches see both positive and negative
22 polarity. This makes reconfiguring the power converter of
23 FIG. 21 much more difficult and costly than reconfiguring
24 the power converter shown in FIG. 19.

25 FIG. 22 shows a power converter similar to that shown
26 in FIG. 21, but with the exception that the switching
27 network **12A** is implemented as a dual-phase switched-
28 capacitor circuit instead of as a single-phase switched-
29 capacitor circuit. In addition, both the pump capacitors

1 **C4-C9** and dc capacitors **C0-C3** are in series. This means
2 that their negative terminals are not pegged to a common
3 voltage. Despite these differences, the power converters
4 shown in FIGS. 21-22 operate in a similar manner.

5 The switching network **12A** shown in FIG. 22 has more
6 components than that shown in FIG. 21. However, each dc
7 capacitor in the dual-phase switching network **12A** shown in
8 FIG. 22 can have a smaller capacitance than a corresponding
9 dc capacitor in the single-phase switching network **12A**
10 shown in FIG. 21. This is because, in the single-phase
11 switching network **12A** shown in FIG. 21, the dc capacitors
12 store charge from the pump capacitors. In contrast, in the
13 dual-phase switching network **12A** of FIG. 22, the dc
14 capacitors only store charge from the boost converter
15 during the dead-time during which the switching network **12A**
16 is transitioning between first and second states.

17 In the power converters described thus far, adiabatic
18 charging and discharging of capacitors in the switching
19 network **12A** is made possible by an inductor in the
20 regulating network **16A**. However, it is possible to separate
21 the function of enabling adiabatic charge transfer and
22 regulation by providing a separate magnetic filter. In FIG.
23 23, the power converter of FIG. 1 is modified to include a
24 magnetic filter between the load **18A** and the switching
25 network **12A**. In FIG. 24, the power converter of FIG. 1 is
26 modified to include a magnetic filter between the power
27 source **14** and the switching network **12A**.

28 It is also possible to incorporate a magnetic filter
29 into the power converters shown in FIGS. 5-6. In fact, as
30 the duty cycle of the second regulating network **16B** shown

1 in FIG. 5 approaches 100%, the second regulating network
2 **16B** effectively becomes a magnetic filter. For a regulating
3 network **12A** implemented as shown in FIG. 15C, the second
4 regulating network **16B** can be transformed into a magnetic
5 filter by permanently closing the first switch **S1** and
6 opening the second switch **S2**.

7 In some embodiments, the regulating network **16B**
8 participates in enabling adiabatic charge transfer even
9 when a magnetic filter is present. For example, the
10 magnetic filter may cause a first capacitor to charge
11 adiabatically while the regulating network **16A** causes the
12 same first capacitor to discharge adiabatically, or vice
13 versa.

14 FIG. 25 shows the power converter of FIG. 22 modified
15 to include a magnetic filter between the switching network
16 **12A** and the load **18A**. The illustrated magnetic filter
17 comprises an inductor **L2** and a capacitor **C0**. As described
18 in FIGS. 23-24, the presence of a magnetic filter provides
19 for adiabatic charging or discharging of capacitors in the
20 switching network **12A**. The magnetic filter constrains the
21 flow of current at the output of the switching network **12A**
22 thereby reducing the redistribution current among the
23 capacitors in the switching network **12A**, and hence loss
24 arising from such redistribution.

25 The use of a magnetic filter provides another way to
26 span the gap that arises when, in order to meet a voltage
27 requirement, a regulating network **16A** would have to operate
28 at a duty cycle outside its permissible range of duty
29 cycles. In embodiments without a magnetic filter, these

gaps were filled by using a switch as a linear regulator.
However, linear regulators are inefficient.

When a magnetic filter is made available, one can avoid using an inefficient linear regulator to span the gap by chopping the output of the switching network **12A** and passing it through the magnetic filter to produce a dc output. In some embodiments, switches in the switching network **12A** carry out the chopping. In other embodiments, an additional switch **S12** can be added to aid in chopping. Note that elements shown connected with dotted lines are optional. In those embodiments in which a buck-boost converter implements the regulating network **16A**, neither a linear regulator nor voltage chopping at the switching network **12A** is required.

Table 4 below summarizes operation of two embodiments, one with and one without an additional switch **S12**. Option 1 of the table shows how the switches in the switching network **12A** transition between first and second states to carry out chopping. Option 2 shows how the use of the additional switch **S12** effectively adds a third state between the first and second states. A benefit of Option 2 is that it avoids having two series-connected switches conduct, thus reducing losses. In addition, Option 2 provides for a body diode that can conduct when the switching network **12A** is transiting between states.

State 3	1A	2A	1B	2B	1	2	S12
OPTION 1	ON	ON	ON	ON	OFF	OFF	-
OPTION 2	OFF	OFF	OFF	OFF	OFF	OFF	ON

Table 4

FIG. 26 shows a power converter that uses a two-phase step-down switching network **12A** connected in series with a step-down regulating network **16A** to limit an output voltage V_o to be between two volts and four volts. The switching network **12A** can be of any type. However, a good choice is a cascade multiplier in part because the regulating network **16A** will then permit adiabatic charge transfer between capacitors in the switching network **12A**. A buck converter having first and second switches **3**, **4**, an inductor **L1**, and a capacitor **C1** implement the regulating network **16A**.

During normal operation the regulating network **16A** alternates between a first and second state at a specific frequency and duty cycle, with the duty cycle determining the transformation ratio. During the first state, the first switch **3** closes and the second switch **4** opens. During the first switch **3** opens and the second switch **4** closes.

FIG. 27 shows a power converter similar to that shown in FIG. 19, but with a wide output voltage V_o range instead of a wide input voltage V_{IN} range. Unlike the power converter in FIG. 19, the power converter of FIG. 27 has a regulating network **16A** that causes voltage to step down instead of to step up. In addition, the order of the switching network **12A** and the regulating network **16A** are opposite to that shown in FIG. 19. The resulting configuration enables adiabatic charge transfer between at least some capacitors in the switching network **12A**.

Operation of the power converter in FIG. 27 proceeds along the lines set forth in connection with FIG. 19. In particular, a controller controls the switches according to the timing pattern in Table 2.

Another way to obtain a wide voltage range is to use a step-down switching network **12A** and to implement the regulating network **16A** with a buck converter with multiple taps, as shown in FIG. 28. The switching network **12A** takes an input voltage V_{IN} and provides two voltage rails: a first rail at two volts and a second rail at four volts. The buck converter features two modes of operation: a first mode in which the LX signal V_{LX} alternates between zero volts and two volts during a switching cycle, and a second mode in which the LX signal V_{LK} alternates between two volts and four volts in a switching cycle. The timing pattern for the switches is set forth in Table 5, with switches labeled "ON" being closed during the complete switching cycle and the switches labeled "OFF" being open during the complete switching cycle.

V_{LX}	1A	2A	1B	2B	1C	2C
0V/2V	3	4	ON	OFF	ON	OFF
2V/4V	ON	OFF	3	4	OFF	ON

Table 5

An advantage of the power converter shown in FIG. 28 is that each switch only has to support two volts. In addition, the switches are configured to avoid the need for body-snatcher circuitry. Switches **1B** and **2A** in particular have body diodes that point to each other and therefore block voltages with any polarity.

To obtain an even wider output range than that given by the power converter shown in FIG. 28, though at the cost of more switches, one can implement the regulating network **16A** with a buck converter having three, rather than two,

modes of operation. Otherwise, operation is similar to that described in connection with FIG. 28.

In FIG. 29, the switching network **12A** maintains three voltage rails at two volts, four volts, and six volts, respectively. In the first operating modes, the LX signal V_{LX} alternates between zero volts and two volts during a switching cycle. In the second operating mode, the LX signal V_{LX} alternates between two volts and four volts during a switching cycle. In the third operating mode, the LX signal V_{LX} alternates between four volts and six volts during a switching cycle.

The timing diagram for the three operating modes is shown in Table 6:

V_{LX}	1A	2A	1B	2B	1C	2C	1D	2D
0V/2V	3	4	ON	OFF	OFF	OFF	ON	OFF
2V/4V	ON	OFF	3	4	ON	OFF	OFF	OFF
4V/6V	OFF	OFF	OFF	ON	3	4	OFF	ON

Table 6

Switches labeled "ON" in Table 6 are closed during the complete switching cycle. Switches labeled "OFF" are open during the complete switching cycle. As is apparent, each switch only has to support at most two volts. In addition, the switches are properly configured such that body snatcher circuits are not required. In particular, switch pair **1B**, **2A** and switch pair **1C**, **2B** show two body diodes pointing at each other. These switch pairs can therefore block voltages of any polarity.

FIG. 30 shows the power converter of FIG. 26 with a two-phase switched-capacitor circuit implementing the

1 switching network **12A** and a buck converter implementing the
2 regulating network **16A**.

3 The buck converter, which has two modes of operation,
4 alternates between the switch configurations shown in
5 Table 5. In the first mode, the LX signal V_{LX} alternates
6 between zero volts and two volts during a switching cycle.
7 In the second mode, the LX signal V_{LX} alternates between two
8 volts and four volts during a switching cycle. The switches
9 labeled "ON" are closed during the complete switching cycle
10 and the switches labeled "OFF" are open during the complete
11 switching cycle. Each switch only needs to be able support
12 two volts. During normal operation the switching network
13 **12A** alternates between the first and second states at a
14 specific frequency and duty cycle. In some embodiments, the
15 duty cycle is 50%.

16 FIG. 31 shows a power converter with first and second
17 regulators in parallel. This provides first and second
18 outputs. In the particular example shown, the first output
19 V_{O1} is between four volts and two volts while the second
20 output V_{O2} is between two volts and zero volts.

21 The first regulator includes first and second switches
22 **3, 4** and a first inductor **L1**. The second regulator includes
23 third and fourth switches **5, 6** and a second inductor **L2**.

24 During normal operation the first regulator alternates
25 between a first and second state at a specific frequency
26 and duty cycle. This duty cycle determines the
27 transformation ratio. During the first state, the first
28 switch **3** is closed and the second switch **4** is opened.
29 During the second state, the states are reversed. The

1 second regulator works in the same way with the third
2 switch **5** replacing the first switch **3** and the fourth switch
3 **6** replacing the second switch **4**. The switching network **12A**,
4 the first regulator, and the second regulator can operate
5 at the same or difference frequency and with any phase
6 difference between them.

7 FIG. 32 shows another embodiment with multiple output
8 voltages. In this case, there are three regulating networks
9 **16A**, **16B**, **16C** corresponding to three output voltages, V_{o1} ,
10 V_{o2} , and V_{o3} . Unlike the power converter shown in FIG. 31,
11 these voltages are less limited on the bottom end.

12 FIG. 33 shows a power converter in which a switching
13 network **12A** in series with a regulating network **16A** are
14 floated above ground. The voltage upon which the switching
15 network **12A** and regulating network **16A** float comes from a
16 third stage. This third stage can be implemented using a
17 switch-mode power converter such as a buck converter or
18 switched-capacitor converter such as a cascade multiplier,
19 or any other type of power converter. The resulting series
20 connected stages to provide a higher output voltage than
21 they normally would be able to. Example voltages are
22 provided in the figure. In particular, in FIG. 33, the
23 third stage produces a two-volt rail. This effectively
24 boosts the output voltage V_o by two volts.

25 An advantage of the configuration shown in FIG. 33 is
26 that only low voltages have to be applied across the
27 terminals of the regulating network **16A**. Thus, only low-
28 voltage transistors are needed. These switch very fast. As
29 a result, one can reduce the size of the inductor.

FIGS. 34-44 show additional embodiments with particular features to be described below. With the exception of a brief dead-time between transitions, during which all switches are open to avoid difficulties that arise from the finite switching time of a real switch, all switches in switch set **1** and switch set **2** are always in opposite states, all switches in switch set **3** and switch set **4** are always in opposite states, and all switches in switch set **5** and switch set **6** are always in opposite states.

FIG. 34 shows an embodiment in which a 4-switch buck-boost converter implements the regulating network **16A** and a reconfigurable single-phase asymmetric cascade multiplier implements the switching network **12A**. In this power converter, the regulating network **16A** connects to the middle of the cascade multiplier within the switching network **12A** thereby enabling the switching network **12A** to cause voltage to either step-up or step-down.

The regulating network **16A** includes an inductor **L1**, a first switch **3**, a second switch **4**, a third switch **5**, and a fourth switch **6**.

When the regulating network **16A** operates in its boost mode, the intermediate voltage V_X is higher than the input voltage V_{IN} . In this mode, the third switch **5** and the fourth switch **6** are active, the first switch **3** is closed, and the second switch **4** is open.

Conversely, when the regulating network **16A** operates in its buck mode, the intermediate voltage V_X is lower than the input voltage V_{IN} . In this mode, the first switch **3** and

the second switch **4** are active, the third switch **5** is closed, and the fourth switch **6** is open.

Meanwhile, the switching network **12A** includes first and second switch sets **1, 2**, four selection switches **S1-S4**, four dc capacitors **C1-C4**, and three pump capacitors **C5-C7**. The voltages on the four dc capacitors **C1-C4** are $4/2V_X$, $3/2V_X$, $2/2V_X$, and $1/2V_X$, respectively.

In operation, the four selection switches **S1-S4** select different dc capacitors **C1-C4** within the switching network **12A** for presentation to the load **18A**. By properly choreographing the enabling and disabling of the selection switches **S1-S4** according to a distinct pattern, one can produce an ac output with a dc offset. This is particularly useful for envelope tracking when providing power to an RF power amplifier.

FIG. 35 illustrates a variation on the embodiment of FIG. 2 in which a dual-inductor buck converter implements the regulating network **16A** and a reconfigurable dual-phase asymmetric step-up cascade multiplier implements the switching network **12A**.

The regulating network **16A** is a dual-inductor buck converter (shown as configuration "C1" in the table in the appendix) having a first inductor **L1**, a second inductor **L2**, a first capacitor **C0**, a first switch **3**, and a second switch **4**. In some embodiments, the first and second inductors **L1, L2** are uncoupled. In others, the first and second inductors **L1, L2** are coupled. These include embodiments that use both positive and negative coupling.

1 Unlike in a single-inductor buck converter, the input
2 current into the dual-inductor converter is relatively
3 constant. This results in lower rms current through the
4 switching network **12A**. Both terminals connected to the
5 switching network **12A** draw a relatively constant current.
6 Because of this behavior, and because a pump capacitor
7 would always be available to feed each inductor, the dual-
8 inductor buck converter is best used with a full-wave
9 cascade multiplier. It is also possible to use a half-wave
10 cascade multiplier. However, in that case, the pump
11 capacitors would only be feeding the inductors half the
12 time. This requires providing high capacitance dc
13 capacitors.

14 The switching network **12A** includes first and second
15 switch sets **1, 2**, eight selection switches **S1-S8**, four dc
16 capacitors **C1-C4**, and six pump capacitors **C5-C10**.

17 A third inductor **L3** that feeds the switching network
18 **12A** promotes adiabatic charge transfer within the switching
19 network **12A**. Because it is only filtering a voltage ripple
20 on the capacitors seen at the input of the switching
21 network **12A**, and because it does not have a particularly
22 large voltage across it, this third inductor **L3** has a much
23 smaller inductance than those required within the
24 regulating network **16A**.

25 Enabling and disabling different selection switches
26 **S1-S8** reconfigures the switching network **12A**, thus enabling
27 one to change the offset voltage V_{off} of the switching
28 network **12A**. Table 7 shows switching patterns used to
29 achieve four different offset voltages.

V_{off}	S1	S2	S3	S4	S5	S6	S7	S8
$3V_4$	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF
$2V_4$	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF
$1V_4$	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
0 V	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON

Table 7

In the particular example shown, the load connected to the output of the power converter comprises a plurality of light-emitting diodes connected in series with each other and with the current path through a transistor biased by a voltage V_B . This permits control over the LED current, thus enabling the brightness of the LED, which is proportional to the LED current I_{LED} , to be controlled. The combination of a power converter and a circuit to control the LED current I_{LED} , which amounts to a current sink, is commonly called an LED driver. In most embodiments, the current sink is somewhat more complicated than a single transistor. However, the principles illustrated in FIG. 35 are applicable to such cases as well.

Instead of using a linear regulator to fill the gaps as discussed in reference to FIG. 19, a current sink along the lines shown in FIG. 35 can be used. However, this is also a somewhat inefficient method.

In another embodiment of the power converter of FIG. 1, which is shown in FIG. 36, a two-phase boost converter implements the regulating network **16A** while a reconfigurable dual-phase asymmetric step-down cascade multiplier implements the switching network **12A**. The particular cascade multiplier shown features an embedded reconfigurable fractional charge pump **22**.

1 The two-phase boost converter includes a first
2 inductor **L1**, a second inductor **L2**, a first switch **5**, a
3 second switch **6**, a third switch **7** and a fourth switch **8**. A
4 circuit **20A** within the regulating network **16A** receives
5 control signals from a controller via a first path **P1**.
6 During normal operation, the circuit **20A** provides first
7 drive signals provided to the first and second switches **5**,
8 **6** and second drive signals to the third and fourth switches
9 **7**, **8**. The first and second drive signals are in phase
10 quadrature. Controlling the duty cycle of at which the
11 switches **4-8** switch regulates the output voltage V_o .

12 The switching network **12A** includes six selection
13 switches **S1-S6**, six pump capacitors **C5-C10**, four dc
14 capacitors **C1-C4**, first and second switch sets **1**, **2**, and a
15 circuit **20B** that provides drive signals to the first and
16 second switch sets **1**, **2** and to the six selection switches
17 **S1-S6** based on control signals received along a path **P2**
18 from the controller.

19 The reconfigurable fractional charge pump **22** has
20 multiple modes. In the particular example described herein,
21 the modes are a 1:1 mode and a 3:2 mode.

22 The reconfigurable fractional charge pump **22** enables
23 the parent cascade multiplier in which it is embedded to
24 output half ratios. Table 8 shows the available
25 transformation ratios ($V_4:V_o$) for the parent cascade
26 multiplier, and both the switch states and the
27 transformation ratio of the embedded reconfigurable
28 fractional charge pump **22** that would be required to achieve
29 those transformation ratios.

$V_4:V_o$	S1	S2	S3	S4	S5	S6	22
4.5:1.0	ON	OFF	OFF	ON	OFF	OFF	3:2
4.0:1.0	ON	OFF	OFF	ON	OFF	OFF	1:1
3.5:1.0	OFF	ON	OFF	OFF	ON	OFF	3:2
3.0:1.0	OFF	ON	OFF	OFF	ON	OFF	1:1
2.5:1.0	OFF	OFF	ON	OFF	OFF	ON	3:2
2.0:1.0	OFF	OFF	ON	OFF	OFF	ON	1:1

Table 8

A particular benefit of providing half ratios is that the resulting power converter operates without the gaps described in connection with FIG. 36.

For example, suppose that the output voltage V_o is one volt and that the input voltage V_{IN} is 3.5 volts. The transformation ratio is 4:1. This requires a duty cycle of 50%, which is well within the permissible range for the regulating circuit (i.e., the dual-phase boost converter).

Suppose now that the input voltage V_{IN} drops to 3.05 volts. At this point, the required duty cycle at the regulating circuit would drop to 5%, which is below the acceptable limit. Ordinarily, this would result in a gap. But not for the circuit shown in FIG. 36. This is because one only has to switch to a 3.5:1 transformation ratio. This raises the required duty cycle back up to 65%, which puts it back within the permissible range of the regulating circuit.

In addition, to eliminating gaps, the ability to provide half ratios enables the regulating circuit to run with a duty cycle between 25% and 75%. This has many benefits, including reducing the rms current and thus boosting the efficiency.

FIG. 37 shows details of the reconfigurable fractional charge pump **22** shown in FIG. 36. The reconfigurable charge pump **22** includes a first switch set **3**, a second switch set **4**, a selection switch **S0**, a dc capacitor **C1**, and first and second pump capacitors **C2**, **C3**. The reconfigurable fractional charge pump **22** is connected to have an input voltage V_1 , an output voltage V_2 , and a ground V_3 .

The reconfigurable fractional charge pump **22** operates in either a first mode or a second mode. When operating in the first mode, the reconfigurable fractional charge pump **22** provides a transformation ratio $V_1:V_2$ of 3:2. When operating in the second mode, the transformation ratio is 1:1.

To operate in the first mode, the selection switch **S0** opens, and the first and second switch sets **3**, **4** switch open and close at some specific frequency. In some embodiments, the switches open and close with a 50% duty cycle. The first switch set **3** and the second switch set **4** are always in opposite states.

To operate in the second mode, the selection switch **S0** closes, and the first and second switch sets **3**, **4** open.

FIGS. 38-39 show alternative embodiments of the power converter shown in FIG. 6 in which a regulating network **16A** is between first and second switching networks **12A**, **12B**. This configuration enables at least one switching network **12A**, **12B** to be adiabatically charged. In addition, the overall transformation ratio becomes the product of the transformation ratios of the first and second switching networks **12A**, **12B**.

1 In the embodiment shown in FIG. 38, a buck converter
2 implements the regulating network **16A**, a single-phase
3 asymmetric step-up cascade multiplier implements the first
4 switching network **16A**, and a single-phase symmetric step-up
5 cascade multiplier implements the second switching network
6 **16B**.

7 The first switching network **12A** includes four dc
8 capacitors **C1-C4**, three pump capacitors **C5-C7**, and first
9 and second switches **1, 2**. In the configuration shown, the
10 first switching network **12A** is not adiabatically charged.
11 Hence, it operates with a duty cycle of near 50%. However
12 this is not required because stability is not an issue. In
13 operation, the first switching network **12A** provides a first
14 voltage V_1 that is four times the input voltage V_{IN} . However,
15 the intermediate voltage V_x that the regulating network **16A**
16 receives from the first switching network **12A** is twice the
17 input voltage V_{IN} .

18 The regulating network **16A** includes a first switch **5**,
19 a second switch **6**, and an inductor **L1**. The regulating
20 network **16A** controls the duty cycle of the first and second
21 switches **5, 6** to regulate its output voltage V_o .

22 The second switching network **12B** includes first and
23 second switch sets **3, 4**, two dc capacitors **C11-C12**, and
24 three pump capacitors **C8-C10**. Unlike the first switching
25 network **12A**, there is an inductor **L1** that feeds the second
26 switching network **12B**. As a result, the second switching
27 network **12B** is adiabatically charged.

28 A dc capacitor **C12** connected at the output of the
29 regulating network **16A** impedes adiabatic operation and is

1 thus optional. This dc capacitor **C12** is typically added
2 only to maintain stability. As a result, its capacitance is
3 much smaller than that of other capacitors in the network.

4 Since the second switching network **12B** is
5 adiabatically charged and its transformation ratio is 1:4,
6 operating it at a duty cycle of 50% promotes stability. The
7 overall output voltage V_o of the power converter is given by
8 $V_o = 8V_{IN}(D+1)$, where the duty cycle D is equal to the duty
9 cycle D of the second switch **6** of the regulating network
10 **16A**.

11 FIG. 39 shows a power converter similar to that shown
12 in FIG. 38, except that a buck-boost converter implements
13 the regulating network **16A** and that the first and second
14 switching networks **12A**, **12B** connect to the regulating
15 network **16A** differently. The result is a different input-
16 to-output transfer function.

17 The regulating network **16A** includes an inductor **L1**, a
18 first switch **5**, and a second switch **6**.

19 The first and second switching networks **12A**, **12B** are
20 the same as those shown in FIG. 38. As was the case in
21 FIG. 38, the second switching network **12B** is adiabatically
22 charged, albeit from a different node. The second switching
23 network **12B** includes first and second dc capacitors **C12**,
24 **C13** that connect to an output of the regulating network **16A**.
25 These capacitors impede adiabatic operation, and are thus
26 optional. However, they are often useful for maintaining
27 stability. Preferably, the values of their capacitances are
28 much smaller than those used in other capacitors within the
29 first and second switching networks **12A**, **12B**.

1 The differences between the power converter in FIG. 39
2 and that in FIG. 38 enable the power converter shown in FIG.
3 39 to have an output voltage V_o that is either positive or
4 negative. Specifically, for a given duty cycle D , of the
5 regulating network's second switch **6**, the output voltage V_o
6 is given by where $V_o = V_{IN}(20D)/(2D-1)$. Thus, the output
7 voltage V_o is positive when the duty cycle D exceeds 0.5 and
8 negative when the duty cycle D falls short of 0.5.

9 FIGS. 40-43 show embodiments of the power converter
10 shown in FIG. 5. Each embodiment features a first
11 regulating network **16A** and a second regulating network **16B**.
12 In each embodiment, controlling the duty cycle D of the
13 switches in both the first and second regulating networks
14 **16A**, **16B** permits control over the output voltage V_o of the
15 power converter. Additionally, in each embodiment, an
16 inductor present in the regulating network **16A** permits
17 adiabatic charge transfer between capacitors in the
18 switching network **12A**. The extent of this adiabatic charge
19 transfer is one of the differences among the different
20 configurations shown in FIGS. 40-43.

21 In the embodiments shown, the first regulating network
22 **16A** is implemented as a step-up converter while the second
23 regulating network **16B** is implemented as a step-down
24 converter. However, this does not have to be the case. For
25 example, the order could be reversed, with the first
26 regulating network **16A** causing a step-down in voltage, and
27 the second regulating network **16B** causing a step-up in
28 voltage. Or, both the first and second regulating networks
29 **16A**, **16B** could cause a step-up or a step-down in voltage.
30 An advantage of the particular configuration shown in the

1 figures is that if the switching network **12A** were a
2 reconfigurable switching network, such as that shown in FIG.
3 19, the illustrated configuration would permit filling-in
4 the gaps in coverage.

5 The illustrated embodiments feature a controller to
6 control operation of switches in the first and second
7 regulating networks **16A**, **16B**. Such a controller can be used
8 to implement a variety of control techniques that can be
9 used in connection with controlling the operation of the
10 first and second regulating networks **16A**, **16B**. In some
11 embodiments, the controller implements feed-forward control
12 over the first regulating network **16A** and feedback control
13 over the second regulating network **16B**. In other
14 embodiments, the controller implements feedback over the
15 first regulating network **16A** and feed-forward control over
16 the second regulating network **16B**.

17 In the embodiment shown in FIG. 40, the first
18 regulating network **16A** is a boost converter and the second
19 regulating network **16B** is a buck converter. The boost
20 converter has a boost-converter inductor **L1** and first and
21 second boost-converter switches **3**, **4**. The buck converter
22 has a buck-converter inductor **L2** and first and second buck-
23 converter switches **5**, **6**.

24 The switching network **12A** includes first and second
25 switch sets **1**, **2**, three dc capacitors **C1-C3**, and six pump
26 capacitors **C4-C9** spread across two symmetric step-up
27 cascade-multipliers. The two cascade multipliers share a
28 common phase pump and operate 180 degrees out of phase. The
29 operation of this switching network **12A** is similar to that
30 of a dual-phase version, or full-wave, cascade multiplier.

1 The main distinction arises from separation of the bottom
2 and top of the switch stacks.

3 Because the stack switches are separate, it is
4 possible to create an intermediate voltage V_{X3} that is a
5 difference between the voltages present at the tops of the
6 switch stacks. In the embodiment shown, the voltage at the
7 top of a first switch stack is $4V_X$, whereas the voltage at
8 the top of a second switch stack is $3V_X + V_{IN}$. Thus, the
9 intermediate voltage V_{X3} is the difference between these,
10 which is $V_X - V_{IN}$.

11 In the embodiment shown in FIG. 41, the first
12 regulating network **16A** is a three-level boost converter and
13 the second regulating network **16B** is a buck converter. The
14 boost converter has a boost-converter inductor **L1**, four
15 switches **3, 4, 5, 6**, and a capacitor **C13**. The buck
16 converter has a buck-converter inductor **L2** and first and
17 second buck-converter switches **7, 8**.

18 FIG. 41 shows a power converter similar to that shown
19 in FIG. 40, but with the first regulating network **16A** being
20 a three-level boost converter. The three-level boost
21 converter requires less inductance for the same amount of
22 filtering compared to the boost converter shown in FIG. 40.
23 In addition, it operates with a reduced voltage stress
24 across its switches. However, it also has many more
25 switches and an additional capacitor. The second regulating
26 network **16B** is again a buck converter like that shown in
27 FIG. 40.

28 The switching network **12A** includes first and second
29 switch sets **1, 2**, three dc capacitors **C1-C3**, and nine pump

capacitors **C4-C12** spread across two symmetric step-up cascade-multipliers. The two cascade multipliers share a common phase pump and operate 180 degrees out of phase. Unlike the switching network **12A** shown in FIG. 40, the two cascade multipliers in FIG. 41 have different numbers of stages. Thus, asymmetry in the number of stages results in a third intermediate voltage V_{x3} presented to the second regulating network **16B**. In particular, the third intermediate voltage, which is $2V_x$, is a difference between a first voltage V_1 , which is equal to $6V_x$, and a second voltage V_2 , which is equal to $4V_x$.

In operation, the three-level boost converter operates in two modes. In each mode, the boost converter cycles through first, second, third, and fourth states at a particular frequency. Each state corresponds to a particular configuration of switches. Table 9A shows the four states in the first mode, and Table 9B shows the four states in the second mode.

State	V_{LX}	3	4	5	6
first	V_x	ON	OFF	ON	OFF
second	$V_x/2$	OFF	ON	ON	OFF
third	V_x	ON	OFF	ON	OFF
fourth	$V_x/2$	ON	OFF	OFF	ON

Table 9A

State	V_{LX}	3	4	5	6
first	0 V	OFF	ON	OFF	ON
second	$V_x/2$	OFF	ON	ON	OFF
third	0 V	OFF	ON	OFF	ON
fourth	$V_x/2$	ON	OFF	OFF	ON

Table 9B

1 Within each mode, the three-level boost converter
2 regulates its output by controlling its generalized duty
3 cycle. The generalized duty cycle is equal to a first time
4 interval divided by a second time interval. The first time
5 interval is equal to the amount of time the three-level
6 boost converter spends in either the first state or the
7 third state. The second time interval is the amount of time
8 the three-level boost converter spends in either the second
9 state or the fourth state.

10 When the three-level buck converter operates in the
11 first mode, the intermediate voltage V_X is greater than two
12 times the input voltage V_{IN} . In contrast, when the three-
13 level buck converter operates in the second mode, the
14 intermediate voltage V_X is less than two times the input
15 voltage V_{IN} .

16 An advantage over the power converter shown in FIG. 41
17 over that shown in FIG. 40 is that it is less complex. In
18 addition, losses resulting from charge redistribution
19 within the switching network **12A** will be reduced because
20 the capacitors within the switching network **12A** will enjoy
21 the benefits of adiabatic charge transfer.

22 The power converter of FIG. 42 combines features of
23 those shown in FIGS. 40-41. As was the case in the power
24 converter shown in FIG. 40, the switching network **12A**
25 receives both the input voltage V_{IN} and the first
26 intermediate voltage V_X to produce a third intermediate
27 voltage V_{X3} . However, like FIG. 41, the number of stages is
28 unequal, with the asymmetry producing the third
29 intermediate voltage V_{X3} .

1 In the switching network **12A** shown in FIG. 42, the
2 first regulating network **16A** no longer drives the phase
3 pump, as was the case in FIGS. 40-41. Thus, the phase pump
4 no longer enjoys the benefit of adiabatic charge transfer
5 resulting from the intervention of the inductor **L1** in the
6 first regulating network **16A**. To make up for this, the
7 switching network **12A** has an additional inductor **L3** that
8 promotes adiabatic charge transfer.

9 In operation, a first voltage V_1 is equal to V_X+5V_{IN} , a
10 second voltage V_2 is equal to V_X+3V_{IN} , and a third
11 intermediate voltage V_{X3} is equal to $2V_{IN}$.

12 An advantage of the power converter shown in FIG. 42
13 over that shown in FIG. 41 is that only a fraction of the
14 input current actually passes through the three-level boost
15 converter. The bulk of the current instead bypasses the
16 three-level boost converter and proceeds directly into the
17 phase pump.

18 Additionally, since the additional inductor **L3** only
19 has to promote adiabatic charge transfer, it can have a
20 smaller inductance than the inductor **L1** in the boost
21 converter. This, in turn, reduces resistive inductor losses.

22 However, a disadvantage of the power converter shown
23 in FIG. 42 is that an additional inductor **L3** is required.
24 In addition, the cascade multiplier requires more stages to
25 achieve the same voltage gain. For example, the first
26 voltage V_1 is equal to $6V_X$ in FIG. 41 while it is equal to
27 V_X+5V_{IN} in the circuit shown in FIG. 42.

28 FIG. 43 shows a power converter in which a boost
29 converter implements the first regulating network **16A**, a

1 buck converter implements the second regulating network **16B**,
2 and a dual-phase asymmetric step-up cascade multiple
3 implements the switching network **12A**.

4 The first regulating network **16A** includes a first
5 switch **3**, a second switch **4**, and an inductor **L1**. The second
6 regulating network **16B** includes a first switch **5**, a second
7 switch **6**, and an inductor **L2**. The switching network **12A**
8 includes a first switch set **1**, a second switch set **2**, four
9 dc capacitors **C1-C4**, and six pump capacitors **C5-C10**.

10 In the power converter shown in FIG. 43, only the
11 switching network **12A** is connected to ground. The first and
12 second regulating networks **16A**, **16B** both float. This
13 reduces the voltage stress across the switches in the first
14 and second regulating networks **16A**, **16B**. Unfortunately,
15 this also narrows the acceptable input voltage V_{IN} range and
16 output voltage V_o range. This disadvantage can be overcome
17 by using a reconfigurable switching network **12A**, but at the
18 added cost of more switches.

19 FIG. 44 shows a particular implementation of the power
20 converter in FIG. 2 in which a reconfigurable dual-phase
21 symmetric step-up cascade multiplier implements the
22 switching network **12A** and a Zeta converter implements the
23 regulating network **16A**.

24 The regulating network **16A** includes a first inductor
25 **L3**, a second inductor **L4**, a capacitor **C10**, a first switch **3**,
26 and a second switch **4**. Depending upon the duty cycle, a
27 Zeta converter can step-up or step-down the voltage.
28 However, a disadvantage of the Zeta converter is the
29 requirement for more passive components. In addition, a

1 Zeta converter is more difficult to stabilize because of
2 the additional poles and zero introduced.

3 The switching network **12A** includes first and second
4 switch sets **1, 2**; two selection switches **S1-S2**, three dc
5 capacitors **C1-C3**, six pump capacitors **C4-C9**, a first
6 inductor **L1**, and a second inductor **L2**.

7 In operation, the switching network **12A** transitions
8 between a first mode and a second mode. During the first
9 mode, the first selection switch **S1** is closed and the
10 second selection switch **S2** is open. The intermediate
11 voltage V_X is then $V_{IN}/2$. During the second mode, the first
12 selection switch **S1** is open and the second selection switch
13 **S2** is closed. In the second mode, the intermediate voltage
14 V_X becomes the input voltage V_{IN} .

15 One way to achieve adiabatic inter-capacitor charge
16 transfer within the switching network **12A** is to place a
17 small inductor in series with the second switch **S2**. However,
18 although this would promote adiabatic charge transfer
19 during the first mode, it would not do so during the second
20 mode.

21 Another way to achieve adiabatic inter-capacitor
22 charge transfer within the switching network **12A** is to
23 embed the first inductor **L1** within the charge pump and the
24 second inductor **L2** in series with the ground terminal of
25 the charge pump.

26 Preferably the first inductor **L1** is embedded at a
27 location that carries a constant current and that connects
28 to charging and discharging paths of as many pump

1 capacitors **C4-C9** as possible. A suitable location is
2 therefore at the phase pump.

3 A charge pump typically has two nodes that carry
4 constant current. As shown in FIG. 44, the first inductor
5 **L1** is at one of these nodes and the second inductor **L2** is
6 at the other. However, only one of these inductors is
7 actually required to promote adiabatic charge transfer.

8 Having described the invention, and a preferred
9 embodiment thereof, what is claimed as new, and secured by
10 letters patent is:

CLAIMS

- 1
2 **1.** An apparatus for providing electric power to a load,
3 said apparatus comprising a power converter, wherein
4 said power converter accepts electric power in a first
5 form and provides electric power in a second form,
6 wherein said power converter comprises a control
7 system, a first stage, and a second stage, wherein
8 said first stage accepts electric power in said first
9 form, wherein said second stage and said first stage
10 are in series, wherein said control system controls
11 operation of said first stage, wherein said control
12 system controls operation of said second stage,
13 wherein said first stage is selected from the group
14 consisting of a switching network and a regulating
15 network, wherein said second stage is a regulating
16 circuit when said first stage is a switching network,
17 and wherein said second stage is a switching network
18 when said first stage is a regulating circuit.
- 19 **2.** The apparatus of claim **1**, wherein said first stage is
20 a regulating network.
- 21 **3.** The apparatus of claim **1**, wherein said first stage is
22 a switching network.
- 23 **4.** The apparatus of claim **1**, wherein said control system
24 controls at least in part based on a voltage measured
25 between said first and second stages.
- 26 **5.** The apparatus of claim **1**, wherein at least one of said
27 stages comprises a switching network, wherein said
28 switching network comprises a first terminal and a
29 second terminal, wherein said first terminal and said
30 second terminal are isolated.

1 **6.** The apparatus of claim **1**, wherein at least one of said
2 stages comprises a switching network, wherein said
3 switching network comprises a first terminal and a
4 second terminal, wherein said first terminal and said
5 second terminal have a common ground.

6 **7.** The apparatus of claim **1**, wherein at least one of said
7 stages comprises a switching network, wherein said
8 switching network comprises a first terminal and a
9 second terminal, wherein said first terminal and said
10 second terminal have a separate ground.

11 **8.** The apparatus of claim **1**, wherein at least one of said
12 stages comprises a switching network, wherein said
13 switching network comprises a first switching circuit
14 having a first terminal and a second terminal, and a
15 second switching circuit having a first terminal and a
16 second terminal, wherein said first terminal of said
17 second switching circuit connects to said second
18 terminal of said first switching circuit.

19 **9.** The apparatus of claim **8**, wherein said first switching
20 circuit has a first voltage transformation ratio,
21 wherein said second switching circuit has a second
22 voltage transformation ratio, and wherein said first
23 and second voltage transformation ratios are different.

24 **10.** The apparatus of claim **8**, wherein said first switching
25 circuit has a first voltage transformation ratio,
26 wherein said second switching circuit has a second
27 voltage transformation ratio, and wherein said first
28 and second voltage transformation ratios are the same.

- 1 **11.** The apparatus of claim **1**, wherein at least one of said
2 stages comprises a switching network, wherein said
3 switching network comprises first and second switching
4 circuits in series.
- 5 **12.** The apparatus of claim **1**, wherein at least one of said
6 stages comprises a switching network, wherein said
7 switching network comprises first and second switching
8 circuits in series-parallel.
- 9 **13.** The apparatus of claim **1**, wherein said power converter
10 further comprises a third stage in series with said
11 first stage and said second stage, wherein said second
12 stage is between said first stage and said third stage.
- 13 **14.** The apparatus of claim **13**, wherein said first and
14 third stages are switching networks.
- 15 **15.** The apparatus of claim **13**, wherein said first and
16 third stages are regulating networks.
- 17 **16.** The apparatus of claim **1**, wherein said switching
18 network comprises a cascade multiplier.
- 19 **17.** The apparatus of claim **16**, wherein said cascade
20 multiplier is a single-phase cascade multiplier.
- 21 **18.** The apparatus of claim **16**, wherein said cascade
22 multiplier is an asymmetric cascade multiplier.
- 23 **19.** The apparatus of claim **16**, wherein said cascade
24 multiplier is a step-down multiplier.

- 1 **20.** The apparatus of claim 16, wherein said cascade
2 multiplier includes any combination of features
3 recited in claims **17-19**.
- 4 **21.** The apparatus of claim **16**, wherein said cascade
5 multiplier comprises a dual-phase cascade multiplier.
- 6 **22.** The apparatus of claim **21**, wherein said cascade
7 multiplier is a symmetric cascade multiplier.
- 8 **23.** The apparatus of claim **21**, wherein said cascade
9 multiplier comprises parallel pumped capacitors.
- 10 **24.** The apparatus of claim **21**, wherein said cascade
11 multiplier lacks DC capacitors.
- 12 **25.** The apparatus of claim **21**, wherein said apparatus
13 comprises one or more features selected from claims
14 **22-23**.
- 15 **26.** The apparatus of claim **21**, wherein said cascade
16 multiplier is configured to create an auxiliary
17 voltage to drive an additional circuit.
- 18 **27.** The apparatus of claim **26**, further comprising a level
19 shifter, wherein said level shifter is connected to be
20 driven by said auxiliary voltage.
- 21 **28.** The apparatus of claim **27**, further comprising a gate
22 driver, wherein said gate driver is connected to be
23 driven by said auxiliary voltage.
- 24 **29.** The apparatus of claim **1**, wherein said switching
25 network comprises first and second dual-phase cascade
26 multipliers, and a phase node, wherein said first

1 cascade multiplier is asynchronous, wherein said
2 second cascade multiplier is synchronous, wherein said
3 first cascade multiplier is stacked on said second
4 cascade multiplier, and wherein said first and second
5 cascade multipliers share said phase node.

6 **30.** The apparatus of claim **29**, wherein said first and
7 second cascade multipliers operate at the same
8 frequency.

9 **31.** The apparatus of claim **29**, wherein said first and
10 second cascade multipliers operate at different
11 frequencies.

12 **32.** The apparatus of claim **1**, wherein said first stage
13 comprises a cascade multiplier.

14 **33.** The apparatus of claim **1**, wherein said second stage
15 comprises a cascade multiplier.

16 **34.** The apparatus of claim **1**, wherein said regulating
17 network comprises a buck converter.

18 **35.** The apparatus of claim **34**, wherein said buck converter
19 comprises first and second terminals with the same
20 reference voltage.

21 **36.** The apparatus of claim **34**, wherein said buck converter
22 comprises first and second terminals with different
23 reference voltages.

24 **37.** The apparatus of claim **34**, wherein said buck converter
25 comprises a floating node, wherein said floating node
26 is at a floating voltage.

- 1 **38.** The apparatus of claim **37**, wherein said floating node
2 is between two loads.
- 3 **39.** The apparatus of claim **37**, wherein said floating node
4 is between two sources.
- 5 **40.** The apparatus of claim **34**, wherein said buck converter
6 is a three-terminal buck converter.
- 7 **41.** The apparatus of claim **1**, wherein said regulating
8 network comprises a buck-boost converter.
- 9 **42.** The apparatus of claim **1**, wherein said regulating
10 network comprises a boost converter.
- 11 **43.** The apparatus of claim **1**, wherein said regulating
12 network comprises a four-terminal non-inverting buck-
13 boost converter.
- 14 **44.** The apparatus of claim **1**, wherein said switching
15 network comprises a step-down single-phase asymmetric
16 cascade multiplier and wherein said regulating network
17 comprises a boost converter.
- 18 **45.** The apparatus of claim **44**, further comprising
19 selection switches connected to said regulating
20 network for causing said switching network to output a
21 fraction of its normal output voltage.
- 22 **46.** The apparatus of claim **44**, further comprising switches
23 oriented so that cathodes of parasitic diodes
24 corresponding to said switches connect to each other.
- 25 **47.** The apparatus of claim **1**, wherein said regulating
26 network regulates plural wires.

- 1 **48.** The apparatus of claim **1**, wherein said regulating
2 network regulates at most one wire.
- 3 **49.** The apparatus of claim **1**, wherein said regulating
4 network regulates a particular one of plural wires
5 based on an input voltage to said regulating network.
- 6 **50.** The apparatus of claim **1**, wherein said regulating
7 network has plural output ports.
- 8 **51.** The apparatus of claim **1**, wherein said regulating
9 network is a multi-tap boost converter.
- 10 **52.** The apparatus of claim **1**, wherein said switching
11 network comprises a single-phase step-down switched-
12 capacitor circuit, and wherein said regulating network
13 comprises a multi-tap boost converter.
- 14 **53.** The apparatus of claim **1**, wherein said switching
15 network is reconfigurable.
- 16 **54.** The apparatus of claim **1**, wherein said regulating
17 network is reconfigurable.
- 18 **55.** The apparatus of claim **1**, wherein said regulating
19 network and said switching network are both
20 reconfigurable.
- 21 **56.** The apparatus of claim **1**, wherein said switching
22 network comprises a dual-phase switched capacitor
23 circuit.
- 24 **57.** The apparatus of claim **56**, wherein said switched
25 capacitor circuit comprises pump capacitors in series
26 and DC capacitors in series.

- 1 **58.** The apparatus of claim **1**, wherein said switching
2 network comprises a dual-phase switching circuit
3 comprising DC capacitors, and wherein said DC
4 capacitors store charge from said regulating network
5 only during a dead-time transition during which said
6 switching network is between states.
- 7 **59.** The apparatus of claim **1**, wherein said regulating
8 network comprises an inductor, and wherein said
9 inductor promotes adiabatic charge transfer within
10 said switching network.
- 11 **60.** The apparatus of claim **1**, further comprising a
12 magnetic filter connected to said switching network to
13 promote adiabatic charge transfer within said
14 switching network.
- 15 **61.** The apparatus of claim **60**, wherein said magnetic
16 filter is connected between said switching network and
17 a load.
- 18 **62.** The apparatus of claim **60**, wherein said magnetic
19 filter is connected between said switching network and
20 a source.
- 21 **63.** The apparatus of claim **60**, wherein said regulating
22 network and said magnetic filter cooperate to promote
23 adiabatic charge transfer within said switching
24 network.
- 25 **64.** The apparatus of claim **15**, wherein said third stage is
26 operated with a duty cycle that causes said third
27 stage to become a magnetic filter.

- 1 **65.** The apparatus of claim **53**, further comprising a
2 magnetic filter connected to said reconfigurable
3 switching network.
- 4 **66.** The apparatus of claim **54**, further comprising a
5 magnetic filter connected to said switching network.
- 6 **67.** The apparatus of claim **1**, further comprising a circuit
7 connected to said switching network to constrain
8 current flow out of said switching network.
- 9 **68.** The apparatus of claim **1**, further comprising a circuit
10 connected to said switching network to promote
11 adiabatic charge transfer within said switching
12 network.
- 13 **69.** The apparatus of claim **1**, wherein said switching
14 network comprises a two-phase step-down switching
15 network and wherein said regulating network is a step-
16 down network.
- 17 **70.** The apparatus of claim **69**, wherein said switching
18 network comprises a cascade multiplier.
- 19 **71.** The apparatus of claim **70**, wherein said regulating
20 network comprises a buck converter.
- 21 **72.** The apparatus of claim **70**, wherein said regulating
22 network promotes adiabatic charge transfer.
- 23 **73.** The apparatus of claim **1**, wherein said switching
24 network comprises a step-down single-phase asymmetric
25 cascade multiplier and wherein said regulating network
26 comprises a converter that causes voltage to step down.

1 **74.** The apparatus of claim **73**, wherein said first stage is
2 a switching network.

3 **75.** The apparatus of claim **1**, wherein said regulating
4 network comprises a buck converter, wherein said buck
5 converter comprises multiple taps, wherein said buck
6 converter is configured to operate in two operating
7 modes.

8 **76.** The apparatus of claim **75**, wherein said switching
9 network provides first and second voltage rails that,
10 in operation, are maintained at different voltages.

11 **77.** The apparatus of claim **1**, wherein said regulating
12 network comprises a buck converter, wherein said buck
13 converter comprises multiple taps, and wherein said
14 buck converter is configured to operate in three
15 operating modes.

16 **78.** The apparatus of claim **77**, wherein said switching
17 network provides first, second, and third voltage
18 rails that, in operation, are maintained at different
19 voltages.

20 **79.** The apparatus of claim **1**, wherein said switching
21 network comprises a two-phase switched-capacitor
22 circuit and wherein said regulating network is a buck
23 converter.

24 **80.** The apparatus of claim **1**, wherein said regulating
25 network comprises first and second regulating circuits
26 in parallel.

1 **81.** The apparatus of claim **1**, wherein said power converter
2 comprises first and second outputs, wherein, in
3 operation, said first output and second outputs are
4 maintained at corresponding first and second voltage
5 differences, wherein said first voltage different is a
6 difference between a first voltage and a second
7 voltage, and wherein said second voltage difference is
8 a difference between a third voltage and said second
9 voltage.

10 **82.** The apparatus of claim **1**, wherein said regulating
11 network comprises first, second, and third regulating
12 circuits in parallel.

13 **83.** The apparatus of claim **1**, wherein said power converter
14 comprises first second, and third outputs, wherein, in
15 operation, said first, second, and third outputs are
16 maintained at corresponding first second, and third
17 voltage differences, wherein said first voltage
18 different is a difference between a first voltage and
19 a second voltage, wherein said second voltage
20 difference is a difference between a third voltage and
21 said second voltage and wherein said third voltage
22 difference is a difference between a fourth voltage
23 and said second voltage.

24 **84.** The apparatus of claim **1**, wherein said power converter
25 floats above ground.

26 **85.** The apparatus of claim **1**, wherein said power converter
27 has a first terminal and a second terminal, wherein,
28 in operation, a first voltage different is maintained
29 across said first terminal and a second voltage

1 difference is maintained across said second terminal,
2 wherein said first voltage difference is a difference
3 between a first voltage and a second voltage, wherein
4 said second voltage difference is a difference between
5 a third voltage and said second voltage, and wherein
6 said second voltage is variable.

7 **86.** The apparatus of claim **85**, further comprising a third
8 stage, wherein said third stage provides said second
9 voltage.

10 **87.** The apparatus of claim **86**, wherein said third stage
11 comprises a switched-mode power converter.

12 **88.** The apparatus of claim **86**, wherein said third stage
13 comprises a switched capacitor converter.

14 **89.** The apparatus of claim **86**, wherein said third stage
15 comprises a buck converter.

16 **90.** The apparatus of claim **86**, wherein said third stage
17 comprises a cascade multiplier.

18 **91.** The apparatus of claim **1**, wherein said power converter
19 is configured to provide AC output with a non-zero DC
20 offset.

21 **92.** The apparatus of claim **1**, wherein said switching
22 network comprises a reconfigurable asynchronous
23 cascade multiplier, and wherein said regulating
24 network is connected to said switching network to
25 enable said switching network to cause either a step
26 up in voltage or a step down in voltage.

- 1 **93.** The apparatus of claim **92**, wherein said regulating
2 network comprises a four-switch buck-boost converter.
- 3 **94.** The apparatus of claim **1**, wherein said first stage is
4 a switching network, wherein said switching network
5 comprises a cascade multiplier that is reconfigurable,
6 that operates in a single-phase, and that operates
7 asynchronously, and wherein said regulating network
8 comprises a four switch buck boost converter.
- 9 **95.** The apparatus of claim **94**, wherein said regulating
10 network connects to said switching network at a point
11 that enables said switching network to step voltage up
12 or step voltage down.
- 13 **96.** The apparatus of claim **1**, wherein said switching
14 network comprises a cascade multiplier and a charge
15 pump embedded in said cascade multiplier.
- 16 **97.** The apparatus of claim **96**, wherein said embedded
17 charge pump is reconfigurable.
- 18 **98.** The apparatus of claim **96**, wherein said embedded
19 charge pump is a fractional charge pump.
- 20 **99.** The apparatus of claim **96**, wherein said embedded
21 charge pump operates in multiple modes, wherein each
22 corresponds to a voltage transformation ratio.
- 23 **100.** The apparatus of claim **96**, wherein said regulating
24 network comprises a two-phase boost converter.
- 25 **101.** The apparatus of claim **96**, wherein said cascade
26 multiplier comprises a reconfigurable two-phase
27 asynchronous step-down cascade multiplier.

1 **102.** The apparatus of claim **1**, wherein said power converter
2 further comprises a third stage in series with said
3 first stage and said second stage, wherein said second
4 stage is between said first stage and said third stage,
5 wherein said first stage and said third stage are
6 switching networks, wherein said regulating circuit
7 comprises a buck converter, wherein said first
8 switching network comprises a single-phase
9 asynchronous step-up cascade multiplier, and wherein
10 said second switching network comprises a single-phase
11 synchronous step-up cascade multiplier.

12 **103.** The apparatus of claim **102**, further comprising a
13 stabilizing capacitor at an output of said regulating
14 network.

15 **104.** The apparatus of claim **1**, wherein said power converter
16 further comprises a third stage in series with said
17 first stage and said second stage, wherein said second
18 stage is between said first stage and said third stage,
19 wherein said first stage and said third stage are
20 switching networks, wherein said regulating circuit
21 comprises a buck-boost converter, wherein said first
22 switching network comprises a single-phase
23 asynchronous step-up cascade multiplier, and wherein
24 said second switching network comprises a single-phase
25 synchronous step-up cascade multiplier.

26 **105.** The apparatus of claim **102**, further comprising a
27 stabilizing capacitor at an output of said regulating
28 network.

1 **106.** The apparatus of claim **1**, wherein said power converter
2 further comprises a third stage in series with said
3 first stage and said second stage, wherein said second
4 stage is between said first stage and said third stage,
5 wherein said first stage and said third stage are
6 regulating networks, wherein said first stage
7 comprises a boost converter, wherein said third stage
8 comprises a buck converter, and wherein said switching
9 network comprises first and second cascade multipliers
10 having equal numbers of stages.

11 **107.** The apparatus of claim **106**, further comprising a phase
12 pump, wherein said first and second cascade
13 multipliers share said phase pump.

14 **108.** The apparatus of claim **106**, wherein said first and
15 second cascade multipliers operate 180 degrees out of
16 phase.

17 **109.** The apparatus of claim **106**, wherein said cascade
18 multipliers comprise corresponding first and second
19 switch stacks, and wherein an output of said switching
20 network is a voltage difference between a top of said
21 first switch stack and a top of said second switch
22 stack.

23 **110.** The apparatus of claim **1**, wherein said power converter
24 further comprises a third stage in series with said
25 first stage and said second stage, wherein said second
26 stage is between said first stage and said third stage,
27 wherein said first stage and said third stage are
28 regulating networks, wherein said first stage
29 comprises a three-level boost converter, wherein said

1 third stage comprises a buck converter, and wherein
2 said switching network comprises first and second
3 cascade multipliers having unequal numbers of stages.

4 **111.** The apparatus of claim **1**, wherein said switching
5 network receives current that has a first portion and
6 a second portion, wherein said first portion comes
7 from said regulating network, wherein said second
8 portion bypasses said regulating network, and wherein
9 said second portion is greater than said first portion.

10 **112.** The apparatus of claim **1**, wherein said power converter
11 further comprises a third stage in series with said
12 first stage and said second stage, wherein said second
13 stage is between said first stage and said third stage,
14 wherein said first stage is a first regulating network,
15 wherein said third stage is a second regulating
16 network, wherein said first stage comprises a boost
17 converter, wherein said third stage comprises a buck
18 converter, and wherein said switching network
19 comprises first and second cascade multipliers having
20 unequal numbers of stages.

21 **113.** The apparatus of claim **112**, wherein said second stage
22 comprises an additional inductor connected to said
23 first stage.

24 **114.** The apparatus of claim **1**, further comprising a third
25 stage, wherein said first stage comprises a regulating
26 network, wherein said third stage comprises a
27 regulating network, wherein said power converter
28 provides a load with a first voltage difference,
29 wherein said first stage provides a second voltage

1 difference to said second stage, wherein said second
2 stage provides a third voltage difference to said
3 third stage, wherein said first voltage difference is
4 a voltage difference between a first voltage and a
5 second voltage, wherein said second voltage difference
6 is a voltage difference between a third voltage and a
7 fourth voltage, wherein said third voltage difference
8 is a voltage difference between a fifth voltage and a
9 sixth voltage, wherein said fourth voltage differs
10 from said second voltage, and wherein said sixth
11 voltage differs from said second voltage.

12 **115.** The apparatus of claim **114**, wherein said second stage
13 comprises a reconfigurable switching network.

14 **116.** The apparatus of claim **1**, wherein said first stage
15 comprises a switching network, wherein said switching
16 network comprises a reconfigurable dual phase cascade
17 multiplier, wherein cascade multiplier comprises an
18 embedded inductor, said embedded inductor being
19 configured to promote adiabatic charge transfer
20 between capacitors in said cascade multiplier.

21 **117.** The apparatus of claim **116**, wherein said second stage
22 comprises a zeta converter.

23 **118.** The apparatus of claim **116**, wherein said inductor is
24 embedded at a location through which a constant
25 current passes.

26 **119.** The apparatus of claim **116**, wherein said cascade
27 multiplier comprises a phase pump and wherein said
28 inductor is embedded at said phase pump.

1 **120.** The apparatus of claim **116**, wherein said cascade
2 multiplier comprises pump capacitors, and wherein said
3 inductor is embedded at a location that maximizes the
4 number of paths that pass between said inductor and a
5 pump capacitor.

6 **121.** The apparatus of claim **1**, wherein said switching
7 network comprises a dual-phase cascade multiplier with
8 pump capacitors in series.

9 **122.** The apparatus of claim **121**, wherein said switching
10 network has a variable transfer function.

11 **123.** The apparatus of claim **121**, wherein said switching
12 network comprises a phase pump, wherein said phase
13 pump comprises an embedded charge pump.

14 **124.** The apparatus of claim **123**, wherein said phase pump
15 said embedded charge pump comprises a plurality of
16 switch sets, a plurality of pump capacitors, and a
17 controller, wherein said controller is configured to
18 operate said switch sets to cause transitions between
19 a first operating mode and a second operating mode,
20 each of which corresponds to a transfer function for
21 said cascade multiplier.

22 **125.** The apparatus of claim **124**, wherein said controller
23 causes is configured to operate said switch sets so as
24 to cause said embedded controller to cause said
25 cascade multiplier to have a transfer function in
26 which the cascade multiplier provides a voltage gain.

27 **126.** The apparatus of claim **124**, wherein said controller
28 causes is configured to operate said switch sets so as

1 to cause said embedded controller to cause said
2 cascade multiplier to have a transfer function in
3 which the cascade multiplier provides a voltage
4 attenuation.

5 **127.** The apparatus of claim **44**, wherein said first stage is
6 a regulating network.

7

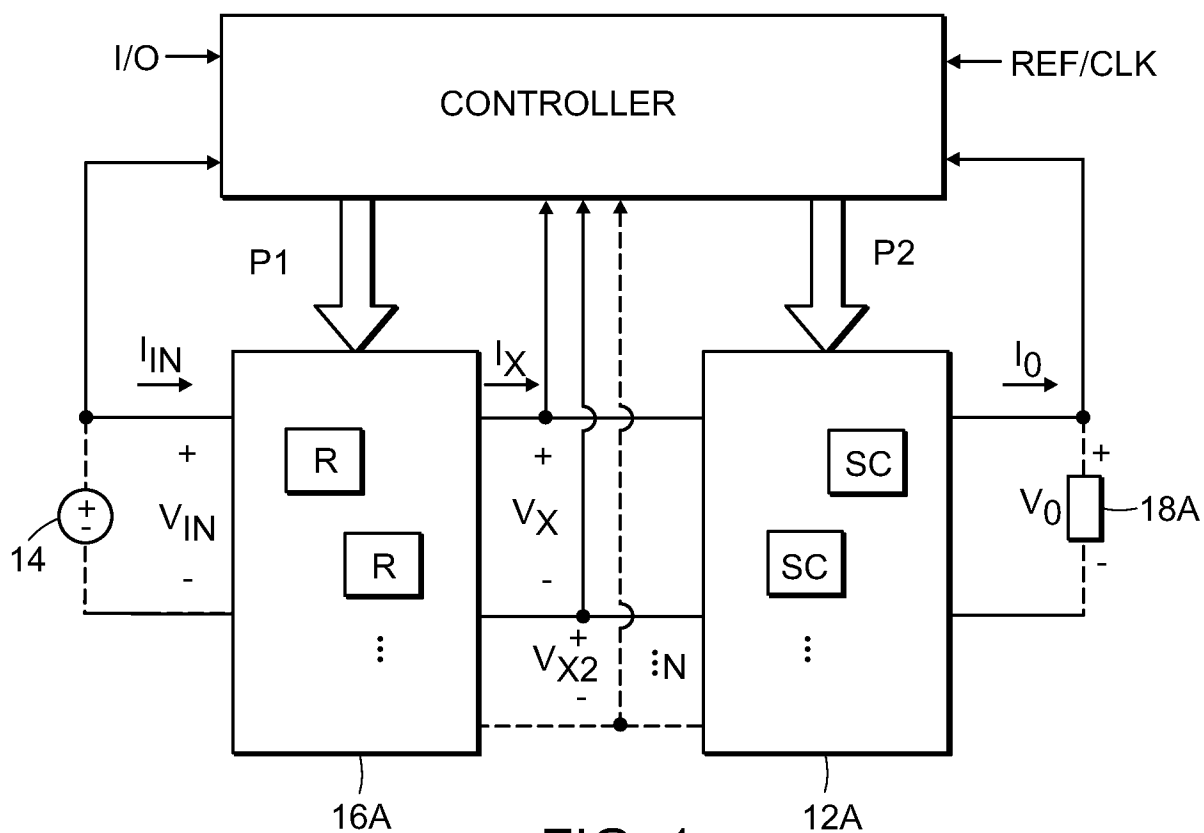


FIG. 1

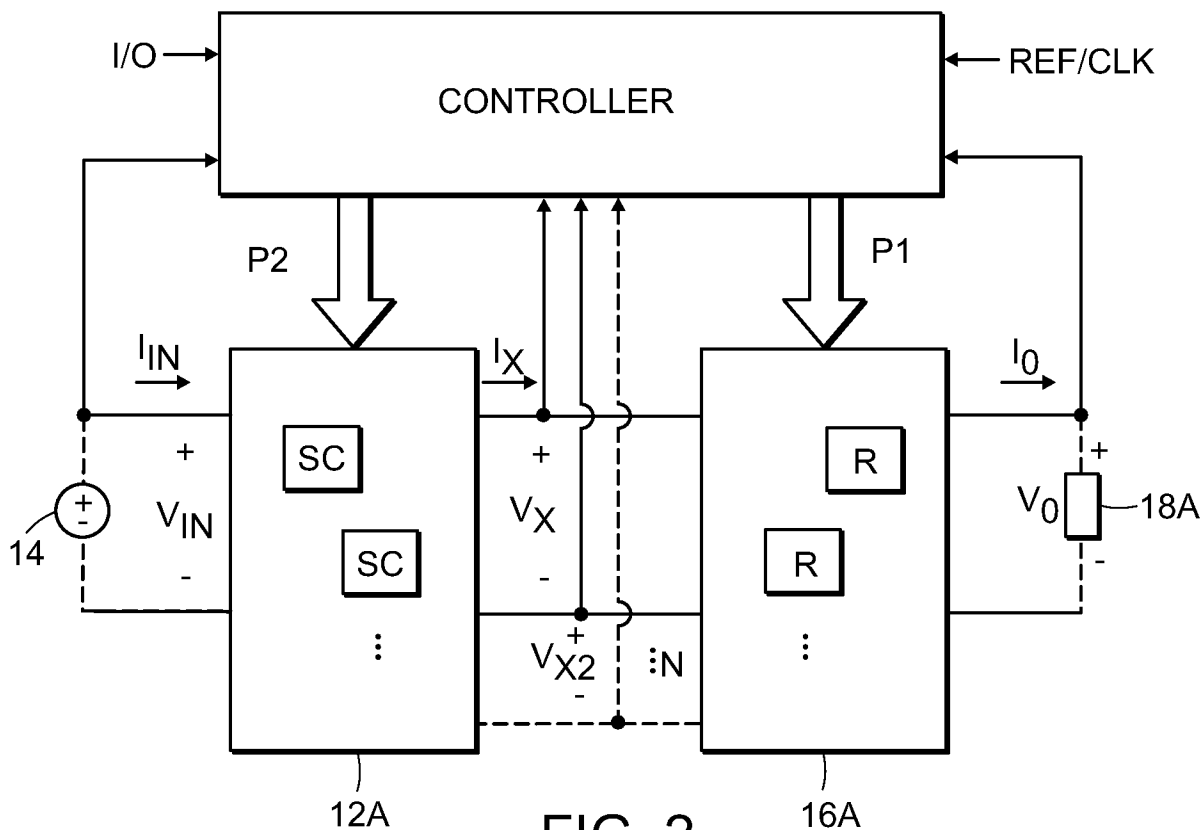


FIG. 2

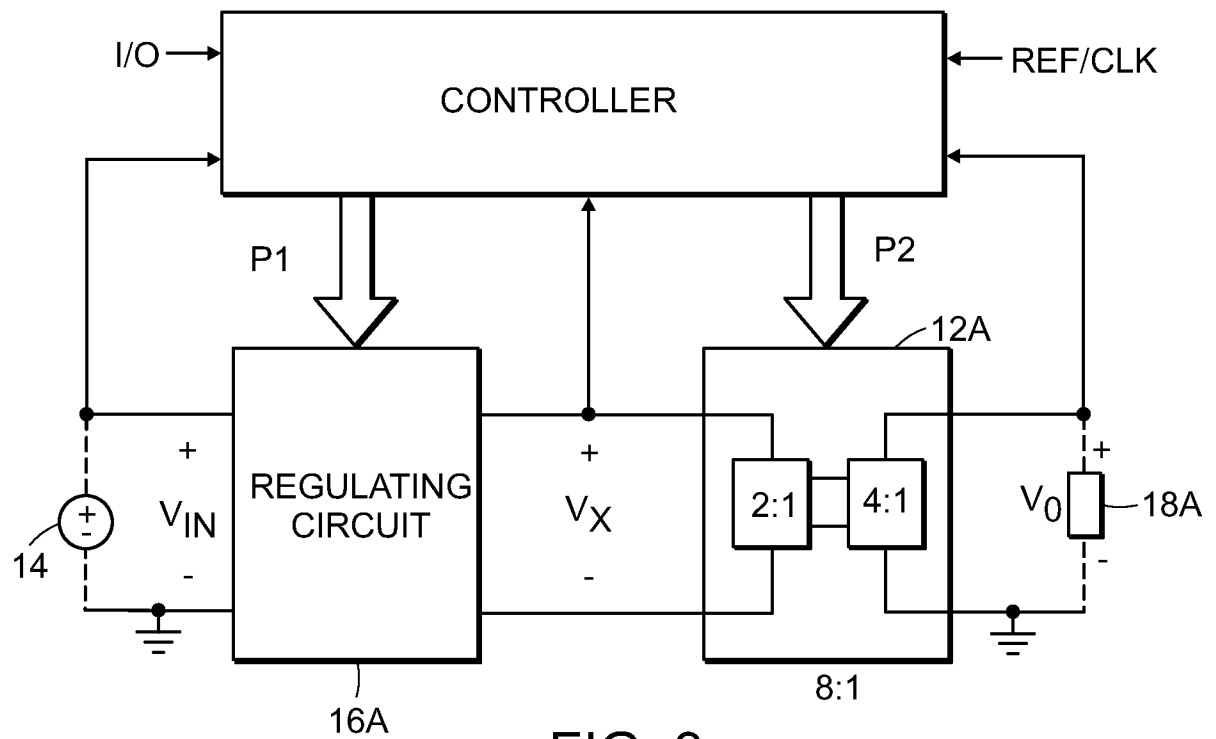


FIG. 3

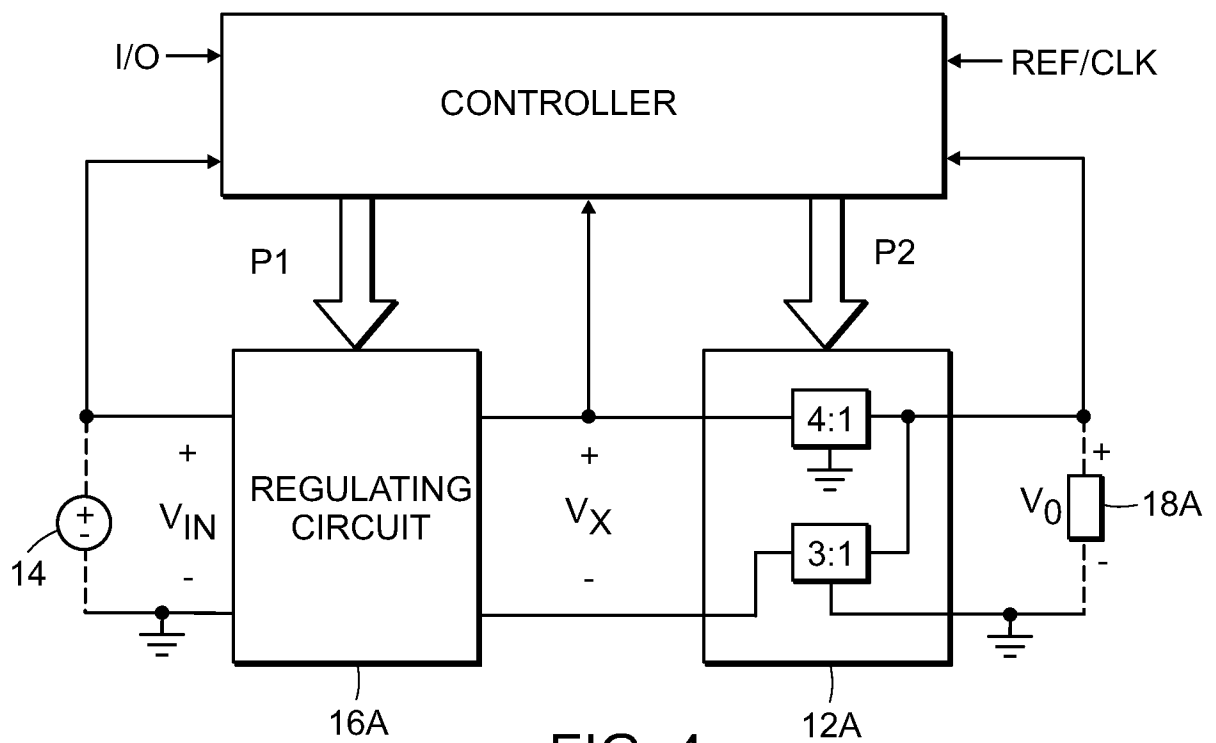


FIG. 4

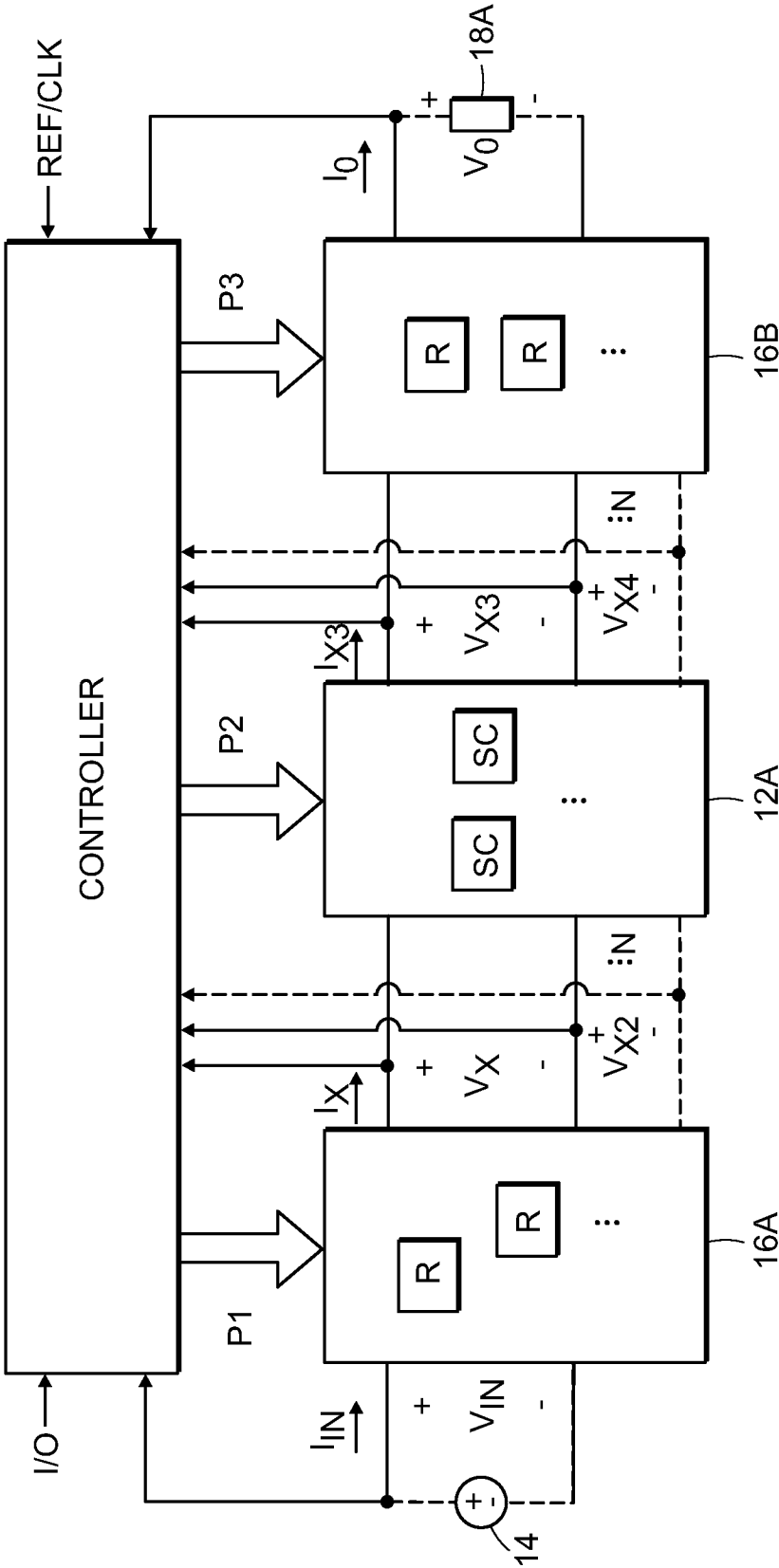


FIG. 5

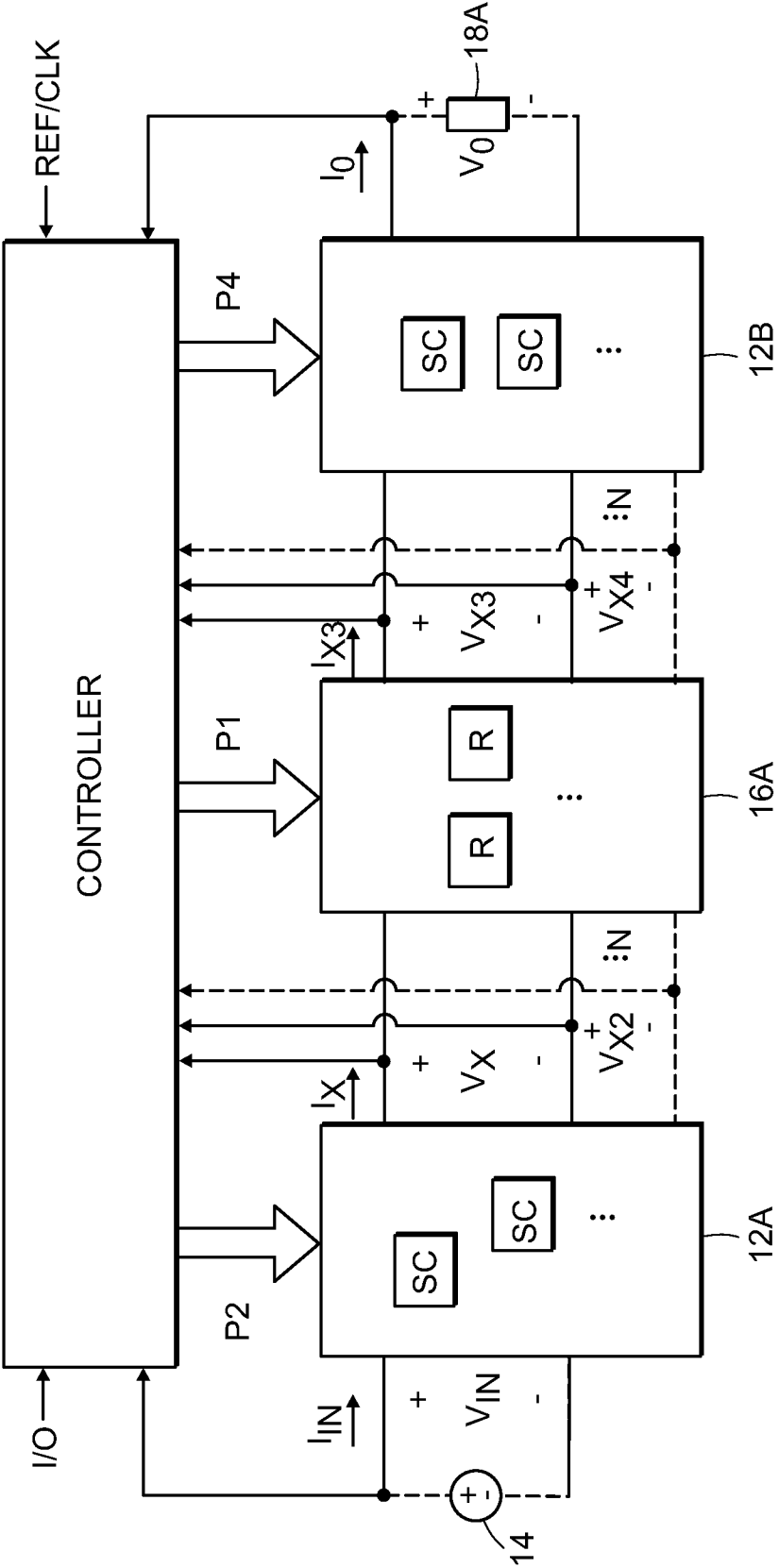


FIG. 6

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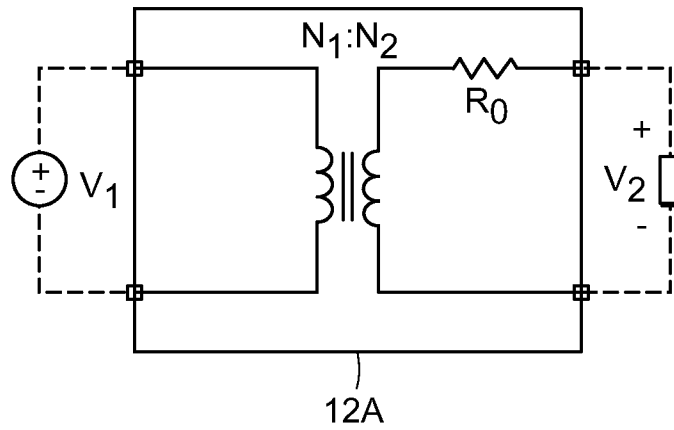


FIG. 7

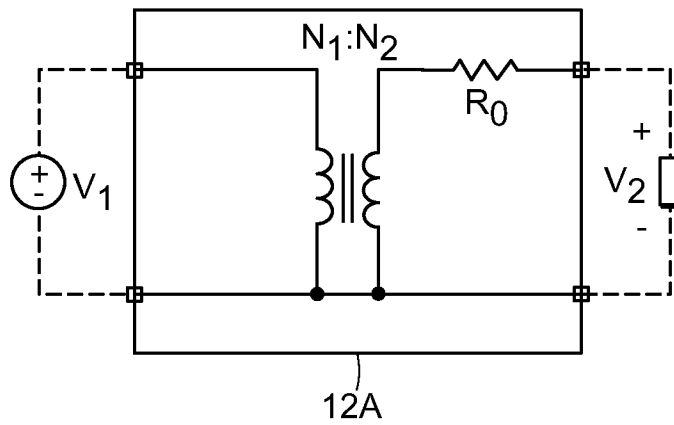


FIG. 8

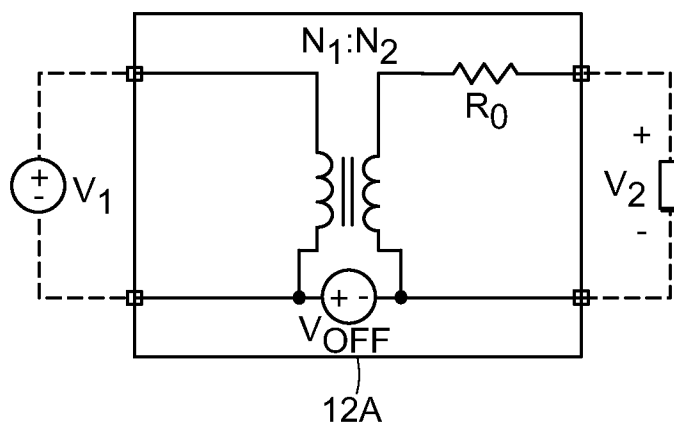


FIG. 9

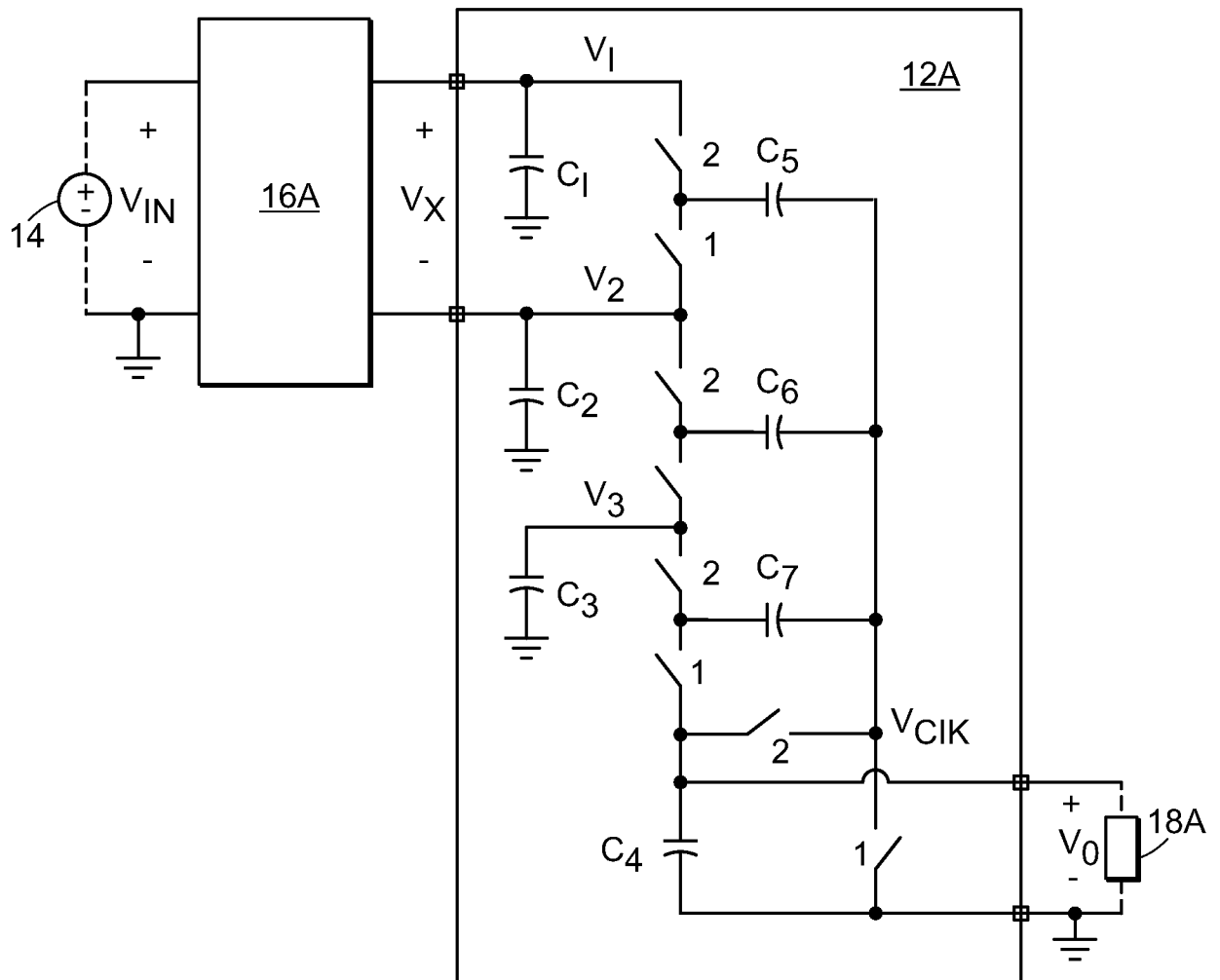


FIG. 10

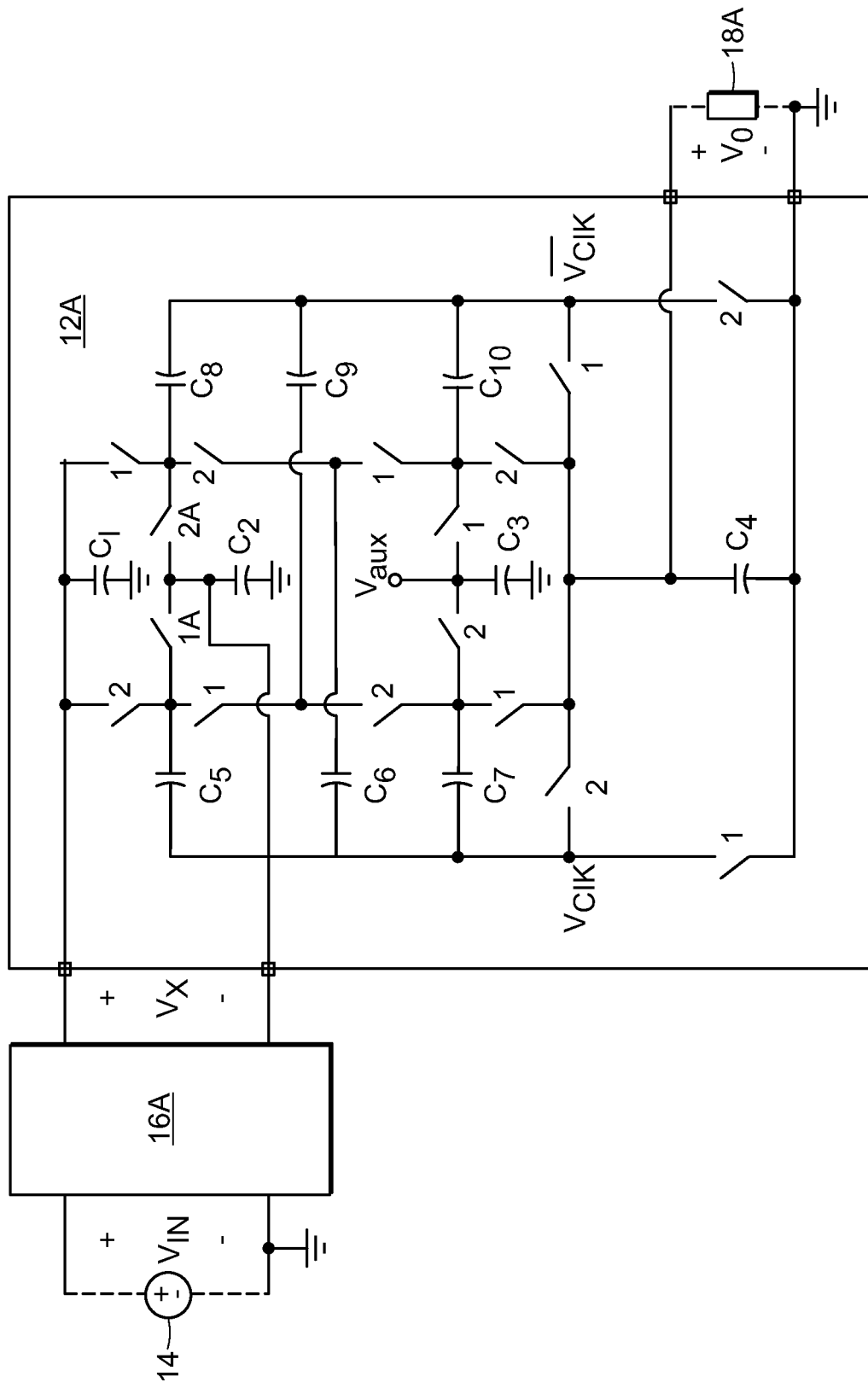


FIG. 11

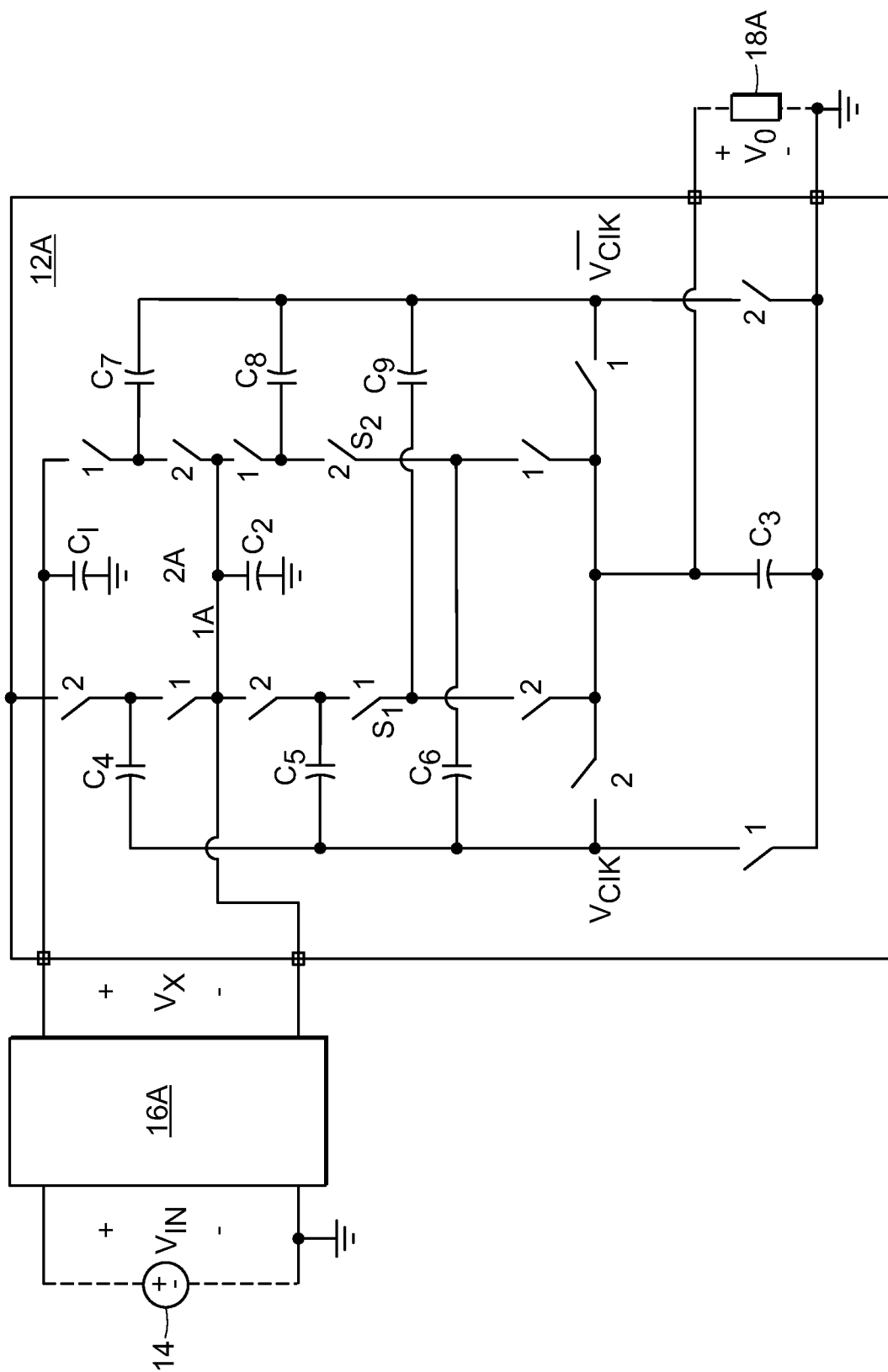


FIG. 12

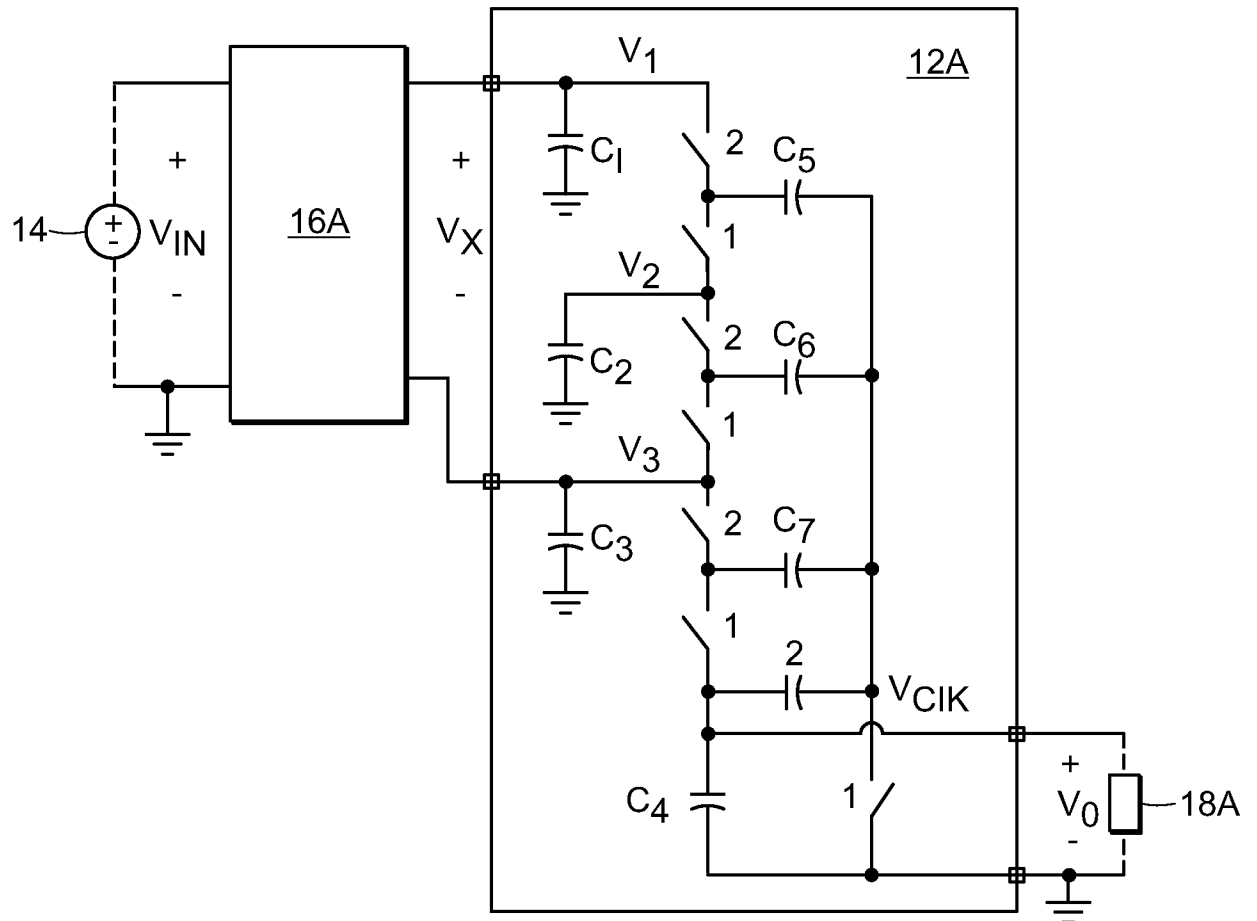


FIG. 13A

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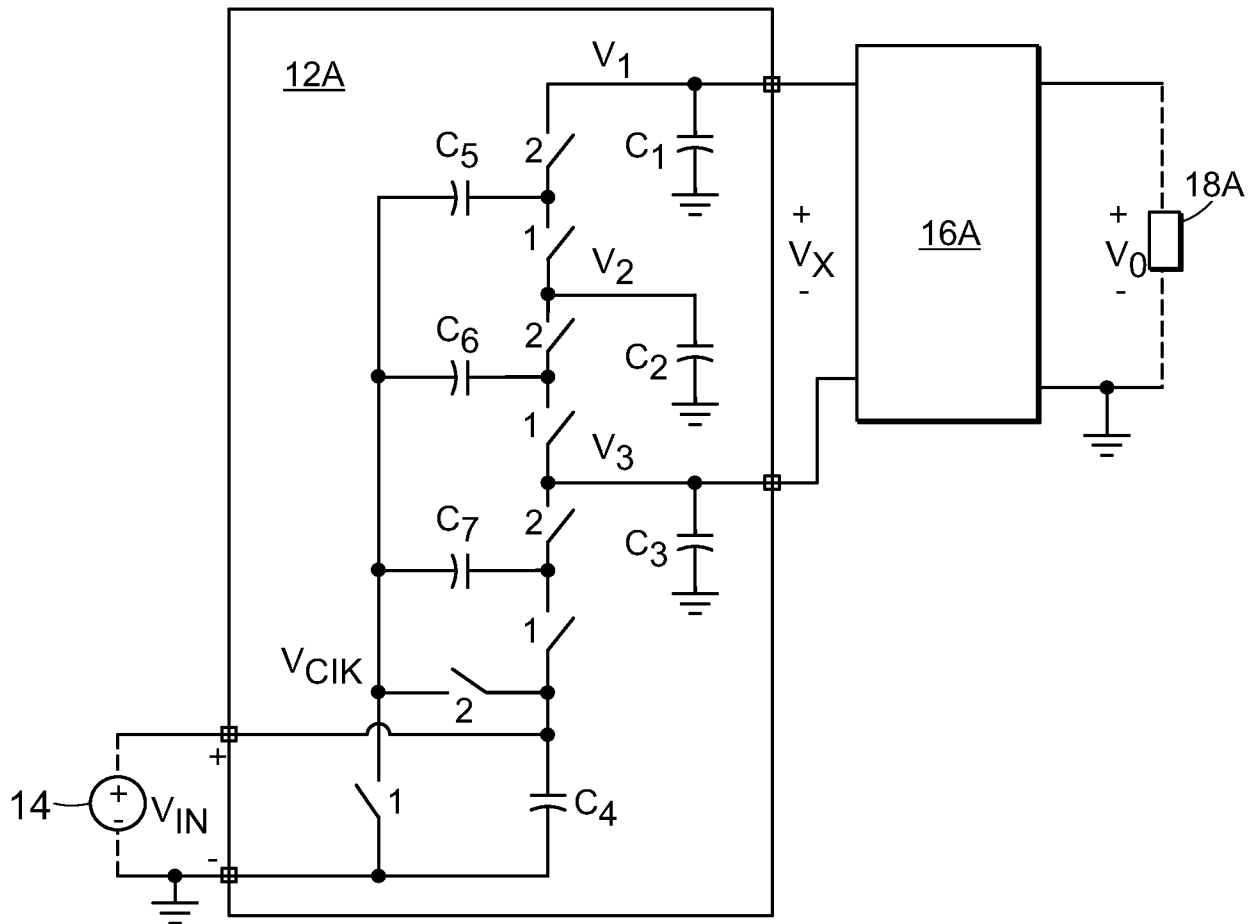


FIG. 13B

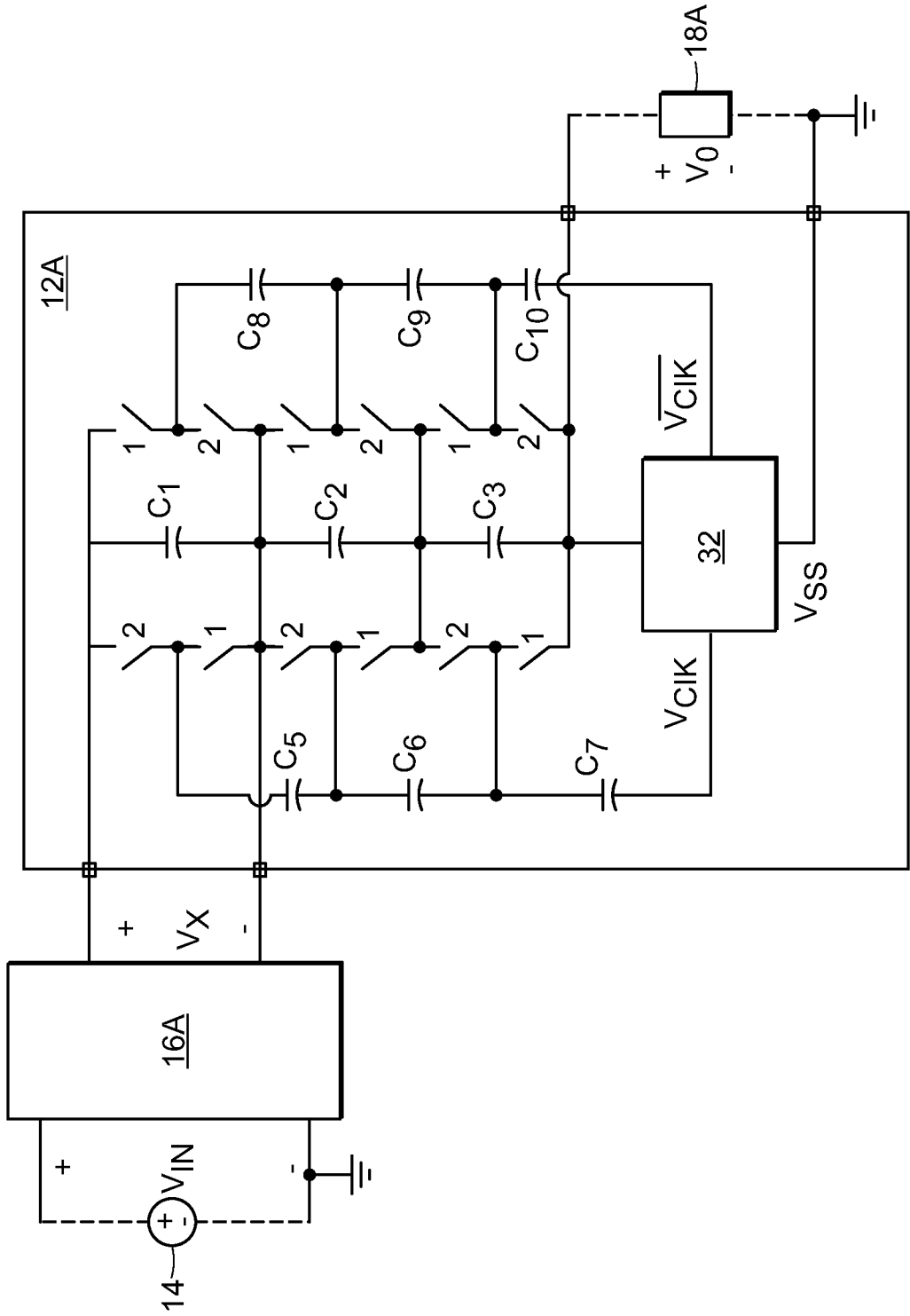


FIG. 14A

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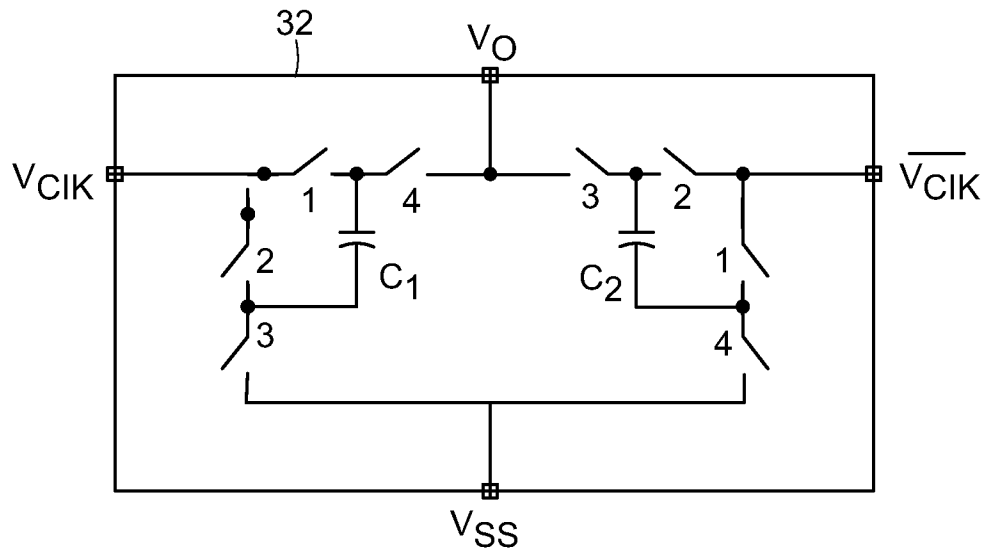


FIG. 14B

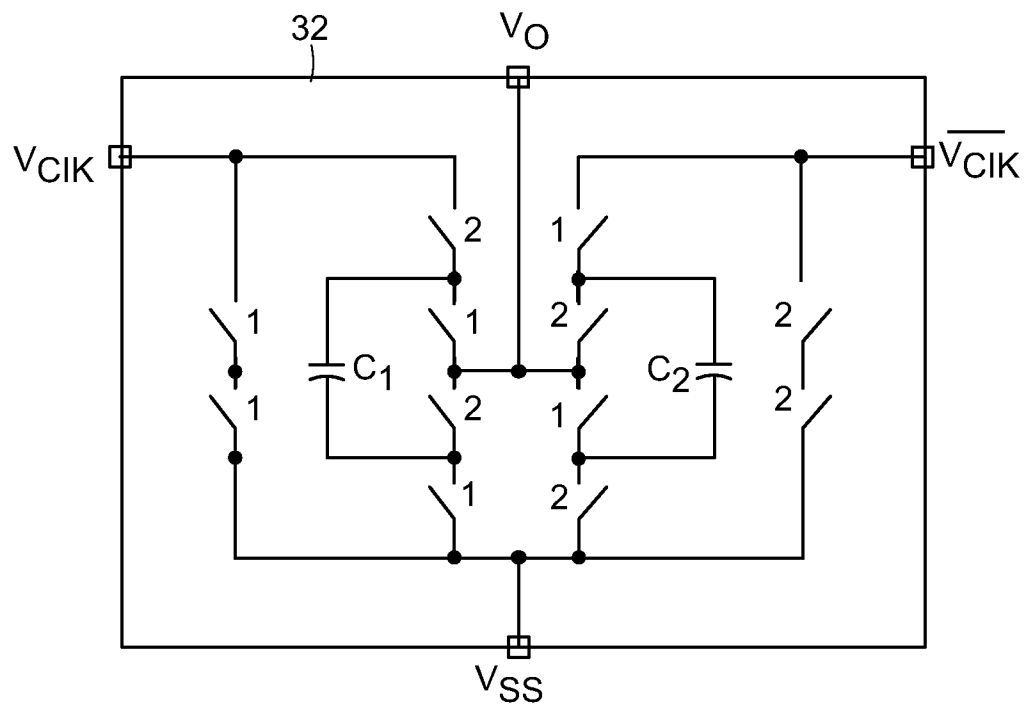


FIG. 14C

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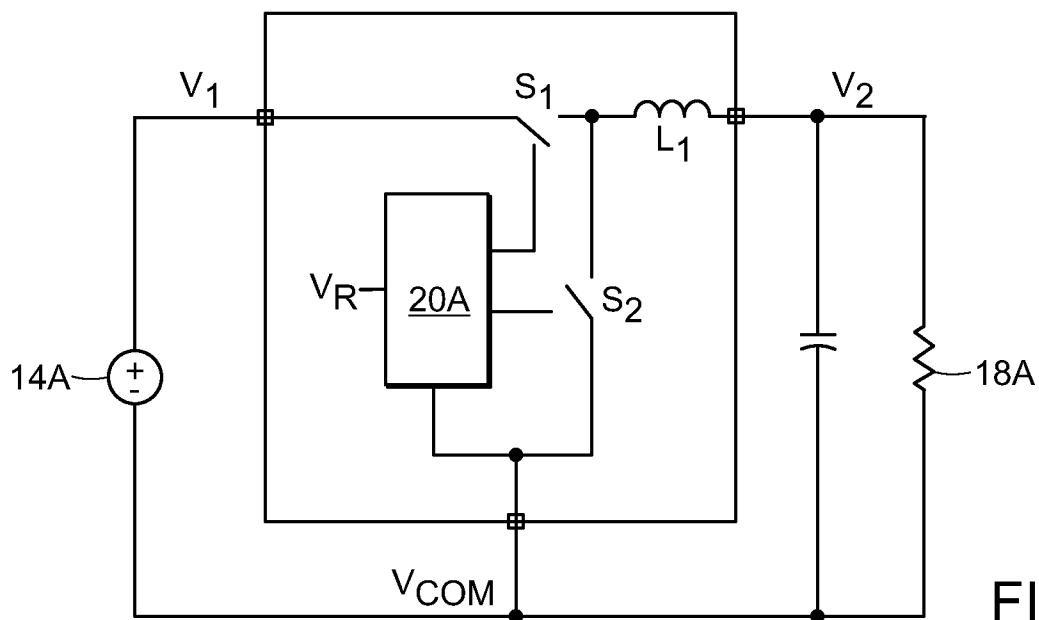


FIG. 15A

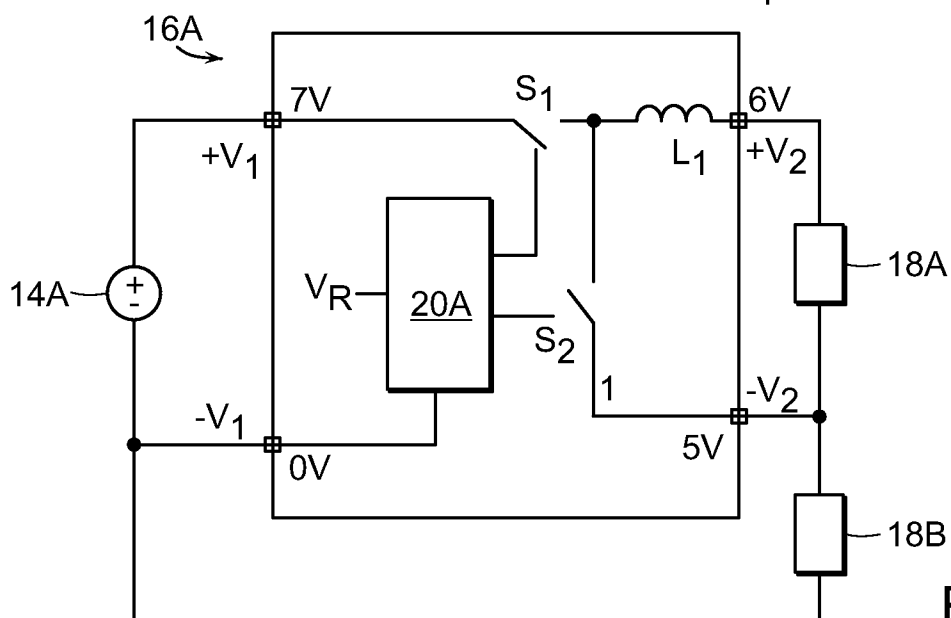


FIG. 15B

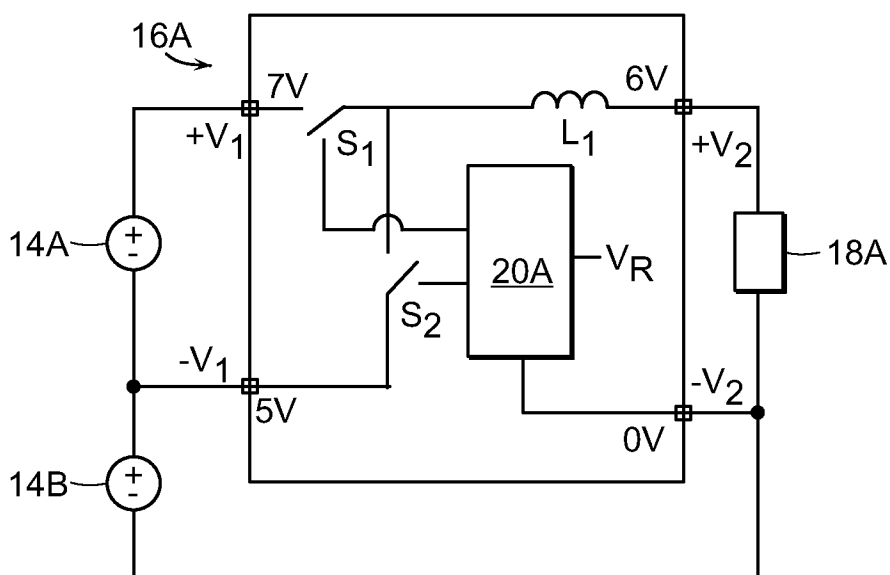
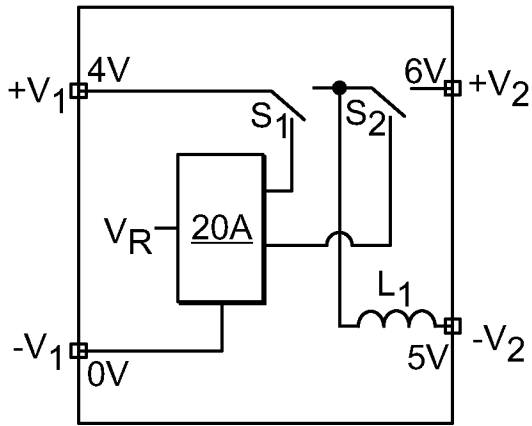


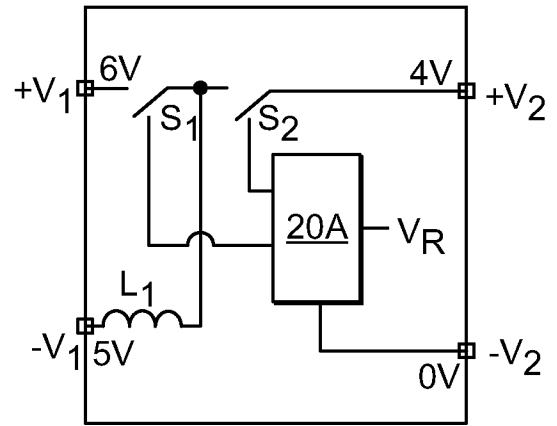
FIG. 15C

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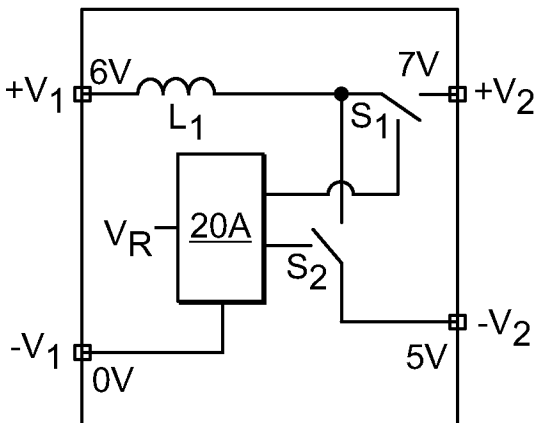
16A

FIG. 16A



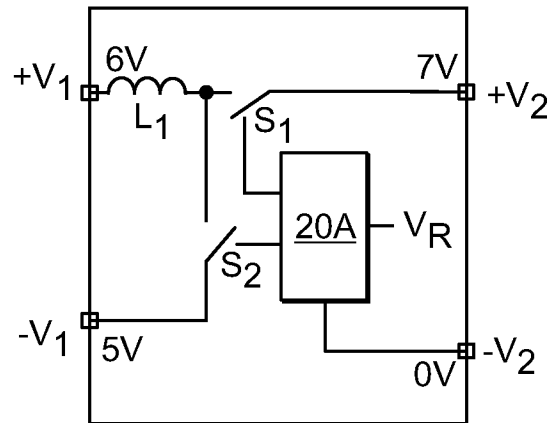
16B

FIG. 16B



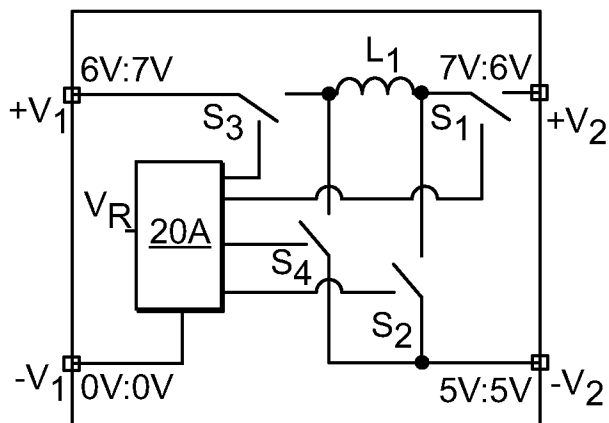
17A

FIG. 17A



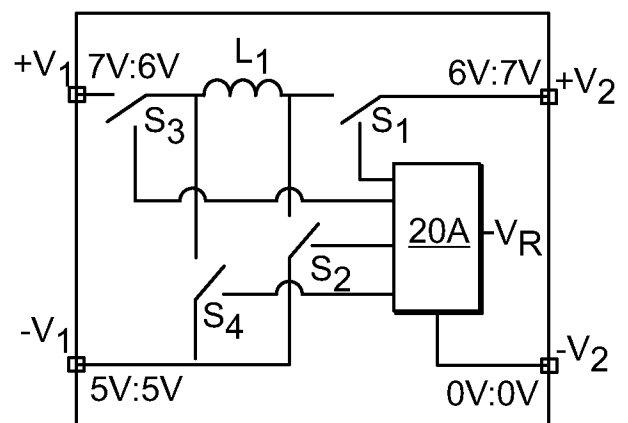
17B

FIG. 17B



18A

FIG. 18A



18B

FIG. 18B

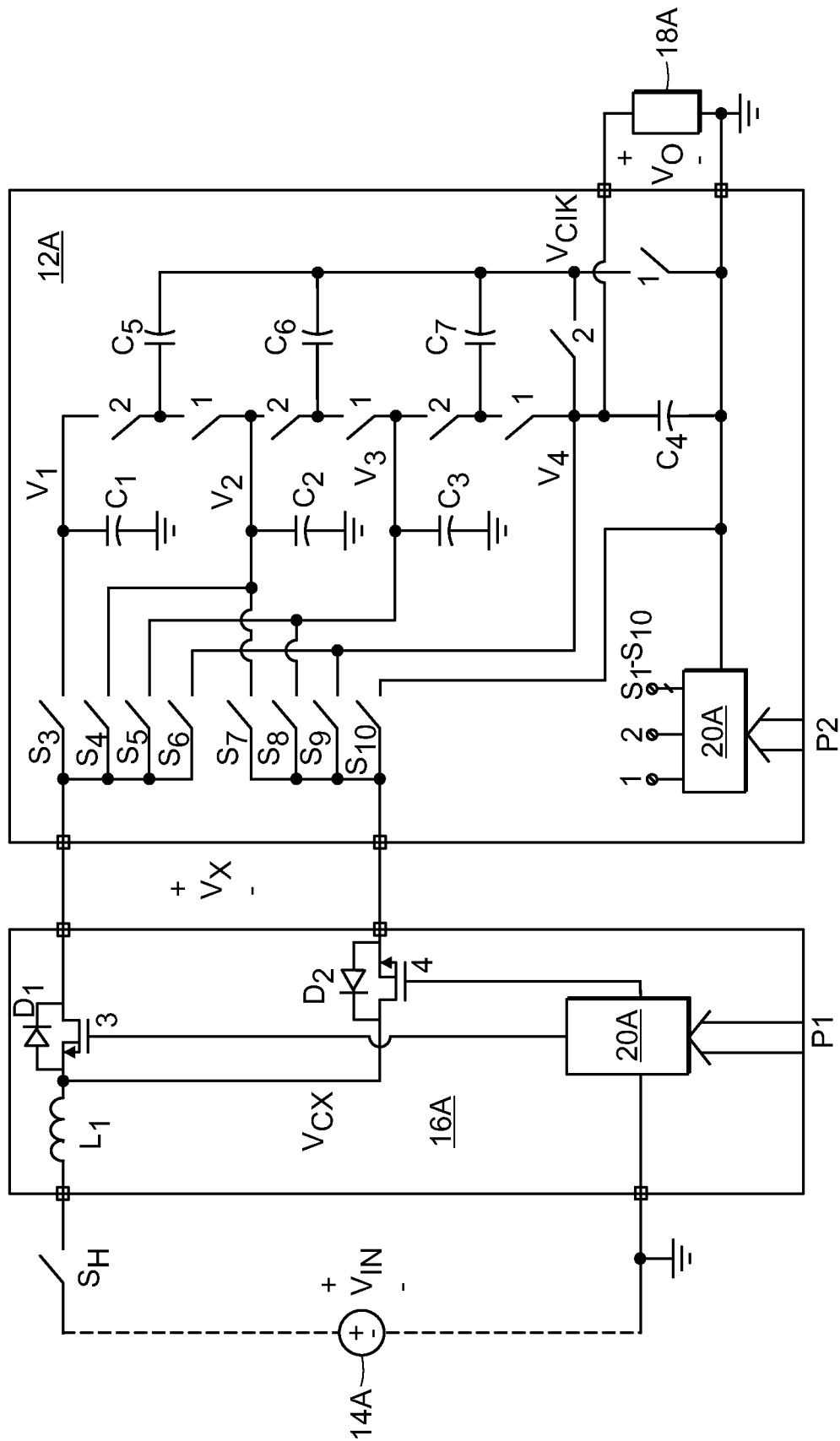


FIG. 19

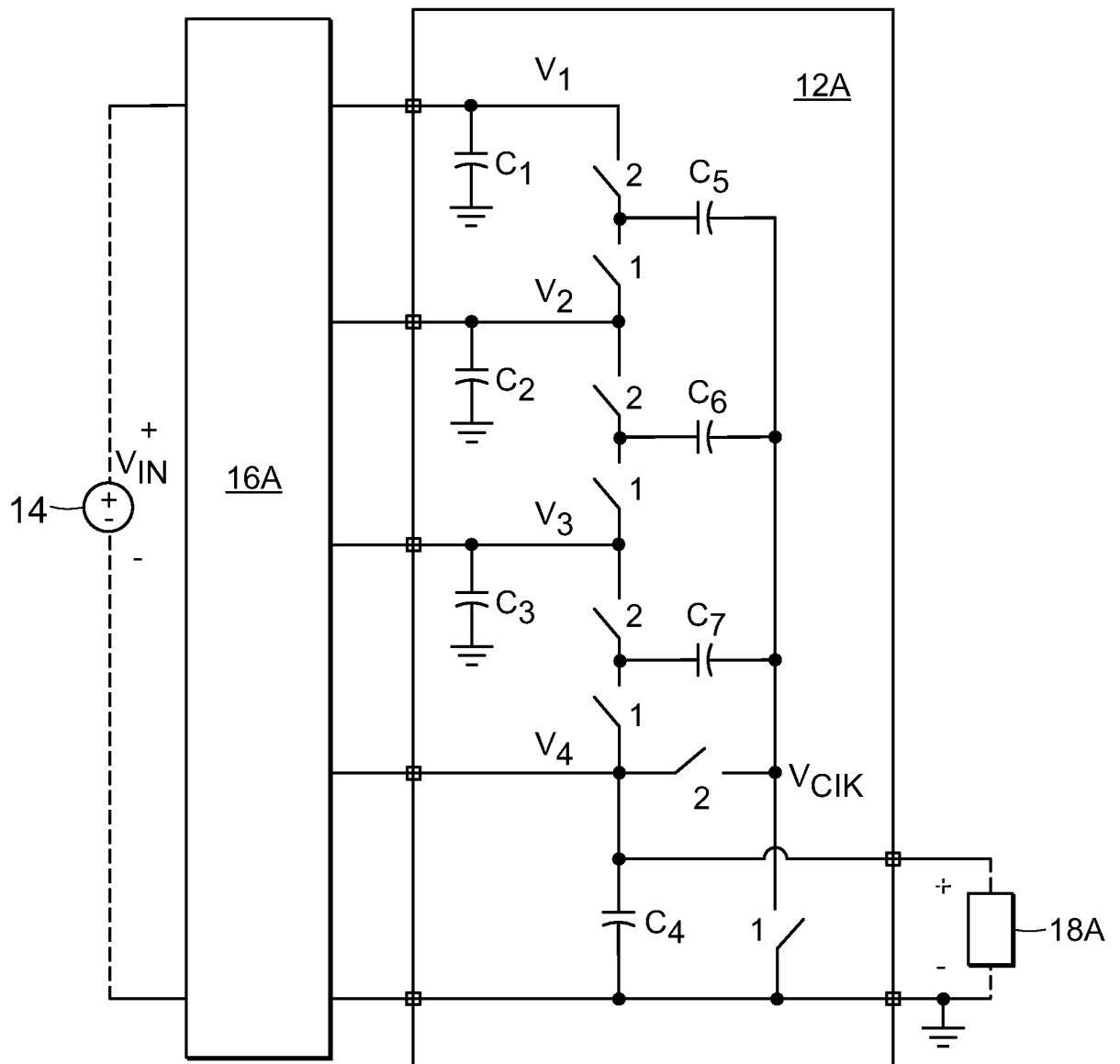
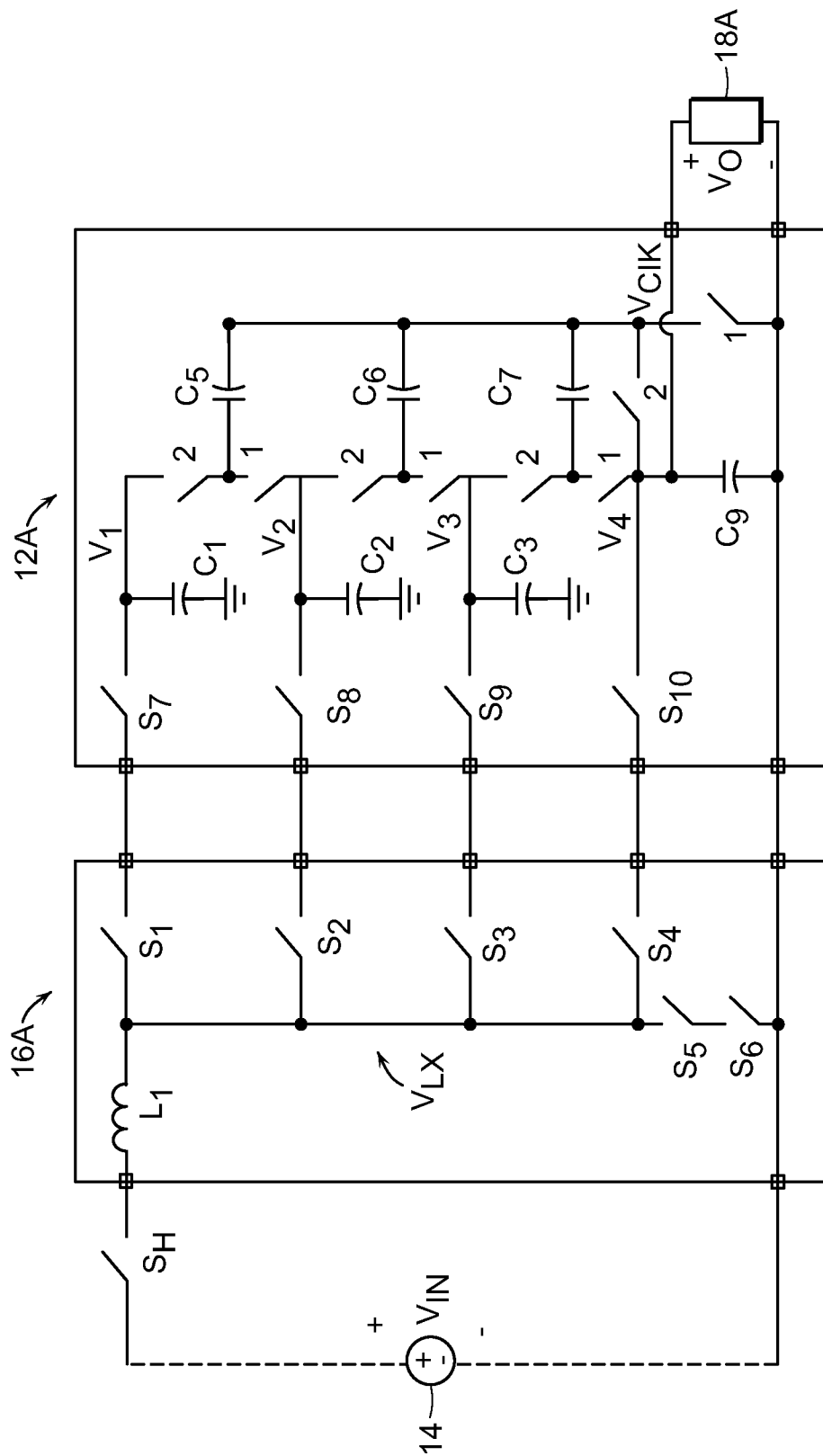
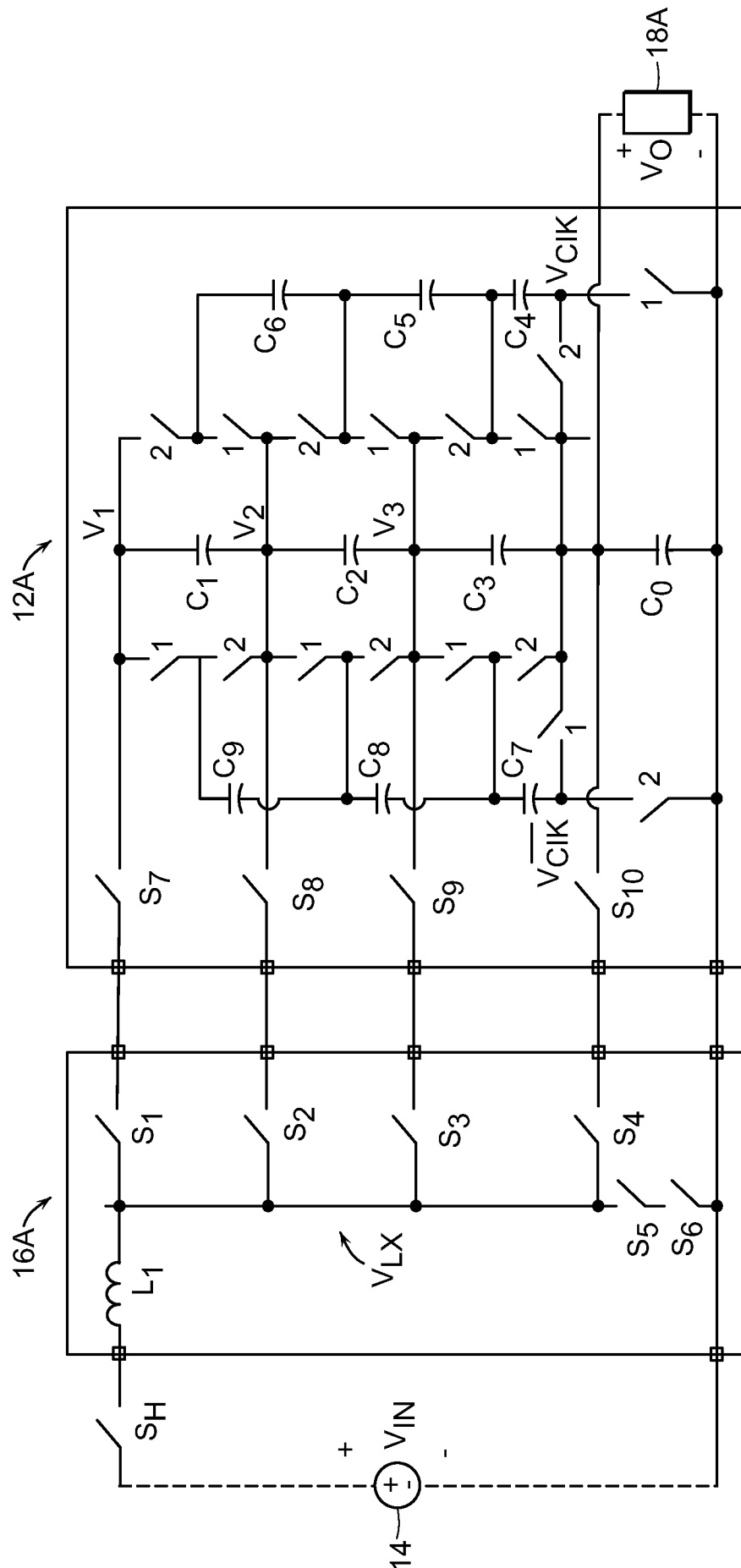


FIG. 20





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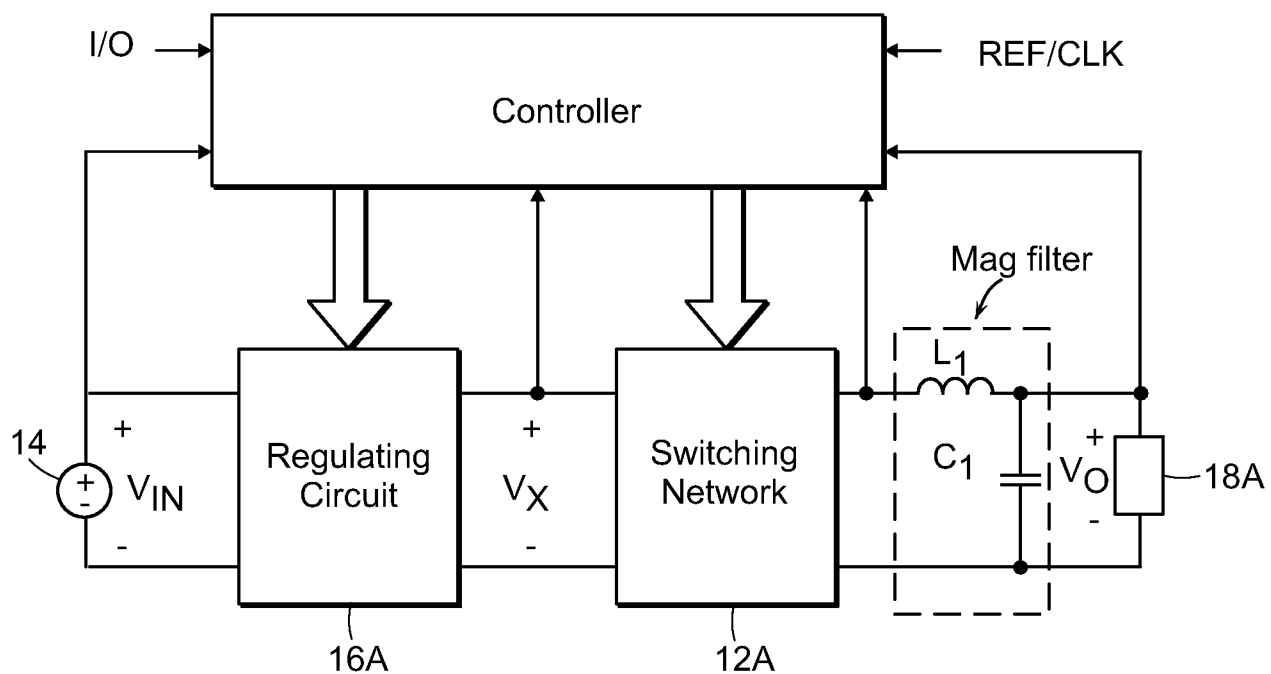


FIG. 23

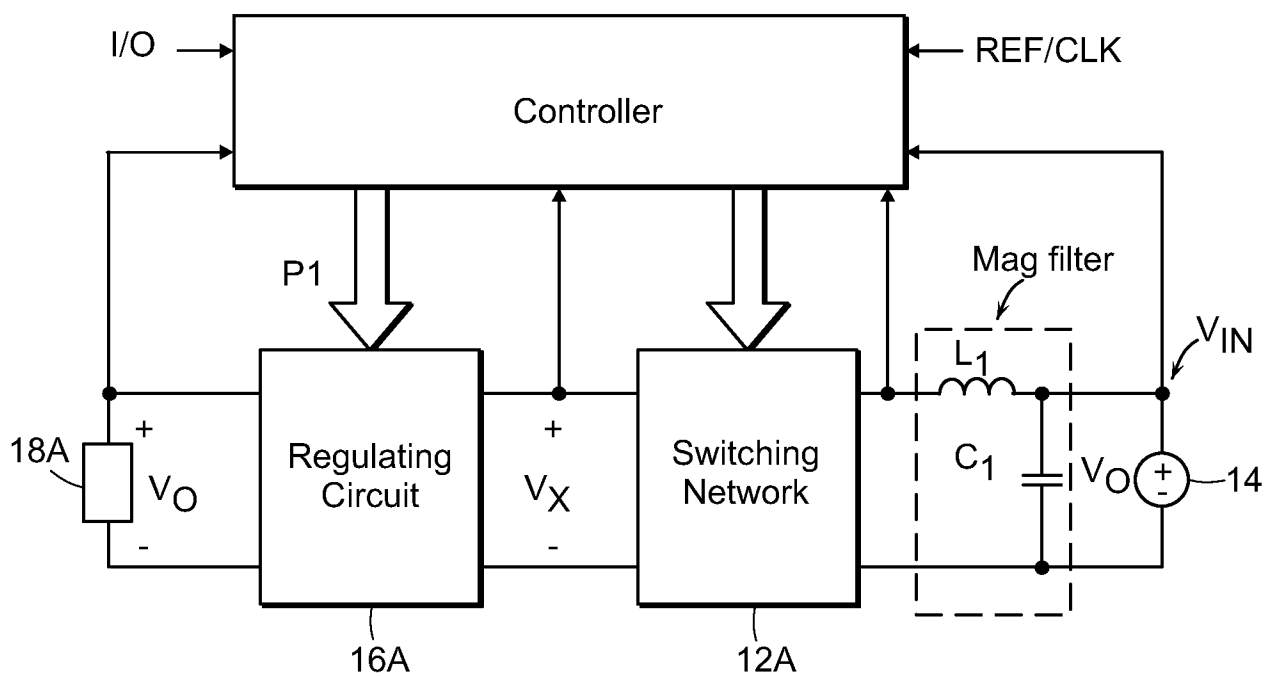


FIG. 24

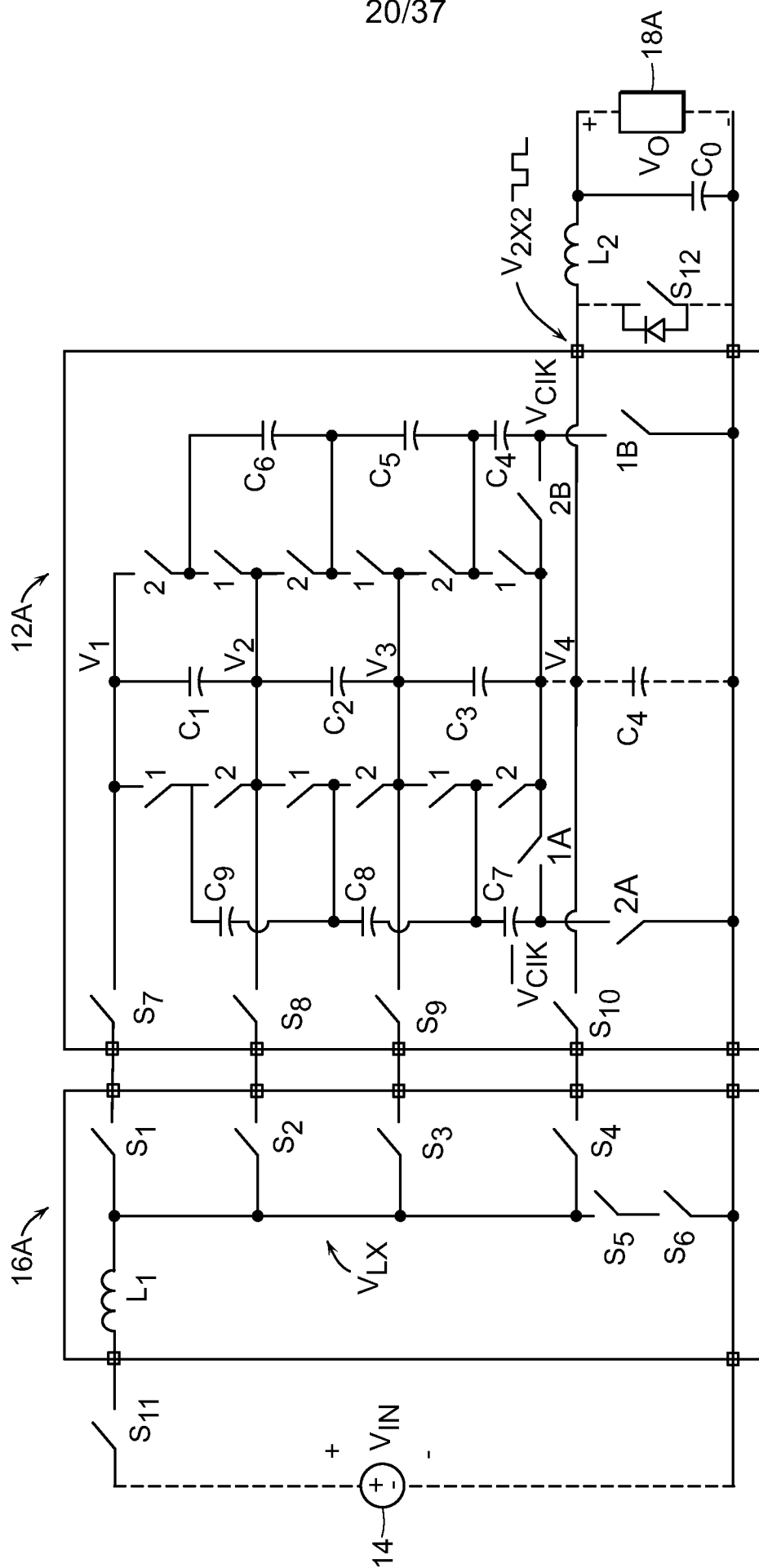


FIG. 25

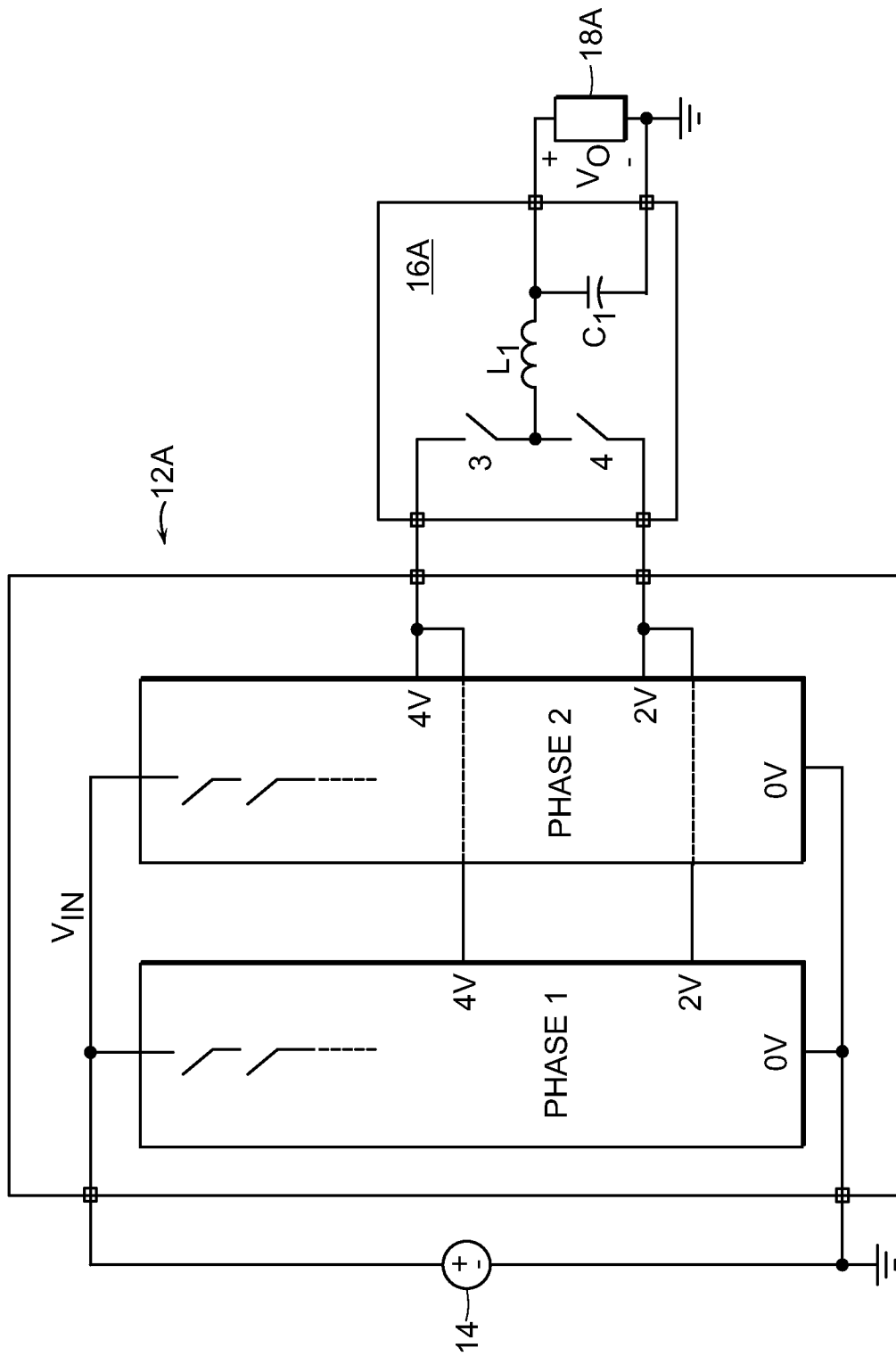


FIG. 26

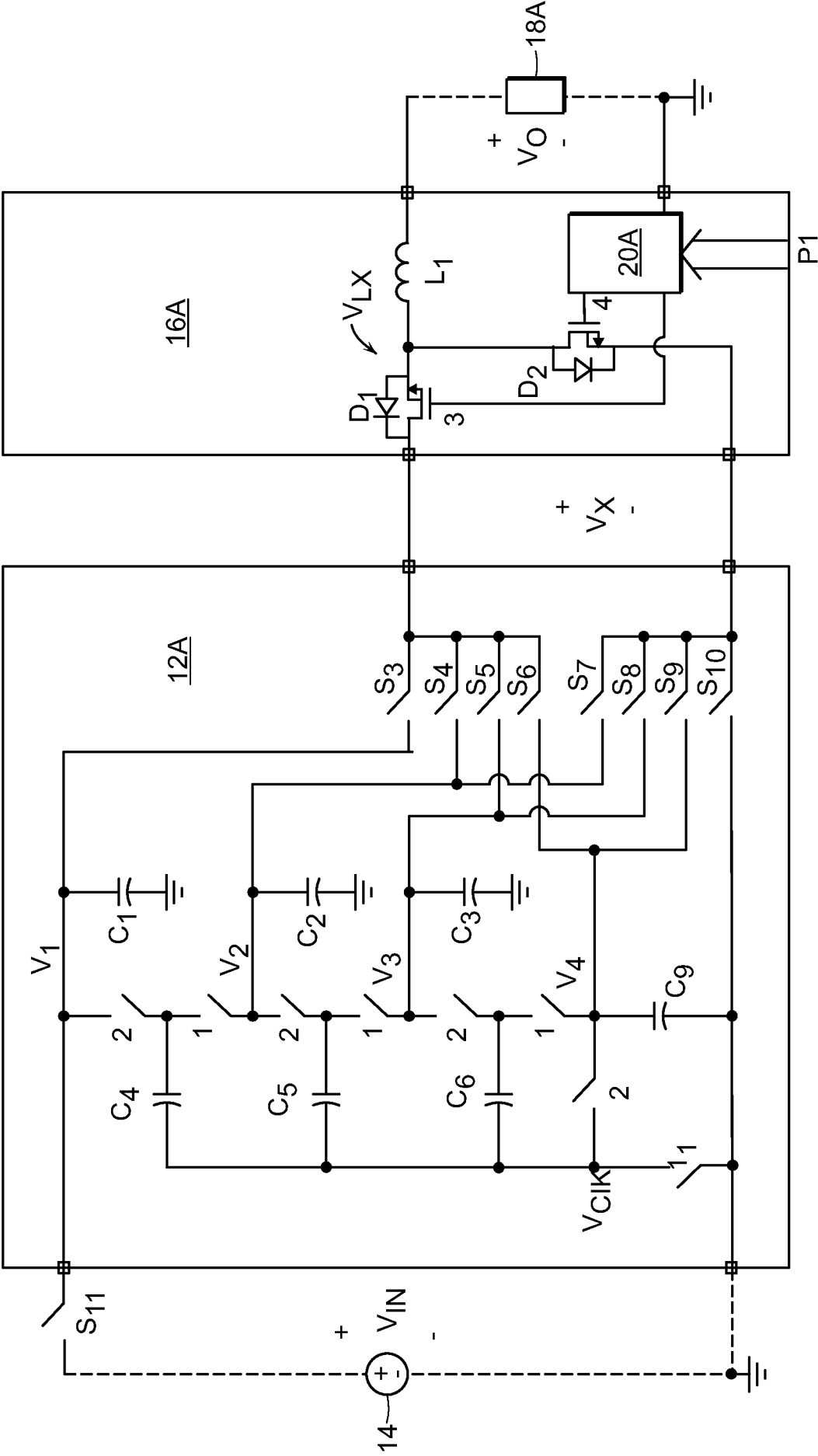


FIG. 27

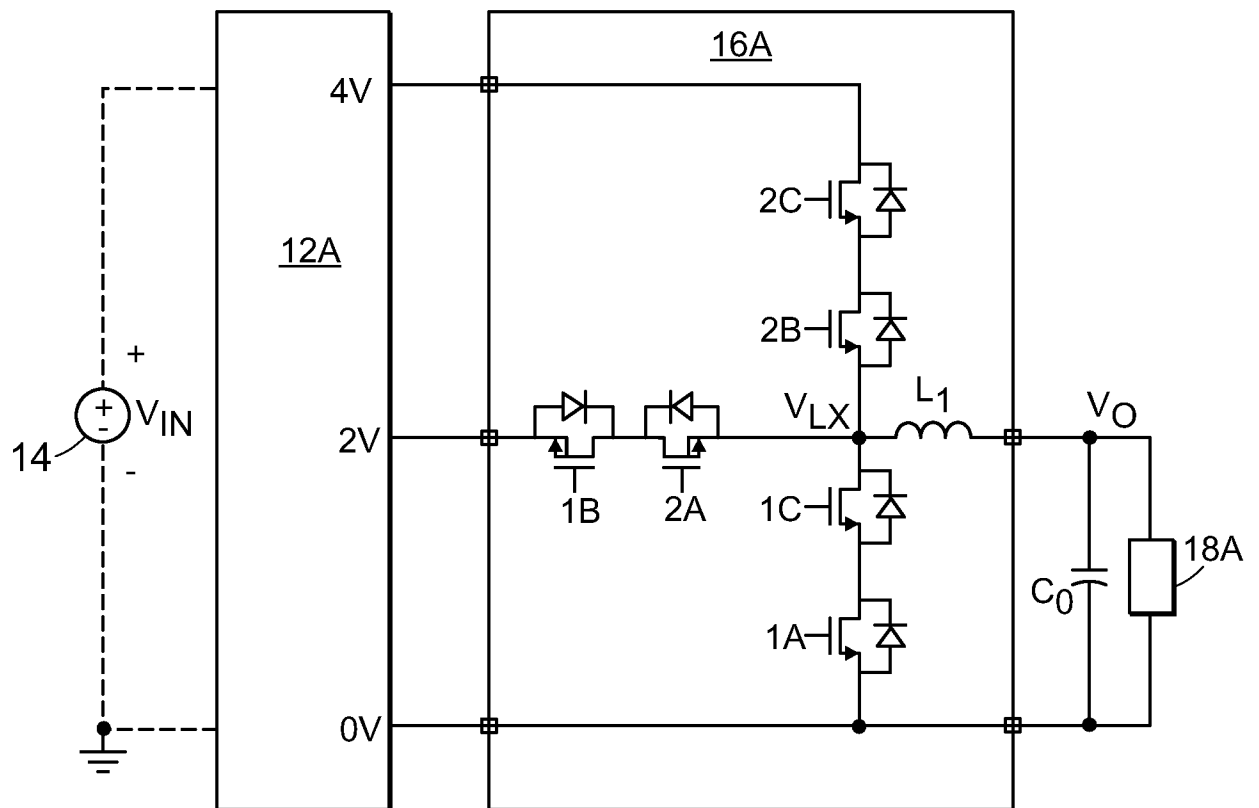


FIG. 28

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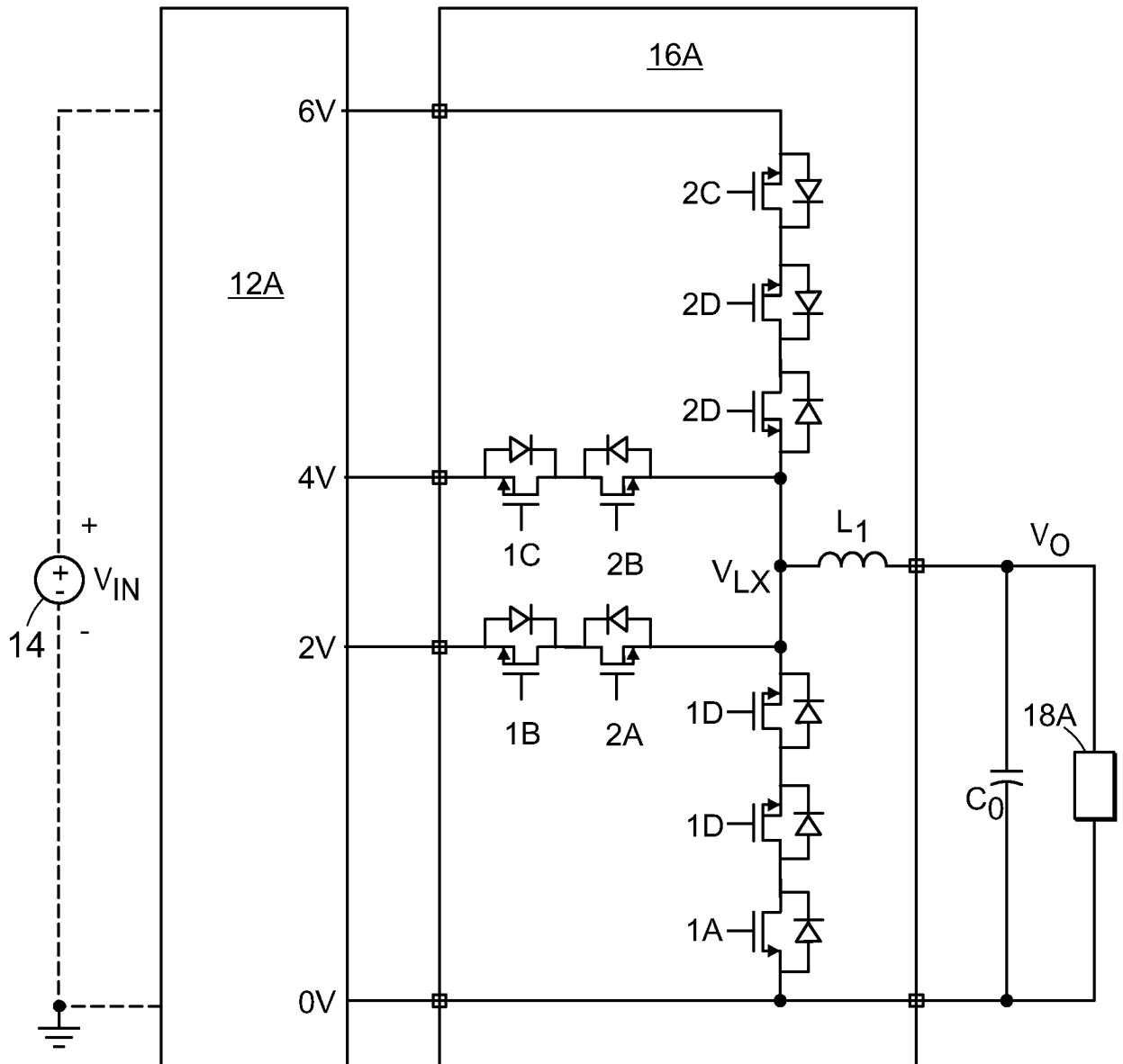


FIG. 29

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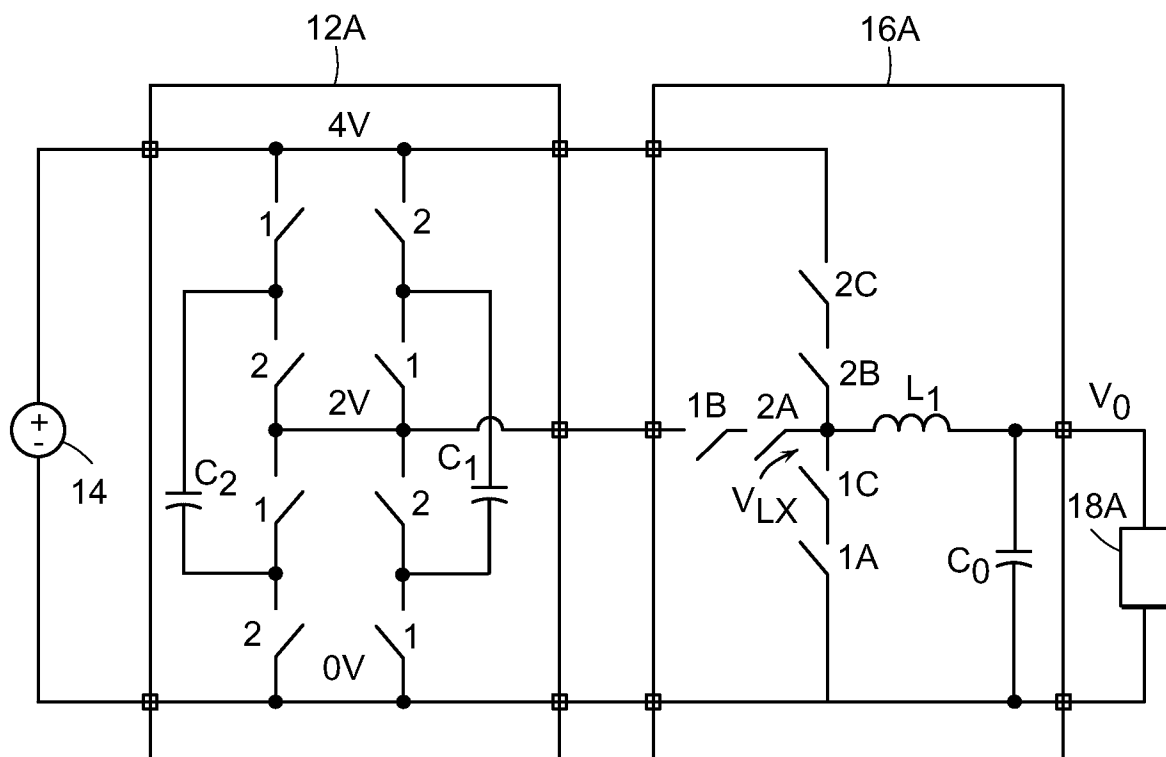


FIG. 30

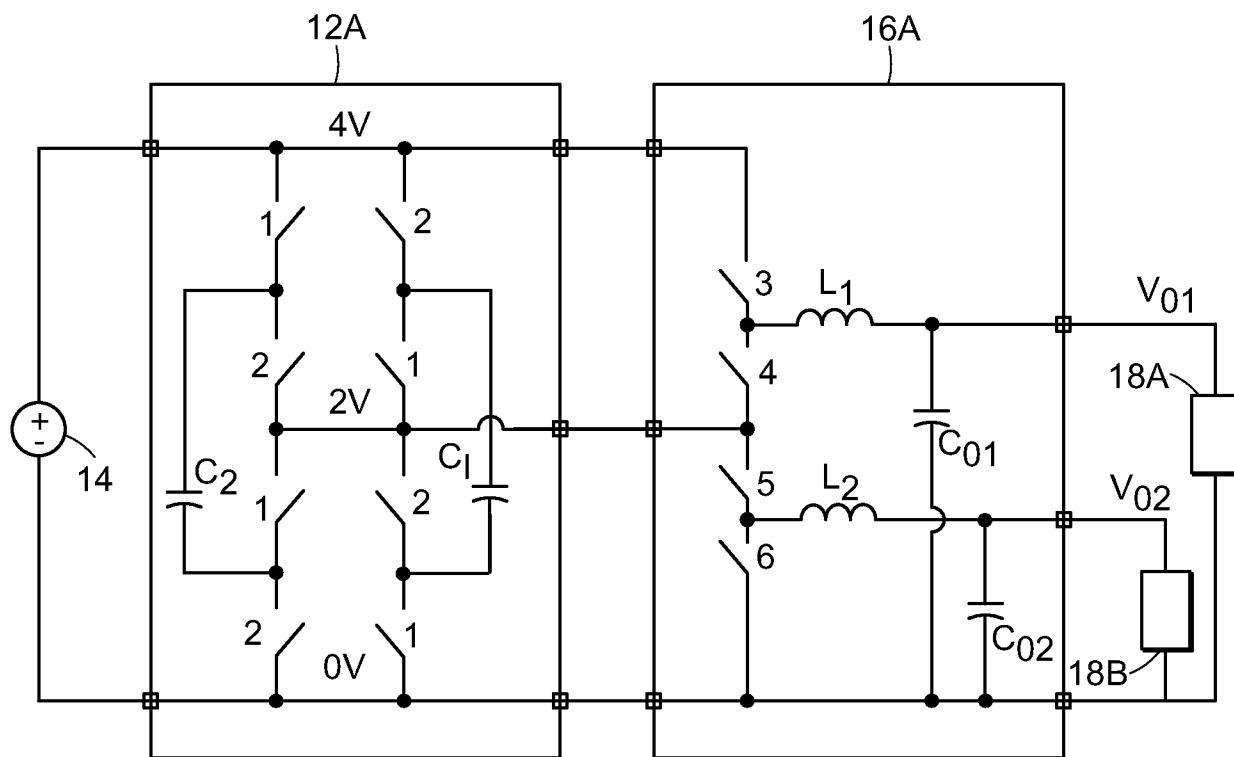


FIG. 31

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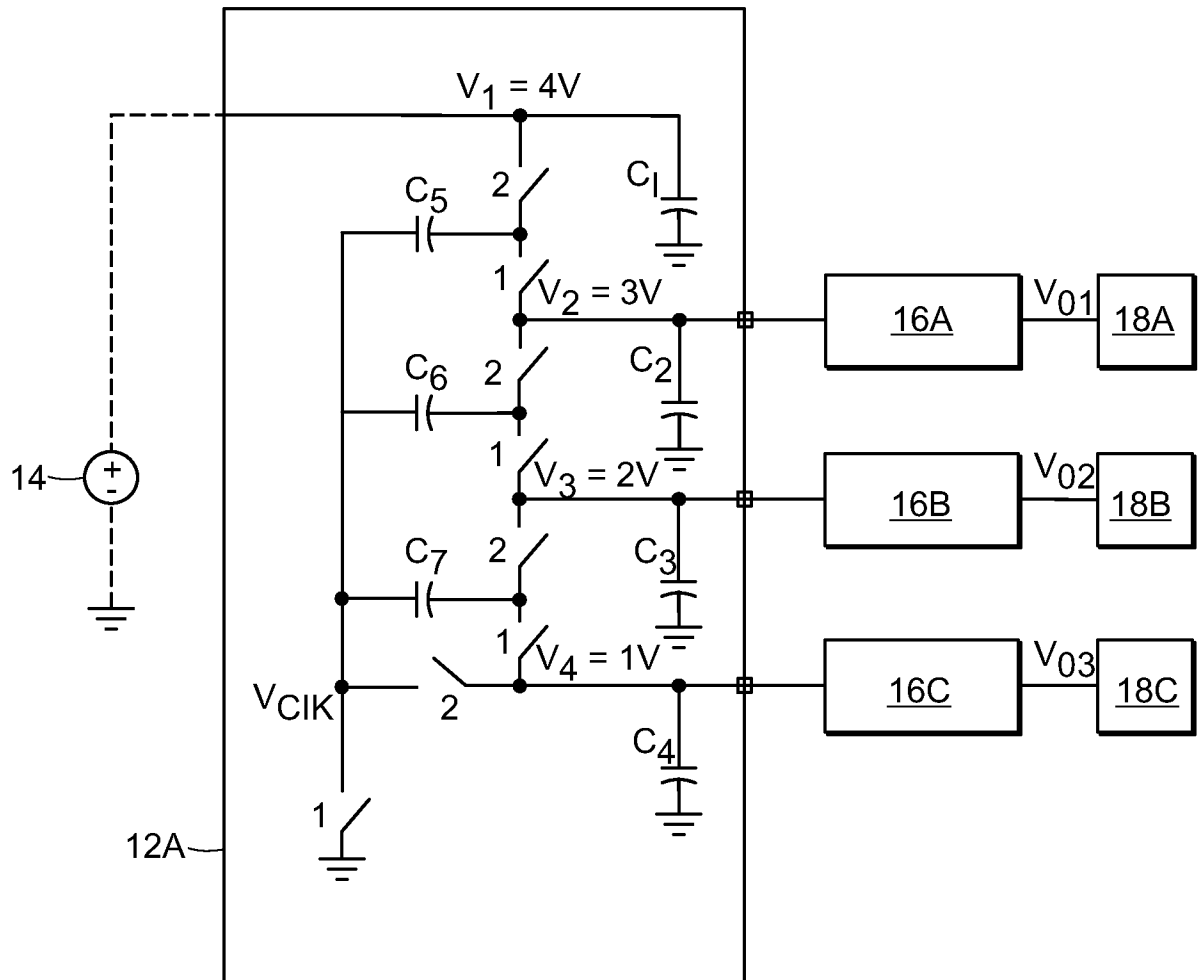


FIG. 32

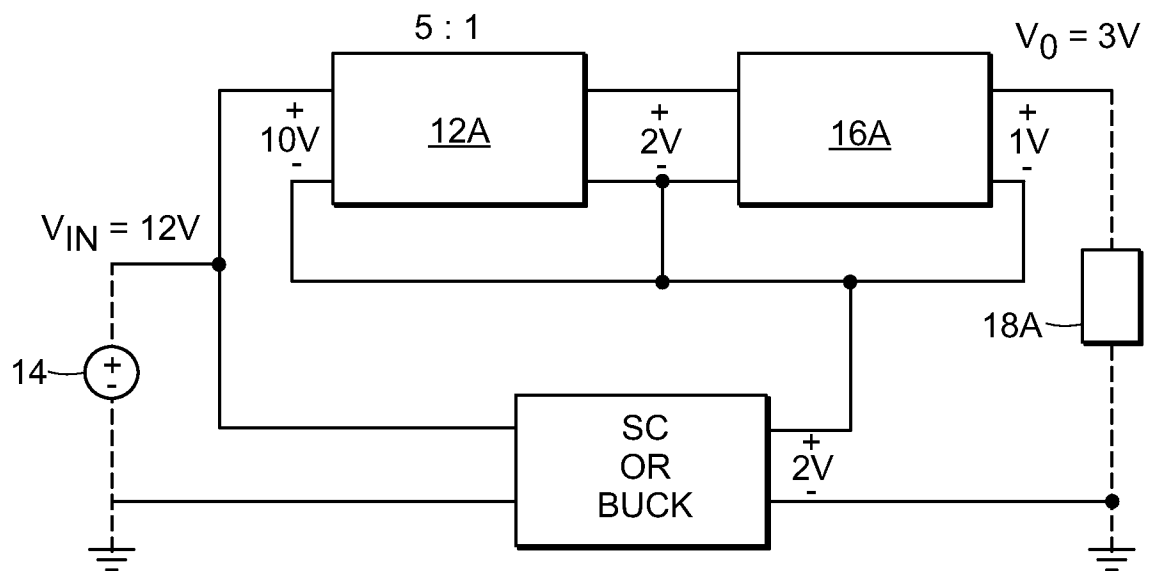


FIG. 33

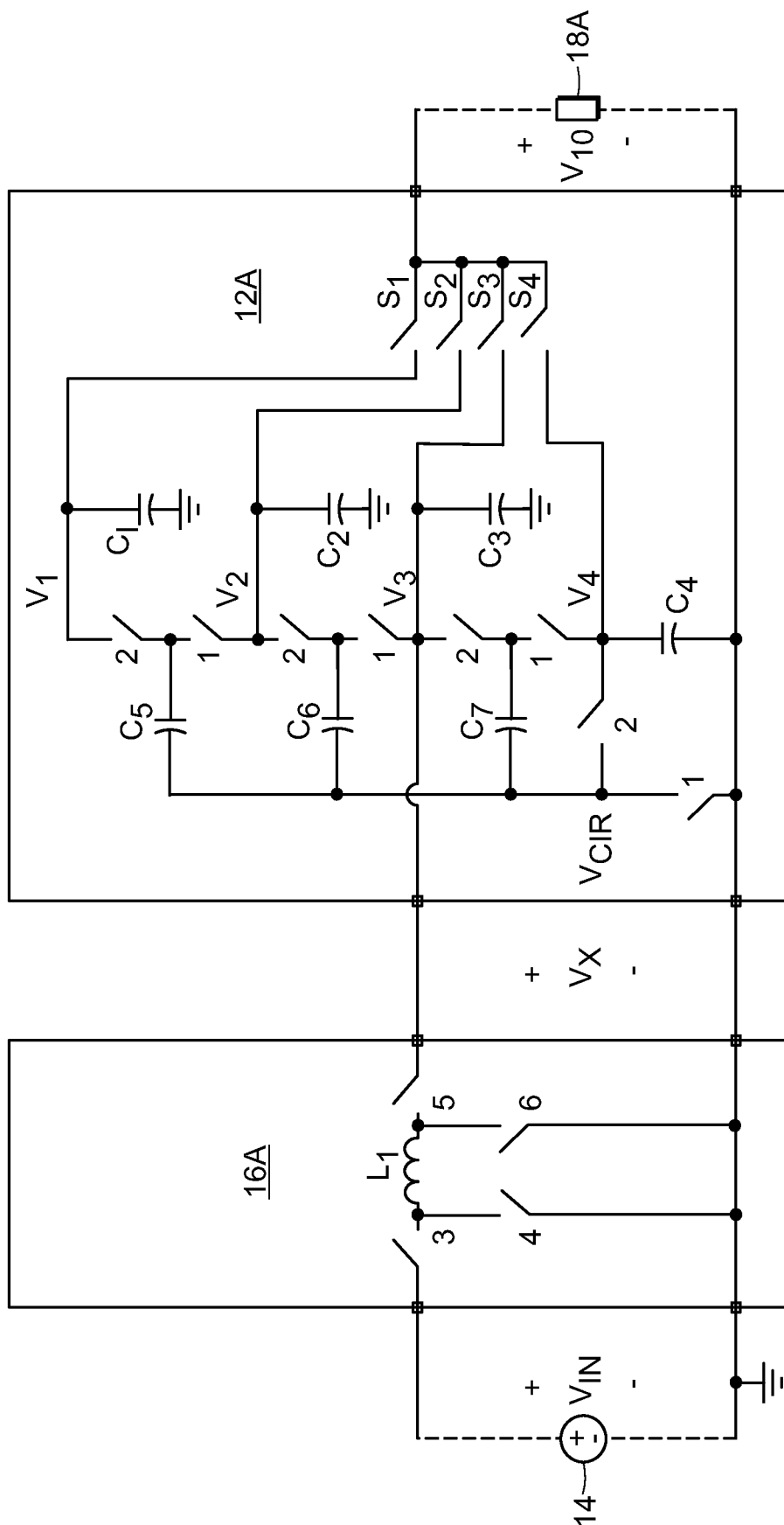


FIG. 34

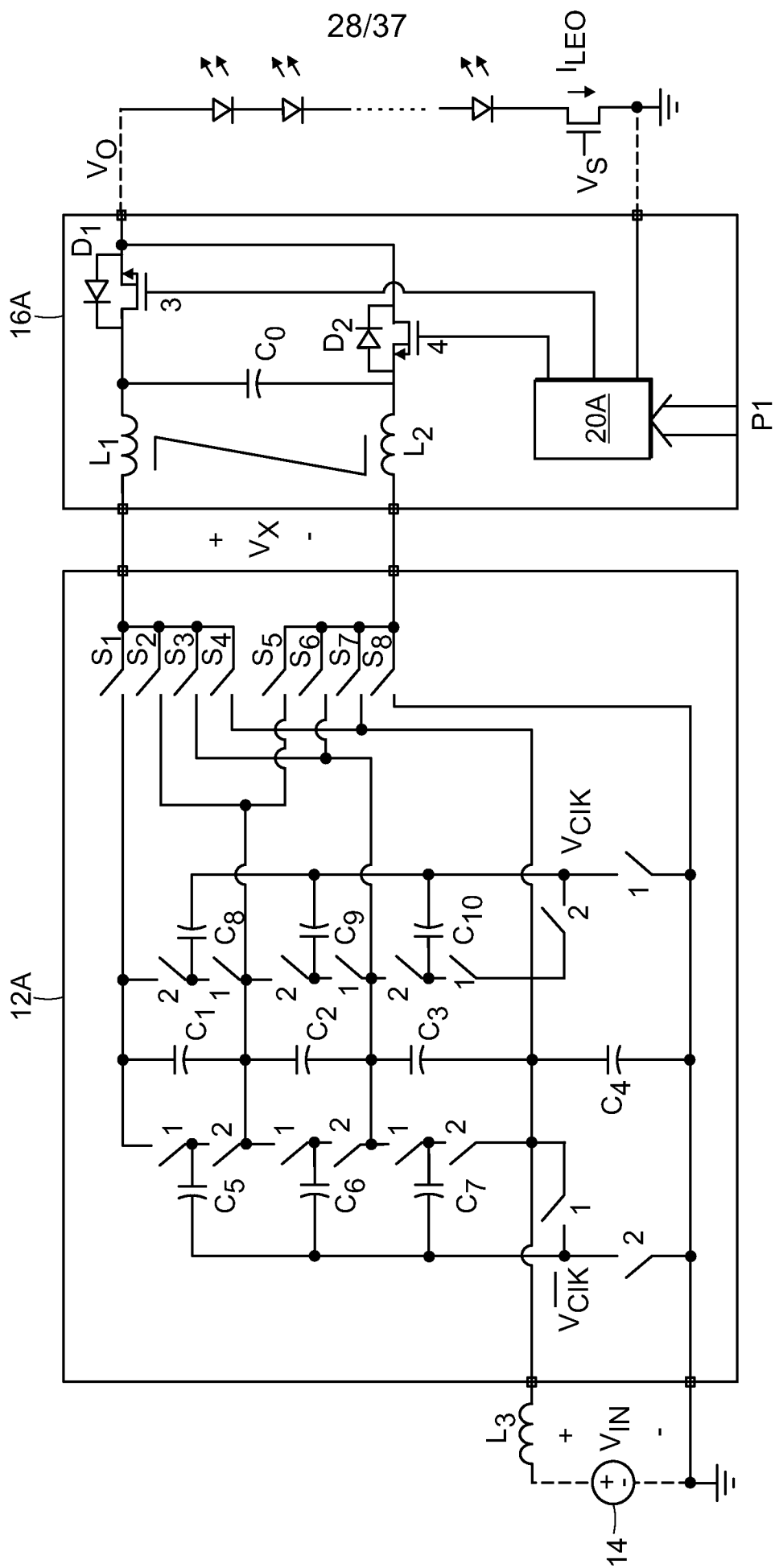


FIG. 35

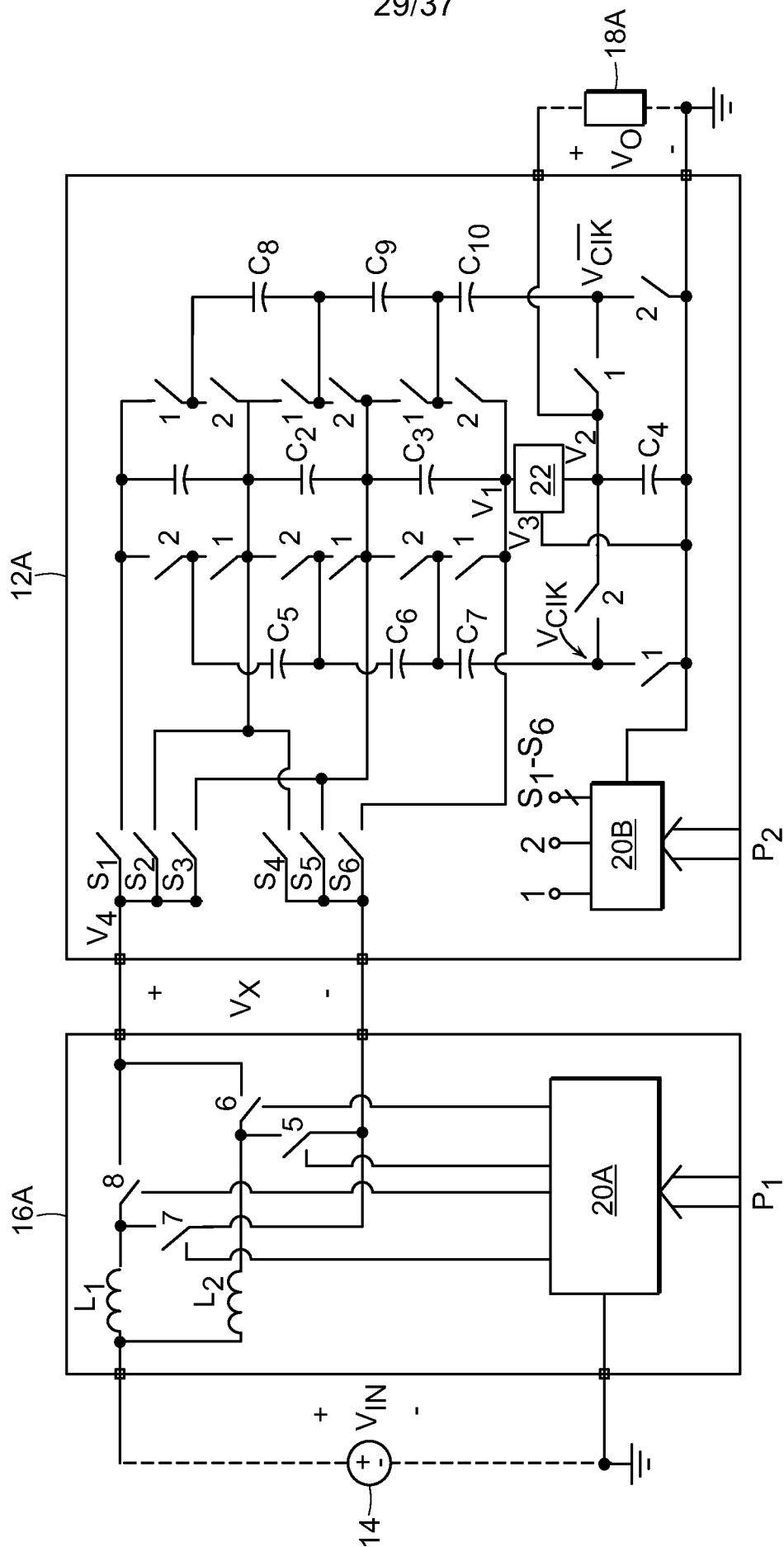


FIG. 36

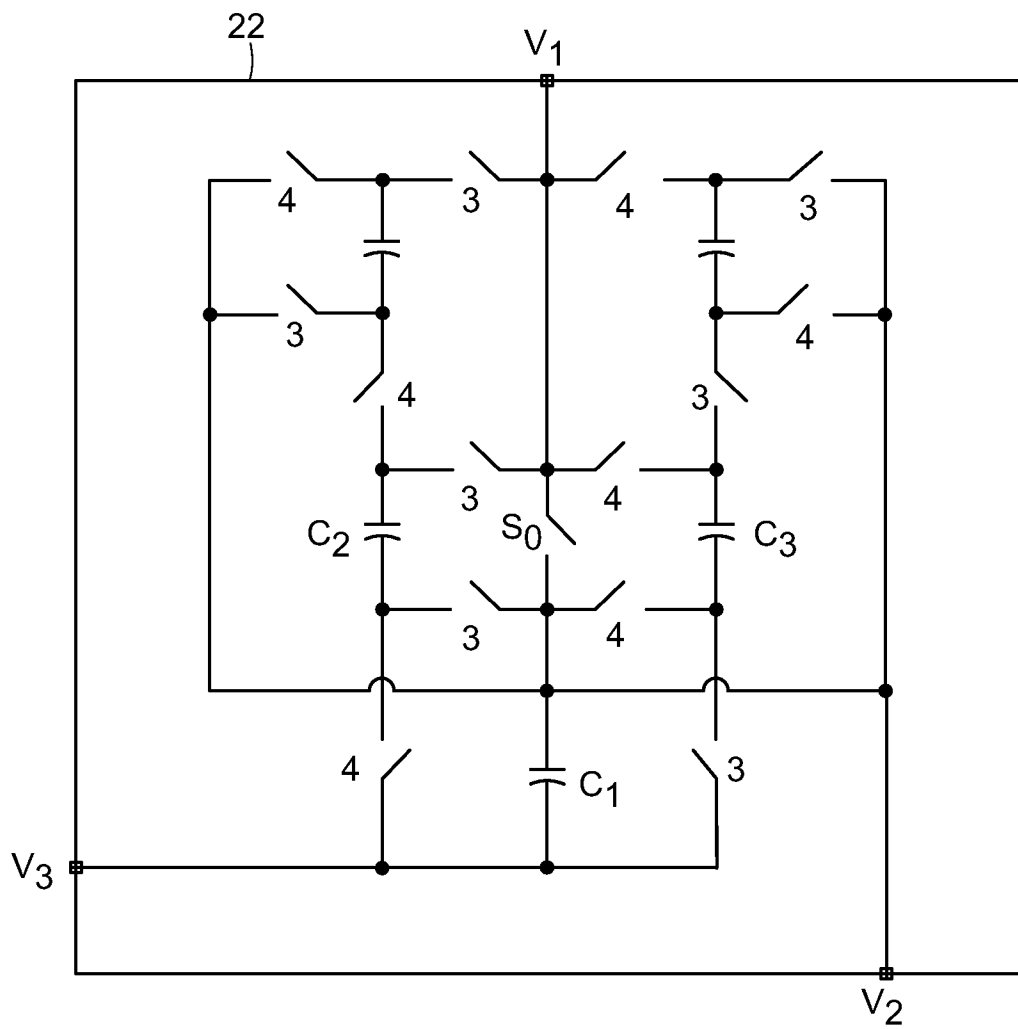


FIG. 37

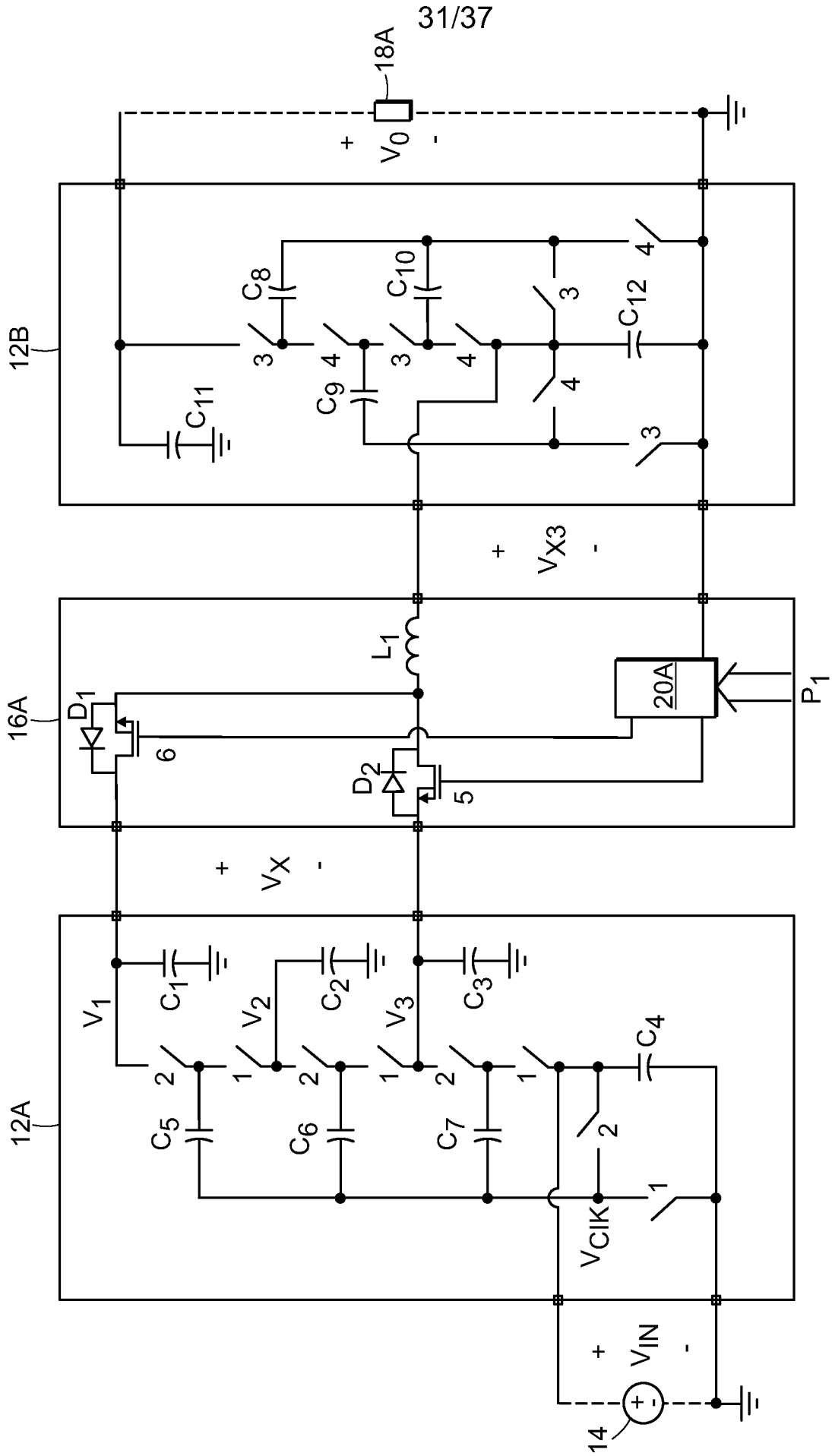


FIG. 38

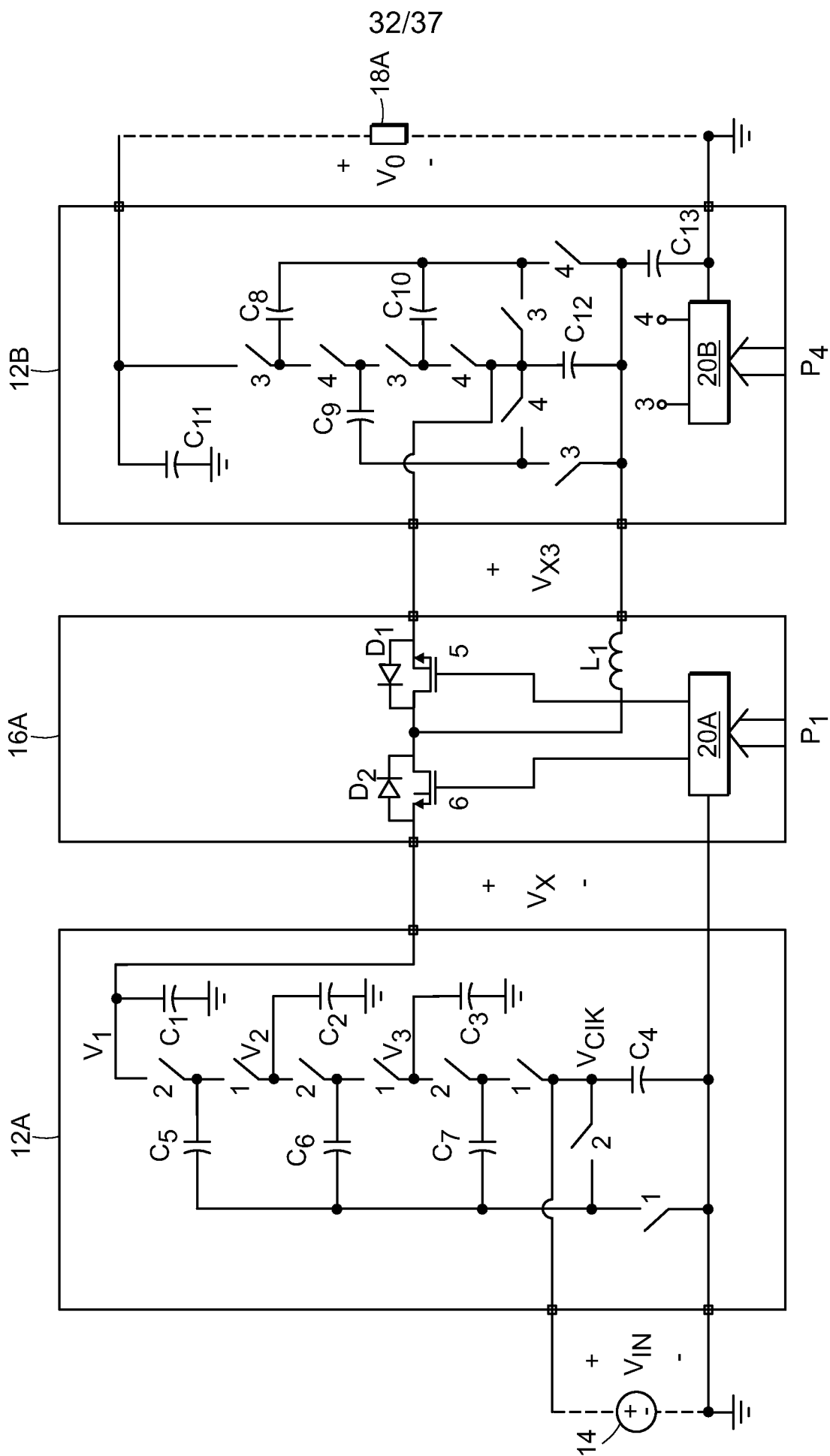


FIG. 39

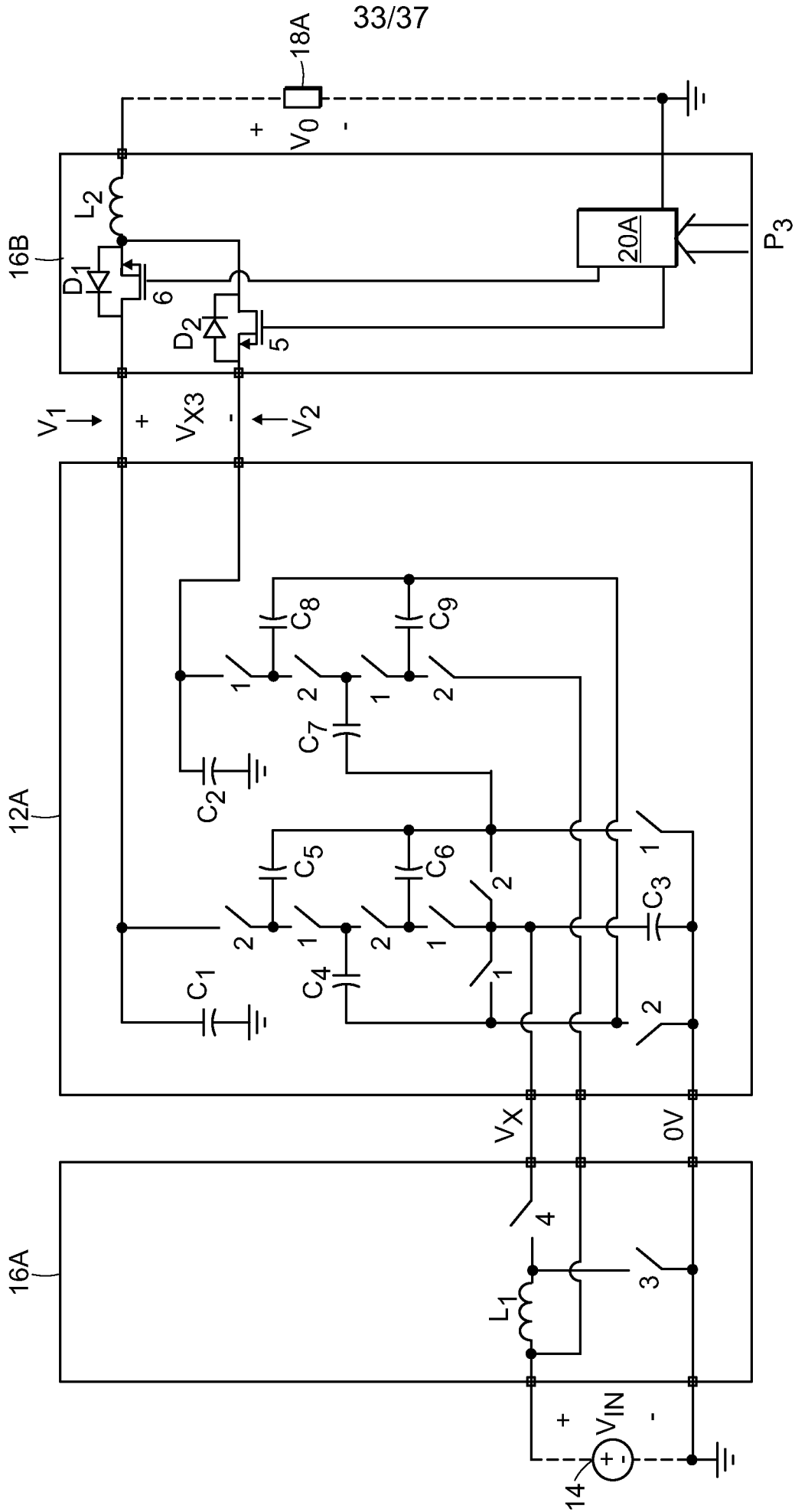


FIG. 40

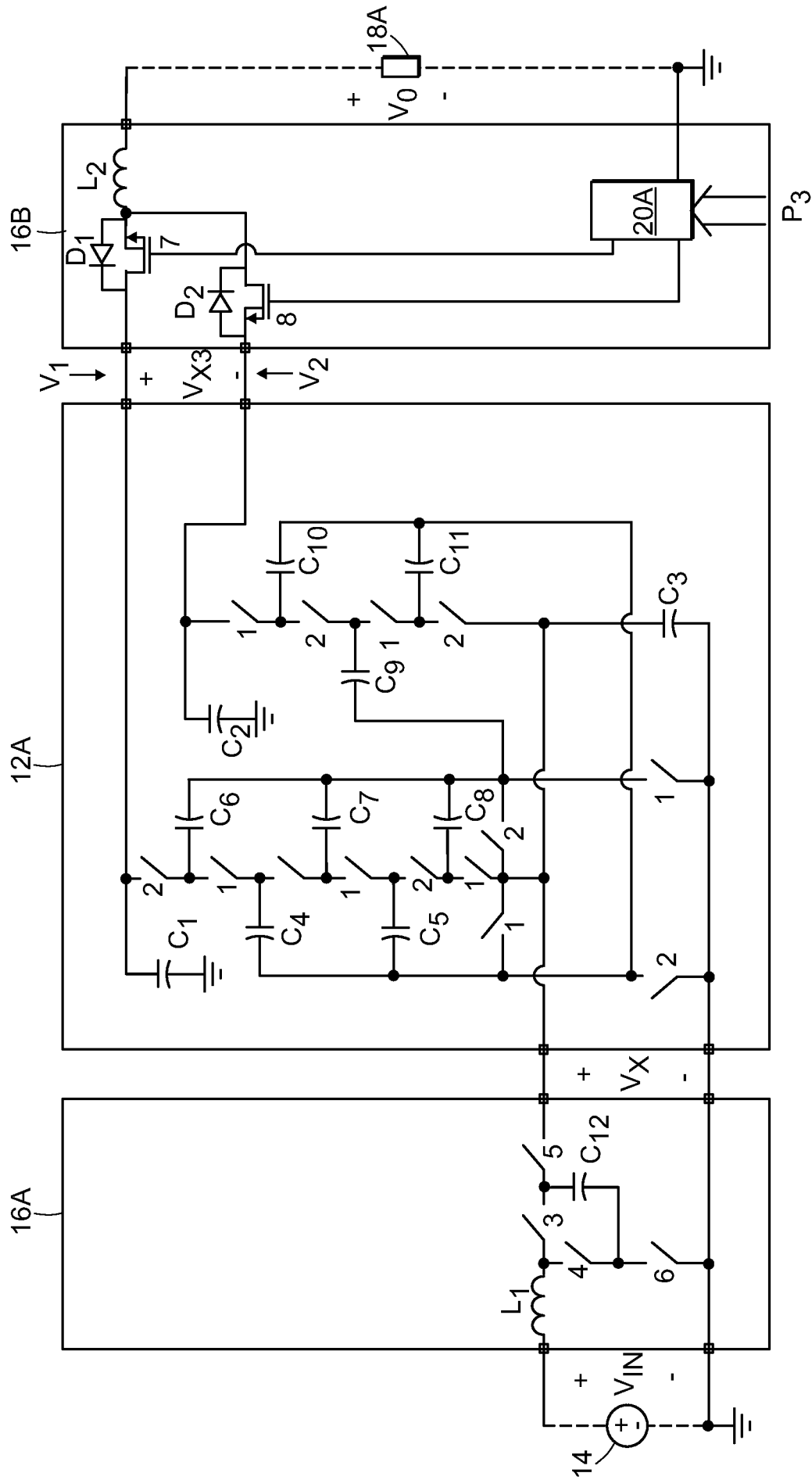


FIG. 41

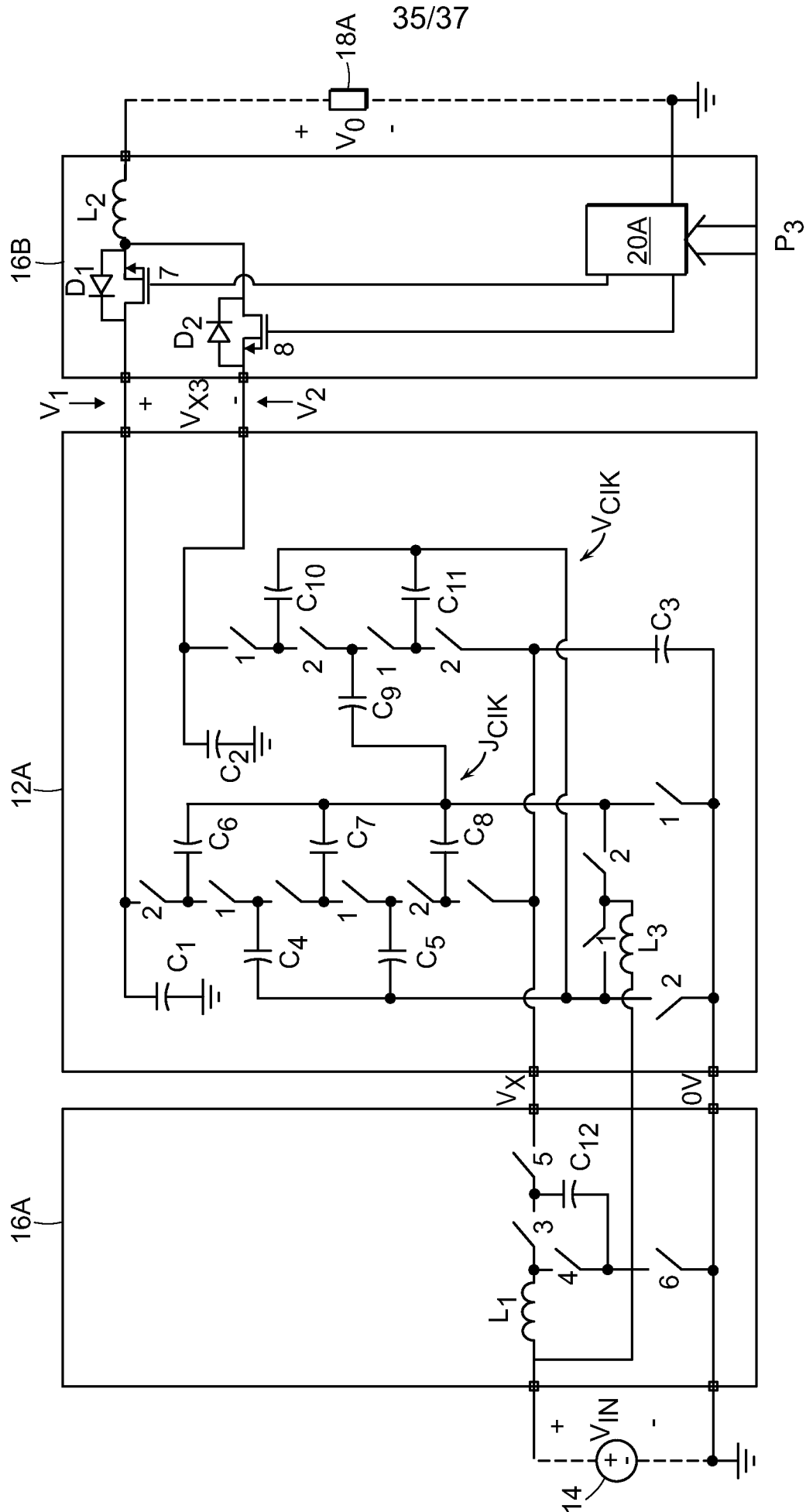


FIG. 42

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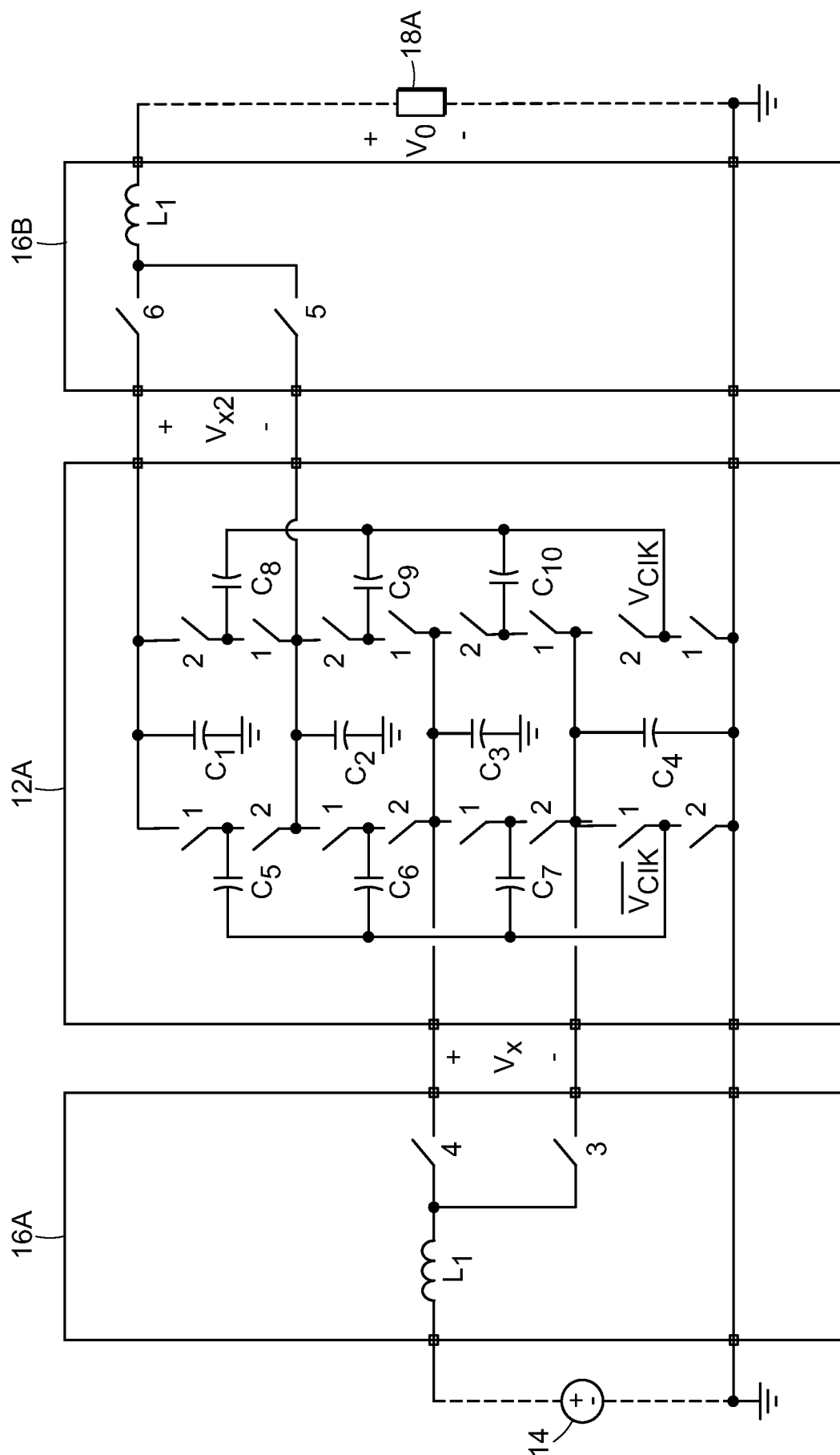


FIG. 43

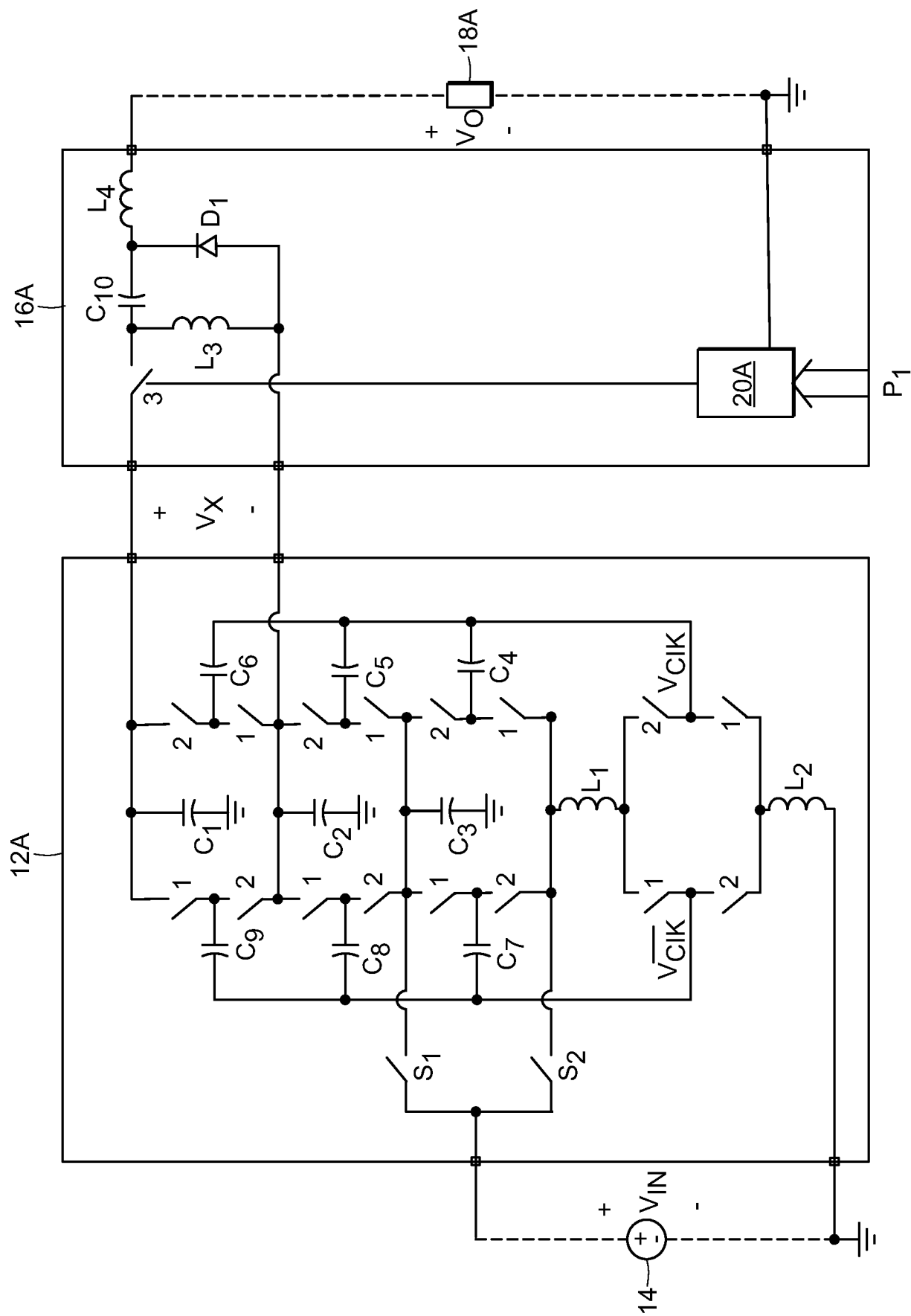


FIG. 44

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/041448**A. CLASSIFICATION OF SUBJECT MATTER****H02M 3/08(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02M 3/08; H03M 1/66; G05F 3/02; G05F 1/10; H02M 3/18; H02M 3/28; H02M 3/07

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: power converter, control, stage, switching, regulating, network, circuit, synchronization

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2014-0300328 A1 (ARCTIC SAND TECHNOLOGIES, INC.) 09 October 2014 See paragraphs 48-71, claims 1-20 and figures 3-10.	1-127
A	WO 2012-151466 A2 (ARCTIC SAND TECHNOLOGIES, INC. et al.) 08 November 2012 See page 8, line 10-page 11, line 16 and figures 1-6.	1-127
A	US 2008-0239772 A1 (BRADLEY S. ORAW et al.) 02 October 2008 See paragraphs 28-55, claims 1-11 and figures 2-20.	1-127
A	US 2005-0285767 A1 (HAISONG WANG et al.) 29 December 2005 See paragraphs 21-97 and figures 1-7.	1-127
A	US 2009-0322414 A1 (BRADLEY S. ORAW et al.) 31 December 2009 See paragraphs 19-37 and figures 2-7.	1-127



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/041448

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