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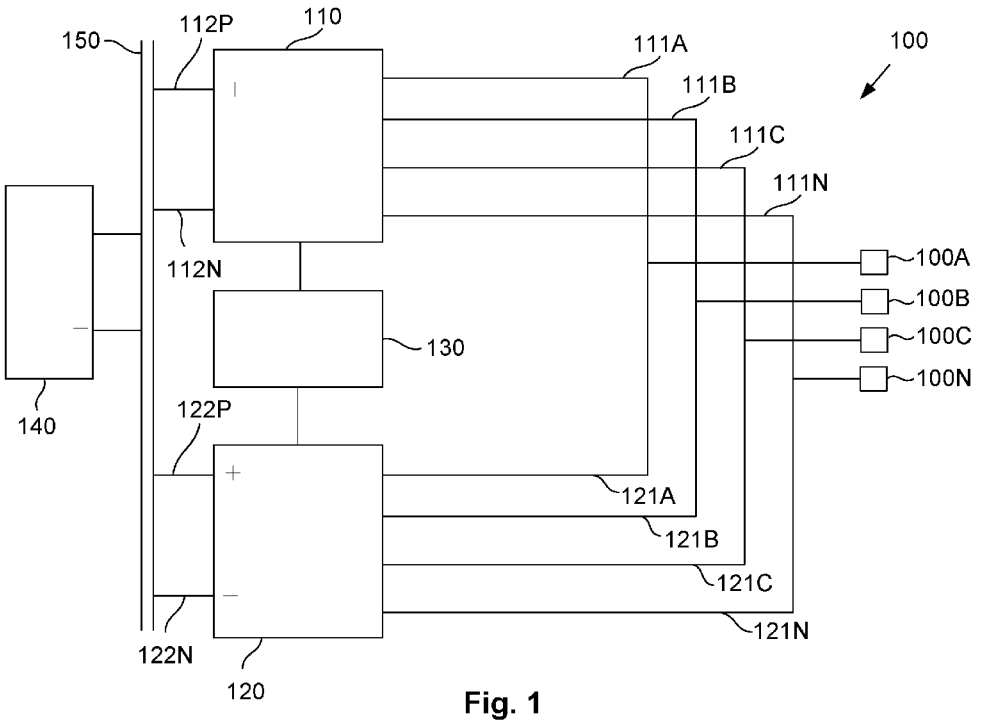

Fig. 1

(57) Abstract: The invention relates to a method of controlling an electrical power regulating system having a plurality of inverters connected in parallel, the inverters being connected to a common DC supply and live and neutral connections of a power supply network, and each inverter including a switching arrangement, the method including, in one or more electronic processing devices: independently controlling the switching arrangements of the plurality of inverters to selectively interconnect the DC supply and the live and neutral connections to thereby regulate power in the power supply network; detecting a circulating current that is circulating though the power supply network, the DC supply, and two or more of the plurality of inverters; and, controlling the switching arrangement of at least one of the inverters to apply a voltage offset to the neutral connection to thereby suppress the circulating current.

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METHOD OF CONTROLLING ELECTRICAL POWER REGULATING SYSTEM AND INVERTER DEVICE THEREOF

Background of the Invention

[0001] The present invention relates to a method of controlling an electrical power regulating system, and in one particular example, the present invention relates to a method of controlling an electrical power regulating system having a plurality of inverters and the inverter thereof.

Description of the Prior Art

[0002] In an electrical power distribution network, inverters, are used to regulate the voltage by exchanging active and reactive power while connected to the electrical power distribution network. In some situations, multiple inverters are connected in parallel to form an electrical power regulating system with greater capacity. However, in this situation, a circulating path is created within the system and a circulating current can be detected. The circulating current may cause increase in power loss of parallel system and distortions to the current outputs. It may also cause additional heat loss in transformers and/or distribution feeders.

[0003] A control method with zero sequence circulating current (ZSCC) is proposed to address the issues associated with the circulating current by cutting down the circulating path using isolation transformers or DC power sources. However, this would incur significant cost and maintenance requirements.

[0004] The reference in this specification to any prior publication (or information derived from it), or to any matter which is known, is not, and should not be taken as an acknowledgment or admission or any form of suggestion that the prior publication (or information derived from it) or known matter forms part of the common general knowledge in the field of endeavour to which this specification relates.

Summary of the Present Invention

[0005] In one broad form an aspect of the present invention seeks to provide a method of controlling an electrical power regulating system having a plurality of inverters connected in parallel, the inverters being connected to a common DC supply and live and neutral

connections of a power supply network, and each inverter including a switching arrangement, the method including, in one or more electronic processing devices: independently controlling the switching arrangements of the plurality of inverters to selectively interconnect the DC supply and the live and neutral connections to thereby regulate power in the power supply network; detecting a circulating current that is circulating though the power supply network, the DC supply, and two or more of the plurality of inverters; and, controlling the switching arrangement of at least one of the inverters to apply a voltage offset to the neutral connection to thereby suppress the circulating current.

[0006] In one embodiment, the method includes, in the one or more electronic processing devices: calculating the circulating current; and, determining the voltage offset based on the calculated circulating current.

[0007] In one embodiment, the method includes in the one or more electronic processing devices, calculating the circulating current value by calculating a sum of currents on the one or more live connections and the neutral connection of one of the plurality of inverters.

[0008] In one embodiment, the method includes, in the one or more electronic processing devices, detecting the circulating current in the electrical power regulating system by: determining a difference between neutral currents of the plurality of inverters; and, determining if the difference exceeds a predetermined current.

[0009] In one embodiment, the method includes in the one or more electronic processing devices, determining the difference between neutral currents of the plurality of inverters by measuring currents at respective terminals of the live and neutral connections.

[0010] In one embodiment, the method includes in the one or more electronic processing devices, controlling the switching arrangement of the at least one of the inverters to apply the voltage offset by controlling a proportional controller to thereby control a duty cycle offset applied to the live connections.

[0011] In one embodiment, the method includes in the one or more electronic processing devices, controlling the proportional controller by connecting and disconnecting the proportional controller to the neutral connection.

[0012] In one embodiment, the method includes applying a phase voltage offset to each of the live connections, and the phase voltage offset is at least: common for all live connections, and the same as the voltage offset.

[0013] In one broad form an aspect of the present invention seeks to provide an inverter, including: at least one live connections connecting to a power supply system; a neutral connection connecting to a neutral of the power supply system; a switching arrangement connected to the at least one live connections and the neutral connection, wherein the switching arrangement includes a proportional controller connected to the neutral connection; and, one or more electronic processing devices being configured to: independently control the switching arrangements of the plurality of inverters to selectively interconnect the DC supply and the live and neutral connections to thereby regulate power in the power supply network; detect a circulating current that is circulating though the power supply network, the DC supply, and two or more of the plurality of inverters; and, control the proportional controller to apply a voltage offset to the neutral connection to thereby suppress the circulating current.

[0014] In one embodiment, the one or more processing devices are configured to: calculate the circulating current; and, determine the voltage offset based on the calculated circulating current.

[0015] In one embodiment, the one or more processing devices are configured to calculate the circulating current value by calculating a sum of currents on the one or more live connections and the neutral connection of one of the plurality of inverters.

[0016] In one embodiment, the one or more electronic processing devices are configured to detect the circulating current in the electrical power regulating system by: determining a difference between neutral currents of the plurality of inverters; and, determining if the difference exceeds a predetermined current.

[0017] In one embodiment, the one or more electronic processing devices are configured to determine the difference between neutral currents of the plurality of inverters by measuring currents at respective terminals of the live and neutral connections.

[0018] In one embodiment, the one or more electronic processing devices are configured to control the proportional controller to control a duty cycle offset applied to the live connections.

[0019] In one embodiment, the one or more electronic processing devices are configured to control the proportional controller by connecting and disconnecting the proportional controller to the neutral connection.

[0020] In one embodiment, the one or more electronic processing devices are configured to apply a phase voltage offset to each of the live connections, and the phase voltage offset is at least: common for all live connections, and the same as the voltage offset.

[0021] It will be appreciated that the broad forms of the invention and their respective features can be used in conjunction and/or independently, and reference to separate broad forms is not intended to be limiting. Furthermore, it will be appreciated that features of the method can be performed using the system or apparatus and that features of the system or apparatus can be implemented using the method.

Brief Description of the Drawings

[0022] Various examples and embodiments of the present invention will now be described with reference to the accompanying drawings, in which: -

[0023] Figure 1 is a schematic diagram of an example of an electrical power regulating system;

[0024] Figure 2 is a flow chart of an example of a method of controlling the electrical power regulating apparatus;

[0025] Figure 3 is a schematic diagram of an example of a processing system;

[0026] Figure 4 is schematic diagram of an example of an electrical power regulating system;

[0027] Figure 5 is a schematic diagram of an example of an inverter;

[0028] Figure 6 is a schematic diagram of an example of a standalone inverter;

[0029] Figure 7 is a schematic diagram of an example of a current control system of an inverter;

[0030] Figure 8 is a schematic diagram of an equivalent circuit of an inverter;

[0031] Figure 9 is a discrete time model of a current loop of an inverter;

[0032] Figure 10 is a discrete time model of a current loop of an inverter;

[0033] Figure 11 is a discrete time model of a current loop of an inverter;

[0034] Figure 12 is a schematic diagram of an example of an electrical power regulating system;

[0035] Figure 13 is a schematic diagram illustrating a circulating current path in the electrical power regulating system of Figure 12;

[0036] Figure 14 is a schematic diagram of an equivalent circuit of in the electrical power regulating system of Figure 12;

[0037] Figure 15 is a simulation results of operating the electrical power regulating system of Figure 12 without circulating current control;

[0038] Figure 16 is a simulation results of operating the electrical power regulating system of Figure 12 with switched circulating current control;

[0039] Figure 17 is a simulation results of proportional controllers in the electrical power regulating system of Figure 12;

[0040] Figure 18 is a simulation results of operating the electrical power regulating system of Figure 12 with switched circulating current control; and,

[0041] Figure 19 is a simulation results of operating the electrical power regulating system of Figure 12 with circulating current control.

Detailed Description of the Preferred Embodiments

[0042] An example of an electrical power regulating system will now be described with reference to Figure 1.

[0043] In this example, an electrical power regulating system 100 includes two inverters 110, 120. The inverter 110 is a four-wire inverter having three live connections 111A, 111B, 111C and a neutral connection 111N. Similarly, the inverter 120 is also a four-wire inverter having three live connections 121A, 121B, 121C and a neutral connection 121N. As shown in Figure 1, the live connections 111A and 121A are electrically connected to form a live terminal 100A of the electrical power regulating system 100. In a similar manner, the live connections 111B and 121B, and the live connections 111C and 121C, are electrically connected to form live terminals 100B and 100C, respectively. The neutral connections 111N, 121N of the inverters 110, 120 are also electrically connected to form a neutral terminal 100N. The terminals 100A, 100B, 100C, 100N of the electrical power regulating system 100 are configured to be connected to corresponding phases and neutral/earth of a power supply network, such as a grid. Moreover, each inverter 110, 120 further includes two DC connections 112P, 112N and 122P, 122N, respectively. In this example, the DC connections are connected to a common DC supply 140 via a DC bus 150. The inverters 110, 120 include switching arrangements that selectively interconnect the DC supply 140 and the live and neutral connections and thereby regulate power in the power supply network.

[0001] The switching arrangements (not shown) are controlled by one or more electronic processing devices 130, which may form part of one or more processing systems, or could be hardware integrated into a network regulating apparatus. Whilst the system can use multiple processing devices, with processing performed by one or more of the devices, for the purpose of ease of illustration, the following examples will refer to a single device, but it will be appreciated that reference to a singular processing device should be understood to encompass multiple processing devices and *vice versa*, with processing being distributed between the devices as appropriate.

[0044] An example of a method of controlling the electrical power regulating system 100 will now be described with reference to Figure 2.

[0045] When in use, the electronic processing device 130 independently controls the live and neutral connections of the inverters 110, 120 at step 200. More specifically, the live connections 111A, 111B, 111C and the neutral connection 111N may be modulated independently of each other. The live connections 121A, 121B, 121C and the neutral

connection 121N are also independently controlled by the electronic processing device 130. As described above, the electronic processing device 130 controls the switching arrangements of the inverters 110, 120 to selectively interconnect the DC supply 140 and the live and neutral connections to thereby regulate power in the power supply network.

[0046] At step 210, the electronic processing device 130 detects a circulating current that is circulating though the power supply network, the DC supply, and two or more of the plurality of inverters. The circulating current is typically driven by a voltage difference between the neutral connections of the two inverters. In one example, the circulating current occurs in a loop of the neutral connection 111N of the inverter 110 through to the neutral connection 121N and returns via the DC bus 150. It is noted that even a very small steady-state difference in the voltages of the neutral connections 111N and 121N can drive a large circulating current.

[0047] At step 220, the electronic processing device 130 controls the switching arrangement of at least one of the inverters 110, 120 to apply a voltage offset to the neutral connection. Applying a voltage offset to the neutral connection is effectively creating a resistance in the path of the circulating current, and thereby, the circulating current is suppressed.

[0048] This allows power loss and/or distortions to the current outputs caused by the circulating current to be reduced or minimised. Suppressing the circulating current may also reduce heat loss in transformers and/or distribution feeders, and allows the system to be accessed safely and avoid damage to the equipment of the system. Therefore, a system with multiple inverters connected in parallel which increases the degrees of freedom of the system may be operated more efficiently, safely and less likely to be damaged.

[0049] A number of further features will now be described.

[0050] In one example, the electronic processing devices may further calculate the circulating current and determine the voltage offset based on the calculated circulating current. The voltage offset are being controlled to be a proportion of the circulating current to avoid unnecessarily large voltage offset which may result in a reduction in the achievable line-to-line voltage. In one example, the voltage offset is 3V to 8V for a 1000V bus. Accordingly, the electronic processing device may calculate the circulating current value by calculating a sum

of currents on the one or more live connections and the neutral connection of one of the plurality of inverters.

[0051] Furthermore, the electronic processing device detects the circulating current in the electrical power regulating system by determining a difference between neutral currents of the plurality of inverters, and determining if the difference exceeds a predetermined current. This avoids erroneously detecting a current fluctuation as the circulating current, which may falsely trigger the voltage offset to be applied.

[0052] The difference between neutral currents of the plurality of inverters may be determined by measuring currents at respective terminals of the live and neutral connections. The measurement may be made directly at the terminals for obtaining accurate current readings in a real-time or without delay.

[0053] In one example, the controlling the switching arrangement of the at least one of the inverters to apply the voltage offset may be implemented by controlling a proportional controller. The proportional controller controls a duty cycle offset applied to the live connections. This allows the circulating current to be suppressed without significantly affecting power carried on the live connections.

[0054] The electronic processing device may control the proportional controller to apply the voltage offset by connecting and disconnecting the proportional controller to the neutral connection.

[0055] Furthermore, a phase voltage offset may be applied to each of the live connections. The phase voltage offset may be common for all live connections and/or the same as the voltage offset. This allows the circulating current to be suppressed without significantly affecting power carried on the live connections.

[0056] An example of a hardware configuration of an electronic processing device will now be described with reference to Figure 3.

[0057] In this example, the electronic processing device 130 includes at least one microprocessor 300, a memory 301, an optional input/output device 302, such as a keyboard

and/or display, an interface 303, interconnected via a bus 304 as shown. In this example the interface 303 can be utilised for connecting the electronic processing device 130 to peripheral devices, such as communications networks, or the like.

[0058] In use, the microprocessor 300 executes instructions in the form of applications software stored in the memory 301 to allow the required processes to be performed, including controlling the electronic processing device 130. The applications software may include one or more software modules, and may be executed in a suitable execution environment, such as an operating system environment, or the like.

[0059] Accordingly, it will be appreciated that the electronic processing device 130 may be formed from any suitable control system and could include be any electronic processing device such as a microprocessor, microchip processor, logic gate configuration, firmware optionally associated with implementing logic such as an FPGA (Field Programmable Gate Array), or any other electronic device, system or arrangement.

[0060] However, it will be appreciated that the above described configuration assumed for the purpose of the following examples is not essential, and numerous other configurations may be used. It will also be appreciated that the partitioning of functionality between the different processing systems may vary, depending on the particular implementation.

[0061] An example of a hardware configuration of an electrical power regulating system will now be described with reference to Figure 4.

[0062] In this example, an electrical power regulating system 400 includes two inverters 410, 420. The inverter 410 is a four-wire inverter having three live connections 411A, 411B, 411C and a neutral connection 411N. Similarly, the inverter 420 is also a four-wire inverter having three live connections 421A, 421B, 421C and a neutral connection 421N. As shown in Figure 4, the live connections 411A and 421A are coupled to form a live terminal 400A of the electrical power regulating system 400. In a similar manner, the live connections 411B and 421B are couple, the live connections 411C and 421C are coupled, to form live terminals 400B and 400C, respectively. The neutral connections 411N, 421N of the inverters 410, 420 are coupled to form a neutral terminal 400N. The terminals 400A, 400B, 400C, 400N of the electrical power regulating system 400 are configured to be connected to corresponding phases

and neutral/earth of a power supply network, such as a grid. Moreover, each inverter 410, 420 further includes two DC connections 412P, 412N and 422P, 422N, respectively. In this example, the DC connections are connected to a common DC supply 440 via a DC bus 450. The inverters 410, 420 include switching arrangements that selectively interconnect the DC supply 440 and the live and neutral connections and thereby regulate power in the power supply network. The switching arrangements (not sure) are controlled by an electronic processing device 430. In one example, the switching arrangements of the inverter 410 include a proportional controller 413 connected to the neutral connection 411N. The electronic processing device 430 controls the proportional controller 413 to apply a voltage offset to the neutral connection to thereby suppress the circulating current.

[0063] An example of the inverter will now be described in more detail with reference to Figure 5.

[0064] An inverter 500 configured to regulate electrical power in an electricity transmission network. The inverter 500 includes a DC contactor 510, a plurality of capacitors 531, a plurality of switches 530, a common-mode (CM) choke 541, a differential-mode (DM) choke 542, an EMI choke 543, a grid connector, and a load connector. The grid connector includes an AC connector 521, an AC relay 522, AC circuit breakers 523, and three AC terminals 520A, 520B, 520C and an AC neutral connector 520N. The load connector includes load circuit breakers 571 and three load terminals 570A, 570B, 570C and the load neutral connector 570N. The inverter 500 also includes three connections 560A, 560B, 560C, and a neutral connection 560N. The three connections 560A, 560B, 560C are connected to the respective live connection with the AC terminals 520A, 520B, 520C.

[0065] The DC contactor 510 having DC terminals 510A, 510B. The DC terminals 510A, 510B are configured to connect to a battery and a low voltage (LV) solar power generator. In this example, the DC contactor 510 includes at least one mechanical switch for switching both terminals 510A, 510B. Mechanical switches are robust and reliable, and can be configured to have a high breaking capabilities in voltage and current to improve electrical safety.

[0066] In one embodiment, a safety interlocking mechanism is implemented. The safety interlocking mechanism may include interlocking multiple AC contactors and/or interlocking

both the AC and DC contactors. The safety interlocking mechanism may utilizes an on-board processor, such as one of the controlling devices 551, 552, and a supplementary external processor to switch on the supply. The on-board processor monitors the status of the inverter 500 while the external processor monitoring at safety considerations, such as battery voltage and/or battery polarity. Both processors crosscheck each other before operating the contactor.

[0067] A DC bus sensor 510C is implemented to monitor the current at the DC terminals 510A, 510B. The DC bus sensor 510C is coupled to the controlling device 551 and allows leakage current or residual current to be detected. In an example, a Sigma-Delta configuration is used for the DC bus sensor 510C, which provides high voltage isolation and accuracy in sensing.

DC Capacitors

[0068] The DC contactor 510 is connected to the switches 530 via the capacitors 531. In this example, the capacitors 531 are polypropylene capacitors. The polypropylene capacitors are capable of operating with relatively high ripple currents, which allows the users to control higher order harmonics without decreasing capacitor life. Polypropylene capacitor also have self-healing capabilities, which allows the size of the capacitors to be reduced for providing a required capacitance and accommodating transient voltage.

[0069] In this example, there are twelve capacitors in the inverter 500. The capacitors are mounted on a multi-layer printed circuit board (PCB) in a three-by-four array arrangement. The tracks connecting the capacitors are on the multi-layer PCB with an interleaving structure to minimise parasitic inductance. In one example, the interleaved structure uses eight layers with approximately 2oz copper per layer, and the layers are separated with FR4 PCB material with a thickness of approximately 0.4 mm. It should be appreciated that other suitable materials and/or thickness may be used depending on different system requirement.

[0070] The interleaving structure allows the parasitic inductance to be reduced as the current is distributed across multiple layers. There are also no 'tracks' on the layers which induces inductance. The parallel layers with alternating polarity may increase the parasitic capacitance to complement the capacitors. As described, there is an alternating plate pattern between positive and negative, thereby minimising parasitic inductance and increasing total capacitance. This also improves the equivalent series resistance (ESR) and temperatures as

there is less eddy current circulation (phenomenon where induced currents from magnetic fields interact with traces/wires). With a more stable temperature the change in capacitance due to temperature during operation is reduced.

[0071] The inverter 500 also includes a failsafe system 533 coupling the capacitors 532 to earth and controls the discharging of the capacitors in the event of a fault. The failsafe system 533 includes a software failsafe and a hardware failsafe mechanisms. When a voltage abnormality is detected, the software failsafe mechanism switches the capacitors on and off rapidly to safely discharge the capacitors. Moreover, if power is lost, the hardware failsafe mechanism opens the DC and AC contactors. The hardware failsafe mechanism also includes an external DC battery fuse and an external AC grid fuse.

Switches

[0072] The capacitors 531 are connected to the switches 530 for modulating the each of the three connections 560A, 560B, 560C, and the neutral connection 560N. An example of the switches 530 includes four symmetrical half bridge topology arms connecting to each of the three connections 560A, 560B, 560C and the neutral connection 560N. Each symmetrical half bridge topology arms includes two MOSFET switches. In this example, the MOSFET switches are silicon carbide switches, particularly, 1200V 55A SCT3040 MOSFET in compliant with the ROHM standard.

[0073] The switching characteristics, such as rise time, fall time, and dead-time, of the switches 530 can be configured by hardware design and/or the controlling devices 551, 552 to optimise the performance. The switches 530 can operate in higher switching frequencies (approximately 100kHz) due to a reduction of the primary side to secondary side capacitance as the specific isolation devices are used. This also allows high voltage isolation barrier to increase noise immunity and provide high voltage protection between primary side and secondary side. The switches 530 may further include a snubber circuit 533 to reduce the voltage changes over time (dv/dt) to meet the EMI/EMC requirements.

CM Choke

[0074] The CM choke 541 is coupled to the switches 530 to suppress and/or reject high frequency common mode current. The live connections 560A, 560B, 560C and the neutral connection 560N are connected to the CM choke 541 and passed through a core. The core of the CM choke 541 may be a powder core and can be configured to operate in high frequency with low loss. The CM choke 541 is also configured to operate in wider temperature range condition while maintaining low energy losses. Furthermore, in one example, the CM choke 541 may be insulated from an outer chassis of the inverter 500, so that high frequency magnetic coupling to the surrounding equipment is minimised. The windings of the CM choke 541 may be of a non-interleaved structure, thereby reducing coupling noise propagating to adjacent conductors. Additionally, the winding may be copper flat bar winding, which minimises copper losses in low and high frequencies. Flat bar winding may also reduce skin effect when compared to round windings. The increased surface area of the flat bar winding may help with heat dissipation of the CM choke 541.

DM Choke

[0075] The CM choke 541 is coupled to a DM choke 542, which acts like a bandpass filter and smooths high frequency from the PWM generated by the switches 530. The DM choke 542 may include individual differential mode inductors that are built of EE cores. The EE cores are compact and easier to manufacture when compared to toroidal cores. The EE core may also shields from high frequency noise and stray magnetic fields. Additionally, the core of the DM choke 542 may be made of a high saturation-point powder core material, so that the DM choke 542 can be configured to operate in high frequency with low loss. This allows the DM choke to have a consistent filter performance, and the inductor to have an overrated capacity a short term. The DM choke 541 can be configured to operate in wider temperature range condition while maintaining low energy losses. Furthermore, the DM choke 542 may be insulated from an outer chassis of the inverter 500, so that high frequency magnetic coupling to the surrounding equipment is minimised.

[0076] The winding of the DM choke 542 includes copper film winding, which may be thin and flat copper film, to minimise copper loss in low and high frequencies. Copper film winding may also reduce skin effect when compared to round windings. The increased surface area of the film winding may help with heat dissipation of the DM choke 542. The use of film winding

also allows an increase in the number of turns without compromising in size and/or skin effect losses.

EMI Filter

[0077] The DM choke 542 is coupled to an EMI filter 543, which filters out high frequency electromagnetic interference. This may help preventing any stray common mode current from exporting to the grid, any common mode current from grid impacting the control circuitry. The EMI filter 543 includes a ring core with nano-crystalline material. Solid enamelled copper wire may be used around core material to minimise copper losses, particularly at 50Hz. The EMI filter 543 includes symmetrical windings to minimise leakage inductance. The EMI filter 543 may also include Y capacitors (Y2 rated) in its PCB design.

[0078] It should be appreciated that current and/or voltage measurements may be implemented at any point in the inverter 500. In one example, the AC current and voltage measurements are implemented between the DM choke 542 and the EMI choke 543. The AC current may be measured with a LEM (100-p) 100A high precision hall-effect sensor.

[0079] The inverter 500 includes Class X capacitors (X2 rated) between the DM choke 542 and the EMI choke 543. The X capacitors can be useful for high voltage applications to minimise high voltage transients. This also allows shielding signal traces from power traces on the PCB and also provide protection from primary side to secondary side. As illustrated in Figure 5, an earth link is provided at this point for the neutral connection 560N through a decoupling capacitor.

Load Contactor

[0080] Optionally, the inverter 500 may include the load connector, so that the inverter 500 can provide UPS functionality while connected to the grid. The load connector has a 63A circuit breaker 571 for each live connection 560A, 560B, 560C. The connectors may be Amphenol connectors. As the inverter 500 is able to compensate the harmonic components to match the load component, this allows the harmonic content to be managed and not passed through to the grid. This also provides the load with a “clean” AC source. The inverter 500 can operate with an unbalanced load condition as the neutral connection 560N can be modulated.

[0081] This allows the inverter 500 to be a source to the load regardless to whether the load is a three-phase, two-phase or a single-phase load. This is particularly useful for off grid loads with large induction machines, such as farming equipment, conveyor belts, fridges etc.

AC Contactor

[0082] The AC contactor 521 is coupled to the EMI filter 543 for connecting to the grid. The AC contactor 521 may be a Semmens three-phase (AC-3 rated) contactor with 38kW breaking capacity which has low power consumption, such as less than 4W. The AC contactor 521 is also robust, reliability and able to break high fault currents while providing short switch on and off response times. The AC contactor 521 may include internal sensors in communications with at least one of the controlling devices 551, 552, so that the AC contactor operational status is monitored and controlled.

AC Relay

[0083] An AC relay 522, 522a, 522b are coupled between the AC contact 521 and the grid to provide an additional isolation. As illustrated in Figure 5, the neutral connection 560N are separately coupled to two AC relay 522a, 522b. The AC relay 522, 522a, 522b are in communication with at least one of the controlling devices 551, 552. Additionally, the AC contactor 521 and the AC relay 522 are controlled by different controlling devices 551, 552. This allows the AC contactor 521 and the AC relay 522 to perform interlocking which provide additional safety. Similarly, the two AC relay 522a, 522b are also controlled by different controlling devices 551, 552 to provide additional safety to the neutral connection 560N.

Circuit Breaker

[0084] Similar to the load connection circuit breakers 571, circuit breakers 523 are coupled to each of the live connections to form the isolation barrier between the AC terminals 520A, 520B, 520C and the AC contactor 521. This provides additional overcurrent protection to the inverter 500. The circuit breakers 523 are rated at 63A to allow operations in various temperatures and no prematurely breakage due to temperature.

MCU

[0085] The controlling devices 551, 552 may be two on-board microprocessors. A first microprocessor 551 includes executable programs to control the operation of the inverter 500, and a second microprocessor 552 is functioned as a safety interlocking controller. An analogue measurement 551a and a temperature measurement 552a may be coupled to the microprocessors 551, 552 respectively. Furthermore, a communication interface 553 is also connected to the microprocessors 551, 552. The communication interface 553 may include one or more interface for Modbus (TCP/IP), USB, RS232/485, Ethernet, demand response mode (DRM) communications. This allows external processors to communicate with the inverter 500 for monitoring, controlling and/or configuration the inverter 500.

[0086] The electrical power regulating apparatus provides at least the following advantages:

- Fast response, often under 20 milliseconds
- Continuous control of voltage
- Addresses flicker issues
- Addresses voltage unbalance issues
- Low power losses
- Capable of generating a 415V three-phase output and interface a three-phase system to one battery. This provides cost advantages in that only one battery and battery management system per apparatus is needed. This also results in a smaller unit as the higher modulation frequency made possible by using MOSFETS. Smaller size means smaller cabinets, saving both space and materials
- Being a four-quadrant device, enables it to be flexible to manage both active and reactive power. This makes it advantageous in managing battery energy storage systems, solar photovoltaic (PV) installations and distribution system voltages
- Reliable as the capacitors and other components are all high-quality components as no electrolytic capacitors are used

[0087] The operation may be automatic based on the program in it, with little need for maintenance and servicing.

[0088] An example of a method of controlling an electrical power regulating system having a plurality of inverters connected in parallel will now be described.

[0089] The following paragraphs disclose control augmentations to allow two Static Synchronous Compensators (STATCOMs) devices to operate in parallel from a shared DC bus. Two parallel connected four-wire STATCOMS will be shown to be highly susceptible to an uncontrolled circulating current in the neutrals when operating with a three degree of freedom current control scheme. The circulating current can be calculated from the local inverter phase currents and neutral current. This disclosure shows the circulating component is readily supressed by a neutral voltage offset that is determined by a proportional control (P) system. The controller is validated by both simulation and experimental results.

[0090] A Static Synchronous Compensator (STATCOM) is used for regulating the voltage, reducing harmonics, power factor correction and sharing the load while connected in parallel to the grid. STATCOM is based on a voltage source converter (VSC) which can exchange active and reactive power while connected to the grid. When two four wire STATCOMS are connected in parallel, a circulating current path is created. The neutral current through this path increases power losses of parallel system and causes distortion on output currents. It may also cause additional heat loss in transformer and distribution feeder. Over the past years many control methods have been proposed in literature. Zero sequence circulating current (SZCC) can be cut down in circulating path by using isolation transformers or DC power sources. However, this process would incur more cost. To minimize the neutral current, modulation techniques have been optimized for two level inverters. A uniform sinusoidal pulse width modulation technique has been studied for parallel inverters. It assumes an ideal operational status of the inverters where the amplitude, phase, frequency would be the same for reference and carrier waves. A comparison study has been done between alternative phase opposition disposition (APOD) and phase disposition (PD) modulation techniques for interleaved parallel inverters. It is found that APOD modulation gives less circulating current than PD modulation. A proportional integral (PI) control system using space vector modulation (SVM) was investigated to suppress ZSCC by adjusting dwell time of zero vectors. In this method the tuning of gains of the controller is not needed. The neutral current can be minimized in both steady state and transient state by using feed forward zero vector with the SVM. A zero sequence controller using the feed forward control has been introduced. Instead of using the phase voltage, grid voltage is for calculating zero sequence voltage. A dead band control strategy using SVM has been proposed for three level neutral-clamped inverters. Another

nonlinear method has been proposed. However, the algorithm seems to be complicated in this case. Two quasi resonant controllers with the PI controllers have been used in three level inverters under unbalanced operating conditions.

[0091] The major contribution of this disclosure is to propose a proportional control system for suppressing circulating current in parallel three phase four leg STATCOMs. This introduces a neutral voltage offset that is proportional to the circulating current. This effectively simulates the resistive voltage drop in the circular path.

Basic STACOM operations

Reactive Current

[0092] The simplest STATCOM operation is to inject a balanced lagging or leading current. If the voltages at the point of connection are:

$$v_{an}(t) = \sqrt{2}V_{ph}sin(\omega t)$$

$$v_{bn}(t) = \sqrt{2}V_{ph}sin(\omega t - 2\pi/3)$$

$$v_{cn}(t) = \sqrt{2}V_{ph}sin(\omega t + 2\pi/3)$$

A leading or lagging current can be injected in the form of following equations:

$$i_a(t) = \sqrt{2}I_{ph}cos(\omega t)$$

$$i_b(t) = \sqrt{2}I_{ph}cos(\omega t - 2\pi/3)$$

$$i_c(t) = \sqrt{2}I_{ph}cos(\omega t + 2\pi/3)$$

Positive value of I_{ph} results in capacitive current. A negative value for I_{ph} results in an inductive current.

Real Current

[0093] The converter can export or import real power by sending a sinusoidal reference current in the form of following equations:

$$i_a(t) = \sqrt{2}I_{ph}sin(\omega t)$$

$$i_b(t) = \sqrt{2}I_{ph}sin(\omega t - 2\pi/3)$$

$$i_c(t) = \sqrt{2} I_{ph} sin(\omega t + 2\pi/3)$$

A positive value for I_{ph} results in power export.

Standalone Inverter Operation

[0094] Figure 6 shows a high-level overview of the inverter and the location of the inductor current measurements. Application of Kirchhoff's Current Law (KCL) to the region under the pale blue square dictates that the sum of the inverter currents in the four connecting wires sum to zero. In this case, the inverter currents have three degrees of freedom (DoF). The neutral current is completely controlled by controlling the three phase currents, I_A, I_B and I_C. The duty cycle for each of the four legs of the inverter has been produced using space vector modulation (SVM) technique which is described.

The current loops

[0095] The converter is current controlled and the current controller block diagram is shown in Figure 7. The current controller uses a nested loop structure with an inner and outer current loop.

[0096] Inner current loop: The equivalent circuit for the current controller is shown in Figure 8. The loop voltage equations are given by:

$$\begin{bmatrix} E_{AN} \\ E_{BN} \\ E_{CN} \end{bmatrix} = R_f \begin{bmatrix} 2 & 1 & 1 \\ 1 & 2 & 1 \\ 1 & 1 & 2 \end{bmatrix} \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} + L_f \begin{bmatrix} 2 & 1 & 1 \\ 1 & 2 & 1 \\ 1 & 1 & 2 \end{bmatrix} \begin{bmatrix} \dot{I}_A \\ \dot{I}_B \\ \dot{I}_C \end{bmatrix} + \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} \quad [1]$$

$$E = R_f K I + L_f K \dot{I} + V \quad [2]$$

Where, L_f and R_f are the inductance and series equivalent resistance, E is the inverter voltage, V is the phase to neutral voltage and the matrix K is:

$$K = \begin{bmatrix} 2 & 1 & 1 \\ 1 & 2 & 1 \\ 1 & 1 & 2 \end{bmatrix} \quad [3]$$

The matrix K also appears in the inner current loop as seen in Figure 7.

[0097] The inner loop aims to force the currents at the end of each sampling instant to a given value. If the current vector at time t=kT is *I(k)* and the desired current at time t=(k+1)T is *I(k+1)* then

$$E(k) \approx R_f K I(k) + \frac{L_f}{T} K\{I(k+1\dot{)} - I(k)\} + V(k) \qquad [4]$$

If the inductor resistance is ignored:

$$E(k) \approx \frac{L_f}{T} K\{I(k+1\dot{)} - I(k)\} + V(k) \qquad [5]$$

or

$$\begin{bmatrix} E_{AN} \\ E_{BN} \\ E_{CN} \end{bmatrix} = \frac{L_f}{T} \begin{bmatrix} 2 & 1 & 1 \\ 1 & 2 & 1 \\ 1 & 1 & 2 \end{bmatrix} \begin{bmatrix} I_A(k+1) - I_A(k) \\ I_B(k+1) - I_B(k) \\ I_C(k+1) - I_C(k) \end{bmatrix} + \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} \qquad [6]$$

Equation [6] can be used to calculate the three phase inverter voltages that will force the inductor current to a prescribed value at each sampling instant.

The discrete time inner current loop model

[0098] The inner control loop is a discrete time system as shown in Figure 9. The currents are feedback to form a current error which drives the calculation for A the inverter voltages. The state model is the averaged model of the inverter, the filter inductors and the output voltages.

The state model is found by rearranging Equation [2]:

$$L_f K\dot{I} = -R_f K I + [E - V] \qquad [7]$$

$$\dot{I} = \frac{-R_f}{L_f} K^{-1} K I + \frac{K^{-1}}{L_f} [E - V] \qquad [8]$$

$$\dot{I} = \frac{-R_f}{L_f} I + \frac{K^{-1}}{L_f} [E - V] \qquad [9]$$

[0099] From a control systems perspective the voltage vector V is a "disturbance" term. If V is an externally forced constant, then it does not affect the control loop stability. The total response of the system can be found using the superposition theorem and this is the summation of the control response and the disturbance current forced by the grid voltage. The grid voltage does strongly impact on the total response but not the loop stability. If *V* is set to zero (for purposes of the stability study) the state equation becomes:

$$\dot{I} = \frac{-R_f}{L_f} I + \frac{K^{-1}}{L_f} E \quad [10]$$

The input voltage vector E is:

$$E = GK[I_f - I] \quad [11]$$

For stability studies the control loop is unforced and $I_f = 0$ so substituting Equation [11] into Equation [10] yields:

$$\dot{I} = \frac{-R_f}{L_f} I + \frac{K^{-1}}{L_f} GK[I_f - I] \quad [12]$$

$$\dot{I} = \frac{-R_f}{L_f} I - \frac{G}{L_f} I \quad [13]$$

$$\begin{bmatrix} \dot{I}_A \\ \dot{I}_B \\ \dot{I}_C \end{bmatrix} = -\frac{G+R_f}{L_f} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} \quad [14]$$

Equation [14] is the effective state model for the controller. In this application G is much greater than R_f. The three phases are decoupled by the use of the K matrix in the forward gains.

[00100] The stability in the discrete time domain can be studied in the z domain. The effective discrete time model for phase A is shown in Figure 10. The forward gain function is given by:

$$G(z) = Z\left\{\frac{G}{L_f} \frac{1-e^{sT}}{s^2}\right\} \quad [15]$$

$$G(z) = \frac{G}{L_f} \frac{T}{z-1} \quad [16]$$

The closed loop transfer function is:

$$\frac{G(z)}{1+G(z)} = \frac{GT}{GT+L_f(z-1)} \quad [17]$$

This is a first order system. The pole location is:

$$z = 1 - \frac{GT}{L_f} \quad [18]$$

[00101] The pole is at z=1 for G=0 and this is the open loop integrator response. If G equals $\frac{L_f}{T}$ the pole is at z=0 which is the deadbeat response. In this case the current error is

reduced to zero in one sample period and this is an ideal response. However, any DSP implementation has an additional sample period delay due to the requirement to read the analogue variables, calculate and load the PWM generators. The control system is modified in Figure 11 to show the sample delay.

The forward gain is now:

$$G(z) = \frac{G}{L_f}\,\frac{T}{z-1}\,\frac{1}{z} \qquad [19]$$

The closed loop gain is:

$$\frac{G(z)}{1+G(z)} = \frac{\acute{G}}{z^2-z+\acute{G}} \qquad [20]$$

Where $\acute{G}$ is a normalised gain:

$$\acute{G} = \frac{GT}{L_f} \qquad [21]$$

[00102] **Outer current loop:** The outer current loop runs at 12kHz to reduce the computational load on the processor. The inner current loop executes four times faster. The inner loop settles to within 13% of its steady state value within four sample periods ($1 - 0.594^4 = 0.875$). The inner loop can be modelled as a unit gain block from the perspective of the outer loop.

[00103] The purpose of the outer loop is to improve the current wave shape. The inner loop attempts to control the value of the current at the sample times and the inductor ripple causes this to vary slightly from the average value of the current over the switching cycle. The outer loop should have a moderate 50Hz gain to supress any current harmonics.

[00104] In the attached Simulink model the outer loop bandwidth is set at 2,000 r/s or approximately 300Hz. This gives a 50Hz gain of six. From a control perspective this bandwidth is low in comparison to the 12 kHz sampling frequency.

Parallel operation of two STATCOMs

[00105] Two parallel inverters with a shared DC bus are shown in Figure 12. The application of KCL to the blue shaded area shows that, for Inverter 1, the four output currents, and the DC bus currents, sum to zero. The KCL constraint now applies on six conductors not

four. To control Inverter 1's four output currents it is no longer possible to rely on the KCL constraint. All four output currents require independent control. A physical interpretation is that one inverter, say Inverter 1, can source a net current from the four wires and the net current can be returned via Inverter 2 and the DC bus connection. The potential path for a circulating current is shown in Figure 13.

[00106] Figure 14 shows the equivalent circuit from a control perspective. Superposition theory can be used to independently calculate the total inverter currents. The phase currents are determined by the actions of the phase current control loops which modulate the phase to neutral voltage set in each converter.

[00107] A circulating current, I_{CIRC}, can be driven by any potential difference between the neutral voltages of the two converters. The circulating current occurs in a loop shaded in blue in Figure 13.

Controller for parallel operation

[00108] The following observations can be made with respect to the circulating current:

- The active voltage sources are the inverter neutral voltages relative to the DC bus negative, E_{N1} and E_{N2}.
- Very small steady state differences in the neutral voltages will drive large circulating currents. The typical neutral voltage is half the DC bus voltage. Given the milliohm impedances in the current loop a 1% voltage difference can drive much more than rated current.
- There is some coupling between the phase current control loops and circulating current loop due to voltages across the shared neutral inductor impedances. The coupling is small relative to the neutral voltage effect.

[00109] Current mode controller has been discussed above for each phase. The circulating current can be directly controlled by adjusting the converter neutral voltages relative to the DC bus negative, E_{N1} and E_{N2}. A uniform offset can be added to each phase leg modulator directly controls the effective neutral voltage without any change to the phase to

neutral voltages. This removes any influence upon the circulating current control upon the phase current control.

[00110] The duty cycle control can be implemented with a controller which responds to any non-zero circulating current. The circulating current can be calculated, for Inverter 1, as:

$$I_{CIRC} = I_{A1} + I_{B1} + I_{C1} + I_{N1} \quad [22]$$

The neutral current is the combination of the circulating current and the phase currents:

$$I_{N1} = I_{CIRC} - I_{A1} - I_{B1} - I_{C1} \quad [23]$$

[00111] Similar equations can be written for Inverter 2. Note that the change of sign is due to chosen direction for the circulating current. The controls for a converter will assume a current direction relative to its own output terminals and within the physical implementation this sign change disappears.

$$I_{CIRC} = -I_{A2} - I_{B2} - I_{C2} - I_{N2} \quad [24]$$

$$-I_{N2} = I_{CIRC} + I_{A2} + I_{B2} + I_{C2} \quad [25]$$

For two STATCOMS controlled with equal phase currents the difference in the neutral currents is

$$I_{N1} - I_{N2} = 2I_{CIRC} \quad [26]$$

[00112] The proposed controller is a proportional controller (P) with a limited output voltage range. This introduces a neutral voltage offset that is proportional to the circulating current. This effectively simulates a resistive voltage drop in the circulating current path. The limitation on the controller output recognises that:

- In a practical system the neutral voltage offsets are small, typically a few volts for a 1000V bus;
- Large neutral offsets will reduce the achievable line to line voltages.

[00113] The proportional control avoids a practical problem observed for proportional plus integral (PI) control. Each converter contains an identical control system. There are then two PI controllers that act in combination to oppose the circulating current. As the circulating current responds to differences in the offset voltage it is possible for the integral element in

each converter to take up equal and opposite steady state voltages. This does occur in simulation cases where the PI controls have saturation limits.

[00114] If both inverters have the same controller, the open loop gain can be considered using one half of the circulating current loop.

The open loop transfer function is:

$$G(s)H(s) = K_p M \frac{1}{R_f + L_f s} \qquad [27]$$

Where K_p is the proportional control gain and M is the modulator gain.

[00115] Where K_p is the proportional control gain and M is the modulator gain. This is a first order system. The inductor resistance can be ignored at frequencies near the gain crossing. The gain crossing can be set to achieve a satisfactory response time. A gain crossing frequency of $10krs^{-1}$, 1.59kHz, is relatively low in comparison to the proposed 48kHz switching frequency and yields a time constant of 100μs. For an inductor L_f=200μH and a modulator gain of M=1000, corresponding to a 1000Vdc bus, a gain of K_p =0.002 is required.

Results

[0116] Figure 15 shows the simulation results obtained for two parallel inverters operating without any circulating current control. Initially it was assumed that it would be necessary to include a voltage offset to cause a circulating current in a simulation model where all components are ideal and perfectly matched. This was not the case. The circulating current path is highly susceptible to even minor simulation numerical errors and uncontrolled circulating currents occur immediately. In a practical implementation, the potential currents resulting from the uncontrolled degree of freedom would be expected to be extremely dangerous for the inverter switches.

[0117] In Figure 15, both inverters are controlled to produce a balanced cosine current set with a magnitude of 56Ap or 40Arms. The inner most current mode control system is included but no outer current or voltage control loops. The phase currents are well controlled. The neutral currents should be zero but an uncontrolled component flows reaching peaks of 200A. The

neutral current is very sensitive to the simulation conditions and this is a characteristic of an uncontrolled low impedance current loop.

[0118] In Figure 16, a proportional controller is introduced with a K_p of 0.002. The controller is switched. It is operational from t=0 to t=0.04s. It is then turned off until t=0.05s. At the instant when the controller is switched off, the circulating current immediately begins to rise. When the control is reactivated, the circulating currents are rapidly suppressed and the control response is a well damped exponential, characteristic of a first order system.

[0119] Figure 17 shows the neutral currents and the outputs of the proportional controllers. The proportional gain is $K_p = 0.002$ and the controller output is limited to the range (-0.1,0.1). The saturation points correspond to a neutral voltage offset of 100V for a 1000V bus. The limits are reached for a circulating current of 50A and the effective "synthetic resistance" introduced is 2Ω.

[0120] The controller is disconnected at t=0.04s until t=0.05s. Prior to disconnection the neutral currents are well controlled and very close to zero. Upon the disconnection of the controllers, the neutral currents immediately start to diverge. At approximately 0.047s the neutral currents exceed 50A and the proportional controls are saturated. Once the controls are reconnected, the circulation current is rapidly decreased.

[0121] In normal operation the controller outputs are a less than 0.001 which equates to an average neutral voltage term of less than 1V, or <0.1%, after the modulator gain. The proportional gain $K_p = 0.002$ introduces an effective resistance of 2Ω in each half of the circulating current loop. The circulating currents are less than 0.5A.

[0122] The proportional only control appears to be very effective and, given its simplicity, is likely to be robust. It is re-emphasised that early experiments with PI controls produced undesirable effects. The two integrators, one per inverter, could take up steady state offsets which resulted in sustained neutral offsets in each inverter. This is not desirable as it limits the available phase to neutral voltage range.

[0123] Figure 18 shows the results for two parallel inverters operating with cases that might be expected to disturb the neutral current. The inverters operate with unbalanced current

demands from t=0s. Phase C is reduced to 20Ap. The neutral currents for the two inverters are balanced and no circulation current flows. The controller is again switched off at 0.04s to 0.05s to illustrate it is active. When the control is off, the neutral currents are seen to start diverging. Restoration of the control quickly rebalances the neutral currents.

[0124] At t=0.07s an output fault is applied from phase A to the neutral at the combined inverter terminals. The phase A voltage is zero from t=0.07s until t=0.085s when the fault initiating breaker recovers. There is no neutral current response.

[0125] Figure 19 shows the experimental results obtained for two parallel inverters operating with the proposed current control. The peak neutral currents from inverter 1 and 2 are 1.7 and 1.3 A respectively. This amount shows that the proposed controller has managed to limit the circulating current within the limit which will not cause any damage to the inverter itself.

Conclusions

[0126] The parallel connection of two STATCOMS on a common dc bus increases the degrees of freedom which need to be controlled for the inverter output currents. Parallel connected STATCOMS with the existing three degree of freedom phase current controllers are highly susceptible to circulating currents in the neutral path. These currents are potentially large enough to be destructive.

[0127] The circulating current between two inverters can be easily, and most obviously, detected as the difference in neutral currents. This detection method would require that both neutral currents are available to each inverter and this imposes a communications requirement. The circulating current can be determined in an alternative way. It is equal to the sum of the inverter four wire currents. These are all local variables and an inverter can be equipped with a local controller to limit the circulating current.

[0128] The circulating current is easily supressed by introducing very small neutral offset voltages. These can be produced by adding a small duty cycle offset to the duty cycles of each of the four inverter legs. A proportional (P) controller, driven by the circulating current, has been shown to be a suitable neutral offset controller. It was noted that PI controller, which is often the controller of first choice, has a specific problem related to the integral action which

can result in unnecessary and sustained neutral offset voltages. The proposed control method is verified by the experimental results.

[0129] Throughout this specification and claims which follow, unless the context requires otherwise, the word “comprise”, and variations such as “comprises” or “comprising”, will be understood to imply the inclusion of a stated integer or group of integers or steps but not the exclusion of any other integer or group of integers. As used herein and unless otherwise stated, the term "approximately" means ±20%.

[0130] It must be noted that, as used in the specification and the appended claims, the singular forms “a,” “an,” and “the” include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to “a support” includes a plurality of supports. In this specification and in the claims that follow, reference will be made to a number of terms that shall be defined to have the following meanings unless a contrary intention is apparent.

[0131] It will of course be realised that whilst the above has been given by way of an illustrative example of this invention, all such and other modifications and variations hereto, as would be apparent to persons skilled in the art, are deemed to fall within the broad scope and ambit of this invention as is herein set forth.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1) A method of controlling an electrical power regulating system having a plurality of inverters connected in parallel, the inverters being connected to a common DC supply and live and neutral connections of a power supply network, and each inverter including a switching arrangement, the method including, in one or more electronic processing devices:
   a) independently controlling the switching arrangements of the plurality of inverters to selectively interconnect the DC supply and the live and neutral connections to thereby regulate power in the power supply network;
   b) detecting a circulating current that is circulating though the power supply network, the DC supply, and two or more of the plurality of inverters; and,
   c) controlling the switching arrangement of at least one of the inverters to apply a voltage offset to the neutral connection to thereby suppress the circulating current.
2) A method according to claim 1, wherein the method includes, in the one or more electronic processing devices:
   a) calculating the circulating current; and,
   b) determining the voltage offset based on the calculated circulating current.
3) A method according to claim 2, wherein the method includes in the one or more electronic processing devices, calculating the circulating current value by calculating a sum of currents on the one or more live connections and the neutral connection of one of the plurality of inverters.
4) A method according to claim 1, wherein the method includes, in the one or more electronic processing devices, detecting the circulating current in the electrical power regulating system by:
   a) determining a difference between neutral currents of the plurality of inverters; and,
   b) determining if the difference exceeds a predetermined current.
5) A method according to claim 4, wherein the method includes in the one or more electronic processing devices, determining the difference between neutral currents of the plurality of inverters by measuring currents at respective terminals of the live and neutral connections.
6) A method according to claims 1 to 5, wherein the method includes in the one or more electronic processing devices, controlling the switching arrangement of the at least one of

the inverters to apply the voltage offset by controlling a proportional controller to thereby control a duty cycle offset applied to the live connections.

7) A method according to claim 6, wherein the method includes in the one or more electronic processing devices, controlling the proportional controller by connecting and disconnecting the proportional controller to the neutral connection.

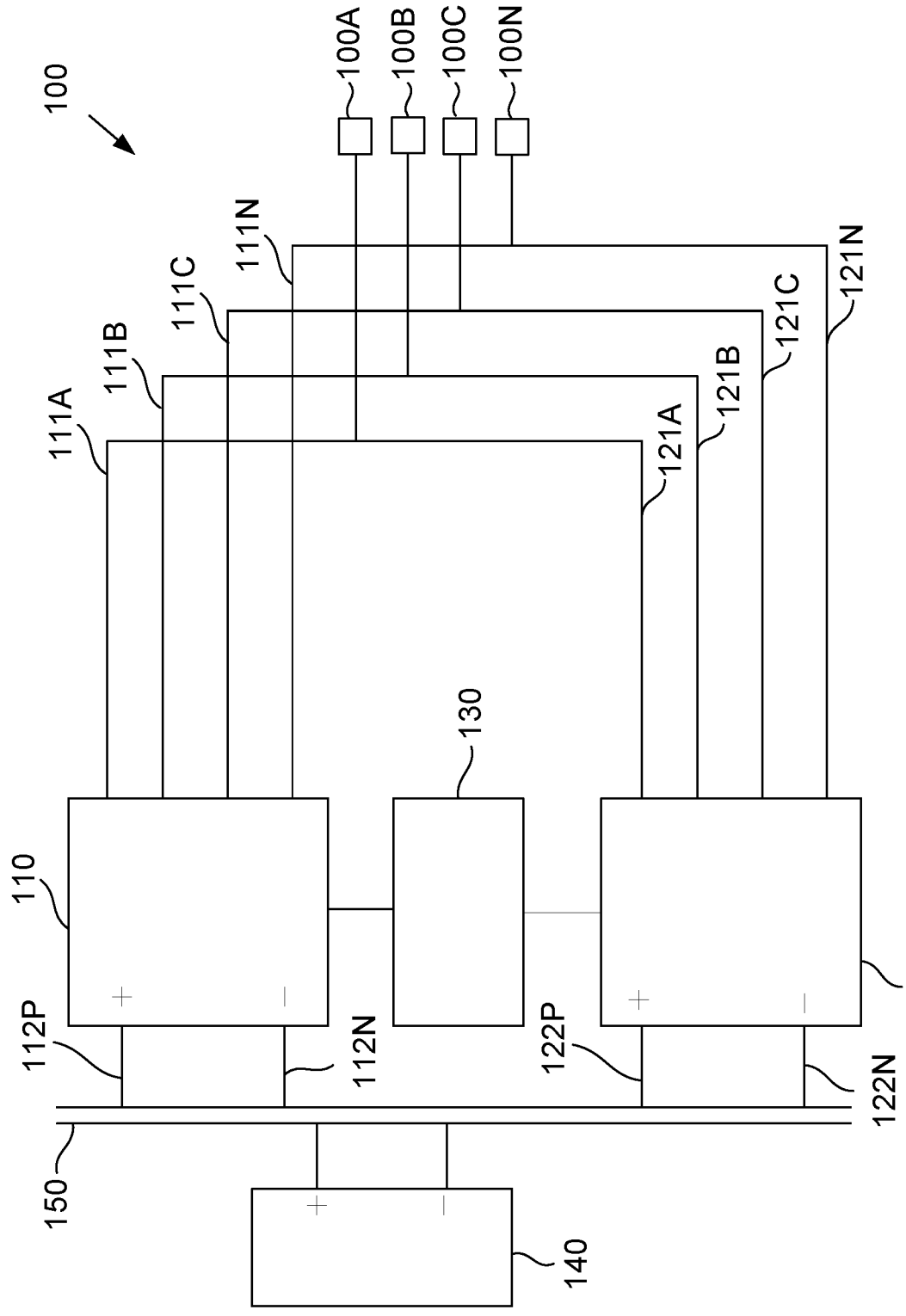
8) A method according to any one of claims 1 to 7, wherein the method includes applying a phase voltage offset to each of the live connections, and the phase voltage offset is at least:
   a) common for all live connections, and
   b) the same as the voltage offset.

9) An inverter, including:
   a) at least one live connections connecting to a power supply system;
   b) a neutral connection connecting to a neutral of the power supply system;
   c) a switching arrangement connected to the at least one live connections and the neutral connection, wherein the switching arrangement includes a proportional controller connected to the neutral connection; and,
   d) one or more electronic processing devices being configured to:
      i) independently control the switching arrangements of the plurality of inverters to selectively interconnect the DC supply and the live and neutral connections to thereby regulate power in the power supply network;
      ii) detect a circulating current that is circulating though the power supply network, the DC supply, and two or more of the plurality of inverters; and,
      iii) control the proportional controller to apply a voltage offset to the neutral connection to thereby suppress the circulating current.

10) An inverter according to claim 9, wherein the one or more processing devices are configured to:
   a) calculate the circulating current; and,
   b) determine the voltage offset based on the calculated circulating current.

11) An inverter device according to claim 10, wherein the one or more processing devices are configured to calculate the circulating current value by calculating a sum of currents on the one or more live connections and the neutral connection of one of the plurality of inverters.

12) An inverter according to claim 9, wherein the one or more electronic processing devices are configured to detect the circulating current in the electrical power regulating system by:
    a) determining a difference between neutral currents of the plurality of inverters; and,
    b) determining if the difference exceeds a predetermined current.
13) An inverter according to claim 12, wherein the one or more electronic processing devices are configured to determine the difference between neutral currents of the plurality of inverters by measuring currents at respective terminals of the live and neutral connections.
14) An inverter according to claims 9 to 13, wherein the one or more electronic processing devices are configured to control the proportional controller to control a duty cycle offset applied to the live connections.
15) An inverter according to claim 14, wherein the one or more electronic processing devices are configured to control the proportional controller by connecting and disconnecting the proportional controller to the neutral connection.
16) An inverter according to any one of claims 9 to 15, wherein the one or more electronic processing devices are configured to apply a phase voltage offset to each of the live connections, and the phase voltage offset is at least:
    a) common for all live connections, and
    b) the same as the voltage offset.


100
100A
100B
100C
100N
111N
111C
111B
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121C
121B
121A
130
110
120
112P
112N
122P
122N
150
140

Fig. 1

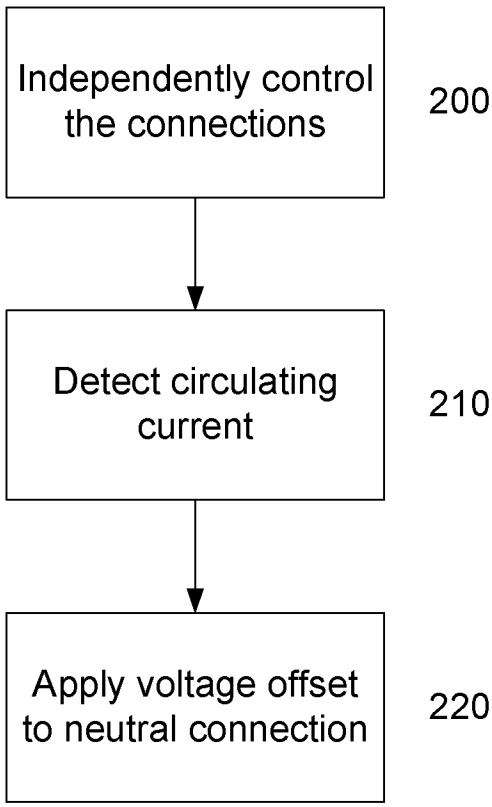
Independently control the connections
200
Detect circulating current
210
Apply voltage offset to neutral connection
220

Fig. 2

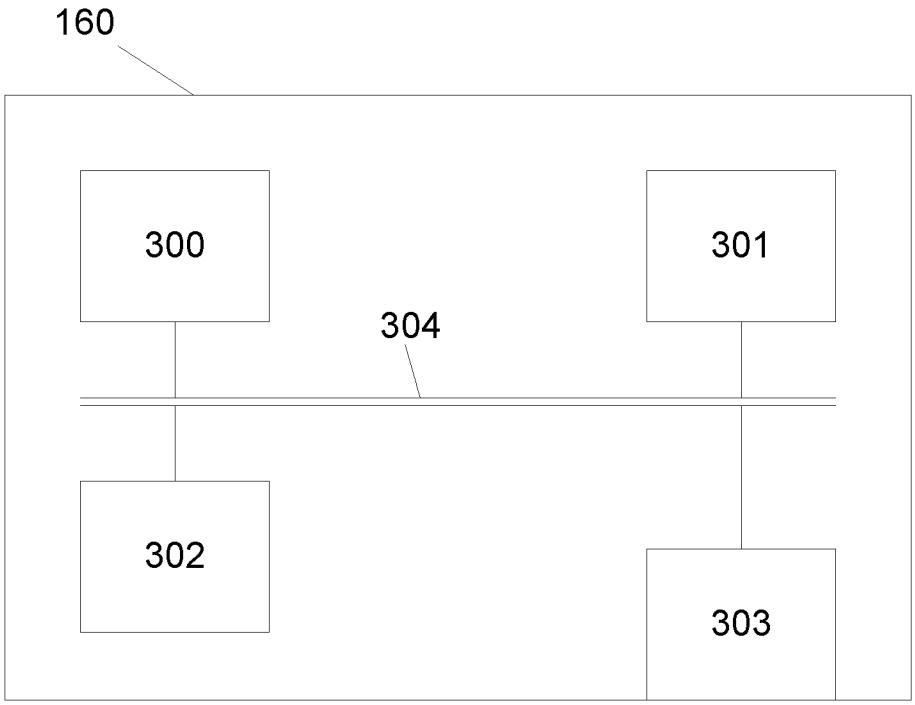

Fig. 3

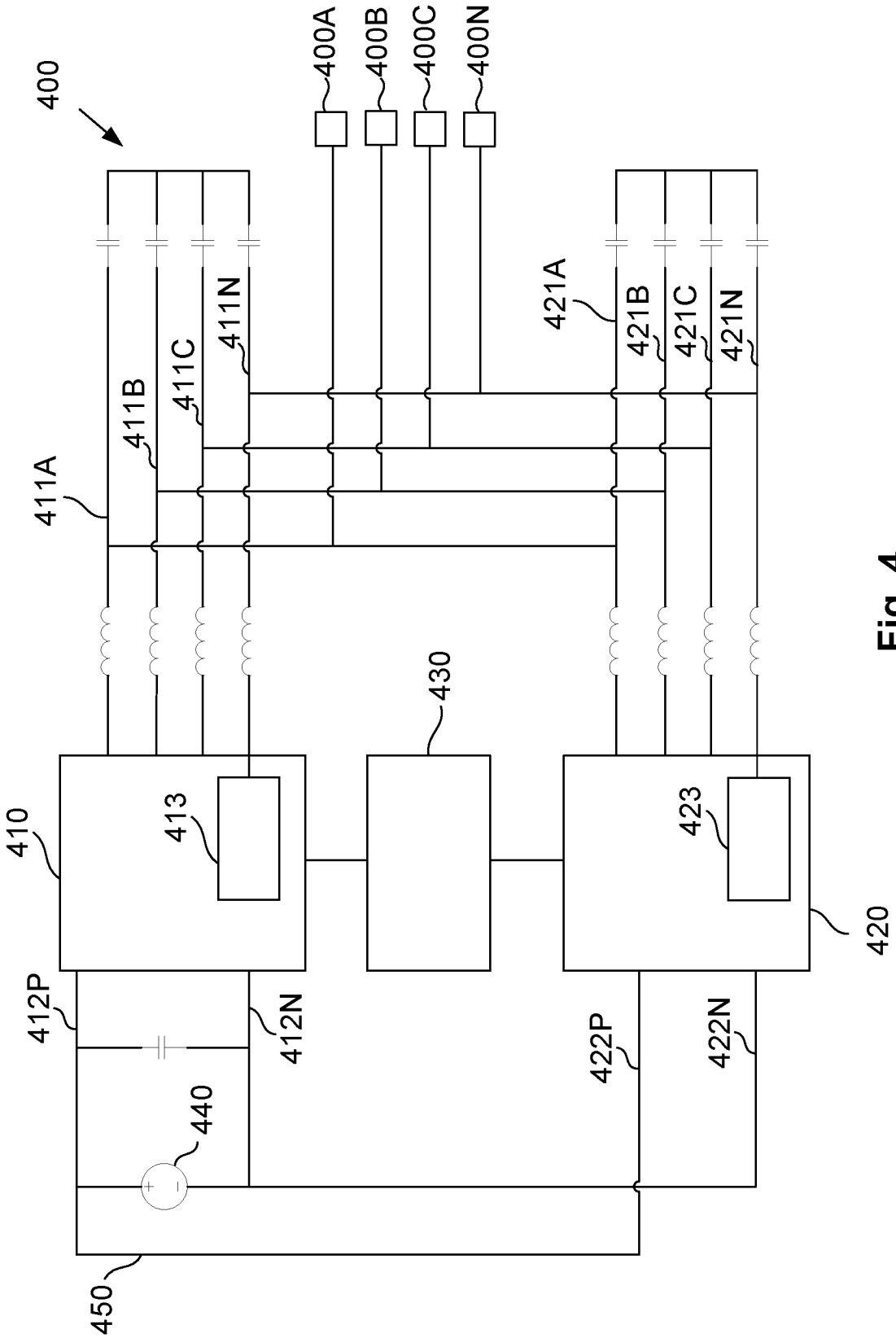
400
400A
400B
400C
400N
411A
411B
411C
411N
421A
421B
421C
421N
410
413
430
420
423
412P
412N
422P
422N
440
450

Fig. 4

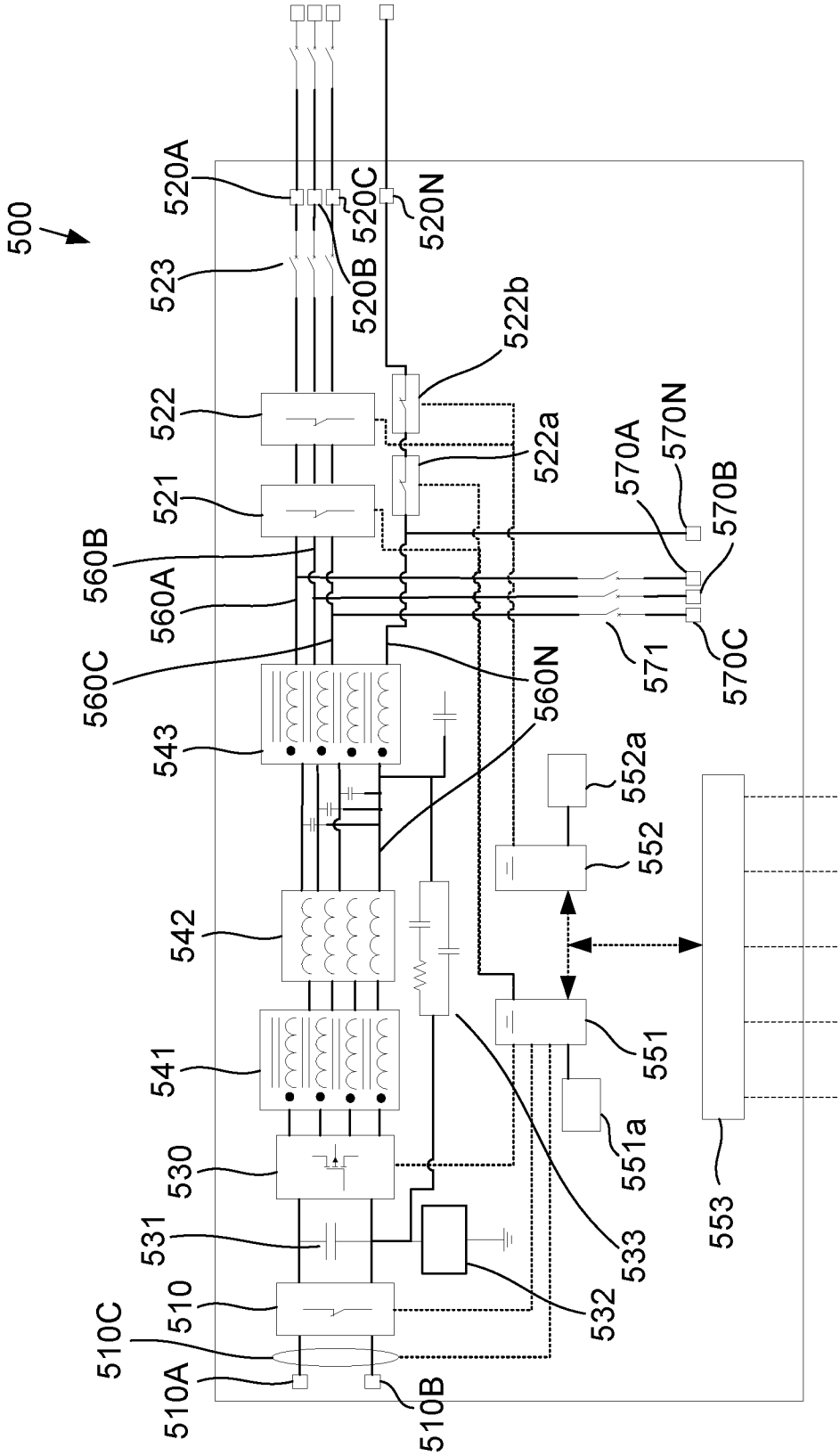
500
520A
520B
520C
520N
523
522b
522
522a
521
570A
570N
570B
560B
560A
560C
560N
571
570C
543
552a
552
542
541
551
551a
553
530
531
533
532
510
510C
510A
510B

Fig. 5

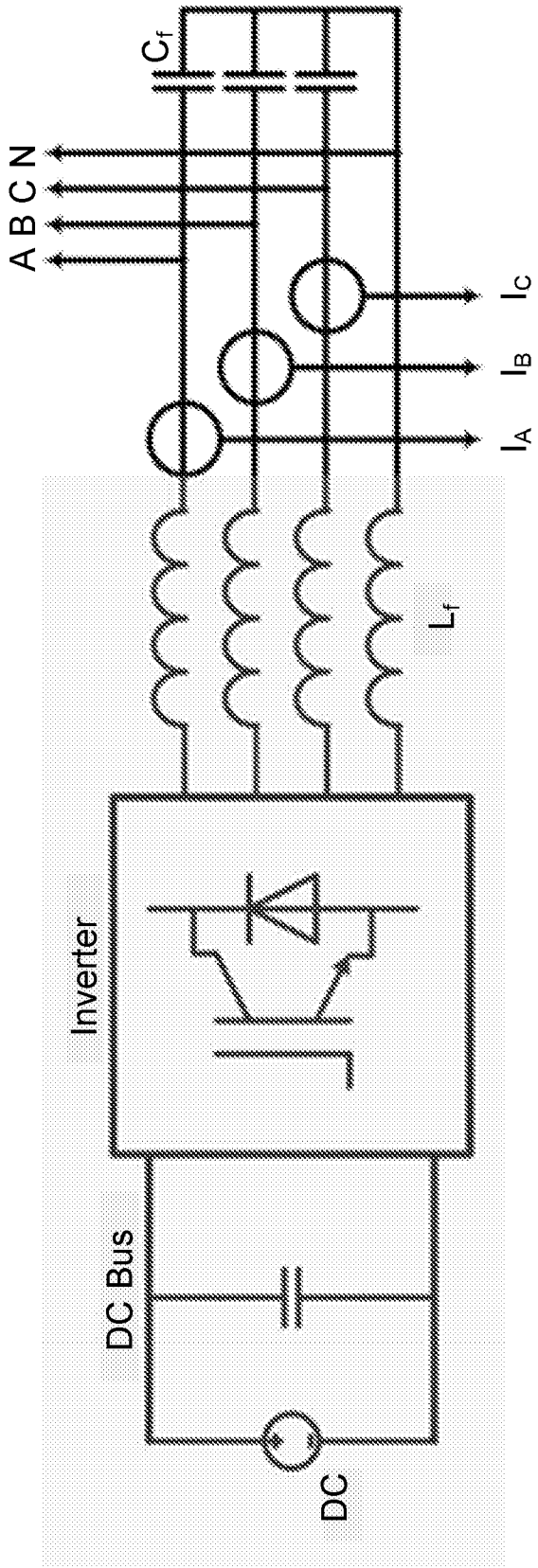

Fig. 6

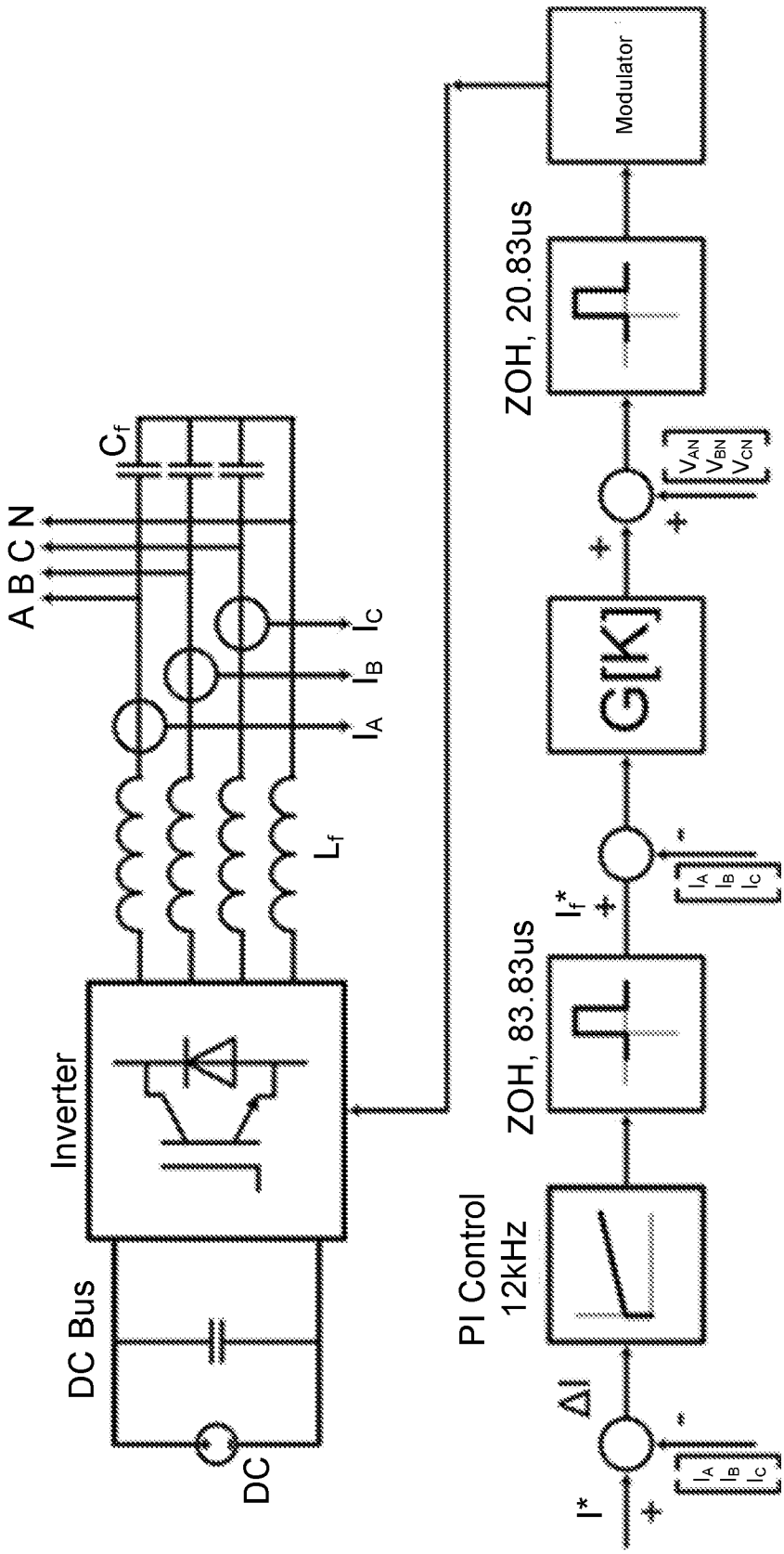
Modulator
ZOH, 20.83us
G[K]
ZOH, 83.83us
PI Control
12kHz
Inverter
DC Bus
DC
A B C N
C_f
L_f
I_A I_B I_C
V_{AN} V_{BN} V_{CN}
I_f^*
ΔI
I*

Fig. 7

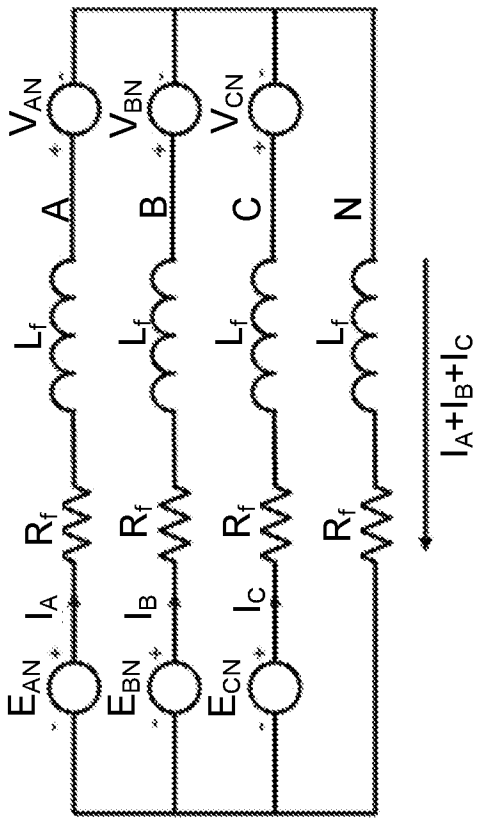
V_{AN}
V_{BN}
V_{CN}
A
B
C
N
L_f
R_f
I_A
I_B
I_C
E_{AN}
E_{BN}
E_{CN}
$I_A+I_B+I_C$

Fig. 8

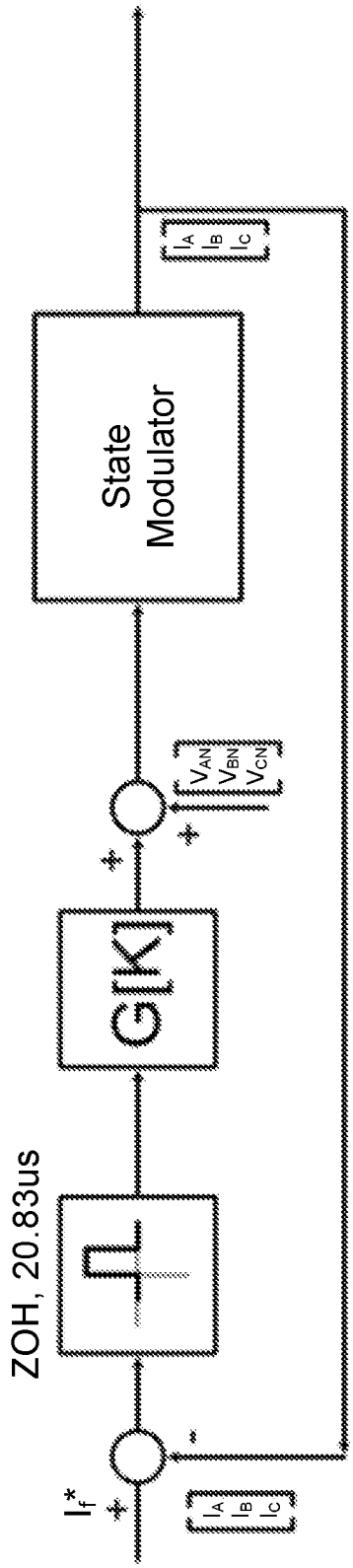
State Modulator
G[K]
ZOH, 20.83us
I_f^*
V_{AN} V_{BN} V_{CN}
I_A I_B I_C

Fig. 9

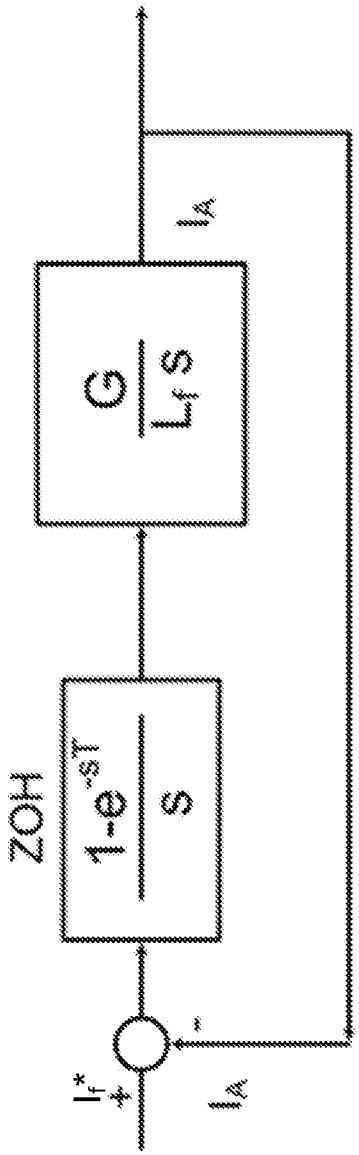
ZOH
1-e^-sT / s
G / L_f s
I_A
I_f*
+
-
I_A

Fig. 10

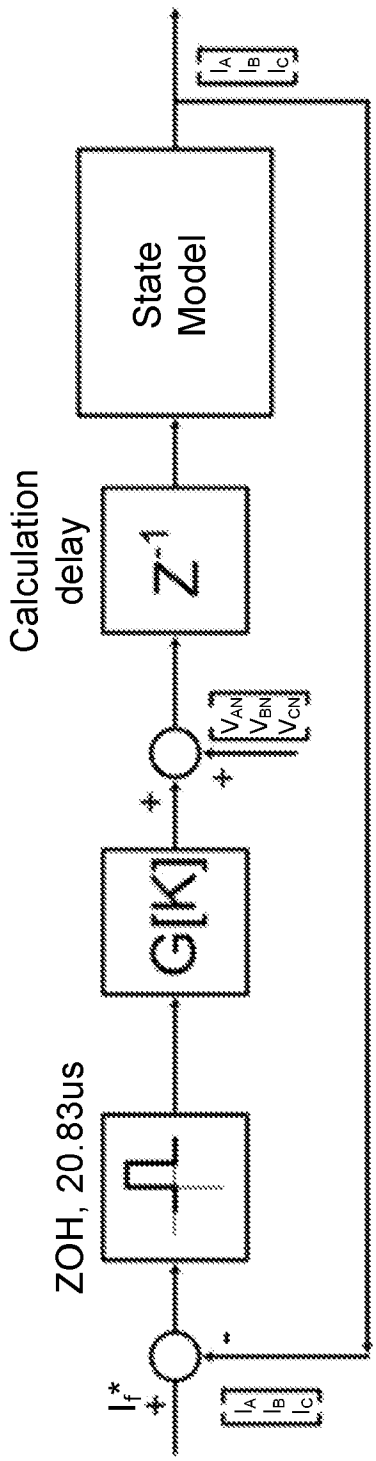
State Model
Calculation delay
Z^-1
G[K]
ZOH, 20.83us
I_A I_B I_C
V_AN V_BN V_CN
I_f*
+
-

Fig. 11

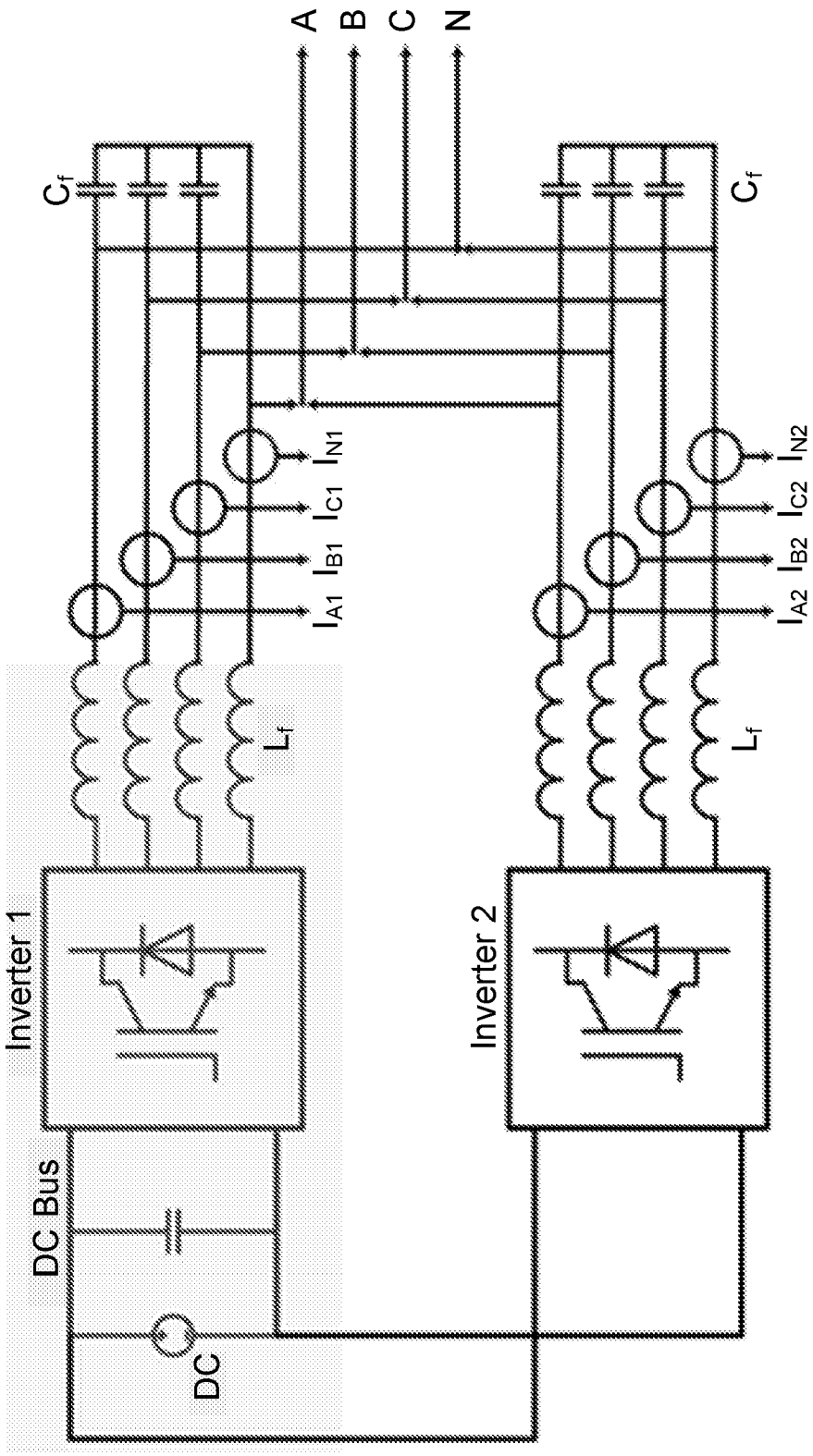
A
B
C
N
C_f
C_f
I_{N1}
I_{C1}
I_{B1}
I_{A1}
I_{N2}
I_{C2}
I_{B2}
I_{A2}
L_f
L_f
Inverter 1
Inverter 2
DC Bus
DC

Fig. 12

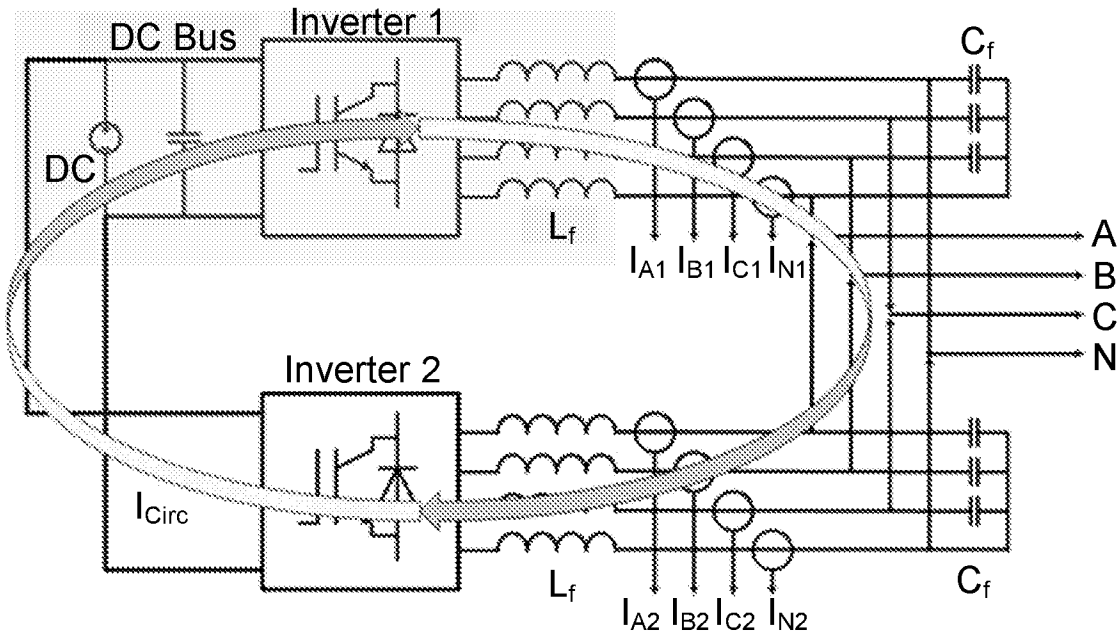
DC Bus
Inverter 1
DC
C_f
L_f
I_{A1} I_{B1} I_{C1} I_{N1}
A
B
C
N
Inverter 2
I_{Circ}
L_f
I_{A2} I_{B2} I_{C2} I_{N2}
C_f

Fig. 13

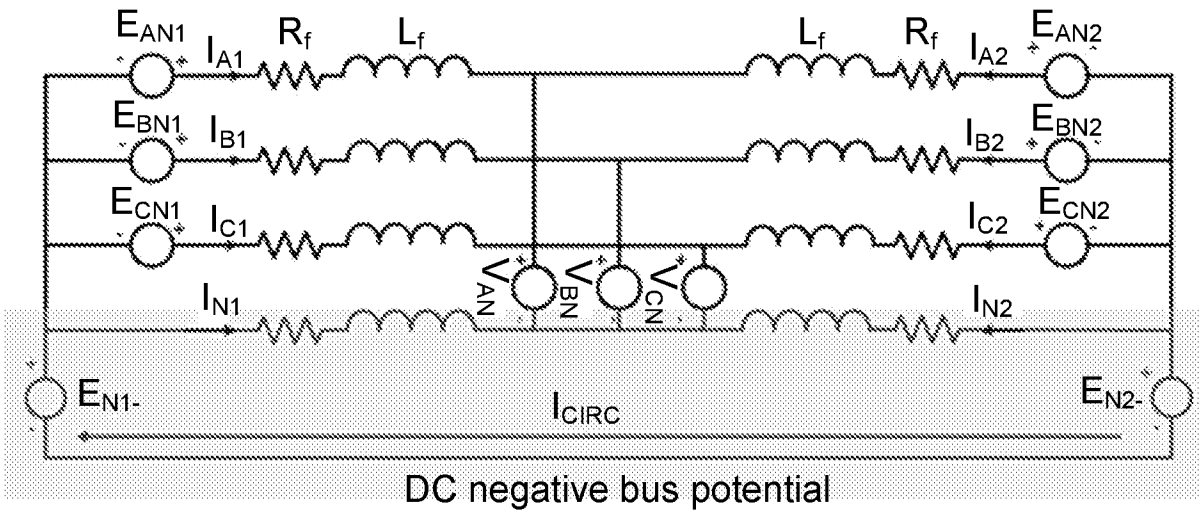
E_{AN1} I_{A1} R_f L_f
L_f R_f I_{A2} E_{AN2}
E_{BN1} I_{B1}
I_{B2} E_{BN2}
E_{CN1} I_{C1}
I_{C2} E_{CN2}
V_{AN} V_{BN} V_{CN}
I_{N1}
I_{N2}
E_{N1-}
I_{CIRC}
E_{N2-}
DC negative bus potential

Fig. 14

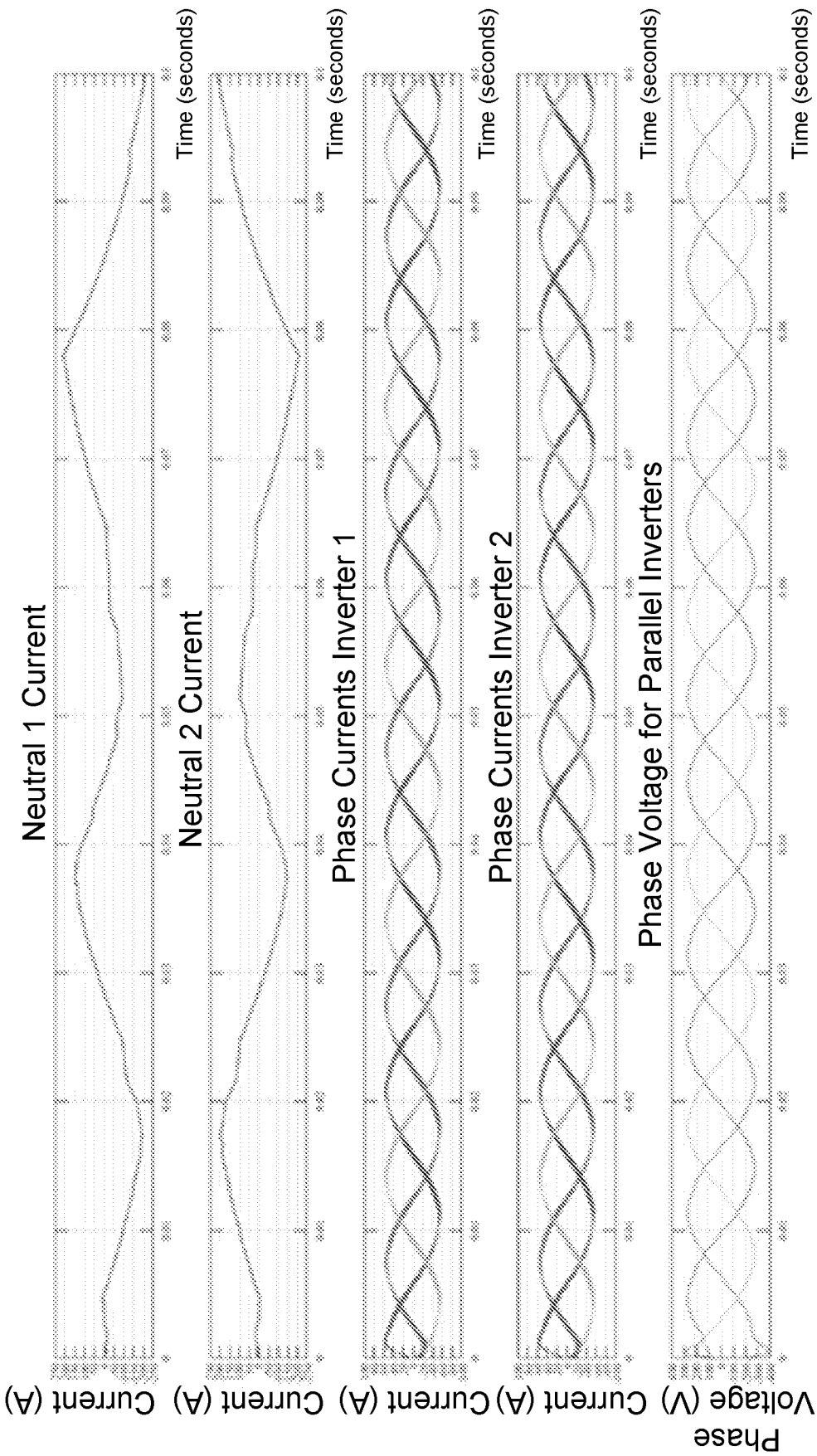
Neutral 1 Current
Current (A)
Time (seconds)
Neutral 2 Current
Current (A)
Time (seconds)
Phase Currents Inverter 1
Current (A)
Time (seconds)
Phase Currents Inverter 2
Current (A)
Time (seconds)
Phase Voltage for Parallel Inverters
Phase Voltage (V)
Time (seconds)

Fig. 15

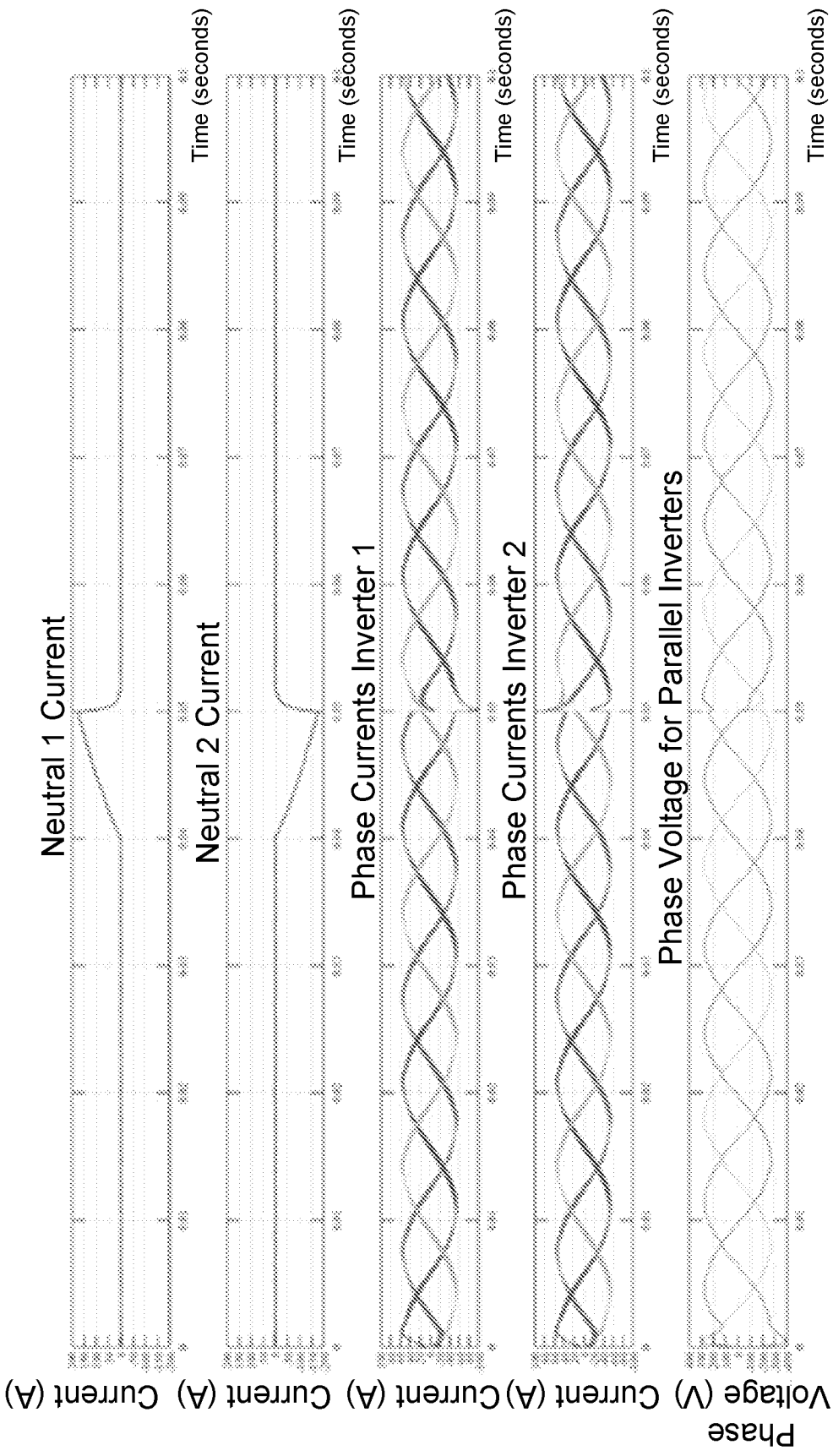
Neutral 1 Current
Current (A)
Time (seconds)
Neutral 2 Current
Current (A)
Time (seconds)
Phase Currents Inverter 1
Current (A)
Time (seconds)
Phase Currents Inverter 2
Current (A)
Time (seconds)
Phase Voltage for Parallel Inverters
Voltage (V)
Time (seconds)

Fig. 16

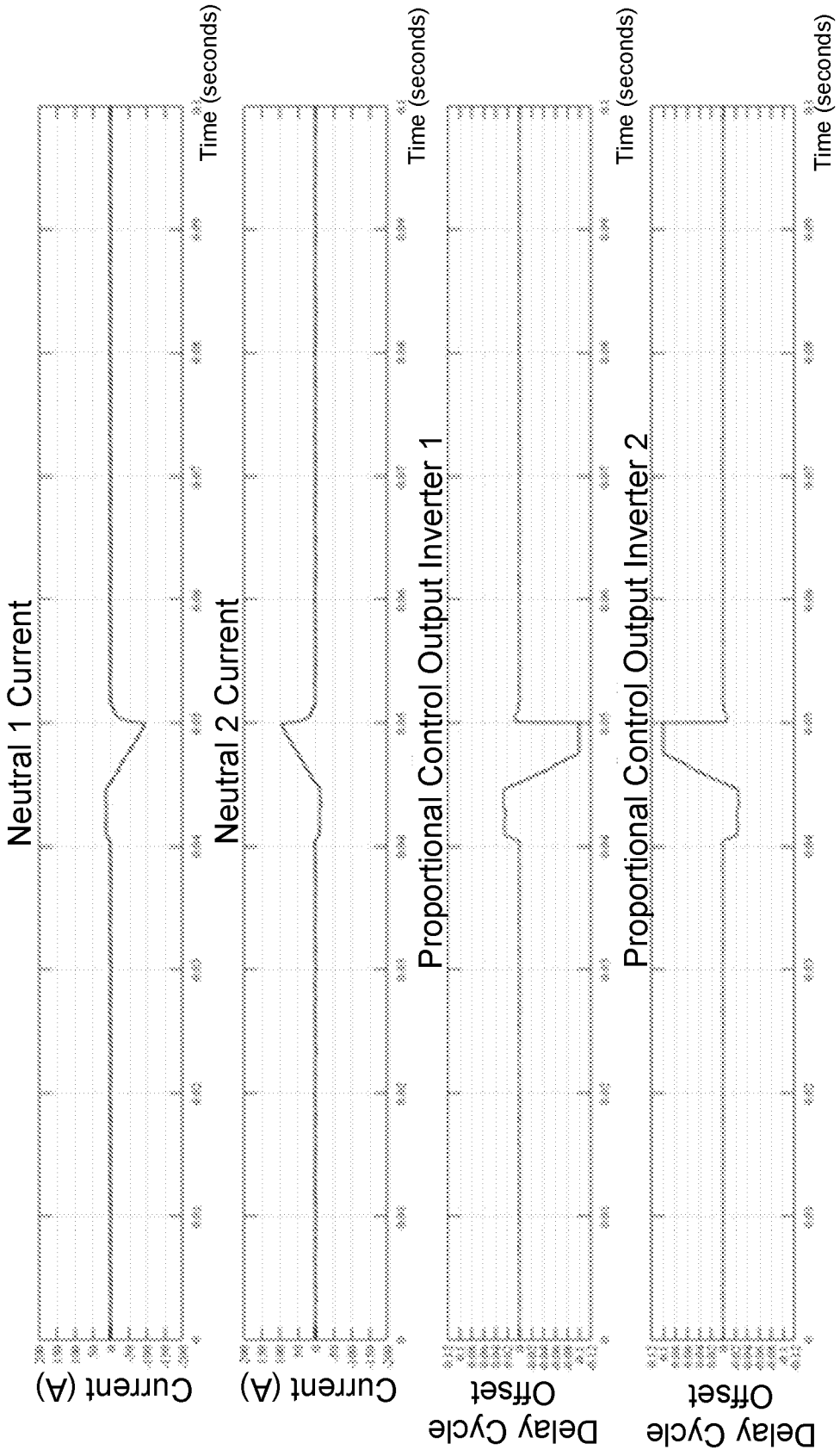
Neutral 1 Current
Current (A)
Time (seconds)
Neutral 2 Current
Current (A)
Time (seconds)
Proportional Control Output Inverter 1
Delay Cycle Offset
Time (seconds)
Proportional Control Output Inverter 2
Delay Cycle Offset
Time (seconds)

Fig. 17

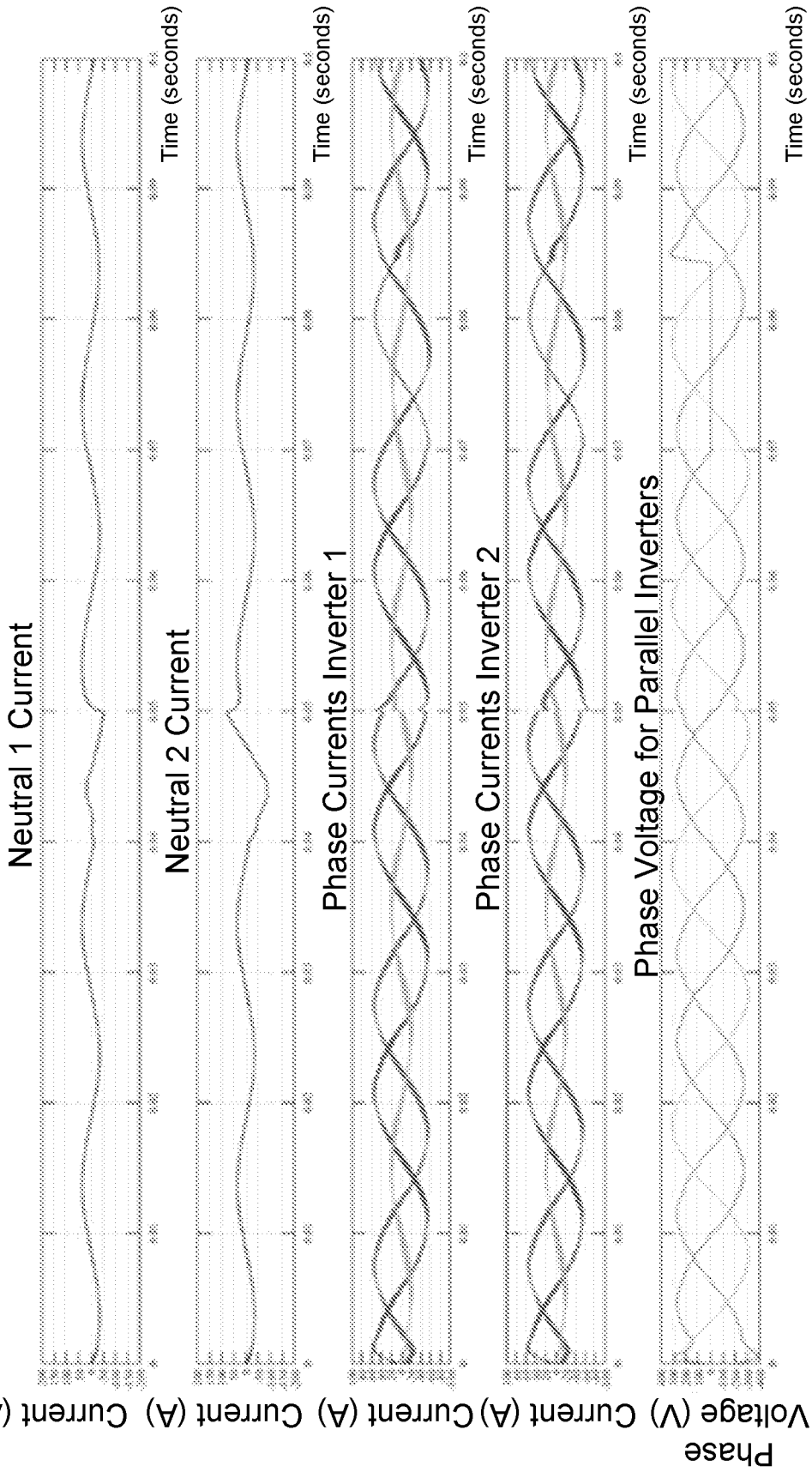
Neutral 1 Current
Current (A)
Time (seconds)
Neutral 2 Current
Current (A)
Time (seconds)
Phase Currents Inverter 1
Current (A)
Time (seconds)
Phase Currents Inverter 2
Current (A)
Time (seconds)
Phase Voltage for Parallel Inverters
Phase Voltage (V)
Time (seconds)

Fig. 18

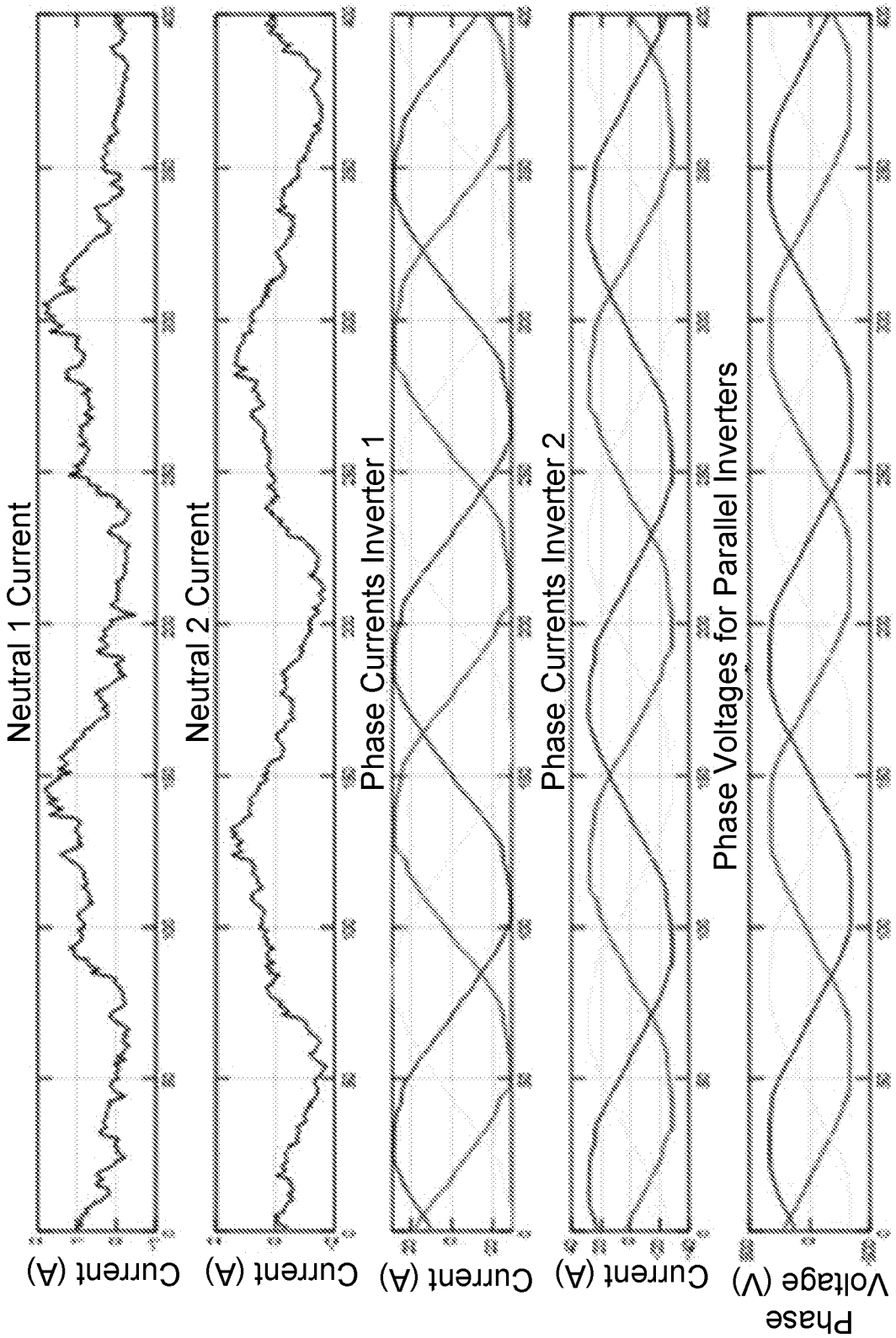
Neutral 1 Current
Current (A)
Neutral 2 Current
Current (A)
Phase Currents Inverter 1
Current (A)
Phase Currents Inverter 2
Current (A)
Phase Voltages for Parallel Inverters
Phase Voltage (V)

Fig. 19

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU2022/050344

A. CLASSIFICATION OF SUBJECT MATTER

H02M 1/00 (2007.01) H02M 7/17 (2006.01) H02J 3/38 (2006.01) H02J 3/00 (2006.01) H02J 3/32 (2006.01) H02J 7/35 (2006.01) H02M 7/06 (2006.01) H02M 3/157 (2006.01) H02M 5/04 (2006.01) H02M 7/493 (2007.01) H02M 1/12 (2006.01) H02M 7/44 (2006.01) H02M 7/487 (2007.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Databases: PATENW (EPODOC, WPIAP, TXTE & TXTMT), GOOGLE PATENTS with IPC/CPC: H02M1/0003, H02M7/17, H02J3/381, H02J3/007, H02J3/32, H02J7/35, H02M1/0009, H02M7/062,H02M1/0006, H02M3/157, H02M5/04, H02M7/493, H02M1/12, H02M7/44, H02M7/487. Databases: PATENW, ESPACENET, GOOGLE PATENTS, GOOGLE, GOOGLE SCHOLAR with keywords:control, electrical, power, regulate, plurality, inverters, parallel, common, DC, supply, live, neutral, switching, selectively, interconnect, detect, circulating, current, voltage, offset, suppress, difference, measure, duty cycle, and the like terms. Applicant(s)/Inventor(s) name searched in DOCDB, DWPI and IP Australia internal databases.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Documents are listed in the continuation of Box C	

[X] Further documents are listed in the continuation of Box C

[X] See patent family annex

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"D" document cited by the applicant in the international application

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 June 2022	20 June 2022

Name and mailing address of the ISA/AU

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Dr. Nahida Akter
AUSTRALIAN PATENT OFFICE
(ISO 9001 Quality Certified Service)
Telephone No. +61262832980

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2016/0373044 A1 (DELTA ELECTRONICS, INC.) 22 December 2016 Whole document in particular Abstract, Figs. 4, 5, 8-1 to 8-2, Para [0010]-[0011], [0023]-[0029], claim 7.	1-16
X	US 9.450,514 B2 (ABB OY) 20 September 2016 Whole document in particular Abstract, Summary, Figs. 1a, 1b, Col. 3 - Col. 6.	1-16
X	US 7,327,588 B2 (OLLILA) 05 February 2008 Whole document in particular Abstract, Col. 3 - Col. 5.	1-16
A	US 2017/0201189 A1 (SUNGROW POWER SUPPLY CO., LTD.) 13 July 2017 Whole document	1-16
A	US 2008/0298103 A1 (BENDRE et al.) 04 December 2008 Whole document	1-16

INTERNATIONAL SEARCH REPORT Information on patent family members	International application No. **PCT/AU2022/050344**

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Patent Document/s Cited in Search Report		Patent Family Member/s	
Publication Number	**Publication Date**	**Publication Number**	**Publication Date**
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		US 9621103 B2	11 Apr 2017
		TW I535183 B	21 May 2016
		TW 201701581 A	01 Jan 2017
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		CN 104638963 B	18 Aug 2017
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		FI 20136117 A	15 May 2015
		FI 125100 B	15 Jun 2015
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		EP 1575156 B1	17 Jun 2015
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		EP 3188336 B1	12 Feb 2020
		JP 2017524322 A	24 Aug 2017
		JP 6364669 B2	01 Aug 2018
		WO 2016029714 A1	03 Mar 2016
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		US 7920393 B2	05 Apr 2011
		EP 2160828 A1	10 Mar 2010
		EP 2160828 B1	04 May 2016
		JP 2010529821 A	26 Aug 2010
		JP 5474772 B2	16 Apr 2014
		WO 2008151145 A1	11 Dec 2008

End of Annex

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

INTERNATIONAL SEARCH REPORT Information on patent family members	International application No. **PCT/AU2022/050344**

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Patent Document/s Cited in Search Report		Patent Family Member/s	
Publication Number	**Publication Date**	**Publication Number**	**Publication Date**

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.