

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
25 January 2007 (25.01.2007)

PCT

(10) International Publication Number
WO 2007/011371 A1

(51) International Patent Classification:
G05F 1/575 (2006.01) **H02M 3/156** (2006.01)

(21) International Application Number:
PCT/US2005/032247

(22) International Filing Date:
8 September 2005 (08.09.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/180,556 14 July 2005 (14.07.2005) US

(71) Applicant (for all designated States except US): **LINEAR TECHNOLOGY CORPORATION** [US/US]; 1630 McCarthy Boulevard, Milpitas, CA 95035 (US).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **LIAO, Chiawei** [US/US]; 6490 Graystone Meadow Circle, San Jose, CA 95120 (US).

(74) Agents: **BECKER, Stephen, A.** et al.; McDermott Will & Emery LLC, 600 13th Street, N.W., Washington, DC 20005-3096 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

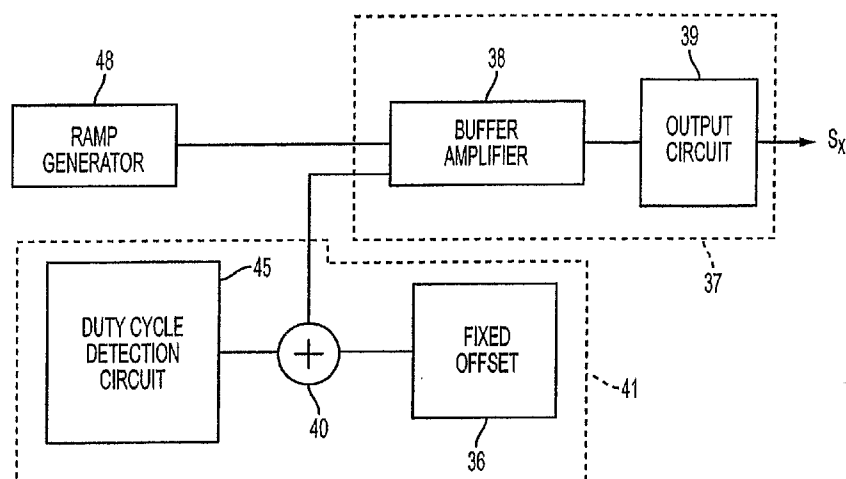
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SWITCHING REGULATOR WITH VARIABLE SLOPE COMPENSATION



(57) Abstract: Controlled compensation for a switching regulator is attained by detecting switching duty cycle of the switching regulator, developing a compensation signal having a time duration that is related to the detected switching duty cycle percentage, and generating a duty cycle control signal for the regulator that is dependent in part on the developed compensation signal. The compensation signal has a slope profile and is initiated during each switching cycle at a set point in the cycle that is related to the switching duty cycle percentage.

WO 2007/011371 A1

SWITCHING REGULATOR WITH VARIABLE SLOPE COMPENSATION

Technical Field

[01] This disclosure is related to switching regulators, and more particularly to compensating control of the switching duty cycle.

Background

[02] The use of current mode switching regulators to control a DC output voltage at a level higher than, lower than, or the same as an input voltage is well known. Typically, one or more switches are activated to supply current pulses via an inductor to charge an output capacitor. The output voltage level is maintained at a desired level by adjusting the on and off times of the switching pulses in accordance with output voltage and load conditions.

[03] Fig. 1 is a block diagram of a typical current mode switching regulator. Switching control circuit 10 may comprise any of various known controllers that provide pulse width modulated output pulses to regulate a DC output voltage V_{OUT} at a level that may be greater than, lower than, or the same as a nominal input voltage V_{IN} . Typically, the control circuit includes a latch, having set and reset inputs, coupled to a controlled switch that supplies switched current I_{SW} to inductor 12. Capacitor 14 is connected between the output V_{OUT} and ground. Resistors 16 and 18 are connected in series between V_{OUT} and ground. A load 20 is supplied from the regulator output.

[04] The set input is coupled to clock 22, which may generate pulses in response to an oscillator, not shown. During normal operation, the latch is activated to initiate a switched current pulse when

the set input receives each clock pulse. The switched current pulse is terminated when the reset input receives an input signal, thereby determining the width of the switched current pulse. The reset input is coupled to the output of comparator 24. An output voltage feedback signal V_{FB} is taken at the junction of resistors 16 and 18 and coupled to negative input of error amplifier 26. A voltage reference V_{REF} is applied to the positive input of error amplifier 26. Capacitor 28 is coupled between the output of error amplifier 26 and ground.

[05] The level of charge of capacitor 28, and thus its voltage V_C , is varied in dependence upon the output of amplifier 26. As load current increases, the output voltage, and thus V_{FB} , decreases. As the feedback voltage V_{FB} decreases, V_C increases. Thus, V_C is proportional to load current. V_C is coupled to the inverting input of comparator 24. The non-inverting input is coupled to adder 30. Adder 30 combines signal I_{sw} , which is proportional to the sensed switch current, with a compensation signal. Upon switch activation in response to a clock set signal, switch current builds through inductor 12. When the level of the signal received from adder 30 exceeds V_C , comparator 24 generates a reset signal to terminate the switched current pulse. During heavier loads V_C increases and the switched current pulse accordingly increases in length to appropriately regulate the output voltage V_{OUT} . As V_C is an indication of load, it can be monitored by internal circuitry, not shown, to detect light load conditions. In response to V_C reaching a predetermined light load condition threshold, the operation can be changed to a "sleep mode," in which some circuit elements can be deactivated to consume power.

[06] For normal regulator operation at duty cycles of fifty percent or higher, compensation is needed in the switching control to avoid sub-harmonic oscillation. A typical approach is termed "slope compensation," wherein a signal of increasing magnitude is added to the current signal I_{sw} , or subtracted from the signal V_C , during each switching cycle. Fig. 2 is a circuit diagram of a prior

art slope compensation generator that may be input to adder 30 to modify the current signal applied to the non-inverting input of comparator 24. The output of the circuit is a current signal S_x corresponding to the current in the series circuit path of transistor 32, resistor 34 (R) and voltage bias (V_B) source 36. The base of transistor 32 is coupled to the output of unity gain buffer amplifier 38. The positive input of amplifier 38 is coupled to receive a ramp signal V_{ramp} . The negative input of amplifier 38 is coupled to the junction between transistor 32 and resistor 34.

[07] Fig. 3 is a simplified waveform diagram illustrative of the compensation function of the circuit of Fig. 2. The V_{ramp} signal is a sawtooth format signal that is generated at the beginning of each clock cycle and extends at linear slope to the end of the cycle, corresponding to one hundred percent duty cycle. As an example, the V_{ramp} magnitude may vary between zero and one volt. Transistor 32 begins conduction at a point T_s in the cycle at which V_{ramp} overtakes the fixed voltage V_B . As compensation is needed at fifty percent duty cycle operation or greater, V_B typically is arbitrarily chosen at one half the value of the maximum V_{ramp} level, or one half-volt in the present example. As V_{ramp} continues to increase after time T_s , the base signal applied to transistor 32 increases and, thus, the output current S_x increases linearly to a maximum S_{max} at the end of the switching cycle. S_x is determined by $(V_{ramp} - V_B)/R$. The compensation curve S_x starting point T_s is thus determined by V_B , and its slope is determined by R . In this example T_s occurs at fifty percent of the switching cycle, regardless of the actual duty cycle.

[08] Because this slope compensation curve starts at fifty percent of the switching cycle, the S_x builds up to a high level at a maximum duty cycle of one hundred percent. The high level of the compensation signal is disadvantageous at or near maximum duty cycle operation. The voltage V_C , the output of feedback amplifier 26 applied to the negative input of comparator 24, has the same value as the sum of the switch current I_{SW} and the slope compensation signal I_{sx} at

the positive input of comparator 24 when the switched pulse terminates. As a high offset has been introduced, V_C will not accurately indicate true output load current. At the high duty cycle operation, the switching current limit level is reduced. At higher duty cycle operation, the sleep mode threshold, based on V_C , will be inaccurate. The need thus exists for an improved compensation scheme that overcomes the drawbacks of the prior art slope compensation.

Disclosure

[09] The above-described needs of the prior art are fulfilled, at least in part, by detecting switching duty cycle of a switching regulator, developing a compensation signal having a time duration that is related to the detected switching duty cycle, and generating a duty cycle control signal for the regulator that is dependent in part on the developed compensation signal. The compensation signal has a slope profile and is initiated during each switching cycle at a set point in the cycle that is related to the switching duty cycle.

[10] The duty cycle may be detected by generating a repetitive pulse signal, coordinated with the regulator switching, and integrating the pulse signal. The point in each cycle at which the compensation signal is initiated may be set by generating a ramp signal at the onset of each switching cycle, modifying the duty cycle signal, and comparing the repetitive ramp signal with the modified duty cycle signal. When the ramp signal is equal in magnitude to the modified duty cycle signal, the compensation signal commences. Preferably, the duty cycle signal is modified by offsetting the duty cycle signal by a fixed voltage.

[11] In an exemplified implementation, a variable compensation circuit is coupled to an input of a switching controller input for terminating a switching pulse during each switching cycle. In a preferred configuration, an amplifier circuit output is coupled to the controller input. A ramp

generator provides a ramp signal to an input of the amplifier circuit, and a variable offset circuit provides a variable offset signal to the amplifier input of the amplifier. The variable offset circuit is coupled in series with the amplifier circuit output. The amplifier output signal is proportional to the difference between the ramp signal and the variable offset signal. The compensation circuit thus outputs a signal that has an offset level that varies as a function of the duty cycle of the regulator switching operation.

[12] The amplifier circuit may be configured with an amplifier having a positive input terminal coupled to the ramp generator, a negative input terminal coupled to the variable offset circuit, and an output. A control terminal of a transistor is coupled to the amplifier output. The transistor is coupled between the variable offset circuit and the amplifier circuit output. An impedance is coupled in series with the transistor, thereby determining the slope of the compensation circuit output signal.

[13] The variable offset circuit may be exemplified by a duty cycle detection circuit and a constant offset voltage circuit, each coupled to an adder output circuit is coupled to the amplifier input. The duty cycle detection circuit may include an integrator circuit configured to receive a repetitive pulse signal that is coordinated with the regulator switching.

[14] Additional advantages of the present invention will become readily apparent to those skilled in this art from the following detailed description, wherein only the preferred embodiment of the invention is shown and described, simply by way of illustration of the best mode contemplated of carrying out the invention. As will be realized, the invention is capable of other and different embodiments, and its several details are capable of modifications in various obvious respects, all without departing from the invention. Accordingly, the drawings and description are to be regarded as illustrative in nature, and not as restrictive.

Brief Description of the Drawings

[15] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawing and in which like reference numerals refer to similar elements and in which:

[16] Fig. 1 is a block diagram of a typical current mode switching regulator.

[17] Fig. 2 is a circuit diagram of a prior art slope compensation generator.

[18] Fig. 3 is a simplified waveform diagram illustrative of the compensation function of the circuit of Fig. 2.

[19] Fig. 4 is a block diagram exemplifying slope compensation in accordance with the present invention.

[20] Fig. 5 is a circuit diagram of the slope compensation generator of Fig. 4.

[21] Fig. 6a is a waveform diagram illustrative of various signals of the circuit of Fig. 5. Fig. 6b is a waveform diagram in which the compensation signals of the circuits of Figs. 2 and 5 are compared.

Detailed Description

[22] An underlying concept of the present disclosure is based on the realization that slope compensation is needed only at the instant when the regulator switch turns off. If the regulator of Fig. 2 of the prior art is operating at ninety percent duty cycle, for example, the build up of compensation signal starting at fifty percent is unnecessary until near the ninety percent point. By that time, a substantial offset signal magnitude has been developed. Fig. 4 is a block diagram of a variable compensation circuit that permits generation of the compensation signal to start in advance of the duty cycle by a fixed small value in each switching cycle. With this circuit, the operating duty

cycle is sensed and the slope compensation signal is started only slightly before the regulator switch turns off. The unnecessary slope compensation over lower duty cycles is avoided. Sleep mode level can be detected more accurately. The magnitude of the slope compensation signal at switching pulse termination is at a level that does not significantly lower the switch current limit level.

[23] Amplifier circuit 37 outputs a compensation signal S_x , having a constant slope, that may be coupled as an input to the adder 30 of Fig. 1. Buffer amplifier 38 receives a ramp signal from ramp generator 48. The ramp generator may comprise a well known capacitive circuit that is synchronized with a clock signal to provide a sawtooth type waveform having a constant slope. The buffer amplifier 38 receives a second signal from variable offset circuit 41, which adds, via summer 40, a fixed offset voltage from source 36 to a signal provided by duty cycle detection circuit 45. The output of duty cycle detection circuit 45 is proportional to the regulator duty cycle. The output of the circuit 41 is proportional to the regulator duty cycle offset by the fixed level of the source 36. The output circuit 39 initiates output signal S_x in each cycle when the ramp generator signal exceeds the signal received from variable offset circuit 41. The output signal S_x commences later in a switching cycle for higher duty cycle operation than for lower duty cycle operation and is thus variable with respect to its phase in the switching cycle. There is fixed phase difference between S_x and the operating duty cycle.

[24] Fig. 5 is a partial circuit diagram of the variable compensation circuit of Fig. 4. Transistor 32 is coupled in series with resistor 34 and adder 40. These elements form, in part, the output circuit 39 that produces the compensation signal S_x . A first input of adder 40 is coupled to fixed offset voltage 36. The second input of adder 40 is coupled to buffer 42. The input of buffer 42 is coupled to a junction between resistor 44 and capacitor 46. Buffer 42, resistor 44 and capacitor 46 form the duty cycle detection circuit 45. Voltage signal V_1 is coupled to resistor 44. The positive input of

amplifier 38 is coupled to receive a ramp signal V_{ramp} . The negative input of amplifier 38 is coupled to the junction between transistor 32 and resistor 34.

[25] Reference is made to the waveforms of Fig. 6a in describing the operation of the circuit of Fig. 5. For clarity of explanation, an example is taken in which the regulator is operating at a ninety percent duty cycle and in which the V_{ramp} and V_1 signals have upper and lower limits of one volt and zero volt, respectively. It should be understood that the regulator is capable of operation throughout the complete duty cycle range and that the voltage parameter ranges are subject to selection.

[26] The V_1 signal is a square signal that coincides with the regulator switching. As shown, V_1 is at a level of one volt for ninety percent of the cycle and at zero the last ten percent. This signal is averaged by the integrator formed by resistor 44 and capacitor 46. The voltage at the junction of these two circuit elements thus is 0.9 volt at ninety percent duty cycle. This averaged voltage is buffered by buffer 42 and input to the adder 40 where it is added to the fixed voltage offset of voltage source 36 to provide a voltage V_x at the adder output. In this example, the fixed voltage offset has been selected at -0.1 volt. V_x is thus 0.8 volt. Prior to conduction of transistor 32, the voltages at both the transistor emitter and the negative input of amplifier 38 are at the level of V_x .

[27] The V_{ramp} signal is generated at the start of each clock cycle and increases linearly until the next clock. The slope of this signal is selected such that its magnitude corresponds in number with the duty cycle. That is, for example, V_{ramp} at 0.5 volt occurs at fifty percent duty cycle. When the V_{ramp} signal rises to the level of V_x , amplifier 38 will drive transistor 32 to conduction. As V_{ramp} continues to increase, the voltage applied to the base of transistor 32 continues to increase and its conduction current, S_x , increases. In the illustrated example, the fixed offset voltage of source 36 has been chosen to be -0.1 volt, whereby V_x becomes 0.8 volt. As both voltage inputs to amplifier

are equal at 0.8v, the compensation signal is initiated at eighty percent duty cycle, as illustrated in Fig. 6a. The particular voltage offset selection has been made so that the slope compensation curve starts at only a small percent duty cycle ahead of the regulator operating duty cycle, ten percent in this example. If the duty cycle were to change to seventy percent, V_x would change to 0.6 volt and the compensation signal would commence at sixty percent duty cycle. When the transistor conducts, a voltage drop occurs across resistor 34. The value of resistor 34 is selected to set a slope of S_x so that it is suitable for compensation without reaching a high level having the drawbacks of the prior art.

[28] The waveform diagram of Fig. 6b is illustrative of the compensation signals produced by the prior art circuit of Fig. 2 and the circuit of Fig. 5 for ninety percent duty cycle operation, corresponding to the above described example. Compensation signal S_{x1} of the Fig. 2 circuit commences at fifty percent duty cycle and builds up to a high level at ninety percent duty cycle at which point switch cutoff occurs. At this point, the output current of adder 30 is equal to V_C and comprises a large S_{x1} component. At the illustrated compensation signal slope, the S_{x1} component appears to be approximately eighty percent of the magnitude of the V_{ramp} signal and a significantly large value in comparison with the V_C level. In contrast, compensation signal S_{x2} of the circuit of Fig. 5 commences at eighty percent duty cycle with the same slope. At the ninety percent duty cycle cutoff, the S_{x2} component of the output of adder 30 appears to be approximately twenty percent of the magnitude of the V_{ramp} signal. As a result, the accuracy of V_C as an indicator of output load current and the switching current limit level are greatly improved.

[29] In this disclosure there are shown and described only preferred embodiments of the invention and but a few examples of its versatility. It is to be understood that the invention is capable of use in various other combinations and environments and is capable of changes or

modifications within the scope of the inventive concept as expressed herein. The principles of the invention are applicable to a variety of voltage regulators, including buck, boost, and buck-boost regulators. By appropriate selection of the parameters of the resistor 34, the duty cycle detection elements, and the operating voltage levels, the slope of S_x and its onset in relation to duty cycle operation can be adjusted to desired levels.

CLAIMS

What is claimed is:

1. A switching regulator, comprising:

a switching controller having an input configured to receive a signal for terminating a switching pulse during a regulator switching cycle to establish regulator duty cycle, and an output to which a load may be coupled;

a variable compensation circuit coupled to the controller input;

wherein the compensation circuit is configured to output a signal that varies as a function of the regulator duty cycle.

2. A switching regulator as recited in claim 1, wherein the compensation circuit comprises:

an amplifier circuit having an output coupled to the controller input;

a ramp generator coupling a ramp signal the amplifier circuit; and

a variable offset circuit coupling a variable offset signal to the amplifier;

wherein an output signal of the amplifier is proportional to the difference between the ramp signal and the variable offset signal.

3. A switching regulator as recited in claim 2, wherein the variable offset circuit is coupled in series with the amplifier circuit output.

4. A switching regulator as recited in claim 3, wherein the amplifier circuit comprises:
an amplifier having a positive input terminal coupled to the ramp generator, a negative input terminal coupled to the variable offset circuit, and an output; and
a transistor having a control terminal coupled to the amplifier output;
wherein the transistor is coupled between the variable offset circuit and the amplifier circuit output.

5. A switching regulator as recited in claim 4, wherein the amplifier circuit further comprises an impedance coupled in series with the transistor; and
the compensation circuit output signal has a slope that is fixed in accordance with the value of the impedance and is repeated in each switching cycle.

6. A switching regulator as recited in claim 2, wherein the variable offset circuit comprises:
a duty cycle detection circuit;
a constant offset voltage circuit; and
an adder having a first input coupled to the duty cycle detection circuit, a second input coupled to the constant voltage circuit, and an output circuit coupled to the amplifier input.

7. A switching regulator as recited in claim 6, wherein the duty cycle detection circuit comprises:
an integrator circuit configured to receive a repetitive pulse signal that is synchronized with the regulator switching.

8. In a switching regulator, a method comprising:
detecting a switching duty cycle of the regulator;
developing a compensation signal is related to the detected switching duty cycle; and
generating a duty cycle control signal for the regulator that is dependent in part on the
developed compensation signal.

9. A method as recited in claim 8, wherein the compensation is repeated in each
switching cycle of the regulator and the duration of the compensation signal in each switching
cycle is related to the detected switching duty cycle.

10. A method as recited in claim 8, wherein the compensation signal comprises a slope
profile and the step of developing comprises initiating the compensation signal during each
switching cycle at a set point in the cycle that is related to the switching duty cycle.

11. A method as recited in claim 10, wherein the step of detecting comprises:
generating a repetitive pulse signal in accordance with regulator switching; and
integrating the pulse signal to obtain a signal indicative of duty cycle.

12. A method as recited in claim 11, wherein the step of initiating comprises:
generating a ramp signal at the onset of each switching cycle;
modifying the duty cycle signal; and
comparing the repetitive ramp signal with the modified duty cycle signal;
wherein the set point is the point in each switching cycle at which the ramp signal is equal

in magnitude to the modified duty cycle signal.

13. A method as recited in claim 12, wherein the step of modifying comprises offsetting the duty cycle signal by a fixed amount.

14. A method as recited in claim 12, further comprising the step of fixing the slope of the compensation signal.

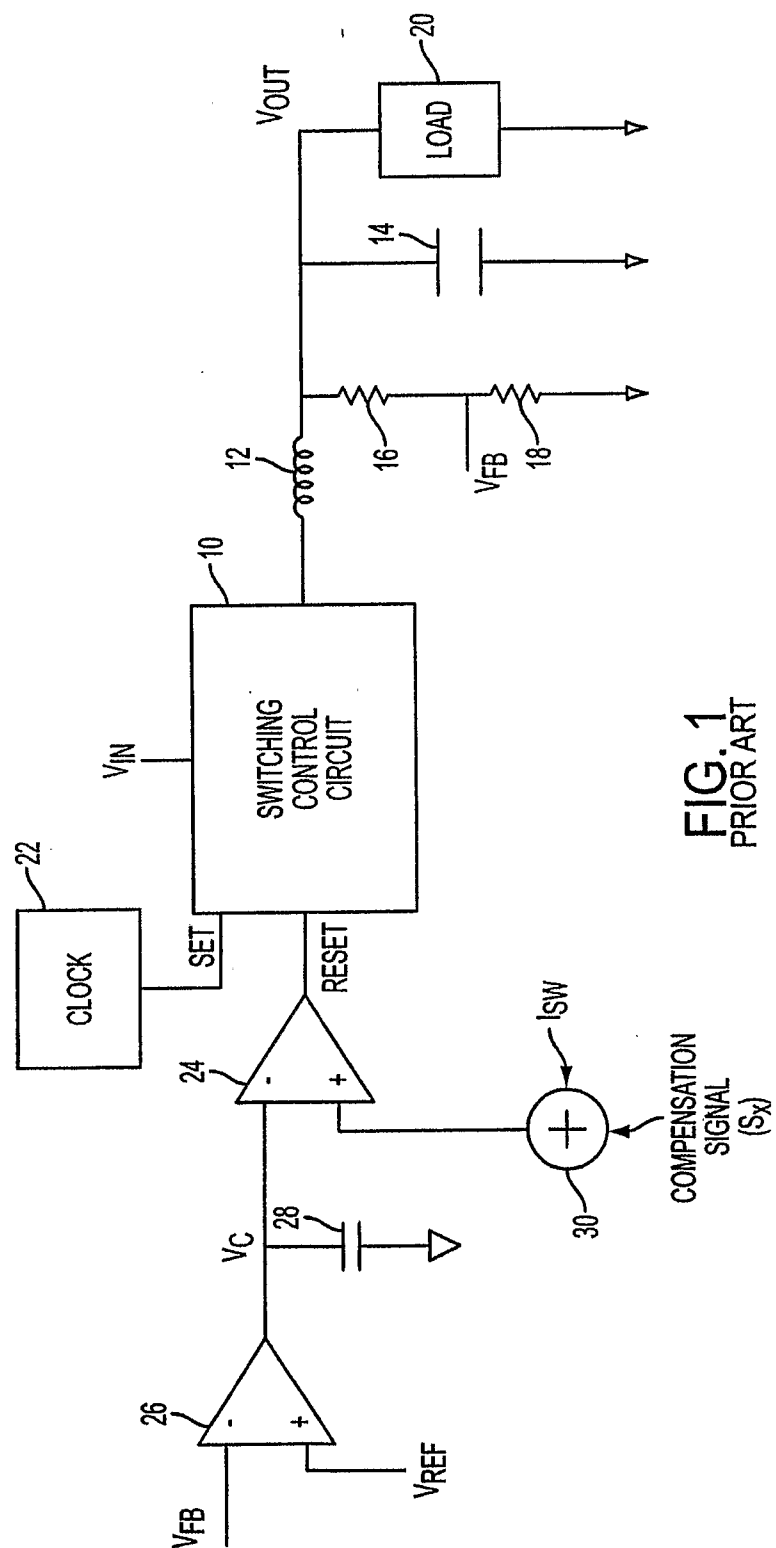


FIG. 1
PRIOR ART

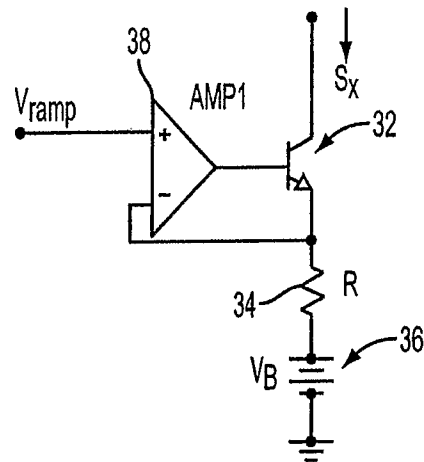


FIG. 2
PRIOR ART

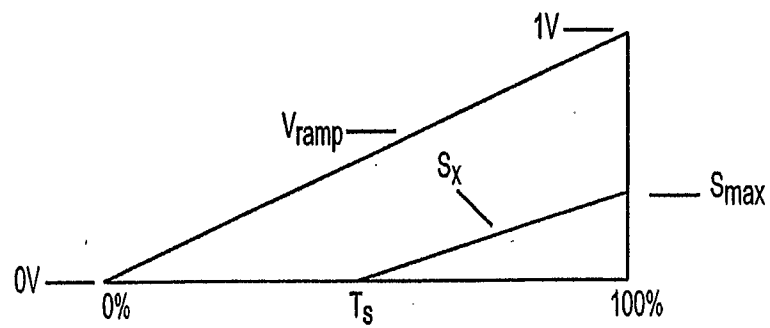


FIG. 3

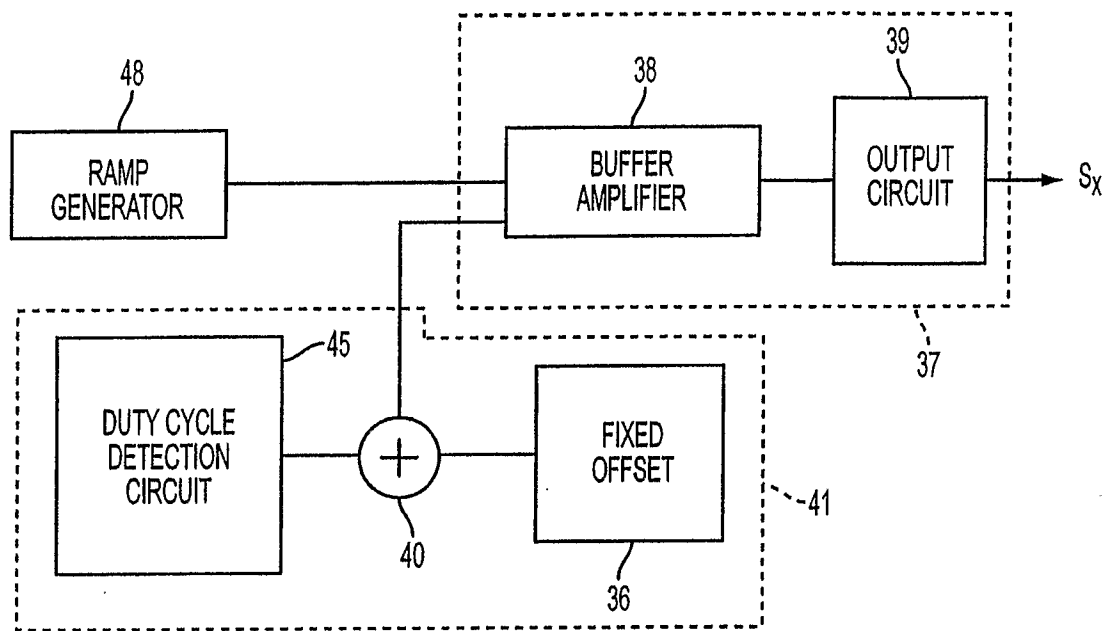


FIG. 4

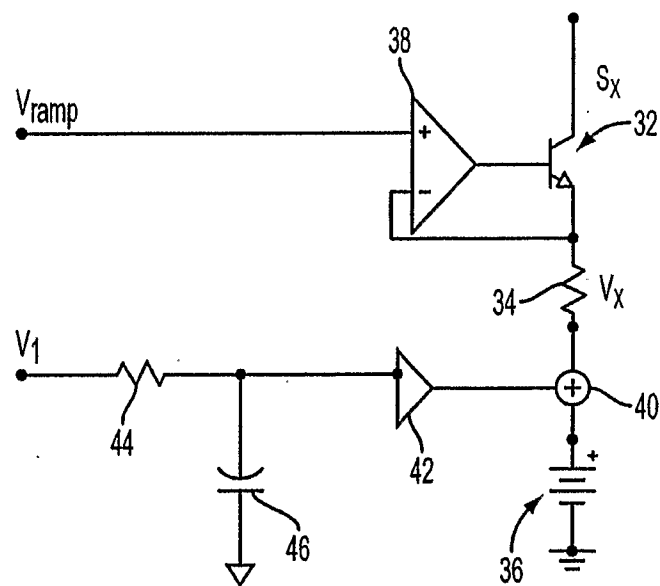


FIG. 5

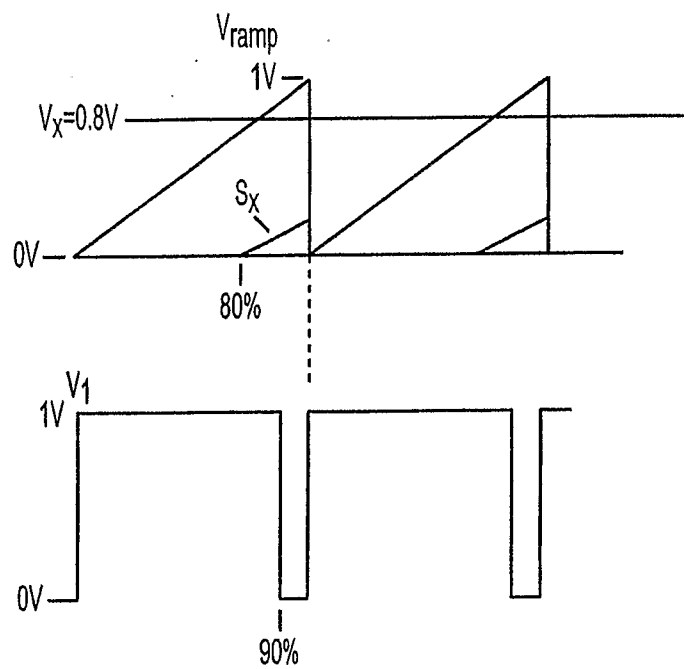


FIG. 6A

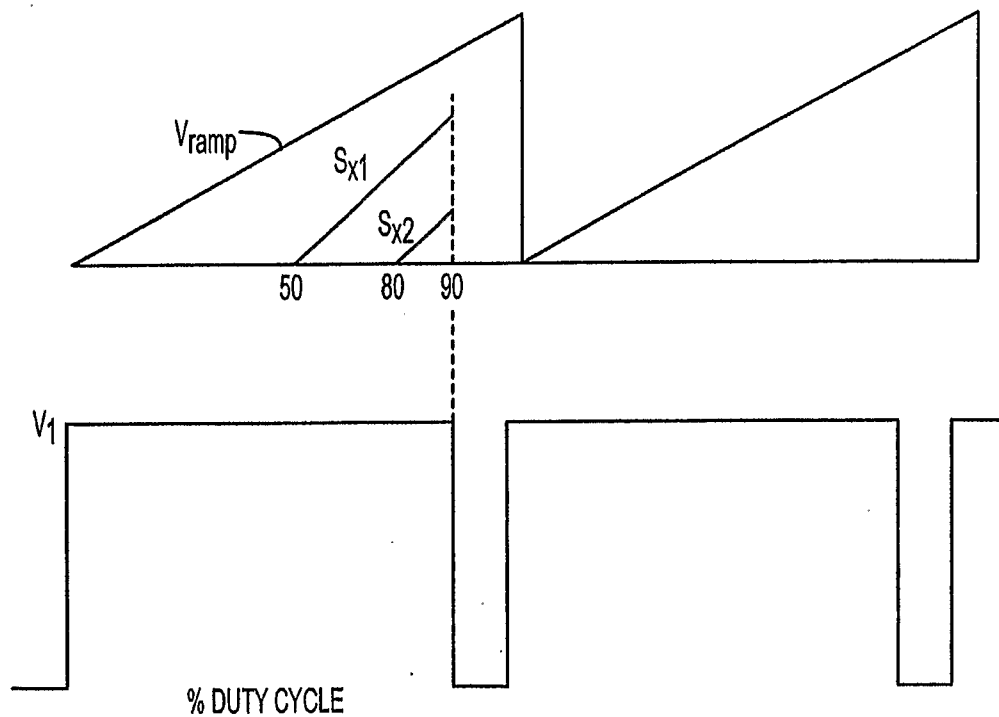


FIG. 6B

INTERNATIONAL SEARCH REPORT

International Application No
PC1/US2005/032247

A. CLASSIFICATION OF SUBJECT MATTER
G05F1/575 H02M3/156

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G05F H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, COMPENDEX, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	MAC LEAN D N: "A Simplified Current Mode Control Model With Optimum Slope Compensation" PROC. INTERSOC ENERGY CONVERTS ENG CONF; PROCEEDINGS OF THE INTERSOCIETY ENERGY CONVERSION ENGINEERING CONFERENCE, vol. 2, 12 August 1990 (1990-08-12), pages 37-42, XP010301332 page 41	1,8,9
X	US 5 903 452 A (YANG ET AL) 11 May 1999 (1999-05-11) abstract; figure 7 column 4, line 44 - column 6, line 64 ----- -/--	1,2,8,9

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents:

A document defining the general state of the art which is not considered to be of particular relevance

E earlier document but published on or after the international filing date

L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

O document referring to an oral disclosure, use, exhibition or other means

P document published prior to the international filing date but later than the priority date claimed

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

Z document member of the same patent family

Date of the actual completion of the international search

26 January 2006

Date of mailing of the international search report

03/02/2006

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Braccini, R

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/032247

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 415 244 A (NATIONAL SEMICONDUCTOR CORPORATION) 6 March 1991 (1991-03-06) abstract; figures 2a-2i, 4 page 1, line 1 - line 56 -----	1-3, 8, 9
A	US 6 498 466 B1 (EDWARDS KARL) 24 December 2002 (2002-12-24) the whole document -----	1-14
A	SAKURAI H ET AL: "ANALYSIS AND DESIGN OF A CURRENT-MODE PWM BUCK CONVERTER ADOPTING THE OUTPUT-VOLTAGE INDEPENDENT SECOND-ORDER SLOPE COMPENSATION SCHEME" IEICE TRANSACTIONS ON FUNDAMENTALS OF ELECTRONICS, COMMUNICATIONS AND COMPUTER SCIENCES, ENGINEERING SCIENCES SOCIETY, TOKYO, JP, vol. E88-A, no. 2, February 2005 (2005-02), pages 490-497, XP001224568 ISSN: 0916-8508 the whole document -----	1-14
A	HOLLAND B: "MODELLING, ANALYSIS AND COMPENSATION OF THE CURRENT-MODE CONVERTER" PROCEEDINGS OF POWERCON. ANNUAL INTERNATIONAL POWER ELECTRONICS CONFERENCE, 1984, pages 1-6, XP001057745 the whole document -----	1-14

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US2005/032247

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 5903452	A	11-05-1999	CN 1271473 A	25-10-2000
			EP 1012953 A1	28-06-2000
			WO 9908372 A1	18-02-1999
EP 0415244	A	06-03-1991	DE 69027896 D1	29-08-1996
			DE 69027896 T2	27-02-1997
			JP 3178551 A	02-08-1991
			US 4975820 A	04-12-1990
US 6498466	B1	24-12-2002	US 2003025484 A1	06-02-2003