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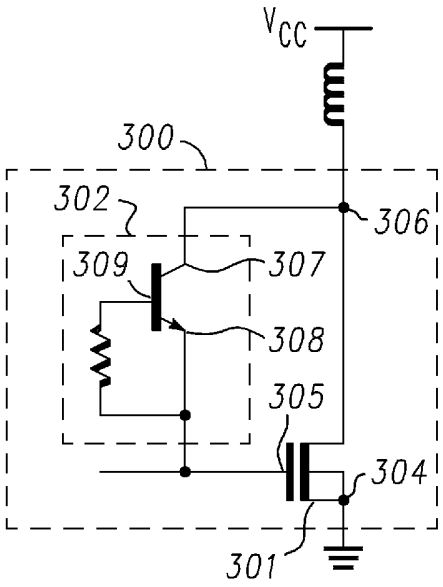
(54) Title: A SEMICONDUCTOR SWITCH ARRANGEMENT AND AN ELECTRONIC DEVICE



(57) Abstract: A semiconductor switch arrangement (300) comprises a bipolar transistor (302) and a semiconductor power switch (301) having an input node (306), an output node (304) and a control node (305) for allowing a current path to be formed between the input node (306) and the output node (307). The bipolar transistor (302) is coupled between the input node (306) and the control node (305) such that upon receiving an electro-static discharge pulse the bipolar transistor (302) allows a current to flow from the input node (306) to the control node (305) upon a predetermined voltage being exceeded at the input node (306) to allow the control node (305) to cause a current to flow from the input node (306) to the output node (307). Thus, the bipolar transistor device protects the semiconductor switch device, such as an LDMOS device, against ESD, namely protection against power surges of, say, several amperes in less than 1usec.

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A SEMICONDUCTOR SWITCH ARRANGEMENT AND AN ELECTRONIC DEVICE

Field of the Invention

The present invention relates to a semiconductor switch arrangement for an electronic device.

Background of the Invention

Semiconductor power switches, for example MOSFET devices, are frequently used to control the flow of current within an electronic device, and in particular to control the supply of current through an inductive load, such as those used in large motors and generators.

By way of illustration a MOSFET device 100 configured to operate as a switch for controlling a current through an inductive load 101 is shown in figure 1, where the drain 102 of a MOSFET device 100 is coupled to a voltage supply Vcc via the inductive load 101 and a resistive load 104, the source 105 of the MOSFET device 100 is coupled to ground and the gate 106 of the MOSFET device 100 is coupled to a control signal for switching the MOSFET device on or off (i.e. cause the drain/source to become closed or open circuit).

For an N-channel MOSFET device a positive control voltage will cause the MOSFET device to turn on, for a P-channel MOSFET device a negative control voltage will cause the MOSFET device to turn on.

As is well known to a person skilled in the art, the source and drain of a MOSFET device are formed in a

semiconductor material such as silicon, while the gate is formed from a conductive material, such as polycrystalline silicon. The gate is separated from the semiconductor material by an insulating layer, for example silicon dioxide. As such, a MOSFET device is susceptible to damage when a breakdown voltage is applied to the MOSFET.

Two types of voltage damage that can occur to a MOSFET device are electro static discharge ESD and electrical over stress EOS.

In the case of EOS there are three possible failure modes. First, a breakdown voltage of the gate oxide is reached; second, a breakdown voltage of the drain to source BVDSS junction is reached; and third, a maximum junction temperature is reached due to high temperature generated by energy discharges.

In the case of ESD there are two possible failure modes. First, the breakdown voltage of the parasitic bipolar transistor is reached; and second, a breakdown voltage of the gate oxide is reached.

One solution that has been adopted to avoid a voltage that could damage the semiconductor power switch involves the use of a zener clamp 200, where the anode of the zener clamp 200 is coupled to the gate 106 of the MOSFET device 100 and the cathode is coupled to the drain 202, as shown in figure 2.

The zener clamp 200 (i.e. zener diode) is chosen to have a breakdown voltage below that of the maximum drain to source voltage. As such, if the zener clamp breakdown

voltage is applied to the cathode of the zener clamp current is caused to flow through the zener clamp from the drain to the gate, resulting in the MOSFET device switching on and allowing current to flow from the drain to the source, thereby allowing the voltage at the drain to be reduced and consequently avoid damage to the MOSFET device.

As such, this solution provides a means for clamping the voltage generated at the drain of the MOSFET device to a predetermined voltage (i.e. the breakdown voltage of a zener diode).

However, typically, the breakdown voltage of a zener clamp is relatively low compared to the maximum drain to source voltage of a MOSFET device. As such, to allow an appropriate clamp voltage to be selected a zener clamp comprising a plurality of zener diodes placed in series is needed. Consequently, this solution can result in a voltage clamp circuit being relative large in size. Further, the coupling of zener diodes in series can make it difficult to provide an accurate clamp voltage.

Additionally, as the switching characteristics of the zener diode are slow they are not suitable for providing ESD protection to a MOSFET device. As such, additional ESD protection circuitry is required, thereby resulting in a further increase in size and complexity of a switching circuit.

US 5,812,006 discloses an optimized output clamping structure that includes a power output transistor having a first breakdown voltage and a breakdown structure having a second breakdown voltage coupled to the power

output transistor. The second breakdown voltage is less than the first breakdown voltage and follows the first breakdown voltage across all temperature and semiconductor process variations. Notably, the source and drain doping profiles of the power MOS are used to create a switch device (NPN or MOS) in order to protect 'circuits'. Thus, US005812006A discloses a diode that used to clamp a MOSFET, which operates as a diode during electro-static discharge, thereby failing to protect against ESD. Furthermore, there is no solution to integrate a clamp inside the MOSFET.

It is desirable to provide a semiconductor switch arrangement and an electronic device that provides improved protection against electro-static discharge.

Statement of Invention

The present invention provides a semiconductor switch arrangement and electronic device as described in the accompanying claims.

This provides the advantage of providing a single voltage clamp device that can provide protection to a semiconductor power switch, for example a MOSFET, insulated gate bipolar transistor IGBT, gate turn off thyristor GTO, or power bipolar transistor, from both electrostatic discharge and electrical over stress (EOS) like energy discharges.

Further, it allows a reduction in die size and improved voltage clamp accuracy.

Brief Description of the Drawings

The present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 illustrates a semiconductor switch arrangement as known in the prior art;

Figure 2 illustrates a semiconductor switch arrangement incorporating a voltage clamp as known in the prior art;

Exemplary embodiments of the present invention will now be described with reference to the accompanying drawings, in which:

Figure 3 illustrates a semiconductor switch arrangement according to an embodiment of the present invention;

Figure 4 illustrates a semiconductor switch arrangement incorporating two voltages clamp as known in the prior art;

Figure 5 illustrates a cross-sectional view of a semiconductor switch according to an embodiment of the present invention;

Figure 6 illustrates a further cross-sectional view of a semiconductor switch according to an embodiment of the present invention;

Figure 7 illustrates a yet further cross-sectional view of a semiconductor switch according to an embodiment of the present invention;

Figure 8 illustrates voltage levels within a semiconductor switch arrangement according to an embodiment of the present invention.

Description of a Preferred Embodiment

Figure 3 shows a semiconductor switch arrangement 300, having a MOSFET device 301 and a bipolar transistor 302, arranged to control the flow of current in an inductive load 303, for example a motor. The source 304 (i.e. input node) of the MOSFET device 301 is electrically coupled to ground, as is a connection to the substrate of the MOSFET device 301. The gate 305 (i.e. control node) of the MOSFET device 301 is electrically coupled to a control circuit (not shown) for controlling the switching of the MOSFET device 301. The drain 306 of the MOSFET device 301 is coupled to a supply voltage Vcc, via the inductive load 303.

Although the preferred embodiment of the present invention uses a MOSFET device to provide the switching facility, other forms of semiconductor switches could be used, for example, IGBT, GTO, and power bipolar transistors.

The MOSFET device 301 illustrated is an N-type device. However, as would be appreciated by a person skilled in the art, a P-type device could also be used.

Coupled between the drain 306 and gate 305 of the MOSFET device 301 is the bipolar transistor 302, where the collector 307 of the bipolar transistor 302 is electrically coupled to the drain 306 of the MOSFET device 301. The emitter 308 and base 309 of the bipolar

transistor 302 are electrically coupled to the gate 305 of the MOSFET device 301. The bipolar transistor 302 illustrated is an npn device. However, as would be appreciated by a person skilled in the art, a pnp device could be used.

The bipolar transistor 302 is arranged to provide voltage clamping to prevent the maximum drain to source voltage of the MOSFET device 301 being exceeded. A first example of when the voltage clamping may be required are when the load current (i.e. the current flowing through the inductive load 303) is switched off by the MOSFET device 301 and a voltage is generated by the inductive load 303 trying to maintain the current through the load. A second example is when an electro-static discharge (ESD) pulse causes a voltage differential to form across the MOSFET device 301. For the purposes of providing ESD protection the bipolar transistor 302 should be configured to be suitable to respond to electro static discharges, for example to have low capacitance and be suitable for high currents.

To determine the voltage clamping requirements for a MOSFET device the energy dissipation specification for the MOSFET device 301 should be known. In knowing the energy dissipation specification for a MOSFET device 301, it is necessary to ensure that the actual energy dissipation is kept within the energy dissipation specification for the MOSFET device 301. The energy dissipation into the MOSFET can be calculated using:

$$E_D = \frac{1}{2} LI^2 x \frac{Vclamp}{Vclamp - Vcc}$$

where:

L is the inductive load (not shown),

I is the current generated by the inductive load,

Vclamp is the clamp voltage, and

Vcc the voltage supply.

Accordingly, Vclamp should be chosen such that E_D is less than the maximum allowable energy dissipated into the MOSFET device.

With the emitter 308 and base 309 of the bipolar transistor 302 being coupled together the bipolar transistor 302 acts as an insulator for voltages applied to the collector 307 less than a predetermined voltage. However, if the collector or base voltage exceeds a predetermined voltage (i.e. the clamp voltage), the bipolar transistor 302 begins to conduct from the collector 307 to the emitter 308. The base 309 is electrically coupled to the emitter 308 by a resistor than can be formed by diffusion, metal, oxide or ballast for example

The breakdown voltage (i.e. clamp voltage) of the bipolar transistor 302 is determined by the distance between the collector 307 and base 309, where increasing the distance results in an increase in breakdown voltage. Alternatively, the breakdown voltage of the bipolar transistor 302 could also be determined by the doping concentration of the collector and the base. Accordingly, the clamp voltage provided by the bipolar transistor 302 can be accurately selected by selecting a suitable distance between the collector 307 and base 309 of the bipolar transistor 302.

In addition to the switch arrangement 300 of Figure 3, it is envisaged that the gate voltage can be clamped by a second bipolar transistor arrangement 400 as described in Figure 4. In the transistor arrangement 400 of Figure 4, the transistor 402 is the same as transistor 302 of Figure 3. However, coupled between the gate 405 and the source 406 of the MOSFET device 401 is a second bipolar transistor 412, where the collector 417 of the second bipolar transistor 412 is electrically coupled to the gate 405 of the MOSFET device 401. The emitter 418 is electrically coupled to the base 419 of the second bipolar transistor 412.

The transistor 412 is arranged to provide voltage clamping in order to prevent the maximum gate to source voltage of the MOSFET device 401 being exceeded. A first example is when the voltage clamping between the drain port 406 and the gate port 405, as defined by the transistor 402, is reached. Then, a current is able to flow from the transistor 402 to the source 404 through a resistive path thereby creating a voltage drop between the gate port 405 and the source port 406.

A second example is when an electrostatic discharge (ESD) is applied on the drain port 406 of the LDMOS. Here, a transient current is able to flow through the intrinsic drain to gate capacitance and creates a voltage drop between the gate port 405 and the source port 406.

In both of the above examples, the bipolar transistor 412 clamps the voltage between the gate port 405 and the source port 406 during any stress on the drain, as it absorbs a part of the energy. Notably, the energy is

dissipated through both clamp structures and the MOSFET device 401.

The second bipolar transistor 412 illustrated is a NPN device. However, as would be appreciated by a person skilled in the art, a PNP device could be used. Transistor 402 can be integrated in the MOSFET in the same way as transistor 302.

In the same manner described previously for clamping the voltage between drain and gate using transistor 402, the clamp voltage between gate and source can also be controlled using the second bipolar transistor 412.

Although figures 3 and 4 show a single MOSFET device, typically to achieve the power levels required a plurality of MOSFET fingers will be used, where a single bipolar transistor, acting as a voltage clamp as described above, may be used to support a number of the MOSFET fingers.

By way of illustration, and with reference to Figure 5, the operation of the semiconductor switch arrangement 300 will be described with reference to the variations in voltage and current during the switching 'on' and 'off' of the MOSFET device 301 where the bipolar transistor 302 has a breakdown voltage of A1.

Furthermore, although the bipolar transistors 302, 402, 412 can form a separate element that are coupled to the MOSFET device 301 401, it is envisaged that the bipolar transistors 302 402, 412 can be formed from the same integrated circuit die from which the MOSFET device is

formed, as illustrated in Figure 5, Figure 6 and Figure 7.

Figure 5 shows a single integrated circuit die 500 on which is formed the MOSFET device 301, 401 and the bipolar transistors 302, 402, 412 configured as described above.

The integrated circuit die 500 is formed between an N- buried layer 501, a collector N- region 502 and a drain N- region 503 in which an N+ well region 504 is formed. Notably, the N- region under the drain does not contact N- buried layer 501. Such an arrangement enables the inventive concept to be used in an isolated LDMOS implementation if the EPI layer is N doped or none isolated LDMOS if the EPI layer is P doped. Located above the integrated circuit body is a plurality of gate regions 505 isolated from the integrated circuit body via insulation regions 506.

The N- region 502 acts as the collector for the protective bipolar transistor.

The N+ well region 504 acts as a drain for the MOSFET device, say MOSFET 301 or 401 of Figure 3 or Figure 4.

Sandwiched between the N- region 502 and the N- region 503 are two P- regions 507, 508 and the second N- region 509. Notably, the preferred embodiment of the present invention can be used in both a NEPI and a PEPI arrangement. In a NEPI arrangement, the LDMOS is not isolated because the drain region N- is connected the NBL through the N- region. In a PEPI arrangement, the LDMOS is isolated because the drain region N- is separated from

the NBL by the P-. The preferred embodiment of the present invention operates successfully in both cases.

The P- region 507 closes to the N- region 502 has a P+ well region 510, which forms the base for the protective bipolar transistor (say transistor 302 of Figure 3 or transistors 402 and/or 412 of Figure 4), and an N+ well region 511, which forms the emitter for the protective bipolar transistor.

The N- region 509 has an N+ well region 512 that also acts as a drain for the MOSFET device.

The other P- region 508 has two N+ well regions 513, 514 and a P+ well region 515 that act as the source for the MOSFET device.

To configure the semiconductor switch arrangement 300 of Figure 3 or the alternative semiconductor switch arrangement 400 of Figure 4, the gate regions 505 are electrically coupled to the P+ and N+ well regions 510, 511 that form the base and emitter, via a first conductive strip, and the N- region 503, 509 is coupled to the N+ well regions 504, 512 that forms the drain, via a second conductive strip.

It is envisaged that the P+ doping 510 that is used to contact the base of the bipolar transistor can be placed between the collector region 502 and N+ emitter region 511, as shown in Figure 5.

Referring now to Figure 6, an alternative cross-sectional view of a semiconductor switch 600 implemented on silicon, is illustrated according to the preferred

embodiment of the present invention. In the semiconductor switch 600, it is envisaged that the N+ doping 511 that is used to contact the emitter of the bipolar transistor can be placed between the collector region 502 and the P+ base region 510.

Referring now to Figure 7, a yet further alternative cross-sectional view of a semiconductor switch 700 implemented on silicon, is illustrated according to the preferred embodiment of the present invention. In the semiconductor switch 700, it is envisaged that two P+ regions 510 and 516 may be located at both sides of the emitter 511.

The first waveform 800 shown in figure 8 illustrates the current flow through the inductive load 303 and the MOSFET device 301. The second waveform 801 shown in figure 8 illustrates the voltage across the MOSFET device 301. The third waveform 802 shown in figure 8 illustrates the control voltage applied to the semiconductor switch arrangement 300. The fourth waveform 803 shown in figure 8 illustrates the voltage applied to the gate 305 of the MOSFET device 301.

At time T1 the control signal, as shown in the third waveform 802, goes high causing the voltage applied to the gate 305 of the MOSFET device 301 to go high, thereby causing the voltage across the MOSFET device 301 to go low and the load current to go high.

At time T2 the control signal goes low causing the voltage applied to the gate 305 of the MOSFET device 301 to go low, thereby causing the voltage across the MOSFET

device 301 to go high and the load current to begin to decrease.

The decrease in load current between times T2 and T3 causes an increase in voltage across the MOSFET device 301, which if left unchecked could reach a value many times higher than Vcc and cause damage to the MOSFET device 301.

At time T3 the voltage across the MOSFET device 301 reaches the breakdown voltage A1 of the bipolar transistor 302. When this occurs current will flow from the load side of the MOSFET device 301 through the bipolar transistor 302 to the gate 305 of the MOSFET device 301 causing the voltage applied to the gate 305 of the MOSFET device 301 to increase, as shown in the fourth waveform 803. In this case, the bipolar transistor 412 described FIG. 4 clamps the voltage between the gate and source terminals between time T3 and T4

At time T3 the current to the MOSFET gate 305 causes the MOSFET device 301 to switch on, allowing the energy stored in the inductive load 303 to flow through the MOSFET device 301 during the time period between T3 and T4.

At time T4 the breakdown voltage goes below A1 causing the bipolar transistor 302 to stop conducting and causing the voltage to the gate 305 of the MOSFET device 301 to drop and the load current to drop to zero.

Based upon a similar process to that described above, the bipolar also provides protection from an ESD pulse by allowing the MOSFET device 301 to be switched on when an

ESD pulse causes a voltage to be formed across the semiconductor switch 300 that equals the clamp voltage of the bipolar transistor 302.

Additionally, for an ESD pulse if the control impedance (i.e. the impedance between the gate and the source of the power MOSFET) is very low, the discharge current could flow through the clamp and the low resistance to the ground.

It will be understood that the aforementioned arrangements embodying the inventive concept described above, tend to provide at least one or more of the following advantages:

(i) The bipolar transistor device is arranged to act as a bipolar transistor in a first mode of operation during any ESD and act as a diode for other stress related scenarios in a second mode of operation.

(ii) The inventive concept provides a bipolar transistor device that protects the MOS device, such as an LDMOS device, against ESD, namely protection against power surges of, say, several amperes in less than 1usec.

(iii) The inventive concept provides a fully integrated solution, requiring a low silicon area, to protect the MOS device from energy and electrostatic discharge.

(iv) The inventive concept describes a solution that allows the energy in the MOSFET device to be dissipated, whilst the clamps used to protect the MOSFET are capable of sustaining some of the energy stress. In this way, both the energy capability and the ESD robustness of the system are fully optimised.

Whilst specific implementations of the present invention have been described, it is clear that one skilled in the art could readily apply further variations and modifications of such implementations within the scope of the accompanying claims.

Thus, a semiconductor switch arrangement and an electronic device have been described to alleviate the aforementioned disadvantages of prior art arrangements and devices.

Claims

1. A semiconductor switch arrangement (300) comprising a bipolar transistor (302) and a semiconductor power switch (301) having an input node (306), an output node (304) and a control node (305) for allowing a current path to be formed between the input node (306) and the output node (307), characterised in that the bipolar transistor (302) is coupled between the input node (306) and the control node (305) such that upon receiving an electro-static discharge pulse the bipolar transistor (302) allows a current to flow from the input node (306) to the control node (305) upon a predetermined voltage being exceeded at the input node (306) to allow the control node (305) to cause a current to flow from the input node (306) to the output node (307).

2. A semiconductor switch arrangement (300) according to claim 1, wherein the semiconductor switch (301) is switched on when an ESD pulse causes a voltage to be formed across the semiconductor switch 300 that equals a clamp voltage of the bipolar transistor (302).

3. A semiconductor switch arrangement (300) according to claim 1 or Claim 2, wherein the bipolar transistor (301) operates as a bipolar transistor during a first mode of operation when the semiconductor switch receives an electro-static discharge and a diode in a second mode of operation.

4. A semiconductor switch arrangement (300) according to any preceding claim, wherein the semiconductor switch (301) is a MOSFET device, wherein the input node (306) is a drain node, the control node

(305) is a gate node and the output node (307) is a source node.

5. A semiconductor switch arrangement (300) according to any preceding claim, wherein a base (308) and an emitter (309) of the bipolar transistor (302) are electrically coupled to the control node (305) of the semiconductor switch (301) and a collector (307) of the bipolar transistor (302) is electrically coupled to the input node (306) of the semiconductor switch (301).

6. A semiconductor switch arrangement (300) according to any preceding claim, wherein the semiconductor switch (301) and the bipolar transistor (302) are formed in a single integrated circuit die.

7. A semiconductor switch arrangement according to any preceding claim, wherein the bipolar transistor (302) is an NPN transistor.

8. A semiconductor switch arrangement (300) according to any preceding claim, wherein a gate voltage of the semiconductor power switch (301) is clamped by a second bipolar transistor arrangement (412).

9. A semiconductor switch arrangement (300) according to claim 8, wherein a collector (417) of the second bipolar transistor arrangement (412) is electrically coupled to a gate (405) of the semiconductor power switch (301).

10. A semiconductor switch arrangement according to claim 6, wherein the single integrated circuit die comprises an N- buried layer (501) and an N- region under

a drain of the semiconductor power switch (301) is arranged not to contact with the N- buried layer (501).

11. A semiconductor switch arrangement according to any preceding claim, wherein the semiconductor power switch (301) is an LDMOS device.

12. A semiconductor switch arrangement (300) according to any preceding claim, wherein P+ doping (510) is used to contact a base of the bipolar transistor (302).

13. A semiconductor switch arrangement (300) according to any preceding claim, wherein the P+ doping base (510) of the bipolar transistor (302) is located between the collector region (502) and an N+ emitter region (511) of the bipolar transistor (302).

14. A semiconductor switch arrangement (300) according to any preceding Claim, wherein N+ doping (511) is used to contact the emitter of the bipolar transistor (302) and the emitter is located between a N- collector region (502) and the P+ base region (510).

15. A semiconductor switch arrangement (300) according to any preceding claim, wherein P+ regions (510, 516) of the gate of the bipolar transistor (302) are located at both sides of the emitter (511).

16. An electronic device having a semiconductor switch arrangement (300) according to any preceding claim, wherein the semiconductor switch arrangement (300) is arranged to control the passing of current through a load (303) by means of a control signal applied to the control node (305) of the semiconductor switch (301), wherein if

a voltage is formed at the input node (306) of the semiconductor switch (301) that exceeds the predetermined voltage the current flow from the input node (306) to the control node (305) causes current generated by the load (303) to flow from the input node (306) to the output node (307).

AMENDED CLAIMS

+ STATEMENT

1. A semiconductor switch arrangement (300) comprising a bipolar transistor (302) and a semiconductor power switch (301) formed in a single integrated circuit die and having an input node (306), an output node (304) and a control node (305) for allowing a current path to be formed between the input node (306) and the output node (307), characterised in that the bipolar transistor (302) is coupled between the input node (306) and the control node (305) such that upon receiving an electro-static discharge pulse the bipolar transistor (302) allows a current to flow from the input node (306) to the control node (305) upon a predetermined voltage being exceeded at the input node (306) to allow the control node (305) to cause a current to flow from the input node (306) to the output node (307) wherein the semiconductor switch arrangement (300) is characterised in that the single integrated circuit die comprises an N- buried layer (501) and an N- region under a drain of the semiconductor power switch (301) arranged not to contact with the N- buried layer (501).

2. A semiconductor switch arrangement (300) according to claim 1, wherein the received ESD pulse causes a voltage to be formed across the semiconductor switch 300 that equals a clamp voltage of the bipolar transistor (302) thereby switching 'on' the semiconductor switch (301).

3. A semiconductor switch arrangement (300) according to claim 1 or Claim 2, wherein the bipolar transistor (301) operates as a diode until, in response

to the semiconductor switch receiving the electro-static discharge pulse, it is arranged to operate as a bipolar transistor.

4. A semiconductor switch arrangement (300) according to any preceding claim, wherein the semiconductor switch (301) is a MOSFET device, wherein the input node (306) is a drain node, the control node (305) is a gate node and the output node (307) is a source node.

5. A semiconductor switch arrangement (300) according to any preceding claim, wherein a base (308) and an emitter (309) of the bipolar transistor (302) are electrically coupled to the control node (305) of the semiconductor switch (301) and a collector (307) of the bipolar transistor (302) is electrically coupled to the input node (306) of the semiconductor switch (301).

6. A semiconductor switch arrangement according to any preceding claim, wherein the bipolar transistor (302) is an NPN transistor.

7. A semiconductor switch arrangement (300) according to any preceding claim, wherein a gate voltage of the semiconductor power switch (301) is clamped by a second bipolar transistor arrangement (412).

8. A semiconductor switch arrangement (300) according to claim 7, wherein a collector (417) of the second bipolar transistor arrangement (412) is electrically coupled to a gate (405) of the semiconductor power switch (301).

9. A semiconductor switch arrangement according to any preceding claim, wherein the semiconductor power switch (301) is an LDMOS device.

10. A semiconductor switch arrangement (300) according to any preceding claim, wherein P+ doping (510) is used to contact a base of the bipolar transistor (302).

11. A semiconductor switch arrangement (300) according to claim 10, wherein the P+ doping base (510) of the bipolar transistor (302) is located between the collector region (502) and an N+ emitter region (511) of the bipolar transistor (302).

12. A semiconductor switch arrangement (300) according to Claim 10 or Claim 11, wherein N+ doping (511) is used to contact the emitter of the bipolar transistor (302) and the emitter is located between a N- collector region (502) and the P+ base region (510).

13. A semiconductor switch arrangement (300) according to any preceding claim, wherein P+ regions (510, 516) of the base of the bipolar transistor (302) are located at both sides of the emitter (511).

14. An electronic device having a semiconductor switch arrangement (300) according to any preceding claim, wherein the semiconductor switch arrangement (300) is arranged to control the passing of current through a load (303) by means of a control signal applied to the control node (305) of the semiconductor switch (301), wherein if a voltage is formed at the input node (306) of the

semiconductor switch (301) that exceeds the predetermined voltage the current flow from the input node (306) to the control node (305) causes current generated by the load (303) to flow from the input node (306) to the output node (307).

Statement under Article 19(1) PCT

Re: Patent Application PCT/EP2005/053819 in the name of Freescale Semiconductor, Inc. and CNRS

Amendments and support therefor:

(i) Claim 1 has been amended to include the feature that the bipolar transistor (302) and a semiconductor power switch (301) formed in a single integrated circuit die. Support for this feature can be found throughout the Specification as originally filed, not least Claim 6.

(ii) Claim 1 has been amended to include the single integrated circuit die comprises an N- buried layer (501) and an N- region under a drain of the semiconductor power switch (301) arranged not to contact with the N- buried layer (501). Support for this feature can be found throughout the Specification as originally filed, not least Claim 10.

(iii) Claim 6 and Claim 10 have been deleted without prejudice, with subsequent Claims and their dependencies renumbered accordingly.

(iv) The features of Claim 2 and Claim 3 have been re-crafted to an apparatus form.

(v) The dependency of Claim 12 and Claim 13 (re-numbered from Claim 14 and Claim 15) have been corrected and the 'gate' term in Claim 13 has been corrected to 'base'.

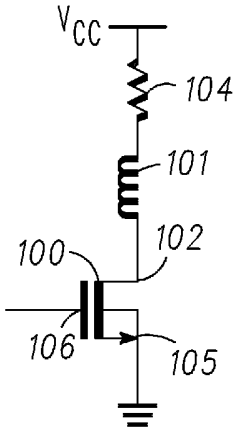


FIG. 1
-PRIOR ART-

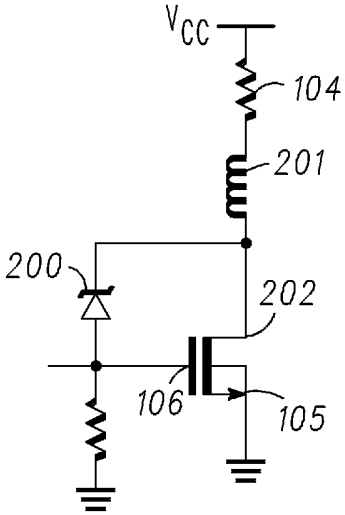


FIG. 2
-PRIOR ART-

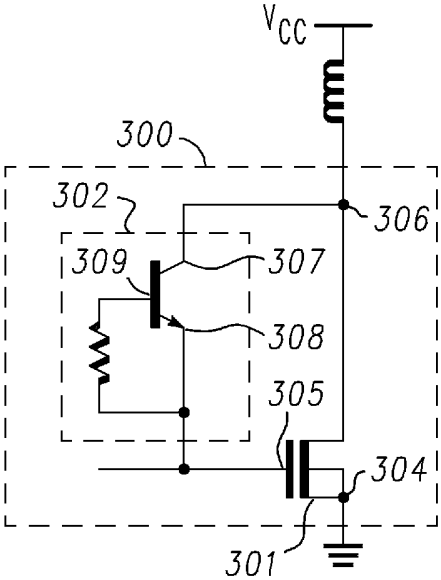


FIG. 3

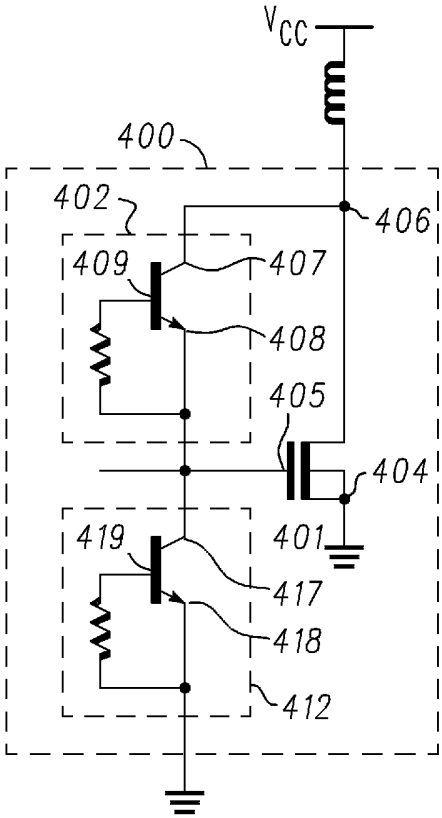
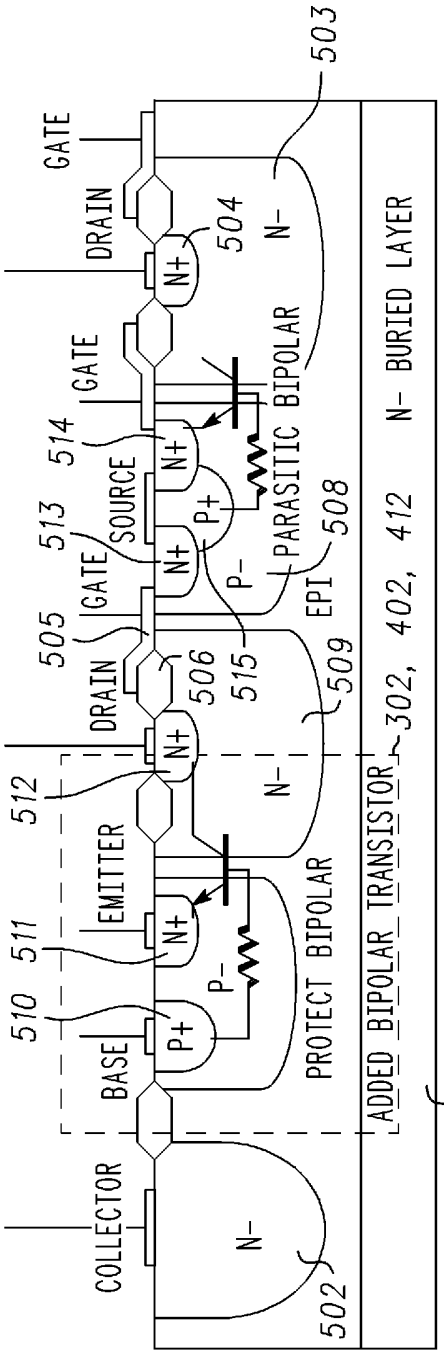


FIG. 4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N-
503
GATE
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SOURCE
513
GATE
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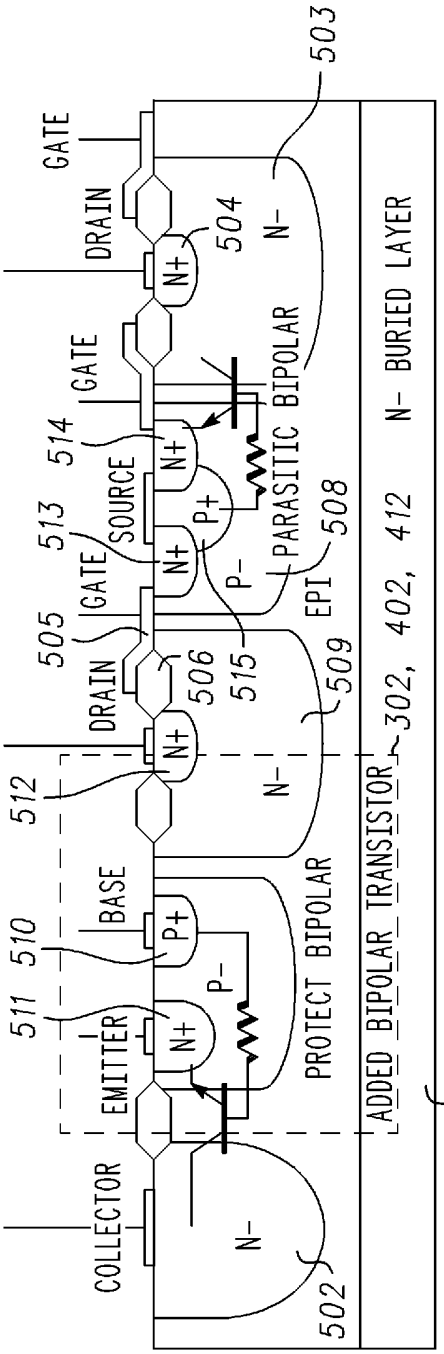
DRAIN
506
N+
P+
N+
P-
PARASITIC BIPOLAR
508
EPI
509
515
N-
512
EMITTER
511
BASE
510
P+
N+
P-
PROTECT BIPOLAR
ADDED BIPOLAR TRANSISTOR
302, 402, 412
N- BURIED LAYER
COLLECTOR
N-
502
501
500

FIG. 5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GATE
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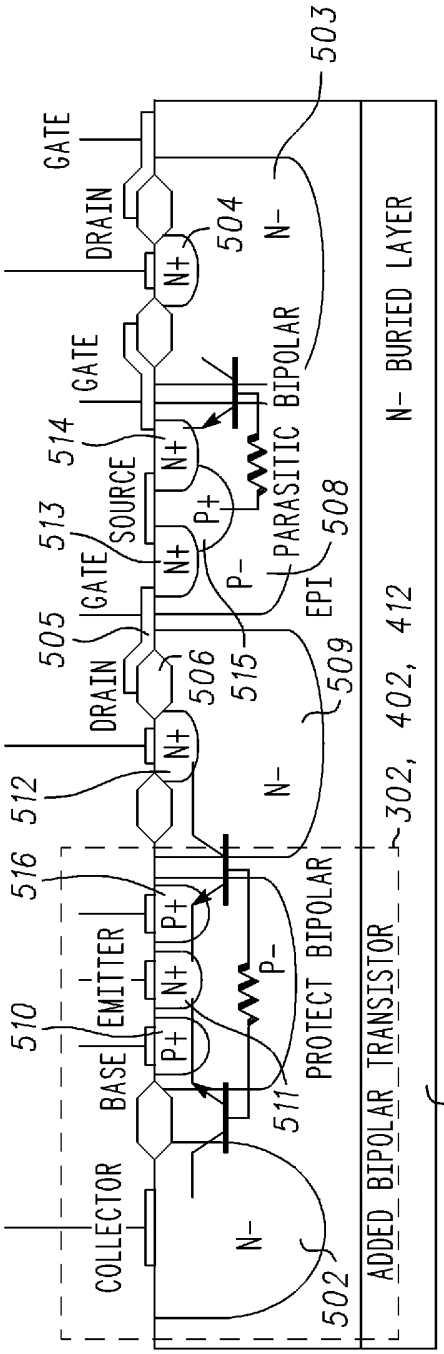
P+
N+
P-
PARASITIC BIPOLAR
508
EPI
509
515
N-
512
BASE
510
EMITTER
511
P+
N+
P-
PROTECT BIPOLAR
ADDED BIPOLAR TRANSISTOR
302, 402, 412
N- BURIED LAYER
COLLECTOR
N-
502
501
600

FIG. 6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GATE
P-
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DRAIN
506
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509
EPI
N+
512
N-
N- BURIED LAYER
516
302, 402, 412
P+
EMITTER
N+
P+
510
BASE
P-
PROTECT BIPOLAR
511
COLLECTOR
N-
502
ADDED BIPOLAR TRANSISTOR
501
700

FIG. 7

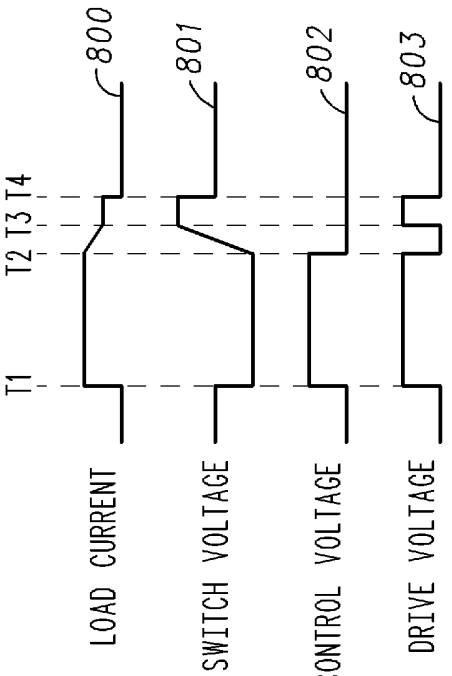
T1
T2 T3 T4
800
801
802
803
LOAD CURRENT
SWITCH VOLTAGE
CONTROL VOLTAGE
DRIVE VOLTAGE

FIG. 8

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP2005/053819

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03K17/082

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 6 614 633 B1 (KOHNO KENJI) 2 September 2003 (2003-09-02) column 2, line 39 - line 42 column 13, line 19 - column 14, line 50 column 19, line 41 - column 20, line 67 column 21, line 48 - column 22, line 33 column 23, line 39 - column 25, line 30 column 25, line 47 - line 52 column 25, line 59 - line 60 column 26, line 27 - line 41 figures 6,15A,15B,17A,17B,28,29,33 -/--	1-7,11, 16 8,9,12, 13,15

[X] *Further documents are listed in the continuation of box C.*

[X] *Patent family members are listed in annex.*

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 October 2005	07/11/2005
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Authorized officer Balbinot, H

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP2005/053819

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DE 199 22 924 A (SIEMENS AG) 30 November 2000 (2000-11-30) column 2, line 50 - column 4, line 63; figures 1,2	1-4,6,7, 11-16
Y		8,9

X	US 5 812 006 A (BUSS KENNETH G ET AL) 22 September 1998 (1998-09-22) cited in the application column 2, line 37 - column 4, line 64 claims 11-13 figure 3	1-3,6,7, 16
Y		8,9,12, 13,15

Y	BERTRAND G ET AL: "ANALYSIS AND COMPACT MODELING OF A VERTICAL GROUNDED-BASE N-P-N BIPOLAR TRANSISTOR USED AS ESD PROTECTION IN A SMART POWER TECHNOLOGY" IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE INC. NEW YORK, US, vol. 36, no. 9, September 2001 (2001-09), pages 1373-1381, XP001168170 ISSN: 0018-9200 abstract page 1373, paragraph II figure 1	8,9,12, 13,15

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/EP2005/053819

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6614633 B1	02-09-2003	NONE	
DE 19922924 A	30-11-2000	NONE	
US 5812006 A	22-09-1998	NONE	