United States Patent [19]

Webb et al.

[11] **3,904,922**

[45] **Sept. 9, 1975**

[54] **LAMP CONTROL AND LAMP SWITCH CIRCUIT**

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[73] Assignee: **Xerox Corporation**, Stamford, Conn.

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[21] Appl. No.: **416,921**

[52] **U.S. Cl.** ..... **315/151**; 315/194; 307/252 M; 307/252 P

[51] **Int. Cl.** **H05B 37/02**; H05B 39/04; H05B 41/36

[58] **Field of Search** ..... 315/194, DIG. 7, DIG. 5, 315/151; 307/252 P, 252 M

[56] **References Cited**

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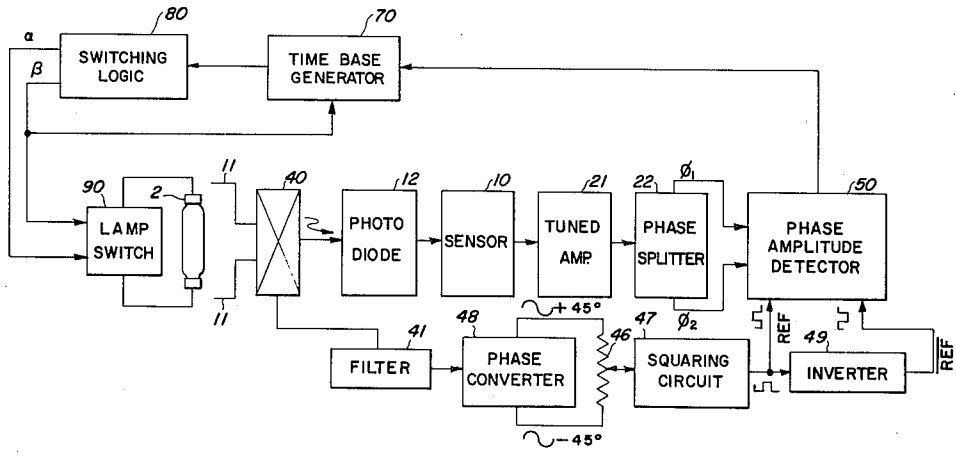
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Primary Examiner—James W. Lawrence
Assistant Examiner—T. N. Grigsby
Attorney, Agent, or Firm—James J. Ralabate; David C. Petre; Charles E. Smith

[57] **ABSTRACT**

Control and switching circuits for maintaining appropriate balance of light output of a long multi-vapor arc lamp. The control circuit includes sensing, amplifier-reference, phase amplitude detector, time base generator and lamp switching logic branches. The switching circuit includes a silicon controlled rectifier bridge for reversing the polarity of current flow through the lamp. The silicon controlled rectifier bridge is triggered by output pulse chains from the lamp switching logic branch in the control circuit.

1 Claim, 13 Drawing Figures



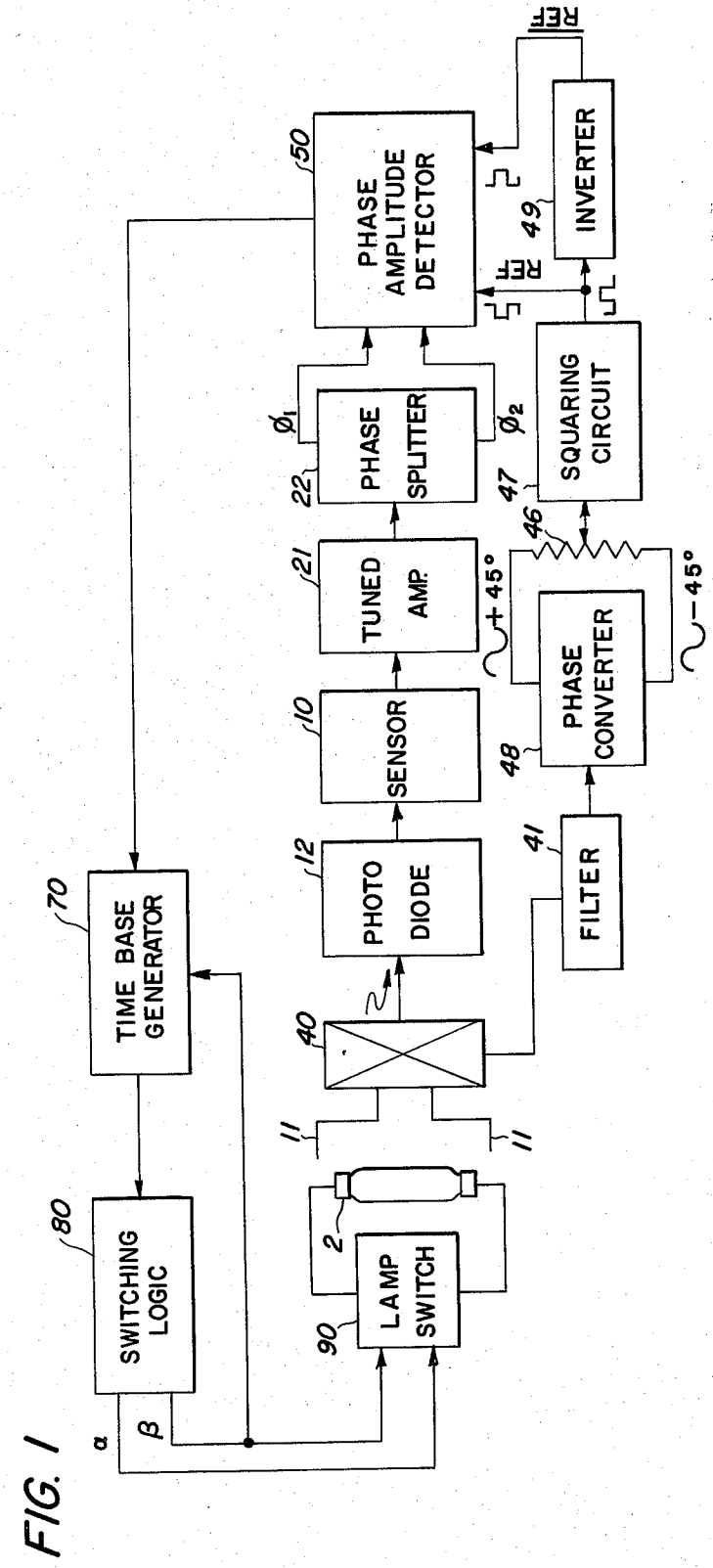

TIME BASE GENERATOR
70
SWITCHING LOGIC
80
α
β
LAMP SWITCH
90
2
11
11
40
PHOTO DIODE
12
SENSOR
10
TUNED AMP.
21
PHASE SPLITTER
22
Ø1
Ø2
PHASE AMPLITUDE DETECTOR
50
REF
REF
INVERTER
49
SQUARING CIRCUIT
47
46
+45°
−45°
PHASE CONVERTER
48
FILTER
41

FIG. 1

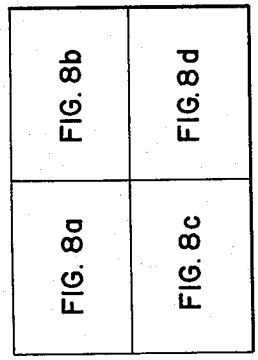

FIG. 8a
FIG. 8b
FIG. 8c
FIG. 8d

FIG. 9

FIG. 2

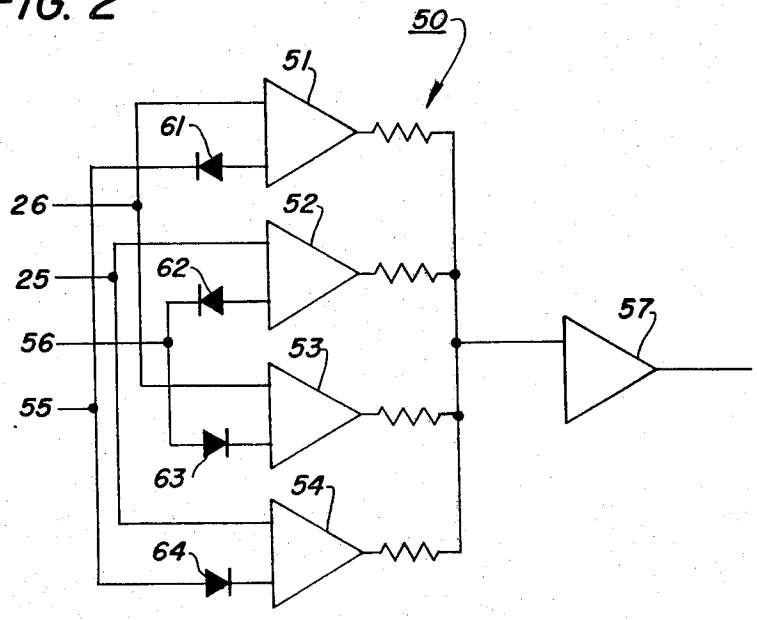

50
51
61
26
52
25
62
57
56
53
55
63
54
64

FIG. 7

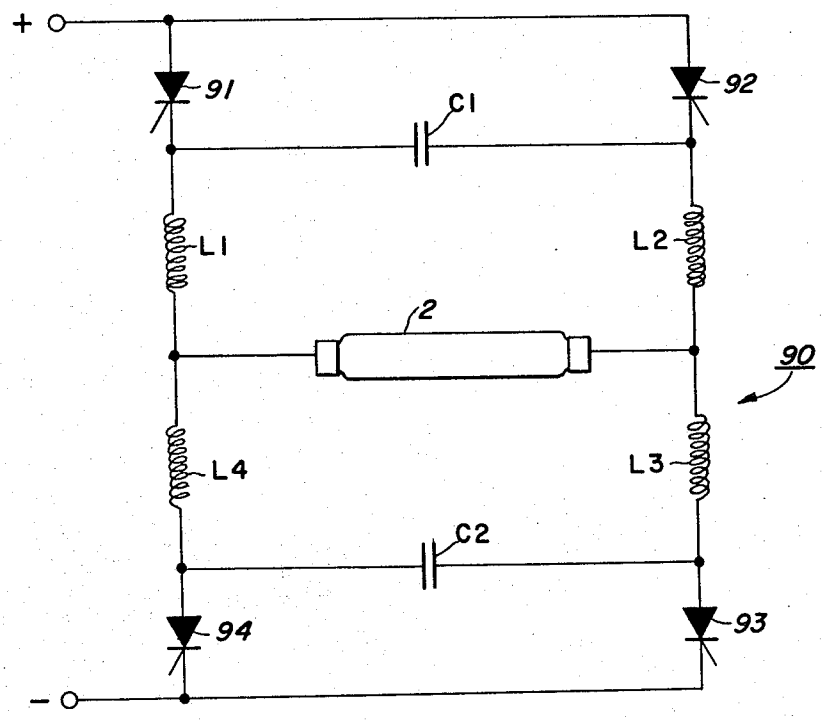

+
91
92
C1
L1
L2
2
90
L4
L3
C2
94
93
−

FIG. 3

FIG. 4

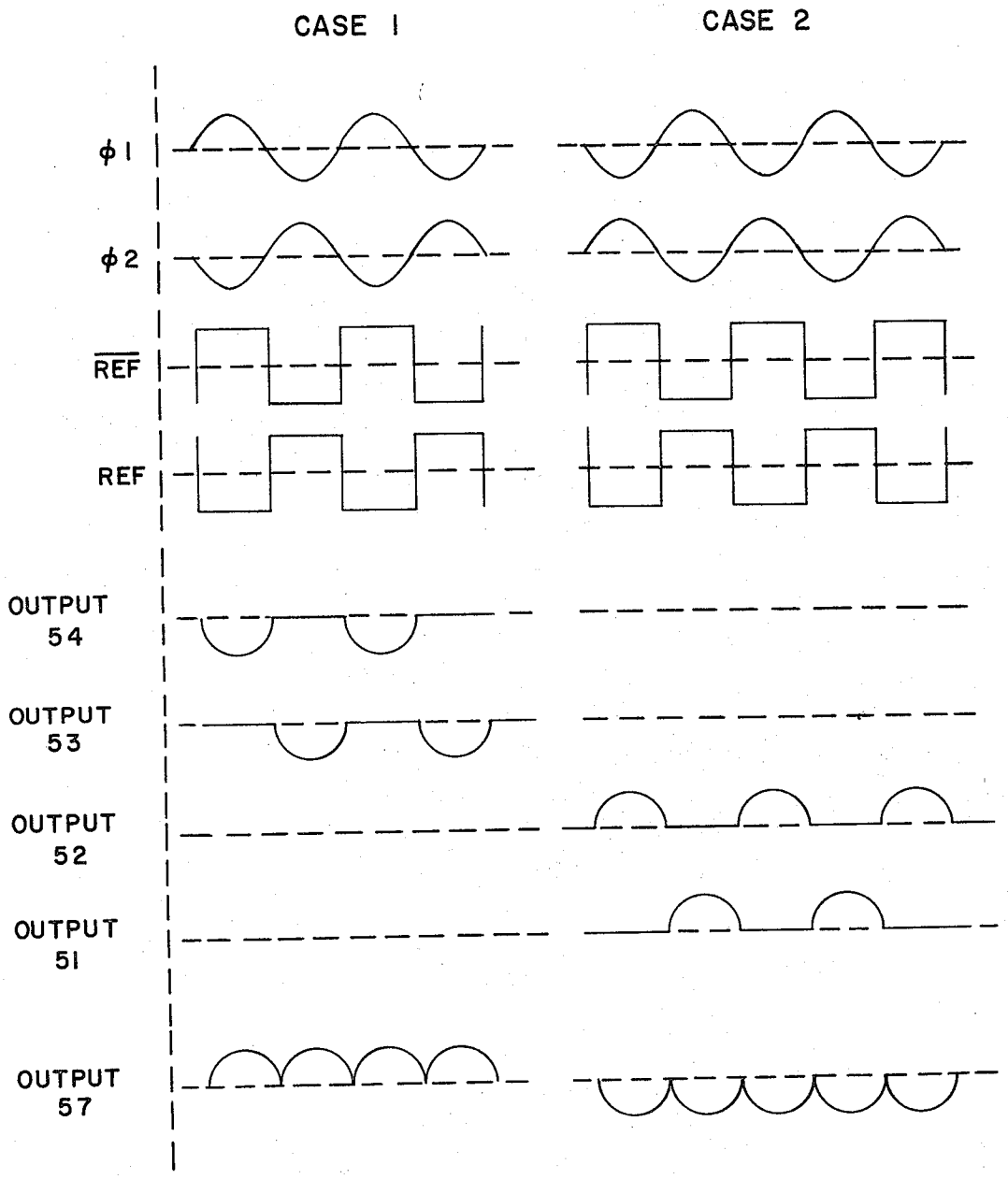
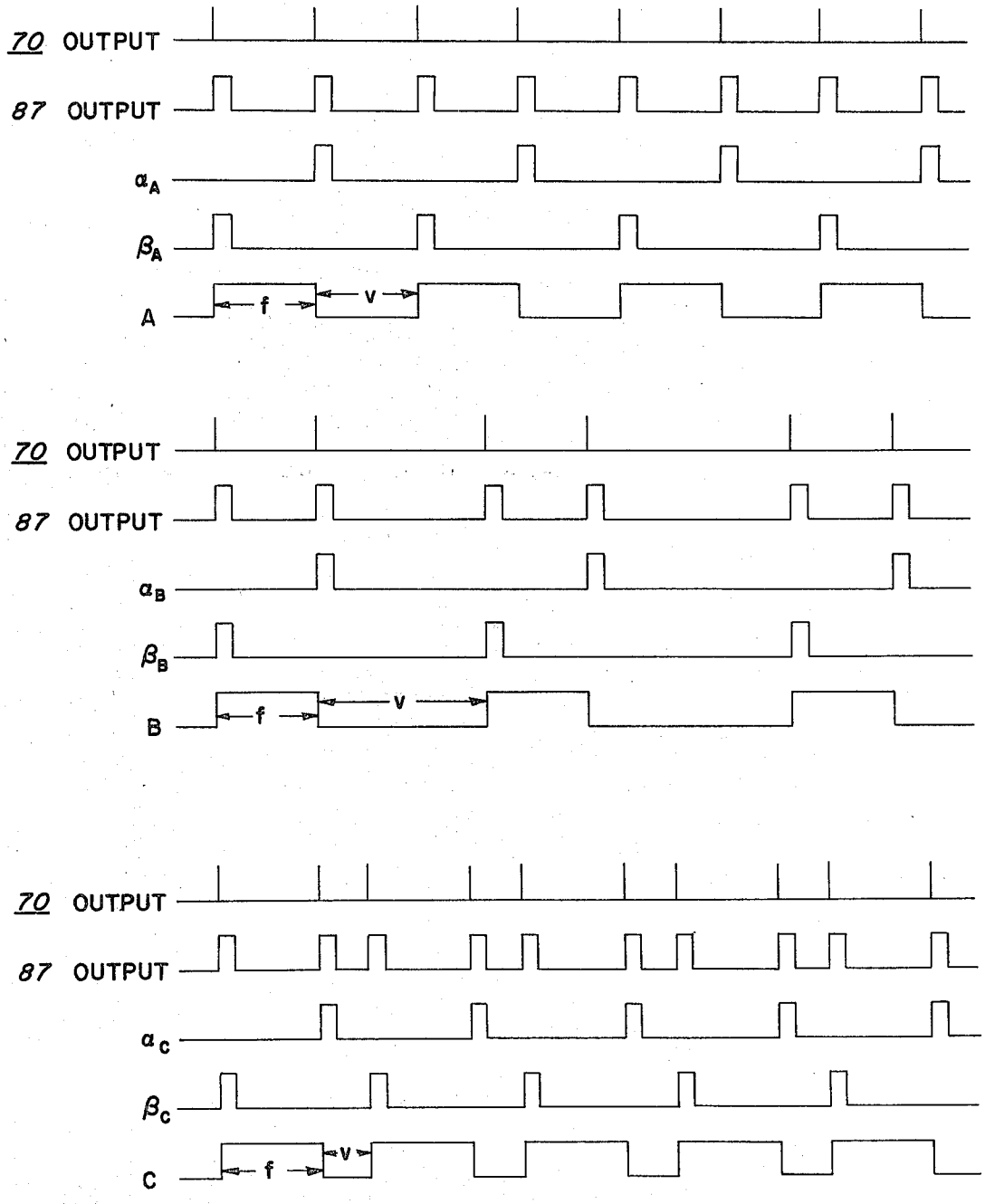

CASE 1
CASE 2
φ1
φ2
REF
REF
OUTPUT 54
OUTPUT 53
OUTPUT 52
OUTPUT 51
OUTPUT 57

FIG. 5


70 OUTPUT
87 OUTPUT
α_A
β_A
A
f
v
70 OUTPUT
87 OUTPUT
α_B
β_B
B
f
v
70 OUTPUT
87 OUTPUT
α_C
β_C
C
f
v

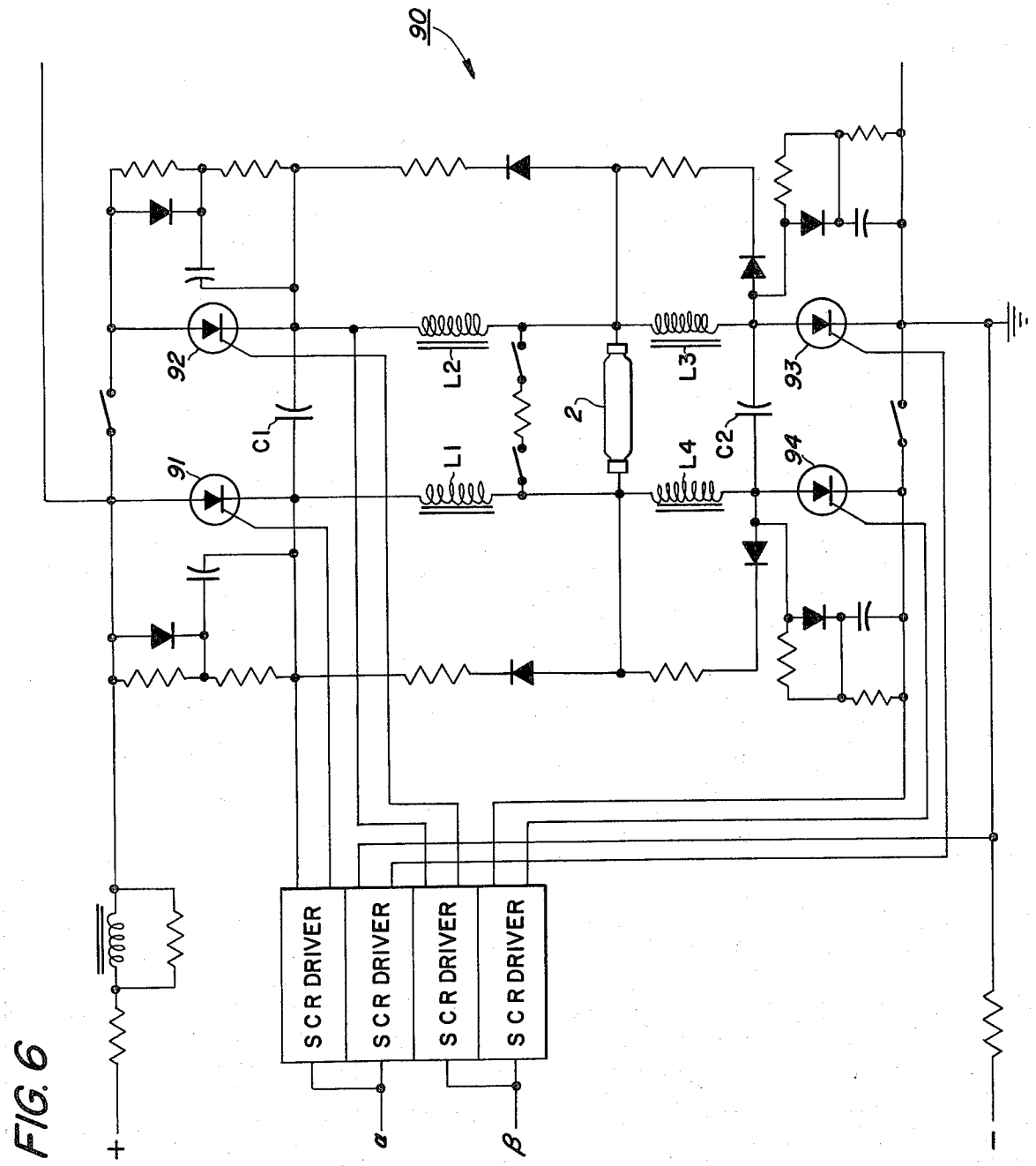

90
92
91
93
94
C1
C2
L1
L2
L3
L4
2
SCR DRIVER
SCR DRIVER
SCR DRIVER
SCR DRIVER
α
β
+
-

FIG. 6

FIG. 8a

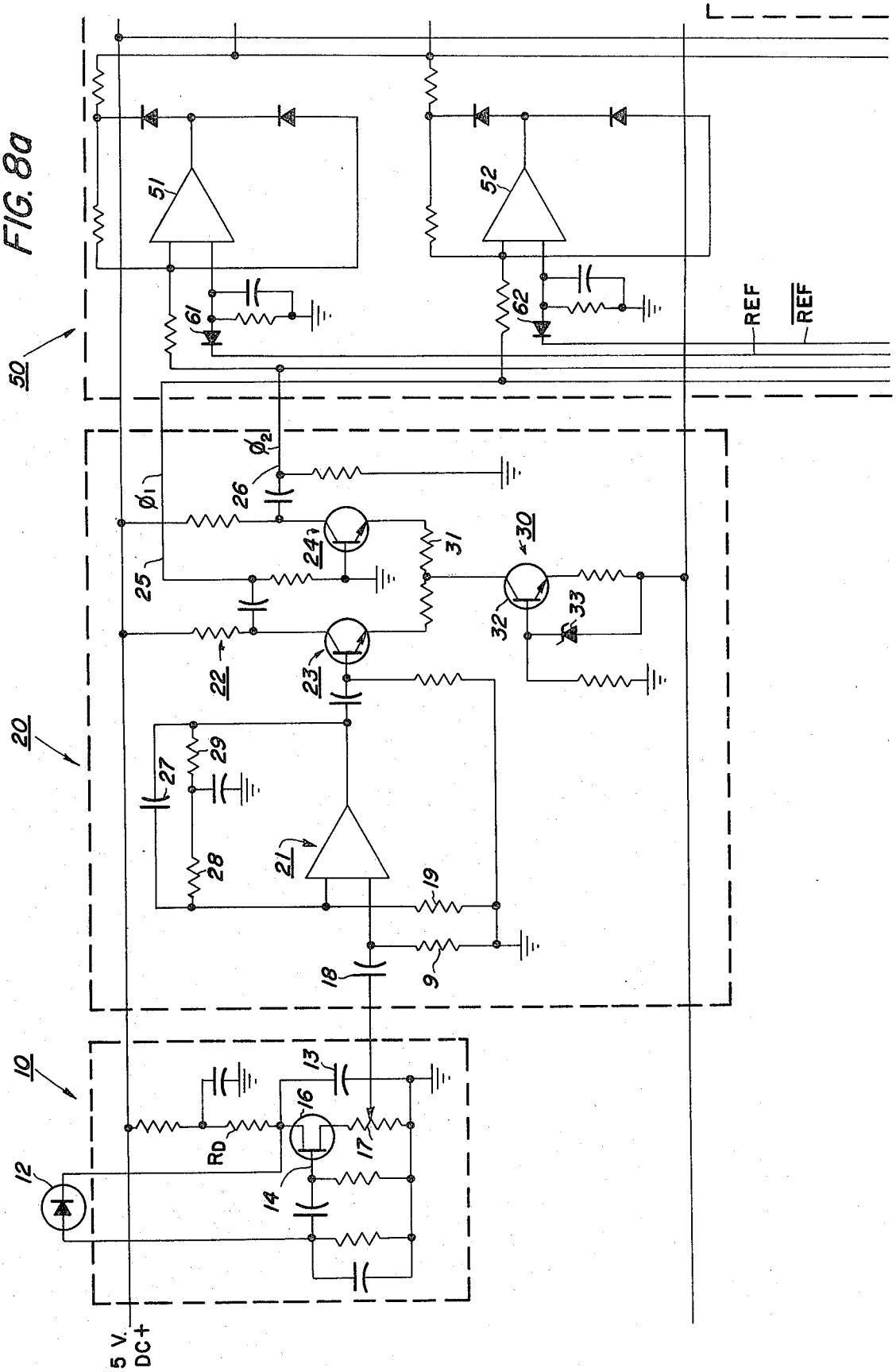

50
51
52
61
62
REF
$\overline{REF}$
ϕ_2
ϕ_1
26
24
31
30
25
32
33
22
23
20
27
29
28
21
19
18
9
10
13
16
17
R_D
12
14
15 V. DC+

FIG. 8b

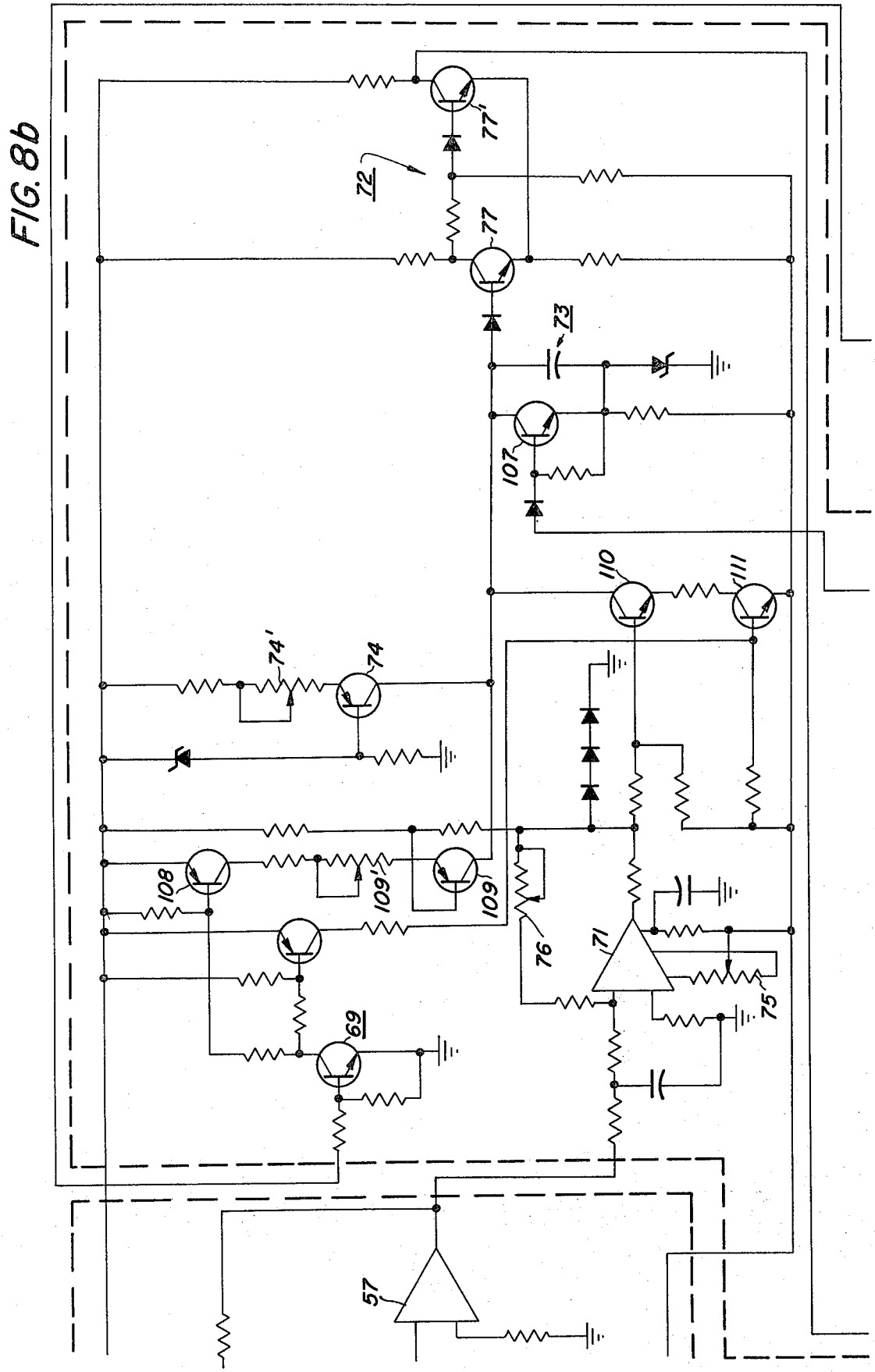


FIG. 8c

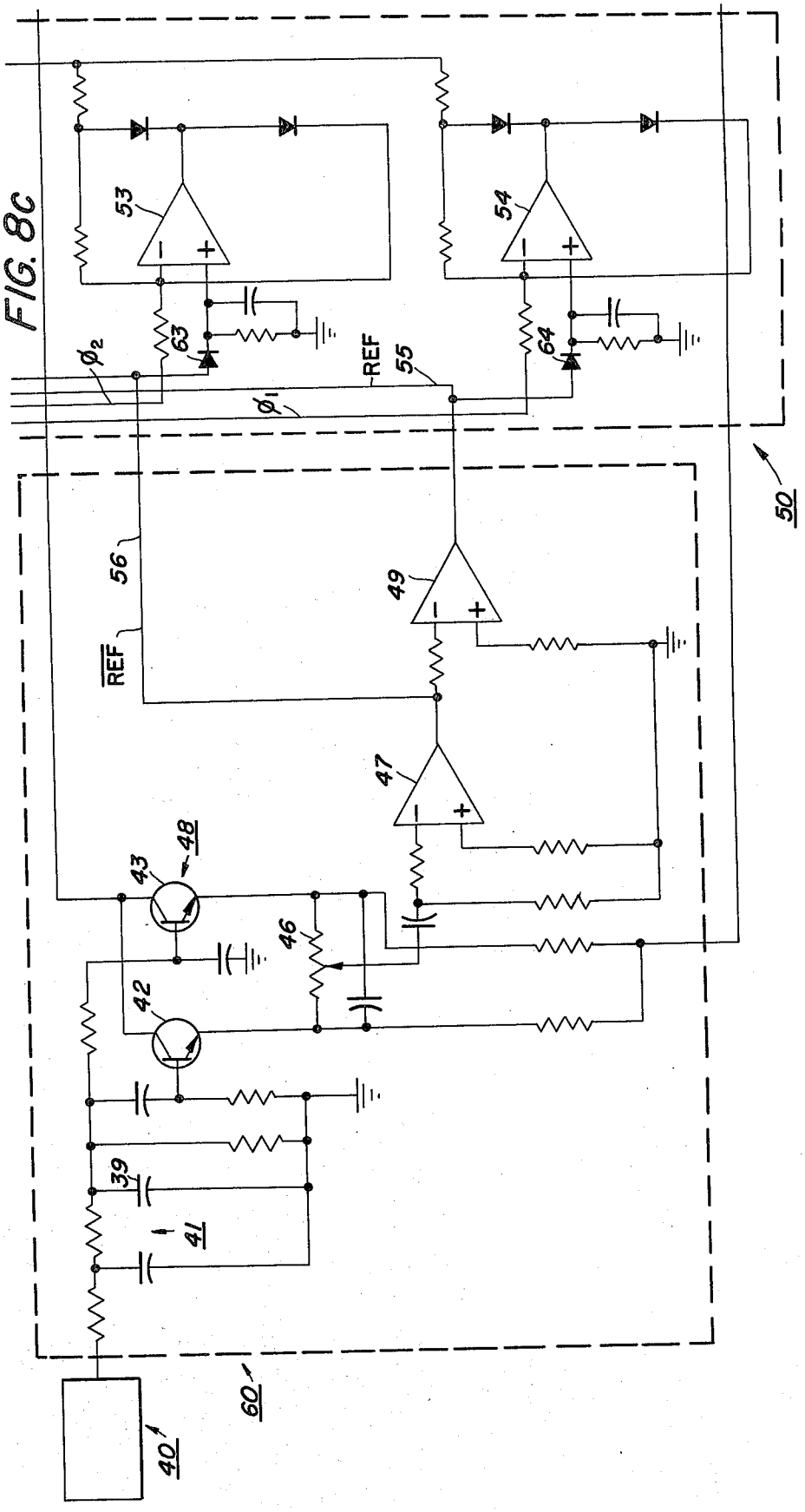


FIG. 8d

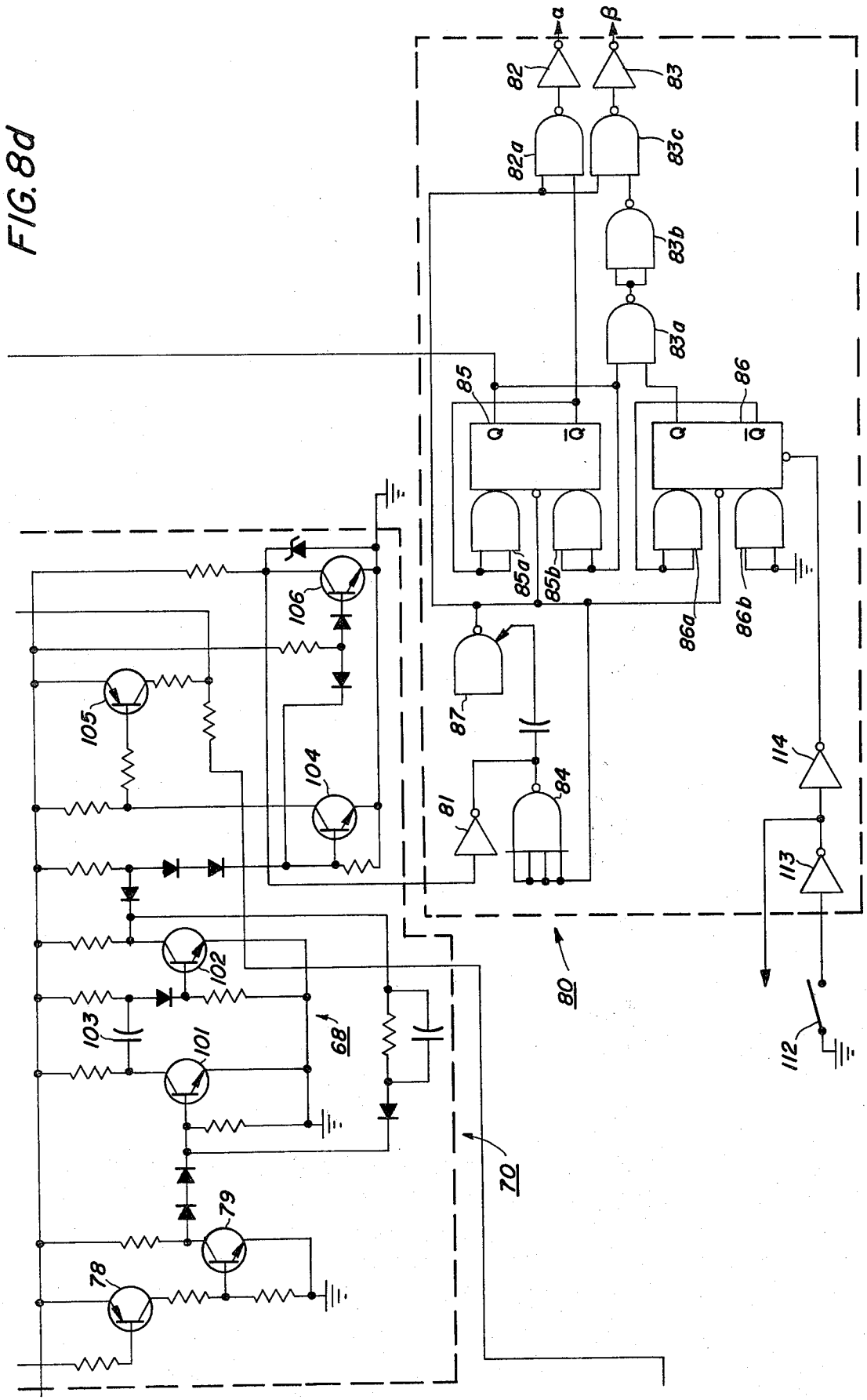
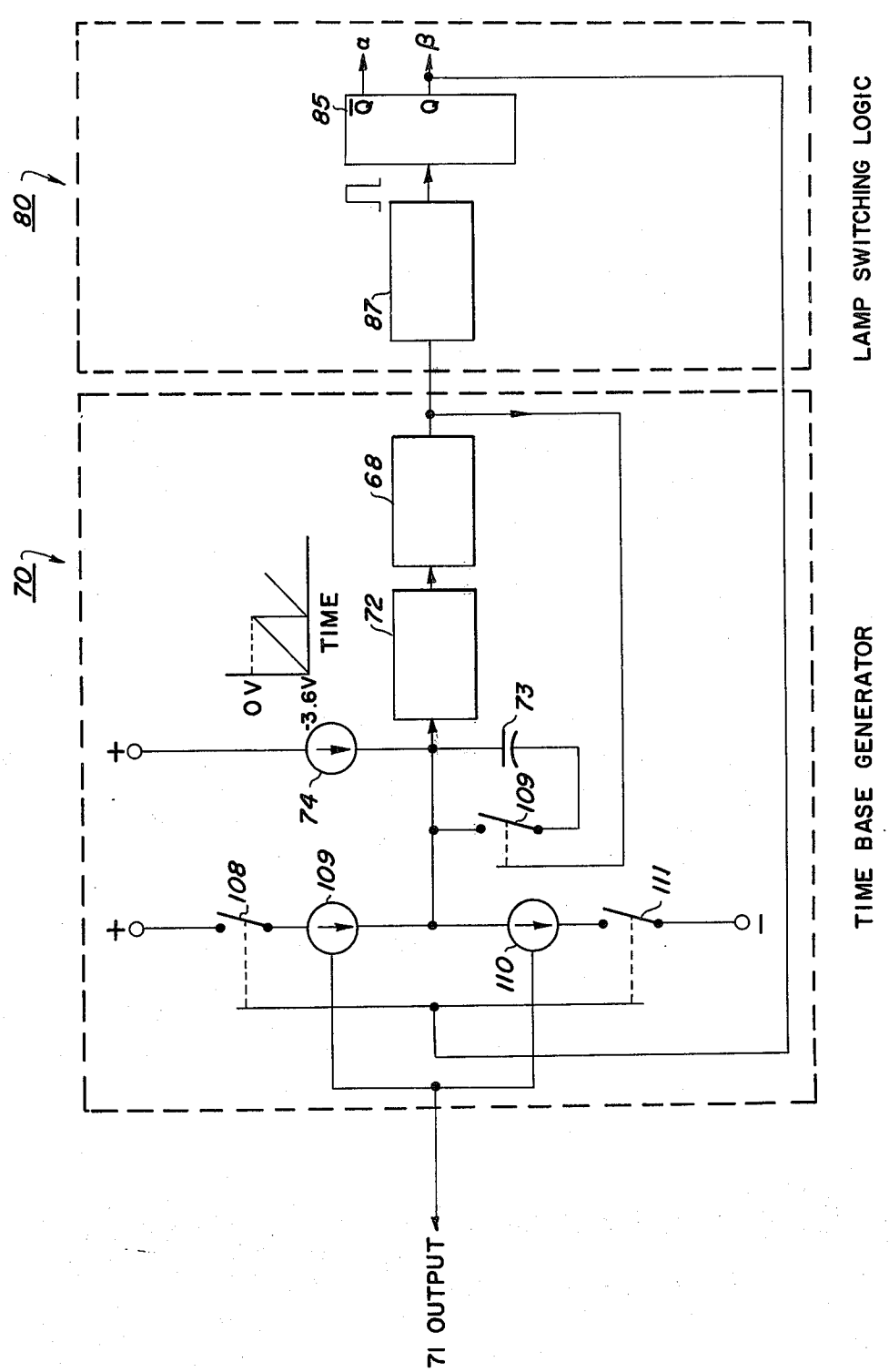

α
β
82
83
82a
83c
83b
83a
85
86
Q
Q̄
85a
85b
86a
86b
87
81
84
114
113
112
80
70
68
106
105
104
102
103
101
79
78

FIG. 10


80
85
α
β
Q̄
Q
87
LAMP SWITCHING LOGIC
70
68
72
0V
-3.6V
TIME
73
74
109
108
109
111
110
+
+
−
TIME BASE GENERATOR
71 OUTPUT

LAMP CONTROL AND LAMP SWITCH CIRCUIT

BACKGROUND OF THE INVENTION

This invention relates generally to lamp control and lamp switch circuits and more particularly, to electrical circuits for controlling and maintaining the appropriate balance of light output, end-to-end of a long multi-vapor arc lamp.

In the photoelectrophoretic imaging process, black and white or full color images are formed through the use of photoelectrophoresis. An extensive and detailed description of the photoelectrophoretic process is found in U.S. Pat. No. 3,384,488 and 3,384,565 to Tulagin and Carreira, U.S. Pat. No. 3,383,933 to Yeh and U.S. Pat. No. 3,384,566 to Clark, which disclose a system where photoelectrophoretic particles migrate in image configuration providing a visual image at one or both of two electrodes between which the particles suspended within an insulating carrier is placed. The particles are photosensitive and are believed to bear a net electrical charge while suspended which causes them to be attracted to one electrode and apparently undergo a net change in polarity upon exposure to activating electromagnetic radiation. The particles will migrate from one of the electrodes under the influence of an electric field through the liquid carrier to the other electrode.

The photoelectrophoretic imaging process is either monochromatic or polychromatic depending upon whether the photosensitive particles within the liquid carrier are responsive to the same or different portions of the light spectrum. A full-color polychromatic system is obtained, for example, by using cyan, magenta and yellow-colored particles which are responsive to red, green and blue light respectively.

It has been found that long multi-vapor lamps with their high efficiencies and controllable spectral outputs show great promise in producing optimum results in photographic systems using artifical light. The most important factor in controlling the spectral energy distribution uniformity along the length of the lamp is the metal halide materials present in the vapor. For example, in the photoelectrophoretic imaging process using opaque or transparent originals, selecting appropriate metal halide materials and balancing their ratios to match photoelectrophoretic pigment sensitivities for the best process response is a major area of concern. Some long multi-vapor arc lamps in commercial use require about 2 mg. or mercury to facilitate starting. In connection with certain photoelectrophoretic imaging operations, the photoelectrophoretic process should not "see" the spectral emission lines of mercury vapor for optimum images. In other photoelectrophoretic imaging systems, mercury may be virtually absent from the lamps used, nevertheless, there are special characteristics and problems associated with them. For example, as soon as the lamp is ignited, the metal halide materials within the lamp tends to selectively migrate to one end of the lamp with a resultant end-to-end unbalance in light output. This migration of materials is called cataphoretic migration.

Other inventions have been discovered for controlling the operation of the lamp intensity of vapor lamps. One such process is disclosed in the patent to Dessoulavy et al., U.S. Pat. No. 3,514,667 issued May 26, 1970. This patent shows a circuit for controlling operation of a discharge tube which includes rectifier means

for converting current from an alternating current source into direct current to be delivered to the tube. The rectifier includes controlled rectifier elements having control terminals or gates, and controllable supply of impulses operable to determine the portion of a cycle of alternating current supply during which direct current flows through the tube. However, this patent is not concerned with the drawbacks of cataphoretic migration in long multi-vapor arc lamps.

Accordingly, it is an object of this invention to provide an electrical control system for maintaining appropriate balance of light output along the length of long multi-vapor arc lamps.

Another object of this invention is to compensate for changes in spectral energy distribution of long multi-vapor arc lamps with operating time and variations from lamp to lamp.

A further object of this invention is to provide for effects of ambient temperature cooling of long multi-vapor arc lamps end-to-end.

It is another object of this invention to employ a lamp switching circuit to periodically reverse the direction of current flow through long multi-vapor arc lamps for use in photoelectrophoretic imaging systems.

Another object of this invention is to control the relative dwell times of the two polarities of alternating voltage supply source to long multi-vapor arc lamps in order to prevent the same migrations that can also be contributed to by differential end-to-end temperatures of the lamp and end-to-end imperfections in the lamp.

Another object of this invention is to provide control circuits for starting and operating long multi-vapor arc lamps.

Still a further object of this invention is to improve the application of long multi-vapor arc lamps to photoelectrophoretic imaging techniques.

SUMMARY OF THE INVENTION

These and other objects of this invention are accomplished by providing a lamp sensing circuit for detecting light intensity differences at opposite ends of a lamp using a single photodiode.

The signal from the photodiode, which may be sinusoidal, is detected, amplified and then split into two signals, equal in amplitude and separated in phase by 180°. The reference signal out of the chopper driver is shifted to be exactly in phase with the signal from the photodiode. The reference signal is then simultaneously squared and split into two signals separated in phase by 180°.

The two reference square waves gate four linear amplifiers of the phase-amplitude detector on and off. Two amplifiers are "on" and two are "off" at any given instant in time. Two amplifiers are capable of positive (+) outputs only, and two are capable of negative (−) outputs only.

The "D.C." output signal from the phase amplitude detector is used to control the period of time between alternating pairs of pulses in a pulse chain in a time base generator. The time period between the other alternate pairs of pulses in the pulse chain may be a fixed time interval. The time variance of the variable half of each period is proportional to the phase amplitude detector D.C. output signal. The peak amplitude of this varying D.C. signal is proportional to the imbalance of the lamp and the polarity indicates the direction of any such imbalance.

The direction of current flow in the lamp is reversed by triggering on two SCR's in a bridge circuit that were not conducting. When a set of SCR's in the bridge are triggered on, this immediately places each of the two "commutating" capacitors across the connected conducting SCR's applying a reverse bias potential to that SCR equal to the lamp voltage. The initially conducting SCR's are "cut-off" by the applied reverse bias. The capacitors discharge through the newly conducting SCR's, the previous current conducting inductors and the lamp. The current flow continues in the same direction as the lamp half cycle just being completed. The capacitors then reverse charge as the lamp begins to conduct in the new direction.

DESCRIPTION OF THE DRAWINGS

These and other objects and advantages will become apparent to those skilled in the art after reading the following description taken in conjunction with the accompanying drawings wherein:

FIG. **1** illustrates a simplified block diagram of the lamp control and lamp switch according to this invention.

FIG. **2** is a simplified schematic circuit diagram of the phase amplitude detector portion of the lamp control circuit.

FIGS. **3** and **4** are waveform graphs of the time, phase and polarity relations of input and output signals of the phase amplitude detector circuit.

FIG. **5** is a waveform graph of the time base generator output and the lamp polarity dwell time relations.

FIG. **6** is a schematic circuit diagram of the lamp switch according to this invention.

FIG. **7** is a simplified schematic circuit diagram of the lamp switch.

FIGS. **8***a–d* combine to form a schematic circuit diagram of the lamp control circuit according to this invention.

FIG. **9** shows how FIGS. **8***a–d* are connected together.

FIG. **10** shows a simplified diagram of the time base generator and lamp switching logic circuits.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention herein is described and illustrated in a specific embodiment having specific components listed for carrying out the functions of the apparatus. Nevertheless, the invention need not be thought of as being confined to such a specific showing and should be construed broadly within the scope of the claims. Any and all equivalent structures known to those skilled in the art can be substituted for specific apparatus disclosed as long as the substituted apparatus achieves a similar function. It may be that other apparatus will be invented having similar needs to those fulfilled by the apparatus described and claimed herein and it is the intention herein to describe an invention for use in apparatus other than the embodiment shown.

FIG. **1** illustrates in block diagram form the lamp control and lamp switch circuits according to this invention. The lamp **2** is mounted for exposure within an imaging system which, in a preferred embodiment, may be a photoelectrophoretic imaging system. The photoelectrophoretic imaging process is described in detail in U.S. patents referred to hereinearlier. The lamp **2** may be a metal halide lamp about 15 inches in length.

In operation, the light signal, alternating from end-to-end of the lamp **2**, is sampled to a single silicon photodiode **12**. The photodiode **12** is looking at apertures of two light pipes **11**, one from each end of the lamp **2**. The light, in one embodiment, may be fed to the photodiode **12** through a red filter (not shown) and a light chopper **40**.

The light chopper **40** may be a tuning fork clock unit with movable chopper vanes (not shown) driven at sinusoidal velocity to alternately sample light from the light pipes **11** to photodiode **12**. Many chopper configurations are as useable as the tuning fork clock unit. For example, the light chopper may be a machine driven rotating disk. To minimize interference, the chopper vanes are driven at a constant frequency other than power line frequencies, or multiples thereof, used near the system. For example, a suitable frequency of 1.0 KHz may be used as the frequency of the chopper vanes.

It is appreciated that the light pipes **11** apertures and the position and motion of the light chopper **40** chopper vanes may be adjusted to produce a D.C., plus sinusoidal output signal from the photodiode **12** whenever the light pipes **11** are transmitting different light intensity levels. Although a sinusoidal signal is preferred for the output from photodiode **12**, a sinusoidal signal is not required. For example, the output signal may be in the form of a square wave. The alternating component of the D.C., plus sinusoidal signal is at the same 1.0 KHz frequency as that of the chopper vanes. It should be apparent that the peak-to-peak amplitude of the D.C., plus sinusoidal signal produced from the photodiode **12** is proportional to the difference in light intensity levels transmitted to it by the two light pipes. The photodiode **12** output signal is coupled into the sensing circuit **10**.

SENSING CIRCUIT

FIG. **8***a* shows a typical arrangement for the sensing circuit **10** used to detect the photodiode output signal. The sensing circuit **10** includes the field-effect transistor (FET) **16** wired across photodiode **12**. The FET **16** uses a single 15 volt D.C. supply with R_D in series in the D.C. loop. The drain to source voltage across FET **16** is taken between capacitor **13** and the sliding contact of source resistor **17**. The FET **16** performs a function of impedance conversion by transforming all impedances and currents on one side with respect to the impedances and currents on the other side. Thus, the FET output signal is the same 1.0 KHz input signal from photodiode **12**. The 1.0 KHz output signal from FET **16** is fed via the sliding contact of resistor **17** to the A.C. coupling capacitor **18** of the tuned amplifier circuit **20**.

TUNED AMPLIFIER CIRCUIT

Still referring to FIG. **8***a*, there is illustrated a typical tuned amplifier circuit generally designated at 20. The tuned amplifier circuit **20**, which includes the operational amplifier **21**, functions as a band-pass filter. The tuned amplifier **20** operated in a linear mode typically has a bandwidth, as defined by the frequency range between the −3dB points of its gain versus frequency characteristics, of about 80 Hz–100 Hz. Ideally, its center frequency is selected at about 1.0 KHz to filter out any noise associated with the chopper **40**, as well as other extraneous noise, such as may be caused by nor-

mal flunctuations in the voltage level of the power mains.

The operational amplifier **21** functions, essentially, to increase the amplitude of the 1.0 KHz A.C. signal coupled into the coupling capacitor **17.** As will be recalled, the peak-to-peak amplitude of the input signal depends upon the imbalance of the lamp intensity end-to-end. The amplifier **21** is intended to amplify only the narrow bandwidth of 1.0 KHz frequencies. Feedback is provided through the bridged-T-network comprising the high-pass capacitor **27** and the low-pass loop resistors **28** and **29.** Biasing is provided by the resistor **9** and resistor **19** functions as a drift stabilizing resistor. The output signal from amplifier **21** is coupled into the phase-splitter circuit **22.**

PHASE-SPLITTER CIRCUIT

The phase-splitter circuit splits the amplifier signal from the amplifier **21** into two signals, equal in amplitude and separated in phase by 180°. One typical circuit to accomplish this function is shown in FIG. **8***a*.

The phase-splitter circuit **22** is essentially two R-C coupled transistor amplifier stages. The output of transistor **23** amplifier stage is coupled via the capacitor **29** into the input of transistor **24** amplifier stage. The gain for both stages may be unity. Since the output of transistor **24** is 180° out of phase with respect to the input in the normal operating frequency range, the input to transistor **24** is 180° out of phase with the input into transistor **23.** Hence, their outputs are likewise displaced.

The constant current regulator **30** is designed to maintain a fixed current through the output load resistor **31.** The transistor **32** emitter current level is fixed by the zener diode **33.** If the tap on the output load resistor **31** is adjusted correctly, just enough voltage is applied to cause the output of transistor **24** to be equal in amplitude to that of transistor **23.** Thus, the output signal produced from the phase-splitter circuit **22** are two A.C. sinusoidal signals, phase 1 (ϕ_1) and phase 2 (ϕ_2) both at the 1.0 KHz input frequency. The peak-to-peak amplitude of the output signals ϕ_1 and ϕ_2 is proportional to the imbalance of the intensity of the lamp **2** from one end to the other. If there is no imbalance, then the 1.0 KHz a-c signals (ϕ_1 and ϕ_2) will have zero amplitude.

The two A.C. output signals ϕ_1 and ϕ_2 produced from the transistors **23** and **24** are coupled into the phase amplitude detector circuit **50** via leads **25** and **26** from the transistors **23** and **24** respectively. The lead **25** is used to couple the 1.0 KHz a-c sinusoidal signal ϕ_1 from the transistor **23** into the phase amplitude detector circuit **50.** The lead **26** is used to couple the 1.0 KHz a-c sinusoidal signal ϕ_2 from the transistor **24** into the phase amplitude detector circuit **50.** The phase amplitude detector **50** will be described in detail hereinafter.

The 1.0 KHz signal from the light chopper **40** that is used to drive the chopper vanes may also be used as a reference signal.

AMPLIFIER-REFERENCE CIRCUIT

FIG. **8***c* shows a typical circuit arrangement of the amplifier-reference circuit **60.** The amplifier-reference circuit includes the filter **41,** converter **48,** squaring circuit **47** and invertering circuit **49.**

The signal from the chopper **40** is essentially a square wave when it comes out of the chopper driver. The 1.0 KHz chopper driver signal from light chopper **40** is coupled into the π section filter circuit **41** which is intended to pass only the fundamental component of the 1.0 KHz signal and produce attenuation for all frequencies above. After the chopper driver signal has been filtered, it is coupled into the converter circuit **48.**

The converter circuit **48** is used to convert the square wave signal from the light chopper **40** to a sine wave. The filtered square wave signal from the light chopper **40** is coupled via capacitor **39** into the transistor **42** input. Transistor **42** sinusoidal output signal is intended to provide a 45° lead relationship with respect to the input square wave signal. The filtered square wave signal is also connected to the base of transistor **43.** Transistor **43** sinusoidal output signal is intended to provide a 45° lag relationship with respect to the input signal. Thus, there is a 90° phase difference at the common output from the transistors **42** and **43.** This output signal from the converter circuit **48** may then be shifted slightly by the variable resistor **46** to get it in phase with the fundamental alternating component of the output signal from the photodiode **12.**

After the output signal from the converter circuit **44** has been shifted, it is fed via the sliding contact of the variable resistor **46** into a squaring circuit **47.** The squaring circuit **47** output signal is coupled into the inverter circuit **49** which is used to develop the square wave output reference signal REF that is in phase with the input signal from the converter circuit **48.** Since the inverter circuit **49** input signal is 180° out of phase with the input signal into squaring circuit **47,** there is a similar displacement of the outputs. Thus, squaring circuit **47** output signal is the square wave signal $\overline{\text{REF}}$ which is the same amplitude as REF but 180° out of phase (see FIG. **3**).

PHASE AMPLITUDE DETECTOR

In FIGS. **8***a–c* is shown the circuit arrangement of the phase amplitude detector circuit **50.** A simplified schematic diagram of the phase amplitude detector circuit **50** is illustrated in FIG. **2.** The phase amplitude detector circuit **50** may be used to produce a signal indicative of which end of the lamp **2** is the brighter. The output signal from the phase amplitude detector circuit **50** is either a positive or negative D.C. signal depending upon whether the left or giht end of the lamp **2** is brighter. For example, if the output D.C. signal is positive, this means that the left end of the lamp is brighter whereas a negative D.C. output signal means that the right end of the lamp is brighter.

The two reference square wave signals REF and $\overline{\text{REF}}$ produced by the reference circuit **60** may be used to control the operation of the phase amplitude detector circuit **50.** The phase amplitude detector circuit includes four linear amplifiers **51, 52, 53** and **54** arranged in such a manner that the output will provide the phase and amplitude demodulation of the signals ϕ_1 and and ϕ_2. The reference signals REF and $\overline{\text{REF}}$ are only used to turn these four linear amplifiers on and off. The signals REF and $\overline{\text{REF}}$ enable and disable the linear operation of the four linear amplifiers.

The four amplifiers **51, 52, 53** and **54** are each connected with gating diodes **61, 62, 63** and **64** respectively.

The two reference signals control the operation of the phase amplitude detector circuit by gating the four linear amplifiers on and off.

The reference signal REF is applied via lead **55** into the gating diodes **61** and **64** of amplifiers **51** and **54** respectively. The amplifier **51** can only put out a positive signal that is a result of a negative going ϕ_2 input. The REF input signal to amplifier **51** is coupled through gating diode **61** which permits amplifier **51** to linearly amplify the signal on line **26** (ϕ_2) during the negative half cycles of ϕ_2 when REF is concurrently positive. When REF is negative, however, amplifier **51** is disabled from linear operation regardless of the ϕ_2 signal.

The amplifier **54** can only put out a negative signal that is the result of a positive going ϕ_1 input. The REF input signal to amplifier **54** is coupled via lead **55** through gating diode **64** which permits amplifier **54** to linearly amplify the signal on line **25** (ϕ_1) during the positive half cycles of ϕ_1 when REF is concurrently negative. When REF is positive, however, amplifier **54** is disabled from linear operation regardless of the ϕ_1 signal.

The reference signal $\overline{\text{REF}}$ is applied via lead **56** into the gating diodes **62** and **63** of amplifiers **52** and **53** respectively. The amplifier **52** can only put out a positive signal that is the result of a negative going ϕ_1 input. The $\overline{\text{REF}}$ input signal to amplifier **52** is coupled through gating diode **62** which permits amplifier **52** to linearly amplify the signal on line **25** (ϕ_1) during the negative half cycles of ϕ_1 when $\overline{\text{REF}}$ is concurrently positive. Where $\overline{\text{REF}}$ is negative, amplifier **52** is disabled from linear operation, regardless of the ϕ_1 signal.

The amplifier **53** can only put out a negative signal that is the result of a positive ϕ_2 input. The $\overline{\text{REF}}$ input signal to amplifier **53** is coupled via lead **56** through gating diode **63** which permits amplifier **53** to linearly amplify the signal on line **26** (ϕ_2) during the positive half cycles of ϕ_2 when $\overline{\text{REF}}$ is concurrently negative. When $\overline{\text{REF}}$ is positive, however, amplifier **53** is disabled from linear operation regardless of the ϕ_2 signal.

The four amplifiers **51, 52, 53** and **54** arranged in the manner described above form an amplifier gating system, two amplifiers are on and two are off at any given instant in time depending upon the REF and $\overline{\text{REF}}$ signals. Amplifiers **53** and **54** are capable of negative outputs only and amplifiers **51** and **52** are capable of positive outputs only. These amplifiers whose associating circuit arrangement for each is identical, lose nothing at the output terminal for the other polarity and there is no substantial diode drop across the output diode because the gain of the amplifier is used to essentially divide the drop across the diode by the gain of the amplifier. The output diodes are connected so that the output of the amplifier is not connected directly to the output terminal of the amplifier. Instead, the output is connected to a diode which is in series with the output of the amplifier and the feedback resistor of the amplifier.

So long as there are 1.0 KHz REF and $\overline{\text{REF}}$ signals into phase amplitude detector circuit **50,** there will always be two amplifiers that are capable of producing either a positive or negative D.C. output signal. The polarity of the D.C. output signal, positive or negative, depends on whether ϕ_1 or ϕ_2 is in phase with the 1.0 KHz REF signal.

Referring now to FIGS. **3** and **4,** there is shown graphs of the time, phase and polarity relations of input and output signals of the phase amplitude detector circuit **50.**

From the four linear amplifiers **51, 52,** 53 and **54** with their particular outputs, four signals **51** out, **52** out, **53** out and **54** out, respectively, are derived. These four signals, added linearly in the operational amplifier **57,** give either a full wave rectified positive signal out (illustrated as Case 1 in FIG. **3**) or a full wave rectified negative signal out (illustrated as Case 2 in FIG. 4). The peak amplitude of this varying D.C. signal is proportional to the imbalance of the lamp end-to-end and the polarity indicates the direction of any such imbalance. For example, Case 1 output from amplifier **57** means the left end is brighter. Case 2 output means that the right end of the lamp **2** is brighter. To correct for any such imbalance, this D.C. signal is converted into a time variable dwell difference. Thus, if the balance of the lamp **2** is varying as a function of time, the polarity time dwell of the driving voltage for the lamp is varied in synchronism therewith.

TIME BASE GENERATOR CIRCUIT

More particularly, the D.C. signal from the phase amplitude detector circuit **50** is used to control the period between alternate pairs of pulses, time period "V", in a pulse chain in the time base generator **70.** The period between the other alternate pairs of pulses in the chain, time period "*f*", is fixed.

FIGS. **8***b* and **8***d* show a typical arrangement of the time base generator circuit. FIG. **1***a* shows a simplified circuit of the time base generator circuit **70.** FIG. **5** illustrates the time base generator circuit **70** output pulse chain and the lamp polarity dwell time relationships. The time variance of the variable half period, V, is proportional to the D.C. end-to-end balance signal. A illustrates the condition where the lamp **2** intensity is balanced end-to-end ($V=f$), B shows the output wave where the right end of the lamp **2** is brighter ($V>f$) and C illustrates the condition where the left end of lamp **2** is brighter ($V<f$). The **87** output wave shown in FIG. **5** represents regenerated timing pulses to be described hereinafter.

The output signal from amplifier **57** is coupled to the input of the amplifier **71.** The time base generator **70** is designed such that for an input into amplifier **71** other than zero, the time spacing of the chain of pulses will change such that two consecutive pulses will be separated by time *f* and the next succeeding pulse will follow after time period V and the next pulse time period *f*, and etc. The time period V will be controlled by the amplitude and polarity of the finite input signal into amplifier **71.**

SCHMITT TRIGGER CIRCUIT

FIG. **8***b* shows a typical arrangement for the Schmitt trigger circuit **72.** The Schmitt trigger circuit **72** functions as a zero volt level detector. The Schmitt trigger circuit **72** includes transistors **77** and **77'**. When the input to transistor **77** is increased sufficiently, for example, from −3.6 volts to zero, the base-to-emitter voltage is large enough to permit a trigger pulse from the Schmitt trigger circuit **72.**

The trigger pulse from the Schmitt trigger circuit **72** is supplied to the input of the monostable multivibrator (one-shot) **68.** The one-shot **68** develops a trigger pulse of about 2 microseconds in pulse width.

This 2 microsecond trigger pulse is coupled to the inverter **81** in the lamp switching logic circuit **80.**

LAMP SWITCHING LOGIC

Referring now to FIG. **8***d*, the lamp switching logic circuit **80** is illustrated in logical symbols rather than the conventional schematic circuit diagram for purposes of clearity. The lamp switching logic circuit **80** is used to convert the chain of pulses from the time base generator **70** to two pulse chains, Alpha (α) and Beta (β). These two pulse chains (α and β) are employed to control the operation of two pairs of silicon controlled rectifiers (SCR's) in the lamp switch circuit **90** by triggering the SCR's on and off. The lamp switch circuit **90** will be described more particularly hereinafter.

The lamp switching logic circuit **80** includes the inverter **81** and the AND gates **84** and **87.** The inverter **81** and gates **84** and **87** function to convert the chain of pulses from the time base generator **70** to regenerated timing chain of pulses having identical spacing. The widths of these regenerated timing chain of pulses (see FIG. **5**) are suitable for firing the silicon controlled rectifiers (SCR's) in the lamp switch circuit **90,** which will be described in particularity hereinafter. The AND gate **87** provides a one-shot trigger pulse of about 10 microseconds in width. The 10 microsecond trigger pulse is applied to the input terminals of the flip-flops **85** and **86.** The flip-flops **85** and **86** and the steering gates **85***a–d*, 86*a–b*, 82*a* and **83***a–c* associated with their outputs produce the two pulse chains, α and β referred to hereinearlier. The pulse chain may be used to gate or fire the odd numbered SCR's **91** and **93** in the lamp switch circuit **90.** The β pulse chain may be used to gate or fire the even numbered SCR's **92** and **94** in the lamp switch circuit **90.** e or fire the even numbered SCR's **92** and **94** in the lamp switch circuit **90.**

It will be appreciated that the flip-flop **85** changes its state with each input pulse from the time base generator **70.** For example, the Q and $\overline{Q}$ outputs of flip-flop **85** alternately steer the reproduced timing chain either to the inverter **82** or to the inverter **83.** The output produced from inverter **82** is the pulse chain and the output of inverter **83** is the β pulse chain. When the flip-flop **85** output Q is high (the "one" state) the regenerated input timing chain is steered to inverter **83.** When this condition occurs, simultaneously the connection from flip-flop **85** output Q to the base of the transistor **69** in the time base generator **70** (FIG. **8***b*) allows the output signal from the amplifier **71** to influence the current flow in the timing capacitor **73** to set the variable time, V, to the next timing chain pulse which will appear in the β pulse chain. The relationships between the output pulse chain from the time base generator **70,** the regenerated pulse chain and the α and β pulse chains are shown graphically in FIG. **5.**

The flip-flop **86** may be used to inhibit the α pulse chain by the selector switch **112** until the lamp **2** is ignited. Once the lamp **2** has been ignited and requires switching, flip-flop **86** is utilized to initiate that switching after an pulse. In such case, the switch **112** is moved from non-inhibit inverter **114** to the inhibit inverter **113.**

The chain of pulses generated in the time base generator **70** describes the polarity time dwell. The lamp **2** always has, for example, the left side positive and the right side negative for 5 milliseconds. But the left side negative and right side positive polarity, applied to the lamp **2,** how long it dwells there is proportional to the D.C. signal out of the phase amplitude detector **50** and whether it is longer or shorter than 5 milliseconds depends upon the polarity of that D.C. signal. Thus, the lamp intensity is constantly observed and, if the left end is brighter than the right end ($V<f$), that means the polarity need to dwell a shorter amount of time in left end negative, right end positive case. Conversely, if the right end is brighter than the left end ($V>f$), that means the polarity needs to dwell a greater amount of time in left end negative, right end positive case.

The instant the lamp **2** has started conducting, the process of cathaphoretic migration begins. The metal halide materials within the lamp tends to selectively migrate to one end of the lamp with resultant end-to-end imbalance in light output. In connection with photoelectrophoretic opaque imaging, and other photographic systems that require exposure with artifical light, the process should not see an imbalance end-to-end of the light from the lamp as a result of cathophoresis.

Another factor that tends to have an effect on the spectral output of long multi-vapor arc lamps is variations in temperature along the length of the lamp. As the operating temperature increases, there is a resultant shift in spectral output. In order to reduce these characteristics of long multi-vapor lamps and optimize results for exposure with artifical light, the lamp switching logic circuit **80** and lamp switch circuit **90** of this invention is provided.

FIG. **10** is a simplified diagram of the time base generator **70** and lamp switching logic circuit **80** which, in conjunction with the other Figures, may be useful to illustrate the operation of the time base generator and the lamp switching logic circuits.

As recalled earlier, Case 1 positive output from amplifier **57** in the phase amplitude detector **50** indicates that the left end of lamp **2** is brighter and $V<f$. In such case, the output from the amplifier **71** will be negative, increasing the current from the current generator **109** and decreasing the current down in current generator **110.** The constant current generator **74** is not changed, thereby, resulting in a net increase in the current supply to charging capacitor **73,** thus, charging capacitor **73** faster and shortening V. Conversely, when Case **2** output from amplifier **57** is negative, this indicates that the right end of lamp **2** is brighter and $V>f$. The output from amplifier **71** will be positive, decreasing the current from current generator **109** and increasing the current from current generator **110.** The constant current generator **74** is not changed thereby, resulting in a net decrease in the current supply to charging capacitor **73,** thus charging capacitor **73** at a slower rate and lengthening V.

The variable resistor **75** may be adjusted so that whenever the input into amplifier **71** is zero volts the output will also be zero volts. In such case, the current flow through **108–109** is equal to the current flow through **110–111.** Thus, the system is balanced so that there is a fixed time interval for V and f that is equal under the zero volt condition. When there is an input into amplifier **71** other than zero volts, V will vary in proportion to that input signal. The gain resistor **76** may be adjusted to determine how much V varys in proportion to the non-zero volt input condition.

LAMP SWITCH

The lamp switch circuit **90** is used to minimize the effect of cathophoresis by reversing the polarity of current flow through the lamp, and to minimize the transition interval between the time that there is full current flow on in one direction and that time that there is full current flow in the opposite direction. The lamp switch circuit **90** utilizes SCR's in place of conventional mechanical switches and relays so as to provide a high voltage device that is capable of some abuse in the switching.

The use of SCR's in a bridge arrangement across a load is generally known. For example, SCR Manual, Fifth Edition, by General Electric suggests such as configuration at 13.1.3, Inverter Configurations, page 353. However, the triggering and commutation methods of this invention used to reverse the direction of current flow through long multi-vapor arc lamps is of no concern in the discussion therein.

The lamp switch circuit **90** includes four SCR's connected in an SCR bridge configuration. The SCR rectifier bridge has four SCR's **91, 92, 93** and **94** arranged in pairs such that only one pair of SCR's is turned on at any instant of time. Either the odd numbered pair (**91, 93**) or the even numbered pair (**92, 94**) are turned on at any instant. When the odd pair, **91** and **93,** is turned on, current flow through the lamp **2** is in one direction and if the even pair of SCR's, **92** and **94,** is turned on, current flows in the opposite direction through the lamp **2.** The output signal α from **82** of the lamp switching logic circuit **80** is coupled into the gates of SCR's **91** and **93** to trigger these SCR's on. The output signal β from **83** of the lamp switching logic circuit **80** is coupled into the gates of SCR's **92** and **94** to trigger these SCR's on.

A problem encountered in earlier transistor systems is the problem of getting more than two transistors in a bridge turned on at the same time. To prevent this, in the SCR bridge, there are two capacitors, **C1** and **C2,** called commutating capacitors, utilized in the lamp switch circuit **90.** With a current path through a pair of SCR's, odd or even, turned on in the normal manner, the commutating capacitors **C1** and **C2** will charge up to what ever voltage is across the lamp **2** at a particular polarity. Left to right, the two commutating capacitors **C1** and **C2** are always charged the same way. Very quickly after capacitors **C1** and **C2** are charged up, **C1** has the negative charged end at the cathode of a non-conducting SCR and its positive end is at the cathode of a conducting SCR. **C2** has the negative end at the anode of the other conducting SCR and its positive end is at the anode of the other non-conducting SCR. If you now take and turn on the other pair of SCR's, the capacitors **C1** and **C2** are charged up in such a manner as to help the desired SCR's turn on rapidly. This pair of SCR's has a very large supply of current potential available to their cathode and anode in the right direction. Thus, they can turn on very quickly. A feature of the lamp switch circuit **90** is that when you just turn on a SCR that is just gating, it instantly connects charged up capacitor, **C1** or **C2,** through itself across the SCR that was turned on and is desired to be turned off. What ever the value of lamp voltage was is applied as reverse bias to the SCR that was turned on and is desired to be turned off. The current in an SCR and the circuit associated with it (resistor, diode) is reversed or blocked in the system in a few nanoseconds.

When the second pair of SCR's is turned on the charged commutating capacitors **C1** and **C2** are connected in reverse polarity across the previously conducting pair of SCR's. When this occurs, there is the possibility of an instant short through to be produced straight across the right side of the SCR bridge or across the left side of the SCR bridge or across both. If you turn on pair of SCR's on and the other pair of SCR's off, the first pair is simply trying to pump more current, and suddenly provides a very high current path. To prevent a short circuit from happening, the four inductors, **L1, L2, L3** and **L4,** are inserted into the lamp switch circuit. These four inductors or coils are inserted in the lamp switch circuit **90** strictly to prevent a high current flow from starting quickly. On each side of the SCR bridge, one inductor has current flow through it initially and the other inductor has no current flow. The inductors that has no current flow through it when you initially fire an SCR pair is the inductors that are really holding things off and thereby avoiding a short circuit. Once the previously conducting SCR pair is turned off, which happens in a few nanoseconds, (but if it occurs in microseconds it would still be all right), current may now build up to some reasonable value in the previously non-conducting coil because they happen to be the ones that will be conducting lamp current next anyway. Once the predetermined SCR's are shut off, the surplus energy in the capacitors **C1** and **C2** is discharged through the lamp **2.** As soon as the charges drop to zero in the discharging commutating capacitors, **C1** and **C2,** they immediately start to charge in the opposite direction, therefore, getting ready for the next polarity reversal. By the time capacitors **C1** and c2 are charged completely, or very near completely, the lamp **2** is now conducting in the new or opposite polarity from what it was conducting.

In the preferred embodiment of the lamp switch circuit **90,** all inductors are of the same inductance (L=L1=L2=L3=L4), and the capacitors are of the same capacitance (C=C1=C2), and the lamp looks approximately resistive, R_L. For example, the the inductance L for each of **L1, L2, L3** and **L4** is $\approx 50\mu H$. Likewise, the capacitance C for each of **C1, C2, C3** and **C4** is 0.1 μf

If is also appreciated that after an SCR pair is turned on, current continues to flow in the lamp **2** for a delay period, τ_D where:

$\tau_D \approx R_L C$

After this delay period τ_D, a rise time τ_R for current flow in the reverse direction in the lamp **2** is encountered, where:

$\tau_R \approx (4_L/R_L)$

Other modifications to the above described invention will be apparent to those skilled in the art and are intended to be incorporated herein.

What is claimed is:

1. A lamp switch circuit for minimizing effects of cataphoresis in long multi-vapor arc lamps comprising:

a. a long multi-vapor arc lamp mounted for exposure;

b. silicon controlled rectifier bridge means connected across said lamp for establishing polarity of current flow through said lamp;

c. control circuit means for triggering said silicon controlled rectifier means on and off when cataphoresis effect causes said lamp light intensity to

become imbalanced end-to-end, said silicon controlled rectifier bridge means comprises,

i. first and second pairs of silicon controlled rectifiers connected in a bridge configuration across said lamp, said first pair of silicon controlled rectifiers for establishing polarity of current flow through said lamp in a first direction when triggered by said control circuit means, said second pair of silicon controlled rectifiers for establishing polarity of current flow through said lamp in a second direction when triggered by said control circuit means;

ii. commutating means for preventing more than two silicon controlled rectifiers in said bridge from getting triggered on at the same time, said commutating means comprise first and second commutating compacitors, said first commutating compacitor wired between cathodes of said first pair of silicon controlled rectifiers, said second commutating compacitor wired between anodes of said second pair of silicon controlled rectifiers; and

iii. current inhibiting means in series with said commutating means for preventing a rapid high current flow.

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