1 595 229

PATENT SPECIFICATION

(11) 1 595 229

(21) Application No. 20737/80 (22) Filed 24 Oct. 1977
(62) Divided out of No. 1595228
(31) Convention Application No. 2647982
(32) Filed 22 Oct. 1976 in
(33) Federal Republic of Germany (DE)
(44) Complete Specification published 12 Aug. 1981
(51) INT CL³ G05B 1/03
(52) Index at acceptance
G4A CM

(54) IMPROVEMENTS IN OR RELATING TO MOS MULTI-STAGE LOGIC CIRCUITS

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German Company of Berlin and Munich, German Federal Republic, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to MOS multi-stage logic circuits of integrated circuit form, with gates provided for the production and transmission of carry signals between stages.

One known design of logic-linking circuits for binary signal transmission using integrated circuits made by the use of MOS techniques consists in the use of static gates, in which one MOS transistor is connected as load resistor in series with at least one MOS switching transistor. The point of connection of a load transistor and the or each switching transistor represents the output of a stage. The control electrodes of the switching transistors represent the inputs of that stage. Whenever a current path formed by a switching transistor is switched to its conductive state, a d.c. current flows through the entire stage, i.e. a stage of this kind can consume power in the rest state. In the case of multi-stage, logic circuit arrangements which execute logic or arithmetic operations with carry signals which are thereby formed (for example in the addition of multi-bit words), then if gate stages of this kind are employed for feeding on the carry signals, the power loss becomes considerable.

Furthermore, in order to be able to safeguard against any malfunction due to interference, a specific minimum change in signal levels must be available at the output of such gate stages. This signal level change is determined by the conductivity ratio of the one or more switching transistors to the associated load transistor, which conductivity ratio is itself governed by the characteristic transistor values, namely the channel length and the channel width. Therefore gates of this kind are also referred to as ratio gates. In order that the available signal change is great, this ratio of channel width to channel length must be selected to be high for the MOS transistor that is connected as a load resistor. Consequently, there is a limited freedom of dimensioning for static ratio gates. This is a particularly disadvantageous aspect, in respect of the switching times of such gates. If the output resistance is high as a result of the above mentioned dimensioning limitation regarding the signal change, the time constants determined by the output impedance of a preceding stage and the capacitive input impedance of the following stage are also high, as a result of which the switching times are of a corresponding length.

In order to avoid the above mentioned disadvantage in ratio gates, ratio-less, dynamic gates have been proposed, but with such ratio-less, dynamic gates, the advantage of a low d.c. power loss is only acquired at the cost of greater circuit complexity, on account of the requisite control pulse trains.

It is known that MOS transistors possess a symmetrical switching behaviour, i.e. they can have their controlled path between source and drain connected directly into a signal-conducting arm, where a signal transfer is possible in both directions as a function of control signals connected to the control electrode, i.e. the gate electrode.

One object of the present invention is to provide a substantially d.c.-free transmission of carry signals in logic circuit arrangements, in which static switching behaviour is adopted to avoid the use of dynamic, ratio-less gates.

According to this invention there is provided a MOS multi-stage logic circuit in the form of an integrated circuit with gates for the production and transmission of carry

signals between its stages, the logic circuit being in the form of a comparator including a comparator stage for each digit of the numbers which are to be compared, each stage possessing a respective input for each one of two carry signals formed during the comparison of the preceding, lower valued digits and representing the comparison result for said lower valued digits and each stage having an output for each of the two carry signals formed during the comparison of the assigned digits and representing the result of this comparison and/or the comparison result from the preceding stage, where these carry signal outputs are coupled to the carry signal inputs of the following comparator stage for the following, higher valued digits, in which each comparator stage has a transfer gate which comprises a path between the respective carry signal inputs and the respective carry signal outputs, a respective transfer transistor for each path being connected to a common control input by its control electrode which is arranged to receive a signal dependent on the identity of digits compared in that stage, and further comprising a circuit having two branches in each of which first and second transfer transistors are connected in series between a predetermined voltage source and earth, the control electrode of each said first transistor being connected to the control electrode of the second transistor in the other branch and being arranged to receive a respective signal formed in the stage in dependence on non-identity of, and which is greater of, the two digits being compared in that stage, and the respective connection points between the controlled paths of these tranfer transistors being connected to the respective carry signal outputs.

An embodiment of this invention will now be described, with reference to the accompanying drawing, in which the sole figure is a circuit diagram of an embodiment of a comparator constructed in accordance with this invention.

The figure shows an embodiment of one stage of a logic circuit arrangement in the form of a comparator, for comparing multi-digit dual numbers. The particular digits of two dual numbers, which are to be compared in this stage, will be assumed to be the digits *n*. Those digits of the dual numbers which are to be compared with one another are fed into the stage at respective inputs a_n and b_n. In dependence upon whether a_n is smaller than or greater than b_n, a respective output C_n of C'_n supplies an output signal which can form any carry signal for the following stage. Correspondingly, the stage represented in the figure possesses input C_{n-1} and C'_{n-1}, at which the carry signals are fed in from the preceding stage for the comparison of the lower valued digits of the dual numbers which are to be compared. The numbers a_n and b_n which are to be compared are each fed to a respective input of two NOR-gates 17 and 18. The other inputs of these NOR-gates 17 and 18 are respectively fed with an inverted input signal via separate inverters 19 and 20. The respective inputs of the NOR-gates 17 and 18 are connected to respective inputs of a further NOR-gate 21. A respective transfer transistor, T_{15} and T_{16} has its controlled path arranged in the respective signal channels between the carry signal inputs C_{n-1} and C'_{n-1}, and the associated carry signal outputs C_n and C'_n. These two transfer transistors are commonly controlled from the output of the NOR-gate 21, to form a part of the requisite transfer gate for the carry signals.

This transfer gate is completed by a circuit having two arms in which respective series connected transfer transistors T_{10} and T_{14}, T_{13} and T_{12} are respectively connected to a predetermined voltage U_L, whilst the control electrodes of all these last-mentioned transfer transistors are cross-coupled, and the intermediate connection points of the source and drain of the controlled paths of these transfer transistors are respectively connected to the carry signal outputs C_n and C'_n.

Two characteristic conditions of the stage illustrated in the figure will be considered by way of explanation of the mode of operation of a comparator of this kind.

Firstly it will be assumed that the comparison in a lower-valued preceding stage, (not illustrated) has resulted in identity, i.e. that a logic signal "0" is present at each of the carry signal inputs C_{n-1} and C'_{n-1}. It will further be assumed that for the dual numbers a_n and b_n which are to be compared a_n is greater than b_n. Then a logic "1" is present at the input a_n, and a logic "0" is present at the input b_n. As can readily be seen, a logic "0" then occurs at the output of the NOR-gate 21, so that both of the transfer transistors T_{15} and T_{16} are blocked. Since, furthermore, with the selected states of the input signals, a logic "0" is present at the output of the NOR-gate 17 and a logic "1" is present at the output of the NOR-gate 18, the transfer transistors T_{13} and T_{14} are rendered conductive, whereas the transfer transistors T_{10} and T_{12} are blocked. Via the conductive transfer transistor T_{13}, the voltage U_L is transmitted to the carry signal output C'_n, as a result of which it is indicated that a_n is greater than b_n, which corresponds to the above condition. Simultaneously, the carry signal output C_n is connected to earth potential via the conductive transfer

transistor T_{14}, which ensures that a logic "0" is present at the carry signal output C_n.

Irrespectively of the comparison in the preceding stage for the lower valued digit of the dual numbers which are to be compared, only the result of the comparison in the represented stage is transferred to the following stage for a higher valued digit. If in fact, the comparison proves that the dual number *a* in the *n*-th stage is greater, the result of the comparison in the preceding stage for the lower valued digit is immaterial, as then the dual number *a* is in any case greater than the dual number *b*.

To illustrate another characteristic situation, it will now be assumed that the digits a_n and b_n are equal, and that the comparison in the preceding stage for the lower valued digit has proved that a_{n-1} is greater than b_{n-1}, so that a logic "1" is present at the carry input C'_{n-1}. For example, if the input values a_n and b_n are each equal to a logic "0", it will readily be seen that a logic "0" is present at the outputs of the NOR-gates 17 and 18, and a logic "1" is present at the output of the NOR-gate 21. Then all the transfer transistors T_{10} to T_{14} are blocked, whereas both the transfer transistors T_{15} and T_{16} are rendered conductive. Consequently, a logic "1" which is present only at the carry signal input C'_{n-1}, is transmitted to the carry signal output C'_n, so that it is indicated to the following stage for the higher valued digit that a comparison in the preceding stages for the lower valued digits has resulted in non-identity. Thus in the selected example, it can be seen that one of the digits a_1 to a_{n-1} is greater than one of the digits b_1 to b_{n-1}.

WHAT WE CLAIM IS:—

1. A MOS multi-stage logic circuit in the form of an integrated circuit with gates for the production and transmission of carry signals between its stages, the logic circuit being in the form of a comparator including a comparator stage for each digit of the numbers which are to be compared, each stage possessing a respective input for each one of two carry signals formed during the comparison of the preceding, lower valued digits and representing the comparison result for said lower valued digits and each stage having an output for each of the two carry signals formed during the comparison of the assigned digits and representing the result of this comparison and/or the comparison result from the preceding stage, where these carry signal outputs are coupled to the carry signal inputs of the following comparator stage for the following, higher valued digits, in which each comparator stage has a transfer gate which comprise a path between the respective carry signal inputs and the respective carry signal outputs, a respective transfer transistor for each path being connected to a common control input by its control electrode which is arranged to receive a signal dependent on the identity of digits compared in that stage, and further comprising a circuit having two branches in each of which first and second transfer transistors are connected in series between a predetermined voltage source and earth, the control electrodes of each said first transistor being connected to the control electrode of the second transistor in the other branch and being arranged to receive a respective signal formed in the stage in dependence on non-identity of, and which is greater of, the two digits being compared in that stage, and the respective connection points between the controlled paths of these transfer transistors being connected to the respective carry signal outputs.

2. A MOS multi-stage logic circuit in the form of an integrated circuit substantially as described with reference to the accompanying drawing.

For the Applicants,
G. F. REDFERN & CO.,
Marlborough Lodge,
14 Farncombe Road,
Worthing,
West Sussex, BN11, 2BT.

Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1981
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

1595229 COMPLETE SPECIFICATION

1 SHEET