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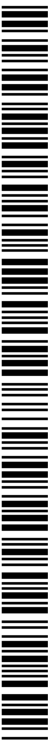

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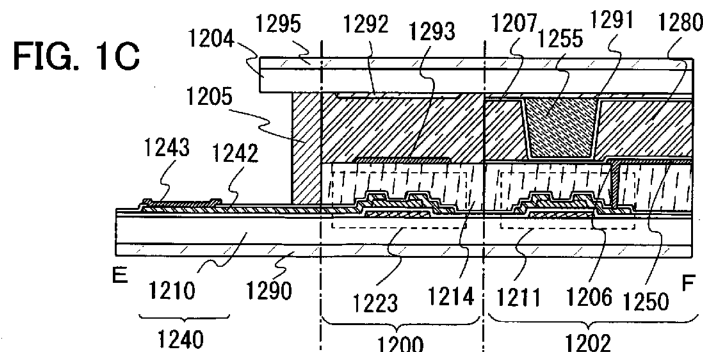


(57) **Abstract**: A semiconductor device according to the present invention has a structure in which: a liquid crystal layer(1280) is provided between a pair of substrates(1204,1210), one of the substrates is provided with a pixel electrode(1250) and a driver circuit(1223); the other of the substrates is a counter substrate which is provided with two counter electrode layers(1291,1292) in different potentials; and one of the counter electrode layers overlaps with the pixel electrode with the liquid crystal layer therebetween and the other of the counter electrode layers overlaps with the driver circuit with the liquid crystal layer therebetween.

DESCRIPTION

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

5

TECHNICAL FIELD

[0001]

The present invention relates to a semiconductor device including a circuit formed using a thin film transistor (hereinafter referred to as TFT) and a manufacturing
10 method thereof. For example, the present invention relates to an electronic device on which an electro-optical device typified by a liquid crystal display panel is mounted as a component.

[0002]

In this specification, a semiconductor device generally means a device which
15 can function by utilizing semiconductor characteristics, and an electro-optical device, a semiconductor circuit, and an electronic device are all semiconductor devices.

BACKGROUND ART

[0003]

20 In recent years, a technique for forming a thin film transistor (TFT) by using a thin semiconductor film (having a thickness of approximately several nanometers to several hundred nanometers) formed over a substrate having an insulating surface has attracted attention. Thin film transistors have been applied to a wide range of electronic devices like integrated circuits (ICs) and electro-optical devices, and
25 development of thin film transistors as switching elements in image display devices, in particular has been hastened.

[0004]

Metal oxides have been known as materials having semiconductor characteristics. The examples of such metal oxides having semiconductor
30 characteristics include a tungsten oxide, a tin oxide, an indium oxide, a zinc oxide, and the like. A thin film transistor in which a channel formation region is formed using such metal oxides having semiconductor characteristics is already known (for example,

see Patent Documents 1 and 2).

[0005]

A liquid crystal display device is known as an example of image display devices. Compared with passive matrix liquid crystal display devices, high-definition images can be obtained with active matrix liquid crystal display devices; therefore, the active matrix liquid crystal display devices have become widely used. In the active matrix liquid crystal display device, pixel electrodes arranged in matrix are driven to display an image on a screen. Specifically, a video voltage is applied between a selected pixel electrode and a counter electrode corresponding to the pixel electrode, and thus, a liquid crystal layer between the pixel electrode and the counter electrode is modulated optically. Light is modulated so that an image is displayed and an observer recognizes the image.

[0006]

An image burn-in may be caused when a voltage is applied to a liquid crystal only in one direction all the time. Thus, an AC drive is employed in which a voltage applied to a liquid crystal layer is periodically inverted. In an AC drive, a voltage applied to a liquid crystal is to be periodically inverted; for example, the polarity of a video voltage based on a voltage of a counter electrode (a common electric potential) is inverted every frame.

[0007]

In addition, an example of an AC drive in which a counter electrode is divided into two counter electrodes and different potentials are applied thereto in a pixel portion is described in Patent Document 3.

[References]

[Patent Documents]

[0008]

[Patent Document 1] Japanese Published Patent Application No. 2007-123861

[Patent Document 2] Japanese Published Patent Application No. 2007-096055

[Patent Document 3] Japanese Published Patent Application No. 2000-347598

DISCLOSURE OF INVENTION

[0009]

A voltage of a counter electrode is adjusted according to a video voltage which is actually applied to a pixel electrode. When the video voltage which is actually applied to a pixel electrode is changed, a defect may occur in a screen; therefore, the voltage of the counter electrode is optimized to correspond to the center of potential
5 amplitude of the pixel electrode.

[0010]

Further, in the case where a pixel portion and a driver circuit are formed over one substrate and a counter electrode is formed over an entire surface of a counter substrate, the driver circuit may be adversely affected by the optimized voltage of the
10 counter electrode.

[0011]

An object of one embodiment of the present invention is to provide a semiconductor device which includes a thin film transistor using an oxide semiconductor layer and in which low power consumption is realized.

15 [0012]

Another object of an embodiment of the present invention is to provide a highly reliable semiconductor device which includes an oxide semiconductor layer.

[0013]

In a semiconductor device according to one embodiment of the present
20 invention, a liquid crystal layer is provided between a pair of substrates, one of which is provided with a pixel electrode and a driver circuit. The other of the substrates is a counter substrate which is provided with two counter electrode layers having different potentials. One of the counter electrode layers overlaps with the pixel electrode with the liquid crystal layer therebetween and the other of the counter electrode layers
25 overlaps with the driver circuit with the liquid crystal layer therebetween.

[0014]

One embodiment of the present invention to be disclosed in this specification is a semiconductor device including: over a first substrate, a first counter electrode layer and a second counter electrode layer having a potential different from that of the first
30 counter electrode layer; a second substrate fixed to the first substrate; a first electrode layer and a second electrode layer over the second substrate; and a liquid crystal layer between the first substrate and the second substrate. The first electrode layer is a pixel

electrode formed in a position overlapping with the first counter electrode layer with the liquid crystal layer therebetween. Further, the second electrode layer is an electrode layer of a driver circuit formed in a position overlapping with the second counter electrode layer with the liquid crystal layer therebetween.

5 [0015]

When the video voltage which is applied to the pixel electrode is changed, a defect may occur in a screen; therefore, the voltage of the first counter electrode layer is optimized to correspond to the center of potential amplitude of the pixel electrode. In this manner, favorable display is conducted. The electric potential of the second
10 counter electrode layer is a ground potential so that static electricity is diffused and let go.

[0016]

With the above structure, at least one of the objects is achieved. The second counter electrode layer which is provided in the driver circuit portion diffuses static
15 electricity applied by electrostatic discharge to let it go or prevents local electric charges (localization of electric charges) i.e., prevents local potential difference, whereby electrostatic breakdown of the semiconductor device can be prevented.

[0017]

In the above-described structure, the first electrode layer is electrically
20 connected to a thin film transistor in a pixel portion, and the second electrode layer is a gate electrode layer of a thin film transistor of the driver circuit.

[0018]

Further, the above-described semiconductor device further includes: a third electrode layer provided over the second substrate; and between the third electrode layer
25 and the first counter electrode layer, a conductive particle electrically connecting the third electrode layer and the first counter electrode layer.

[0019]

The above-described semiconductor device further includes: a fourth electrode layer provided over the second substrate; and between the fourth electrode layer and the
30 second counter electrode layer, a conductive particle electrically connecting the fourth electrode layer and the second counter electrode layer.

[0020]

When a liquid crystal mode such as a TN mode, a VA mode, or an OCB mode which is driven by applying voltage between a pair of substrates, is operated by active matrix driving, voltage is applied through a flexible printed circuit (FPC) which is attached to an active matrix substrate; therefore, in order to generate potential difference between the pair of substrates, a conductor (a common contact portion) which electrically connects a counter electrode of a counter substrate to a connection wiring of the active matrix substrate is needed.

[0021]

This conductor is manufactured in the following manner: a sealing material in which a plurality of conductive particles is mixed is placed in contact with a conductive portion of one of the pair of substrates; and then the substrates are bonded to each other and the conductive particles in the conductive portion are in contact with each electrode of the pair of substrates. Thus, the counter electrode of the counter substrate and a connection wiring of the active matrix substrate are electrically connected to each other.

[0022]

In the above structure, the first electrode layer which is electrically connected to the thin film transistor in the pixel portion is in contact with an oxide semiconductor layer of the thin film transistor. Alternatively, the first electrode layer which is electrically connected to the thin film transistor in the pixel portion is electrically connected to the oxide semiconductor layer of the thin film transistor through an oxide conductive layer. Regarding the above-described connection between the first electrode layer and the oxide semiconductor layer, when the oxide conductive layer is sandwiched therebetween, it is expected to prevent an increase in contact resistance which is caused by formation of an insulating oxide on a surface in the connection portion (contact portion); accordingly, a highly reliable semiconductor device can be provided.

[0023]

As the oxide semiconductor layer, a thin film which is formed using a material denoted as $InMO_3(ZnO)_m$ ($m > 0$) is formed. The thin film is used as an oxide semiconductor layer to fabricate a thin film transistor in an embodiment of the present invention. Note that M denotes one metal element or a plurality of metal elements selected from Ga, Fe, Ni, Mn, and Co. As an example, M may be Ga or may include

the above metal element in addition to Ga, for example, M may be Ga and Ni or Ga and Fe. Moreover, in the above oxide semiconductor, in some cases, a transition metal element such as Fe or Ni or an oxide of the transition metal is contained as an impurity element in addition to a metal element contained as M. In this specification, an oxide
5 semiconductor layer whose composition formula is represented as $InMO_3(ZnO)_m$ ($m > 0$) where Ga is contained as M is referred to as an In-Ga-Zn-O-based oxide semiconductor, and a thin film thereof is also referred to as an In-Ga-Zn-O-based film.

[0024]

As other examples of a metal oxide applicable to the oxide semiconductor layer,
10 any of the following metal oxides can be applied: an In-Sn-O-based metal oxide; an In-Sn-Zn-O-based metal oxide; an In-Al-Zn-O-based metal oxide; a Sn-Ga-Zn-O-based metal oxide; an Al-Ga-Zn-O-based metal oxide; a Sn-Al-Zn-O-based metal oxide; an In-Zn-O-based metal oxide; a Sn-Zn-O-based metal oxide; an Al-Zn-O-based metal oxide; an In-O-based metal oxide; a Sn-O-based metal oxide; and a Zn-O-based metal
15 oxide. A silicon oxide may be contained in an oxide semiconductor layer formed using any of the above metal oxides.

[0025]

Further, in an embodiment of the present invention, the oxide semiconductor layer is subjected to heat treatment for dehydration or dehydrogenation after being
20 deposited. Dehydration or dehydrogenation is heat treatment of the oxide semiconductor layer in an atmosphere of an inert gas such as nitrogen or a rare gas (e.g., argon or helium) at a temperature higher than or equal to 400 °C and lower than or equal to 750 °C, preferably higher than or equal to 425 °C and lower than the strain point of the substrate, so that impurities such as moisture contained in the oxide
25 semiconductor layer is reduced. Further, water (H_2O) can be prevented from being contained in the oxide semiconductor layer again later.

[0026]

The heat treatment for dehydration or dehydrogenation is preferably performed in a nitrogen atmosphere with an H_2O concentration of less than or equal to 20 ppm.
30 Alternatively, the heat treatment may be performed in ultra-dry air with an H_2O concentration of less than or equal to 20 ppm.

[0027]

In the heat treatment for dehydration or dehydrogenation, an instantaneous heating method can be employed, such as a heating method using an electric furnace, a gas rapid thermal annealing (GRTA) method using a heated gas, or a lamp rapid thermal
5 annealing (LRTA) method using lamp light.

[0028]

The conditions of the dehydration or dehydrogenation are determined such that at least a peak at around 300 °C of two peaks derived from water is not detected when the oxide semiconductor layer subjected to the dehydration or dehydrogenation is
10 measured with thermal desorption spectroscopy (TDS) while the temperature is increased to 450 °C. Therefore, even if TDS is performed at up to 450 °C on a thin film transistor including an oxide semiconductor layer which is dehydrated or dehydrogenated in the above conditions, at least the peak of water at around 300 °C is not detected.

15 [0029]

It is important not to allow the oxide semiconductor layer to contact with water or hydrogen, which is achieved by performing the cooling in a furnace used for dehydration or dehydrogenation without exposure of the oxide semiconductor layer to the air. When a thin film transistor is manufactured using an oxide semiconductor
20 layer which is made to be an i-type oxide semiconductor layer in such a manner that an oxide semiconductor layer is placed in an oxygen-deficient state and changed into a low-resistance oxide semiconductor layer, i.e., an n-type (e.g., n^--type or n^+-type) oxide semiconductor layer by dehydration or dehydrogenation and then oxygen is supplied to the low-resistance oxide semiconductor layer so as to change the layer into a
25 high-resistance oxide semiconductor layer, the threshold voltage of the thin film transistor can be a positive voltage, whereby a so-called normally-off switching element can be realized. It is desirable for a display device that a channel be formed with a threshold voltage that is a positive value and as close to 0 V as possible. Note that if the threshold voltage of the thin film transistor is negative, the thin film transistor tends
30 to be normally-on; in other words, current flows between a source electrode and a drain electrode even when gate voltage is 0 V. In an active-matrix display device, electric

characteristics of thin film transistors included in a circuit are important and performance of the display device is dependent on the electric characteristics of the thin film transistors. Among the electric characteristics of thin film transistors, in particular, a threshold voltage (V_{th}) is important. When the threshold voltage value is high or
5 negative even when the field effect mobility is high, it is difficult to control the circuit. When a thin film transistor has a high threshold voltage value, the thin film transistor cannot perform switching function and may be a load when the transistor is driven at low voltage. In the case of an n-channel thin film transistor, it is preferable that a channel is formed and drain current begins to flow after the positive voltage is applied
10 as a gate voltage. A transistor in which a channel is not formed unless the driving voltage is high enough and a transistor in which a channel is formed and drain current flows even in the case of the negative voltage state are unsuitable for a thin film transistor used in a circuit.

[0030]

15 In addition, cooling after the heat treatment may be carried out after switching the gas atmosphere in which the dehydration or dehydrogenation is performed to a different gas. For example, cooling may be performed after the furnace used for dehydration or dehydrogenation is filled with a high-purity oxygen gas, a high-purity N_2O gas, or an ultra-dry air (with a dew point of lower than or equal to −40 °C,
20 preferably lower than or equal to −60 °C) without exposure of the oxide semiconductor layer to the air.

[0031]

The electric characteristics of a thin film transistor are improved using an oxide semiconductor film cooled slowly (or cooled) in a dry atmosphere (with a dew point
25 lower than or equal to −40 °C, preferably lower than or equal to −60 °C) which does not substantially contain moisture after moisture which is contained in the film is reduced by heat treatment for dehydration or dehydrogenation, and high-performance thin film transistors which can be mass-produced are realized.

[0032]

30 As mentioned above, in this specification, heat treatment for an oxide semiconductor layer in an atmosphere of an inert gas such as nitrogen or a rare gas (e.g.,

argon or helium) is referred to as dehydration or dehydrogenation. In this specification, "dehydrogenation" does not indicate elimination of only H_2 by heat treatment. For convenience, elimination of H, OH, and the like is referred to as "dehydration or dehydrogenation".

5 [0033]

FIG. 15 is a longitudinal sectional view illustrating an inverted-staggered thin film transistor which uses an oxide semiconductor. An oxide semiconductor (OS) layer is provided over a gate electrode (GE1) with a gate insulating film (GI) therebetween and a source electrode (S) and a drain electrode (D) are provided
10 thereover.

[0034]

FIGS. 16A and 16B are energy band diagrams (schematic views) each corresponding to a cross section taken along line A-A′ in FIG. 15. A case where the voltage of the source and that of the drain are equal (V_D = 0V) and a case where a
15 positive potential ($V_D > 0$) based on a voltage of the source is applied to the drain are illustrated in FIG. 16A and FIG. 16B, respectively.

[0035]

FIGS. 17A and 17B are energy band diagrams (schematic views) each corresponding to a cross section taken along line B-B′ in FIG. 15. A state where a
20 positive potential ($+V_G$) is applied to the gate (G1), i.e., an on-state in which carriers (electrons) flow between the source and the drain is illustrated in FIG. 17A. A state where a negative potential ($-V_G$) is applied to the gate (G1), i.e., an off-state (in which minority carriers do not flow) is illustrated in FIG. 17B.

[0036]

25 FIG. 18 is a diagram illustrating a relation between a vacuum level and a work function of metal (ϕ_M) and a relation between the vacuum level and electron affinity (χ) of an oxide semiconductor.

[0037]

A conventional oxide semiconductor generally has n-type conductivity and in
30 that case, a Fermi level (E_F) is apart from an intrinsic Fermi level (E_i) at the center of a band gap and is closer to a conduction band. It is known that some hydrogen in an

oxide semiconductor serves as donors and is one of the factors which make the oxide semiconductor have n-type conductivity.

[0038]

On the other hand, an oxide semiconductor according to the present invention
5 is made to be an intrinsic (i-type) or substantially intrinsic oxide semiconductor by removal of hydrogen that is an n-type impurity to be highly purified so that impurities that are not main components of the oxide semiconductor are contained as little as possible. In other words, the oxide semiconductor according to the present invention is not an oxide semiconductor which is made to be an i-type oxide semiconductor by
10 being doped with an impurity but an i-type (intrinsic) or almost an i-type oxide semiconductor which is highly purified by removing impurities such as hydrogen and water as much as possible. In this manner, the Fermi level (E_F) can be extremely close to the intrinsic Fermi level (E_i).

[0039]

15 It is said that electron affinity (χ) of an oxide semiconductor is 4.3 eV when a band gap (E_g) thereof is 3.15 eV. The work function of titanium (Ti) contained in the source and drain electrodes is almost equivalent to the electron affinity (χ) of the oxide semiconductor. In that case, at an interface between the metal and the oxide semiconductor, a Schottky barrier against an electron is not formed.

20 [0040]

That is, in the case where the work function (ϕ_M) of the metal is equivalent to the electron affinity (χ) of the oxide semiconductor, an energy band diagram (a schematic view) similar to that in FIG. 16A is obtained when the metal and the oxide semiconductor are in contact with each other.

25 [0041]

In FIG. 16B, an electron is represented by a black circle (•). When a positive potential is applied to the drain, an electron goes over a barrier to be injected to the oxide semiconductor and flows to the drain. In this case, height (h) of the barrier is varied depending on a gate voltage and a drain voltage and is smaller than height of a
30 barrier in FIG. 16A in which no voltage is applied, i.e., a half value of a band gap (E_g).

[0042]

At this time, an electron moves in a lowest portion in an interface between the gate insulating film and the highly purified semiconductor on the oxide semiconductor side, which is stable in terms of energy.

[0043]

5 Further, in FIG. 17B, when a negative potential (a reverse bias voltage) is applied to the gate electrode (G1), a value of current is almost zero because substantially, there is not any holes, i.e., minority carriers.

[0044]

As described above, the oxide semiconductor is made to be an intrinsic (i-type) 10 or substantially intrinsic oxide semiconductor by being highly purified in such a manner that impurities that are not main components of the oxide semiconductor are contained as little as possible, whereby characteristics at an interface between the oxide semiconductor and the gate insulating film become so distinctive and thus are needed to be considered separately from those in a bulk of the oxide semiconductor. Thus, the 15 gate insulating film is needed to form a favorable interface with the oxide semiconductor. For example, it is preferable to use an insulating film which is formed by a CVD method which uses high density plasma generated with a power frequency from the VHF band to a microwave band or an insulating film formed by a sputtering method.

20 [0045]

By highly purifying an oxide semiconductor and forming a favorable interface between the oxide semiconductor and the gate insulating film, even in the case of an element with a channel width W of 1×10^4 μm and a channel length L of 3 μm, thin film transistor characteristics such as off-current of less than or equal to 10^{-13} A and a 25 subthreshold swing value (S value) of 0.1 V/dec. can be expected (the thickness of the gate insulating film = 100nm).

[0046]

In this manner, by highly purifying an oxide semiconductor so that impurities that are not main components of the oxide semiconductor are contained as little as 30 possible, favorable operation of a thin film transistor can be realized.

[0047]

In a display device, a voltage of the counter electrode is optimized to correspond to an amplitude center of an electric potential of a pixel electrode and high display quality is realized; in addition, an adverse effect of electrostatic on a driver circuit which includes a thin film transistor using an oxide semiconductor layer is
5 reduced so that reliability is improved.

BRIEF DESCRIPTION OF DRAWINGS

[0048]

In the accompanying drawings:

FIGS. 1A to 1C are a top view and cross-sectional views illustrating one
10 embodiment of the present invention;

FIGS. 2A and 2B are a cross-sectional view and a top view illustrating one embodiment of the present invention;

FIGS. 3A and 3B are a cross-sectional view and a top view illustrating one embodiment of the present invention;

15 FIGS. 4A to 4E are cross-sectional views illustrating a manufacturing method of a semiconductor device;

FIGS. 5A to 5E are cross-sectional views illustrating a manufacturing method of a semiconductor device;

FIGS. 6A to 6E are cross-sectional views illustrating a manufacturing method
20 of a semiconductor device;

FIG. 7 is a cross-sectional view illustrating one embodiment of the present invention;

FIGS. 8A to 8E are cross-sectional views illustrating a manufacturing method of a semiconductor device;

25 FIGS. 9A to 9D are diagrams illustrating a multi-tone mask;

FIG. 10 is a cross-sectional view illustrating one embodiment of the present invention;

FIG. 11 is a top view illustrating one embodiment of the present invention;

FIG. 12 is a top view illustrating one embodiment of the present invention;

30 FIG. 13 is an equivalent circuit diagram of a pixel of a semiconductor device;

FIGS. 14A to 14E are views each illustrating an example of an electronic device;

FIG. 15 is a longitudinal sectional view illustrating an inverted-staggered thin film transistor which uses an oxide semiconductor;

FIGS. 16A and 16B are energy band diagrams (schematic views) each corresponding to a cross section taken along line A-A′ in FIG. 15;

5 FIG. 17A is a diagram illustrating a state where a positive electric potential ($+V_G$) is applied to the gate (G1) and FIG. 17B is a diagram illustrating a state where a negative electric potential ($-V_G$) is applied to the gate (G1); and

FIG. 18 is a diagram illustrating a relation between a vacuum level and a work function of metal (ϕ_M) and a relation between the vacuum level and electron affinity (χ)
10 of an oxide semiconductor.

BEST MODE FOR CARRYING OUT THE INVENTION

[0049]

Hereinafter, embodiments of the present invention will be described in detail
15 with reference to the accompanying drawings. However, the present invention is not limited to the description below, and it is easily understood by those skilled in the art that modes and details disclosed herein can be modified in various ways without departing from the spirit and the scope of the present invention. Therefore, the present invention is not construed as being limited to description of the embodiments.

20 [0050]

[Embodiment 1]

A semiconductor device of this embodiment is described with reference to FIGS. 1A to 1C. The semiconductor device of this embodiment is a liquid crystal display device.

25 [0051]

FIG. 1A is a top view of a semiconductor device of this embodiment. FIG. 1A is a top view of a liquid crystal display device in which an FPC has not been attached to a first substrate 1210. FIG. 1B is a cross-sectional view taken along line G-H in FIG. 1A, which shows a connection region of a conductive particle and a connection wiring.
30 FIG. 1C is a cross-sectional view taken along line E-F in FIG. 1A, which shows a connection region of a pixel portion and a connection wiring.

[0052]

The first substrate 1210 which serves as an active matrix substrate and is provided with pixel electrode layers, and a second substrate 1204 provided with a first counter electrode layer 1291 and a second counter electrode layer 1292 are attached to each other with a sealing material 1205, and the interior space surrounded by the sealing material 1205 is filled with a liquid crystal 1280. A signal line driver circuit portion 1200, a scan line driver circuit portion 1201, and a pixel portion 1202 in which pixel electrode layers are formed in matrix are formed over the first substrate 1210.

[0053]

The second counter electrode layer 1292 provided over the driver circuit portion has a potential which is different from that of the first counter electrode layer 1291. The first counter electrode layer 1291 provided over the pixel portion 1202 and the second counter electrode layer 1292 provided over the driver circuit portion are separated electrode layers not being electrically connected to each other and have different potentials.

[0054]

A potential (voltage) applied to the pixel electrode layer is provided through a pixel thin film transistor. Therefore, there is a possibility that the voltage of the pixel electrode layer is smaller than the voltage which is actually applied to the pixel electrode layer through the pixel thin film transistor by several volts. Thus, it is preferable that a potential (voltage) to be applied to the first counter electrode layer 1291 be set in consideration of the difference.

[0055]

The signal line driver circuit portion 1200 provided over the first substrate 1210 includes a circuit comprising a driver circuit thin film transistor 1223.

[0056]

The pixel portion 1202 includes a pixel thin film transistor 1211. Further, a pixel electrode layer 1250 which is connected to the pixel thin film transistor 1211 is formed over and in an insulating layer 1214.

[0057]

The pixel thin film transistor 1211 and the driver circuit thin film transistor 1223 are formed using an oxide semiconductor layer, a gate insulating layer, and a gate

electrode layer. Over the driver circuit thin film transistor 1223, a conductive layer 1293 is provided overlapping with the gate electrode layer and the oxide semiconductor layer with an insulating layer 1214 interposed between the conductive layer 1293, and the gate electrode layer and the oxide semiconductor layer.

5 [0058]

In the driver circuit thin film transistor 1223, the oxide semiconductor layer is interposed between the gate electrode layer and the conductive layer 1293. With such a structure, variation in threshold voltage of the driver circuit thin film transistor 1223 can be reduced, so that a semiconductor device provided with the driver circuit thin film 10 transistor 1223, which has stable electric characteristics, can be provided. The conductive layer 1293 may be at the same potential as the gate electrode layer or may be at a floating potential or a fixed potential such as a GND potential or 0 V. By setting the potential of the conductive layer 1293 to an appropriate value, the threshold voltage of the driver circuit thin film transistor 1223 can be controlled though depending on a 15 distance between the pair of substrates.

[0059]

The conductive layer 1293 may be processed into a pattern having an opening so as to be provided in a region overlapping with the gate electrode layer and the semiconductor layer.

20 [0060]

The second counter electrode layer 1292 provided over the driver circuit portion has a flat shape and may be processed into a pattern having an opening. By processing the second counter electrode layer 1292 into the pattern having the opening, parasitic capacitance to be formed between the second counter electrode layer 1292 and 25 the conductive layer included in the thin film transistor in the driver circuit portion can be reduced. Thus, reduction in power consumption of the semiconductor device can be realized.

[0061]

In this specification, a pattern having an opening (a slit) of the second counter 30 electrode layer 1292 over the driver circuit portion includes patterns which are partly opened, such as a bend portion and a branching comb-like portion as well as a pattern which is opened in a closed space.

[0062]

As each of the first substrate 1210 and the second substrate 1204, any glass substrate used in the electronics industry, called a non-alkali glass substrate, such as an aluminosilicate glass substrate, an aluminoborosilicate glass substrate, or a barium
5 borosilicate glass substrate, a quartz substrate, a ceramic substrate, a plastic substrate, or the like can be used as appropriate. By using a flexible plastic substrate as each of the first substrate 1210 and the second substrate 1204, a flexible semiconductor device can be manufactured.

[0063]

10 The sealing material 1205 is applied over the first substrate 1210 or the second substrate 1204 by a screen printing method, or with an inkjet apparatus or a dispensing apparatus. As the sealing material 1205, typically, a material containing a visible light curable resin, an ultraviolet curable resin, or a thermosetting resin can be used. For example, an epoxy resin such as a liquid bisphenol-A resin, a solid bisphenol-A resin, a
15 bromine-containing epoxy resin, a bisphenol-F resin, a bisphenol-AD resin, a phenol-type epoxy resin, a cresol-type epoxy resin, a novolac-type epoxy resin, a cycloaliphatic epoxy resin, an Epi-Bis type epoxy resin, a glycidyl ester resin, a glycidyl amine resin, a heterocyclic epoxy resin, or a modified epoxy resin can be used. As the sealing material 1205, a material having a viscosity in the range of 40 Pa·s to 400 Pa·s is
20 cured and then used. Further, a filler (1 μm to 24 μm in diameter) may be contained. Note that it is preferable to select, as the sealing material, a sealing material which is insoluble in liquid crystals which are in contact with the sealing material later.

[0064]

As a conductive particle 1270, a conductive particle in which an insulating
25 sphere is covered with a thin metal film can be used. The insulating sphere is formed using silica glass, hard resin, or the like. The thin metal film can be formed to have a single-layer structure or a stacked-layer structure of gold, silver, palladium, nickel, an indium tin oxide (ITO), and/or an indium zinc oxide (IZO). For example, as the thin metal film, a thin gold film, a stack of a thin nickel film and a thin gold film, or the like
30 can be used. By using the conductive particle 1270 in which an insulating sphere is contained at the center, elasticity can be improved so that possibilities of breakdowns

due to external pressure can be suppressed.

[0065]

The materials of the pixel electrode layer 1250 are different between a transmissive liquid crystal display device and a reflective liquid crystal display device.
5 In the case of a transmissive liquid crystal display device, the pixel electrode layer 1250 is formed using a light-transmitting material. As examples of the light-transmitting material, an indium tin oxide (ITO), a zinc oxide (ZnO), an indium zinc oxide (IZO), a gallium-doped zinc oxide (GZO), and the like can be given.

[0066]

10 Further, the pixel electrode layer 1250 can be formed using a conductive composition containing a conductive high-molecular weight material (also referred to as a conductive polymer), as well. The pixel electrode layer formed using the conductive composition has preferably a sheet resistance of less than or equal to 10000 Ω/square and a transmittance greater than or equal to 70 % at a wavelength of 550 nm. Further,
15 the resistivity of the conductive high-molecular weight material contained in the conductive composition is preferably less than or equal to 0.1 Ω·cm.

[0067]

As the high-molecular weight material, a so-called π-electron conjugated conductive polymer can be used. For example, polyaniline or a derivative thereof,
20 polypyrrole or a derivative thereof, polythiophene or a derivative thereof, a copolymer of two or more kinds of them, and the like can be given.

[0068]

On the other hand, in the case of a reflective liquid crystal display device, a metal electrode having high reflectivity is used as the pixel electrode layer 1250.
25 Specifically, aluminum, silver, or the like is used. Further, the reflectivity is increased by making the surface of the pixel electrode layer 1250 rough. Therefore, the insulating layer 1214 under the pixel electrode layer 1250 may be made rough.

[0069]

Further, in the case of a semi-transmissive liquid crystal display device, a
30 transmissive material and a reflective material are used for the pixel electrode layer 1250.

[0070]

Further, a terminal portion 1240 is formed in an edge portion of the first substrate 1210. In the terminal portion 1240, a connection terminal 1241 is formed over the connection wiring 1208.

[0071]

FIG. 1B is a cross-sectional view of a region where the connection terminal 1241 and the conductive particle 1270 are connected to each other. A connection wiring 1208 is formed over the first substrate 1210. A connection terminal 1241 formed at the same time as the pixel electrode layer 1250 is formed over the connection wiring 1208. The connection terminal 1241 is electrically connected to the first counter electrode layer 1291 through the connection wiring 1208 and the conductive particle 1270. Further, the connection terminal 1241 is connected to an FPC (not shown). Note that in FIG. 1B, the conductive particle 1270 is fixed by the resin layer 1235. The resin layer 1235 can be formed using an organic resin insulating material like that used for the sealing material 1205.

[0072]

FIG. 1C is a cross-sectional view of a region where the pixel electrode layer 1250 and a connection terminal 1243 are connected. A connection wiring 1242 formed at the same time as source electrode layers and drain electrode layers of the pixel thin film transistor 1211 and the driver circuit thin film transistor 1223 are formed over the first substrate 1210. A connection terminal 1243 formed at the same time as the pixel electrode layer 1250 is formed over the connection wiring 1242. The connection terminal 1243 is electrically connected to the pixel electrode layer 1250 through the connection wiring 1242. Note that, since an active matrix liquid crystal display device is used in this embodiment, the pixel electrode layer 1250 and the connection wiring 1242 are not directly connected but are connected through the pixel thin film transistor 1211 or a thin film transistor in the signal line driver circuit portion 1200.

[0073]

A first alignment film 1206 is provided over the pixel electrode layer 1250, and rubbing is performed thereon. The first alignment film 1206 and the rubbing are not necessarily required, which depends on the mode of liquid crystals.

[0074]

For the second substrate 1204 which serves as a counter substrate, a black matrix may be provided in a position overlapping with the signal line driver circuit portion 1200, and a color filter, a protective layer, and the like may be provided in a position overlapping with the pixel portion 1202. In a case where color display is performed by a color sequential method called "field sequential", the color filter is not necessarily provided. The second substrate 1204 which serves as a counter substrate is provided with the first counter electrode layer 1291 and the second counter electrode layer 1292, and a second alignment film 1207 is provided for the first counter electrode layer 1291, and rubbing is performed thereon. Similarly to the case of the first substrate 1210, as for the second substrate 1204, an alignment film and rubbing are not necessarily required, which depends on the mode of liquid crystals.

[0075]

Alternatively, liquid crystals exhibiting a blue phase for which an alignment film is unnecessary may be used. A blue phase is one of liquid crystal phases, which is generated just before a cholesteric phase changes into an isotropic phase while the temperature of cholesteric liquid crystal is increased. Since the blue phase appears within a narrow range of temperatures, a liquid crystal composition containing a chiral agent at greater than or equal to 5 wt% is used for the liquid crystal 1280 in order to increase the temperature range. The liquid crystal composition which includes a liquid crystal showing a blue phase and a chiral agent has a short response time less than or equal to 1 msec, has optical isotropy, which makes the alignment step unneeded, and has a small viewing angle dependence.

[0076]

The second substrate 1204 provided with the first counter electrode layer 1291 and the second counter electrode layer 1292 or the first substrate 1210 provided with the pixel electrode layer 1250 is further provided with a pillar spacer 1255. The pillar spacer 1255 is provided to keep a distance between the first substrate 1210 and the second substrate 1204. In this embodiment, an example is described in which the pillar spacer 1255 is provided on the second substrate 1204 side. The pillar spacer 1255 is also called a photolitho spacer, a post spacer, a scallop spacer, or a column

spacer. Alternatively, a spherical spacer may be used. In this embodiment, a pillar spacer is used. As for a method for forming the pillar spacer 1255, an organic insulating material such as photosensitive acrylic is applied to an entire surface of the substrate by a spin coating method, and a series of photolithography steps is performed
5 thereon. Photosensitive acrylic which remains over the substrate serves as the spacer. With this method, a place for disposing a spacer can be exposed to light in accordance with a mask pattern at the time of light exposure; therefore, the pillar spacer 1255 at a portion where the liquid crystal is not driven makes it possible to prevent light of the liquid crystal from leaking as well as to maintain the distance between the upper and
10 lower substrates. Further, the pillar spacer 1255 can be formed by discharging a composition containing an organic insulating material by an inkjet method and performing baking thereon.

[0077]

The space around the conductive particle 1270 may be filled with a conductive
15 polymer as the resin layer 1235 instead of an organic resin insulating material. As typical examples of the conductive polymer, a conductive polyaniline, a conductive polypyrrole, a conductive polythiophene, a mixture of poly(ethylenedioxythiophene) (PEDOT) and poly(styrenesulfonic acid) (PSS), and the like can be given. Further, any of the aforementioned examples of the conductive polymer which can be used for
20 the pixel electrode layer 1250 can be used as appropriate, as well. The conductive polymer is formed by applying the conductive polymer with an inkjet apparatus, a dispensing apparatus, or the like. That is, when the conductive polymer is in contact with the second counter electrode layer 1292 or the connection wiring 1208, the conductive particle 1270 and the conductive polymer are in contact with each other, so
25 that connection resistance between the second counter electrode layer 1292 and the connection wiring 1208 can be reduced.

[0078]

Note that the connection wiring 1208 and the first counter electrode layer 1291 formed for the second substrate 1204 are electrically connected to each other through
30 the conductive particle 1270. Further, the connection wiring 1246 and the second counter electrode layer 1292 formed for the second substrate 1204 are electrically connected to each other through the conductive particle 1270. The connection wiring

1246 and the connection wiring 1208 have different potentials.

[0079]

Further, nanoparticles in each of which a conductive material is covered with a thin organic film may be used as the conductive particle 1270. When such nanoparticles are used, the thin organic films are decomposed in a heating step for realigning the orientation of liquid crystals and hardening the sealing material after the first substrate 1210 and the second substrate 1204 are attached to each other, so that the conductive materials of the nanoparticles are in contact and fused with one another, whereby a conductive particle can be formed.

[0080]

The nanoparticles are dispersed by a droplet discharging method. A droplet discharging method is a method for forming a pattern by discharging droplets containing a predetermined substance through a fine opening. In this embodiment, a composition in which nanoparticles in each of which a conductive material is covered with a thin organic film are dispersed in a solvent, is discharged (jetted) as a droplet, and dried so that the solvent is evaporated.

[0081]

A conductive material for forming nanoparticles may be a metal element selected from gold (Au), silver (Ag), platinum (Pt), nickel (Ni), copper (Cu), palladium (Pd), tantalum (Ta), iridium (Ir), rhodium (Rh), tungsten (W), aluminum (Al), and the like or an alloy material containing such an element as a main component. Further, a metal sulfide of cadmium (Cd) or zinc (Zn), an oxide of iron (Fe), titanium (Ti), germanium (Ge), silicon (Si), zirconium (Zr), barium (Ba), or the like, or one or more silver halides may be mixed. Note that in the case where two or more kinds of elements or compounds are used as conductive materials, the mixture form is not limited in particular, for example, they may be homogeneously mixed, or any one of them may be localized in the center. Further, at least the surfaces of the nanoparticles are formed of a conductive material, and the inside thereof may be formed of an insulating material.

[0082]

The grain diameter of a nanoparticle is greater than or equal to 1 nm and less than or equal to 200 nm, preferably greater than or equal to 1 nm and less than or equal

to 100 nm, and grain diameters of the nanoparticles included in the discharged material are preferably uniform.

[0083]

Note that when voltage is applied, voids may be generated between particles depending on the kind of the conductive material(s) forming the nanoparticles. This is because crystal growth of the conductive material proceeds very fast, and such void generation can be suppressed by setting a voltage to be applied to a liquid crystal display device to be low or using an alloy material for each nanoparticle. Consequently, a highly reliable liquid crystal display device can be provided.

[0084]

The thin organic films coating the nanoparticles correspond to a dispersant having functions of preventing nanoparticles from flocculating in a solvent and stably dispersing the particles. Accordingly, the compound forming the thin organic films is formed using a surfactant, a material which can form a coordinate bond with a metal element contained in the conductive material, or the like. Here, as the substance forming a coordinate bond with a metal element, a substance having a lone electron-pair on an atom of nitrogen, sulfur, oxygen, or the like such as an amino group, a thiol group (–SH), a sulfide group (–S–), a hydroxy group (–OH), an ether group (–O–), a carboxyl group (–COOH), a cyano group (–CN), or the like can be given. For example, a hydroxylamine such as ethanolamine, an amine-based compound such as polyethyleneimine, an amide compound such as polyvinylpyrrolidone, an alcohol such as poly(vinyl alcohol), an alkanethiol, a dithiol, a glycol such as ethylene glycol, or diethylene glycol, an ether compound such as polyethylene glycol, poly(acrylic acid), carboxymethylcellulose, or the like can be used. Further, as the surfactant, for example, an anionic surfactant such as sodium bis(2-ethylhexyl)sulfosuccinate or sodium dodecylbenzenesulfonate, a nonionic surfactant such as an alkyl ester of poly(alkyl glycol), alkyl phenyl ether, a fluorosurfactant, a copolymer of ethyleneimine with a poly(ethylene oxide), or the like can be used. Note that when a dispersant is greater than or equal to 30 wt% with respect to nanoparticles, the viscosity of the discharge material becomes high, so that 1.0 wt% to 30 wt% is preferable.

[0085]

Such nanoparticles in each of which a conductive material is covered with a thin organic film are dispersed in a solvent and discharged. For the solvent, water or an organic solvent can be used, and an organic solvent may be either a water-soluble organic solvent or a water-insoluble organic solvent. For example, as the water-soluble organic solvent, an alcohol such as methanol, ethanol, propanol, butyl alcohol, glycerin, dipropylene glycol, or ethylene glycol, a ketone such as acetone or methyl ethyl ketone, a glycol ether such as ethylene glycol monomethyl ether, ethylene glycol monoethyl ether, ethylene glycol monobutyl ether, or diethylene glycol monobutyl ether, a water-soluble nitrogen-containing organic compound such as 2-pyrrolidone or *N*-methyl pyrrolidone, or the like can be given. Further, as the water-insoluble organic solvent, an ester such as ethyl acetate, a linear alkane such as octane, nonane, or decane, a cycloalkane such as cyclohexane, an aromatic compound such as toluene, xylene, benzene, or dichlorobenzene, or the like can be given. Naturally, not only one solvent is necessarily used but a mixture of a plurality of solvents may be used as long as phase separation does not occur between the solvents.

[0086]

The sealing material 1205 and the conductive particle 1270 are discharged over the first substrate 1210 or the second substrate 1204, and then liquid crystals are discharged in a space surrounded by the sealing material 1205. After that, the first substrate 1210 and the second substrate 1204 are attached to each other under reduced pressure, UV light irradiation is performed thereon to cure the sealing material 1205, and then heat treatment is performed thereon to further cure the sealing material 1205, so that the first substrate 1210 and the second substrate 1204 are firmly fixed. In addition, the alignment of the liquid crystals is made uniform by the heat treatment.

[0087]

Consequently, the first substrate 1210 and the second substrate 1204 can be attached to each other.

[0088]

Then, the first substrate 1210 and the second substrate 1204 are cut to have a panel shape. Furthermore, in order to improve the contrast, a first polarizing plate 1290 and a second polarizing plate 1295 are provided for the outsides of the first substrate 1210 and the second substrate 1204 respectively. Note that the first

polarizing plate 1290 is not necessarily provided in the case of a reflective display device.

[0089]

Although not illustrated in this embodiment, a black matrix (a light-blocking layer), an optical member (an optical substrate) such as a retardation member, or an anti-reflection member, and the like are provided as appropriate. For example, circular polarization obtained by using a polarizing substrate and a retardation substrate may be used. In addition, a backlight, a side light, or the like may be used as a light source.

[0090]

In an active matrix liquid crystal display device, pixel electrodes arranged in matrix are driven to form a display pattern on a screen. Specifically, voltage is applied between a selected pixel electrode and a counter electrode corresponding to the pixel electrode, so that a liquid crystal layer provided between the pixel electrode and the counter electrode is optically modulated and this optical modulation is recognized as a display pattern by an observer.

[0091]

In displaying moving images, a liquid crystal display device has a problem in that a long response time of liquid crystal molecules themselves causes afterimages or blurring of moving images. In order to improve the moving-image characteristics of a liquid crystal display device, a driving method called black insertion is employed in which black is displayed on the whole screen every other frame period.

[0092]

Further, there is a driving technique which is so-called double-frame rate driving. In the double-frame rate driving, a vertical synchronizing frequency is set 1.5 times or more, preferably, 2 times or more as high as a usual vertical synchronizing frequency, whereby the response speed is increased, and the grayscale to be written is selected for every plural fields which have been divided in each frame.

[0093]

Further alternatively, in order to improve the moving-image characteristics of a liquid crystal display device, a driving method may be employed, in which a plurality of LEDs (light-emitting diodes) or a plurality of EL light sources are used to form a surface light source as a backlight, and each light source of the surface light source is

independently driven in a pulsed manner in one frame period. As the surface light source, three or more kinds of LEDs may be used and an LED emitting white light may be used. Since a plurality of LEDs can be controlled independently, the light emission timing of LEDs can be synchronized with the timing at which a liquid crystal layer is optically modulated. According to this driving method, LEDs can be partly turned off; therefore, an effect of reducing power consumption can be obtained particularly in the case of displaying an image having a large part on which black is displayed.

[0094]

By combining these driving methods, the display characteristics of a liquid crystal display device, such as moving-image characteristics, can be improved as compared with those of conventional liquid crystal display devices.

[0095]

In an embodiment of the present invention, a counter electrode layer is provided over a driver circuit portion, whereby the electrostatic breakdown of a thin film transistor can be prevented. However, a protective circuit may be provided as well. The protective circuit is preferably formed with a non-linear element including an oxide semiconductor layer. For example, protective circuits are provided between the pixel portion and a scan line input terminal and between the pixel portion and a signal line input terminal. In this embodiment, a plurality of protective circuits are provided so as to prevent breakage of a pixel transistor and the like which can be caused when a surge voltage due to static electricity or the like is applied to a scan line, a signal line, and a capacitor bus line. Therefore, the protective circuit is formed so as to release charge to a common wiring when a surge voltage is applied to the protective circuit. Further, the protective circuit includes non-linear elements arranged in parallel to each other with the scan line therebetween. The non-linear element includes a two-terminal element such as a diode or a three-terminal element such as a transistor. For example, the non-linear element can also be formed in the same step as the thin film transistor in the pixel portion, and can be made to have the same properties as a diode by connecting a gate terminal to a drain terminal of the non-linear element.

[0096]

In the above-described manner, a liquid crystal display device which includes a thin film transistor using an oxide semiconductor layer and in which resistance to static

electricity is high and low power consumption is achieved, can be provided.

[0097]

[Embodiment 2]

Another example is described in which, over the first substrate, a common connection portion is formed in the connection region for electrical connection of the counter electrode layers (the first counter electrode layer and the second counter electrode layer) which are provided for the second substrate to the connection wiring, in the semiconductor device including the liquid crystal layer between the first substrate and the second substrate as described in Embodiment 1. Note that a thin film transistor is formed as a switching element over the first substrate, and the common connection portion is manufactured in the same process as the switching element in a pixel portion, thereby avoiding complicating the process.

[0098]

In this embodiment, an example is described in which the common connection portion is provided in a position overlapping with a sealing material for bonding the first substrate and the second substrate and is electrically connected to the counter electrode layer through a conductive particle in the sealing material. Alternatively, as illustrated in FIG. 1A, the common connection portion is provided in a position that is outside of the pixel portion and does not overlap with the sealing material and a paste containing conductive particles is provided separately from the sealing material so as to overlap with the common connection portion, whereby the common connection portion is electrically connected to the counter electrode layer.

[0099]

FIG. 2A is a cross-sectional structural view of a semiconductor device in which a thin film transistor and a common connection portion are formed over one substrate (a first substrate 300).

[0100]

In FIG. 2A, a thin film transistor 320 which is electrically connected to a pixel electrode layer 327 is a channel-etched thin film transistor provided in a pixel portion.

[0101]

FIG. 2B illustrates an example of a top view of the common connection portion, and dashed line A1-A2 in FIG. 2B corresponds to a cross section of the common

connection portion in FIG. 2A. Note that in FIG. 2B, the same portions as in FIG. 2A are denoted by the same reference numerals.

[0102]

A common potential line 310 is provided over the gate insulating layer 302, and formed by using the same material and the same step as a source electrode layer and a drain electrode layer of the thin film transistor 320.

[0103]

The common potential line 310 is covered with the protective insulating layer 303. The protective insulating layer 303 has a plurality of opening portions in positions overlapping with the common potential line 310. These opening portions are formed in the same step as a contact hole that connects the drain electrode layer of the thin film transistor 320 and the pixel electrode layer 327.

[0104]

Note that the contact hole in the pixel portion and the opening portions in the common connection portion are distinctively described because their sizes differ considerably. Further, in FIG. 2A, the pixel portion and the common connection portion are not illustrated on the same scale. For example, the length of the dashed line A1-A2 in the common connection portion is about 500 μm while the width of the thin film transistor is less than 50 μm; thus, the common connection portion actually has greater than or equal to ten times as large area as the thin film transistor. However, for simplicity, the pixel portion and the common connection portion are shown on different scales in FIG. 2A.

[0105]

A common electrode layer 306 is provided over the protective insulating layer 303 and formed using the same material and the same step as the pixel electrode layer 327 in the pixel portion.

[0106]

In this manner, the common connection portion is manufactured in the same process as the switching element in the pixel portion.

[0107]

The first substrate provided with the pixel portion and the common connection

portion and the second substrate having the counter electrode layer are fixed with the sealing material.

[0108]

In the case where the sealing material contains conductive particles, the first
5 and second substrates are aligned so that the sealing material overlaps with the common connection portion. For example, in the case of a small liquid crystal panel, two common connection portions overlap with the sealing material at opposite corners of the pixel portion. In the case of a large liquid crystal panel, four or more common connection portions overlap with the sealing material.

10 [0109]

Note that the common electrode layer 306 is an electrode in contact with the conductive particles contained in the sealing material, and is electrically connected to the counter electrode layer of the second substrate.

[0110]

15 In the case of using a liquid crystal injection method, the first and second substrates are fixed with a sealing material, and then a liquid crystal is injected between the first substrate and the second substrate. In the case of using a liquid crystal dropping method, a sealing material is drawn on the second substrate or the first substrate and a liquid crystal is dropped thereon; then, the first and second substrates are
20 bonded to each other under a reduced pressure.

[0111]

This embodiment shows an example of the common connection portion electrically connected to the counter electrode layer. However, the present invention is not particularly limited to the connection of the counter electrode layer with the
25 common connection portion and can be applied to a connection portion for the connection of the counter electrode layer to another wiring or to an external connection terminal or the like.

[0112]

This embodiment can be freely combined with Embodiment 1.

30 [0113]

[Embodiment 3]

In Embodiment 2, an example is described in which a common connection

portion is manufactured using a wiring which is formed using the same material and the same step as source and drain electrode layers as a common potential line. In this embodiment, an example of a common connection portion different from that of FIGS. 2A and 2B is described.

5 [0114]

In this embodiment, an example of manufacturing a common connection portion, in which an electrode formed using the same material and the same step as a gate wiring is formed and a wiring formed using the same material and the same step as a drain electrode layer is provided as a common potential line over the electrode, will be

10 illustrated in FIGS. 3A and 3B.

[0115]

FIG. 3B illustrates an example of a top view of the common connection portion, and dashed line F1-F2 in FIG. 3B corresponds to a cross section of the common connection portion in FIG. 3A.

15 [0116]

Note that as illustrated in FIG. 3A, a thin film transistor in a pixel portion has the same structure as that of Embodiment 2; thus, portions similar to those in FIG. 2A are denoted by the same reference numerals and detailed description is omitted here.

[0117]

20 A common electrode 311 is provided over the first substrate 300 and formed using the same material and the same step as a gate electrode of the thin film transistor 320.

[0118]

In addition, the common electrode 311 is covered with the gate insulating layer

25 302 and the protective insulating layer 303. The gate insulating layer 302 and the protective insulating layer 303 have an opening portion in a position overlapping with the common electrode 311. This opening portion, unlike in Embodiment 2, has a large depth which corresponds to the thickness of the two insulating layers. Note that this opening portion is manufactured by etching in the same step as a contact hole for

30 connecting the drain electrode layer 304 and the pixel electrode layer 327, and then further etching the gate insulating layer selectively.

[0119]

A common potential line 305 is provided over the gate insulating layer 302 and formed using the same material and the same step as the drain electrode layer 304.

[0120]

The common potential line 305 is covered with the protective insulating layer 303, and the protective insulating layer 303 has a plurality of opening portions in positions overlapping with the common potential line 305. These opening portions are formed in the same step as a contact hole that connects the drain electrode layer 304 and the pixel electrode layer 327.

[0121]

The common electrode layer 306 is provided over the protective insulating layer 303 and formed using the same material and the same step as the pixel electrode layer 327 in the pixel portion.

[0122]

In this manner, the common connection portion is manufactured in the same process as the switching element in the pixel portion.

[0123]

Then, the first substrate provided with the pixel portion and the common connection portion and a second substrate having a counter electrode are fixed with a sealing material.

[0124]

Note that in this embodiment, a plurality of conductive particles is selectively disposed in the opening portion of the gate insulating layer. That is, the plurality of conductive particles is disposed in a region where the common electrode layer 306 and the common electrode 311 are in contact with each other. The common electrode layer 306 touching both the common electrode 311 and the common potential line 305 is an electrode in contact with the conductive particles, and is electrically connected to the counter electrode of the second substrate.

[0125]

In the case of using a liquid crystal injection method, after the pair of substrates is fixed with a sealing material, a liquid crystal is injected between the pair of substrates. In the case of using a liquid crystal dropping method, after a sealing material is drawn on the second substrate or the first substrate and a liquid crystal is dropped thereon, the

pair of substrates is bonded to each other under a reduced pressure.

[0126]

This embodiment shows an example of the common connection portion electrically connected to the counter electrode. However, the present invention is not particularly limited to the connection of the counter electrode with the common connection portion and can be applied to a connection portion for the connection of the counter electrode to another wiring or to an external connection terminal or the like.

[0127]

This embodiment can be freely combined with Embodiment 1 or 2. For example, the connection wiring 1208 and the connection wiring 1246 of Embodiment 1, which are adjacent to each other, have different potentials and are connected to the respective counter electrode layers. An electrical short circuit can be prevented and a distance between the wirings can be smaller in the following manner: a structure in which one of the wirings and one of the counter electrode layers are connected is employed in the common connection portion using the common potential line of Embodiment 2 which is formed using the same material and the same step as the source and drain electrode layers; and a structure in which the other of the wirings and the other of the counter electrode layers are connected is employed in the common connection portion using a structure of the common potential line of this embodiment which is formed using the same material and the same step as the drain electrode layer.

[0128]

[Embodiment 4]

In this embodiment, an example of a thin film transistor which is applicable to the semiconductor device disclosed in this specification is described. Thin film transistors 410 and 420 which are described in this embodiment can be used as the driver circuit thin film transistor 1223 and the pixel thin film transistor 1211 in Embodiment 1, and the thin film transistor 320 in Embodiment 2 or 3.

[0129]

One embodiment of a semiconductor device and a manufacturing method of the semiconductor device of this embodiment is described with reference to FIGS. 4A to 4E.

[0130]

FIGS. 4A to 4E illustrate cross-sectional structures of a semiconductor device. The thin film transistors 410 and 420 in FIG. 4D each have one of bottom-gate structures called a channel-etched type and are also referred to as an inverted-staggered thin film transistor. In FIG. 4D, the thin film transistor 410 is the driver circuit thin
5 film transistor and the thin film transistor 420 is the pixel thin film transistor.

[0131]

Although description is given using single-gate thin film transistors as the thin film transistors 410 and 420, multi-gate thin film transistors each including a plurality of channel formation regions may be formed as needed.

10 [0132]

A process of manufacturing the thin film transistors 410 and 420 over a substrate 400 is described below with reference to FIGS. 4A to 4E.

[0133]

First, a conductive film is formed over the substrate 400 having an insulating
15 surface, and then, gate electrode layers 411 and 421 are formed in a first photolithography step. Note that a resist mask may be formed by an inkjet method. When the resist mask is formed by an inkjet method, a photomask is not used; therefore, manufacturing costs can be reduced.

[0134]

20 There is no particular limitation on a substrate that can be used as the substrate 400 having an insulating surface as long as it has at least heat resistance to withstand heat treatment performed later. A glass substrate formed using barium borosilicate glass, aluminoborosilicate glass, or the like can be used.

[0135]

25 When the temperature of the heat treatment performed later is high, a substrate having a strain point higher than or equal to 730 °C is preferably used as the glass substrate. As a material of the glass substrate, a glass material such as aluminosilicate glass, aluminoborosilicate glass, or barium borosilicate glass is used, for example. Note that by containing a larger amount of a barium oxide (BaO) than a boric oxide, a
30 glass substrate is heat-resistant and of more practical use. Therefore, a glass substrate containing a larger amount of BaO than B_2O_3 is preferably used.

[0136]

Note that, instead of the glass substrate described above, a substrate formed using an insulator such as a ceramic substrate, a quartz substrate, or a sapphire substrate may be used as the substrate 400. Alternatively, crystallized glass or the like may be used.

5 [0137]

An insulating film serving as a base film may be provided between the substrate 400 and the gate electrode layer 411 and between the substrate 400 and the gate electrode layer 421. The base film has a function of preventing diffusion of an impurity element from the substrate 400, and can be formed to have a single-layer or 10 stacked-layer structure using one or more of a silicon nitride film, a silicon oxide film, a silicon nitride oxide film, and a silicon oxynitride film.

[0138]

The gate electrode layers 411 and 421 can each be formed to have a single-layer structure or a stacked-layer structure using any of metal materials such as 15 molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, and scandium; or an alloy material containing any of these metal materials as its main component.

[0139]

As a two-layer stacked structure of each of the gate electrode layers 411 and 20 421, for example, a two-layer stacked structure in which a molybdenum layer is stacked over an aluminum layer, a two-layer stacked structure in which a molybdenum layer is stacked over a copper layer, a two-layer structure in which a titanium nitride layer or a tantalum nitride layer is stacked over a copper layer, or a two-layer stacked structure in which a titanium nitride layer and a molybdenum layer are stacked is preferable. As a 25 three-layer stacked structure, a stacked layer of a tungsten layer or a tungsten nitride layer, an alloy of aluminum and silicon or an alloy of aluminum and titanium, and a titanium nitride layer or a titanium layer is preferable.

[0140]

Next, a gate insulating layer 402 is formed over the gate electrode layers 411 30 and 421.

[0141]

The gate insulating layer 402 can be formed to have a single-layer or

stacked-layer structure using a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a silicon nitride oxide layer, a hafnium oxide layer, or an aluminum oxide layer by a plasma CVD method, a sputtering method, or the like. For example, a silicon oxynitride layer may be formed using SiH_4, oxygen, and nitrogen as deposition gases by a plasma CVD method. The thickness of the gate insulating layer 402 is greater than or equal to 100 nm and less than or equal to 500 nm; in the case where the gate insulating layer 402 is formed to have a stacked-layer structure, for example, a first gate insulating layer with a thickness greater than or equal to 50 nm and less than or equal to 200 nm and a second gate insulating layer with a thickness greater than or equal to 5 nm and less than or equal to 300 nm are stacked.

[0142]

An oxide semiconductor which is made intrinsic or substantially intrinsic (a highly purified oxide semiconductor) is sensitive to an interface state or interface electric charge. Thus, a gate insulating film (GI) which is to be in contact with a highly purified oxide semiconductor needs to have high quality.

[0143]

For example, a high-density plasma CVD method with the use of microwaves (2.45 GHz), by which a dense and high-quality insulating film having high withstand voltage can be formed, is preferable. This is because an interface state can be reduced and interface characteristics can be favorable when the highly purified oxide semiconductor and the high quality gate insulating film are in contact with each other.

[0144]

In this embodiment, a silicon oxynitride layer (also referred to as SiO_xN_y, where $x > y > 0$) with a thickness less than or equal to 100 nm is formed as the gate insulating layer 402 using a high-density plasma apparatus. Here, a high-density plasma apparatus refers to an apparatus which can realize a plasma density greater than or equal to $1 \times 10^{11}/cm^3$. For example, plasma is generated by applying a microwave power greater than or equal to 3 kW and less than or equal to 6 kW so that the insulating film is formed.

[0145]

A monosilane gas (SiH_4), nitrous oxide (N_2O), and a rare gas are introduced

into a chamber as a source gas to generate high-density plasma under a pressure greater than or equal to 10 Pa and less than or equal to 30 Pa so that an insulating film is formed over a substrate having an insulating surface, such as a glass substrate. After that, the supply of a monosilane gas is stopped, and nitrous oxide (N_2O) and a rare gas are introduced without exposure to the air, so that plasma treatment may be performed on a surface of the insulating film. The plasma treatment performed on the surface of the insulating film by introducing nitrous oxide (N_2O) and a rare gas is performed at least after the insulating film is formed. The insulating film formed through the above process procedure has a small thickness and corresponds to an insulating film whose reliability can be ensured even though it has a thickness less than 100 nm, for example.

[0146]

In forming the gate insulating layer 402, the flow ratio of a monosilane gas (SiH_4) to nitrous oxide (N_2O) which are introduced into the chamber is in the range of 1:10 to 1:200. In addition, as a rare gas which is introduced into the chamber, helium, argon, krypton, xenon, or the like can be used. In particular, argon, which is inexpensive, is preferably used.

[0147]

In addition, since the insulating film formed by using the high-density plasma apparatus can have certain thickness, the insulating film has excellent step coverage. Further, as for the insulating film formed by using the high-density plasma apparatus, the thickness of a thin film can be controlled precisely.

[0148]

The insulating film formed through the above process procedure is greatly different from an insulating film formed using a conventional parallel plate plasma CVD apparatus. The etching rate of the insulating film formed through the above process procedure is lower than that of the insulating film formed using the conventional parallel plate plasma CVD apparatus by greater than or equal to 10 % or greater than or equal to 20 % in the case where the etching rates with the same etchant are compared with each other. Thus, it can be said that the insulating film formed using the high-density plasma apparatus is a dense film. Needless to say, another method such as a sputtering method or a plasma CVD method can be employed as long

as an insulating film having good quality can be formed. Alternatively, an insulating film whose film quality and interface characteristics with an oxide semiconductor are modified by heat treatment after film deposition may be formed. In any case, the gate insulating film needs not only good film quality but also a reduced interface state density of an interface between the gate insulating film and an oxide semiconductor, which can realize a favorable interface.

[0149]

Then, an oxide semiconductor film 430 is formed to a thickness greater than or equal to 2 nm and less than or equal to 200 nm over the gate insulating layer 402.

[0150]

Note that before the oxide semiconductor film 430 is formed by a sputtering method, dust attached to a surface of the gate insulating layer 402 is preferably removed by reverse sputtering in which an argon gas is introduced and plasma is generated. The reverse sputtering refers to a method in which, without application of voltage to a target side, an RF power source is used for application of voltage to a substrate side in an argon atmosphere to generate plasma in the vicinity of the substrate to modify a surface. Note that instead of an argon atmosphere, nitrogen, helium, oxygen, or the like may be used.

[0151]

The oxide semiconductor film 430 is formed as an In-Ga-Zn-O-based oxide semiconductor film, an In-Sn-Zn-O-based oxide semiconductor film, an In-Al-Zn-O-based oxide semiconductor film, a Sn-Ga-Zn-O-based oxide semiconductor film, an Al-Ga-Zn-O-based oxide semiconductor film, a Sn-Al-Zn-O-based oxide semiconductor film, an In-Zn-O-based oxide semiconductor film, a Sn-Zn-O-based oxide semiconductor film, an Al-Zn-O-based oxide semiconductor film, an In-O-based oxide semiconductor film, a Sn-O-based oxide semiconductor film, or a Zn-O-based oxide semiconductor film. In this embodiment, the oxide semiconductor film 430 is formed by a sputtering method with the use of an In-Ga-Zn-O-based metal oxide target. A cross-sectional view of this stage is illustrated in FIG. 4A. Further, the oxide semiconductor film 430 can be formed by a sputtering method in a rare gas (typically argon) atmosphere, an oxygen atmosphere, or an atmosphere of a rare gas (typically argon) and oxygen. In the case of using a sputtering method, deposition may be

performed with the use of a target containing SiO_2 at greater than or equal to 2 wt% and less than or equal to 10 wt%.

[0152]

5 Here, film deposition is performed using a metal oxide target containing In, Ga, and Zn (In_2O_3: Ga_2O_3: ZnO = 1:1:1 [molar ratio]). The deposition condition is set as follows: the distance between the substrate 400 and the target is 100 mm; the pressure is 0.2 Pa; the direct current (DC) power supply is 0.5 kW; and the atmosphere is a mixed atmosphere of argon and oxygen (argon: oxygen = 30 sccm:20 sccm and the oxygen flow rate is 40 %). Note that a pulse direct current (DC) power supply is preferable 10 because powder substances (also referred to as particles or dust) generated in film formation can be reduced and the film thickness can be uniform. The In-Ga-Zn-O-based film is formed to a thickness greater than or equal to 5 nm and less than or equal to 200 nm. In this embodiment, as the oxide semiconductor film, a 20-nm-thick In-Ga-Zn-O-based film is formed by a sputtering method with the use of an 15 In-Ga-Zn-O-based metal oxide target. As a metal oxide target containing In, Ga, and Zn, a target having a composition ratio of In_2O_3: Ga_2O_3: ZnO = 1:1:2 [molar ratio] or a target having a composition ratio of In_2O_3: Ga_2O_3: ZnO = 1:1:4 [molar ratio] can also be used.

[0153]

20 Examples of a sputtering method include an RF sputtering method in which a high-frequency power source is used as a sputtering power source, a DC sputtering method, and a pulsed DC sputtering method in which a bias is applied in a pulsed manner. An RF sputtering method is mainly used in the case of forming an insulating film, and a DC sputtering method is mainly used in the case of forming a metal film.

25 [0154]

In addition, there is a multi-source sputtering apparatus in which a plurality of targets of different materials can be set. With the multi-source sputtering apparatus, films of different materials can be deposited to be stacked in the same chamber, and a film of plural kinds of materials can be deposited by electric discharge at the same time 30 in the same chamber.

[0155]

In addition, there are a sputtering apparatus provided with a magnet system inside the chamber and used for a magnetron sputtering method, and a sputtering apparatus used for an ECR sputtering method in which plasma generated with the use of microwaves is used without using glow discharge.

5 [0156]

Furthermore, as a deposition method using sputtering, there are also a reactive sputtering method in which a target substance and a sputtering gas component are chemically reacted with each other during deposition to form a thin compound film thereof, and a bias sputtering method in which a voltage is also applied to a substrate

10 during deposition.

[0157]

Then, in a second photolithography step, the oxide semiconductor film 430 is processed into island-shaped oxide semiconductor layers. The resist mask for forming the island-shaped oxide semiconductor layers may be formed by an inkjet method.

15 When the resist mask is formed by an inkjet method, a photomask is not used; therefore, manufacturing costs can be reduced.

[0158]

Next, the oxide semiconductor layers are subjected to dehydration or dehydrogenation. The temperature of first heat treatment for dehydration or

20 dehydrogenation is higher than or equal to 400 °C and lower than or equal to 750 °C, preferably higher than or equal to 400 °C and lower than the strain point of the substrate. Here, the substrate is introduced into an electric furnace which is a kind of heat treatment apparatus, heat treatment is performed on the oxide semiconductor layers in a nitrogen atmosphere at 450 °C for one hour, and then, the oxide semiconductor layers

25 are not exposed to the air so that entry of water and hydrogen into the oxide semiconductor layers is prevented; thus, oxide semiconductor layers 431 and 432 are obtained (see FIG. 4B).

[0159]

The apparatus for the heat treatment is not limited to the electric furnace and

30 may be the one provided with a device for heating an object to be processed, using heat conduction or heat radiation from a heating element such as a resistance heating element.

For example, a rapid thermal anneal (RTA) apparatus such as a gas rapid thermal anneal (GRTA) apparatus or a lamp rapid thermal anneal (LRTA) apparatus can be used. An LRTA apparatus is an apparatus for heating an object to be processed by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. A GRTA apparatus is an apparatus for heat treatment using a high-temperature gas. As the gas, an inert gas which does not react with an object to be processed by heat treatment, such as nitrogen or a rare gas such as argon is used.

[0160]

For example, as the first heat treatment, GRTA may be performed as follows. The substrate is placed in an inert gas which has been heated to a high temperature of 650 °C to 700 °C, heated for several minutes, and transferred and taken out from the heated inert gas. With GRTA, high-temperature heat treatment for a short period of time can be achieved.

[0161]

Note that in the first heat treatment, it is preferable that water, hydrogen, and the like be not contained in nitrogen or a rare gas such as helium, neon, or argon. Alternatively, it is preferable that nitrogen or a rare gas such as helium, neon, or argon introduced into an apparatus for the heat treatment have a purity of greater than or equal to 6N (99.9999 %), preferably, greater than or equal to 7N (99.99999 %) (that is, an impurity concentration is set to less than or equal to 1 ppm, preferably, less than or equal to 0.1 ppm).

[0162]

The oxide semiconductor layers might be crystallized to be a microcrystalline film or a polycrystalline film depending on a condition of the first heat treatment or a material of the oxide semiconductor layers. For example, the oxide semiconductor layers may be crystallized to become microcrystalline oxide semiconductor layers having a degree of crystallization of greater than or equal to 90 %, or greater than or equal to 80 %. Further, depending on the condition of the first heat treatment and the material of the oxide semiconductor layers, the oxide semiconductor layers may become

amorphous oxide semiconductor layers containing no crystalline component. The oxide semiconductor layers might become oxide semiconductor layers in which a microcrystalline portion (with a grain diameter greater than or equal to 1 nm and less than or equal to 20 nm, typically greater than or equal to 2 nm and less than or equal to
5 4 nm) is mixed in an amorphous oxide semiconductor. A needle-like crystal in a longitudinal direction (the film-thickness direction) might be generated on the surface side of the oxide semiconductor layers in the case where heat treatment at a high temperature is performed using RTA (e.g., GRTA or LRTA).

[0163]

10 Alternatively, the first heat treatment may be performed on the oxide semiconductor film 430 which has not yet been processed into the island-shaped oxide semiconductor layers. In that case, after the first heat treatment, the substrate is taken out of the heating apparatus and a photolithography step is performed.

[0164]

15 The heat treatment for dehydration or dehydrogenation of the oxide semiconductor layers may be performed at any of the following timings: after the oxide semiconductor layer is formed; after a source electrode and a drain electrode are formed over the oxide semiconductor layer; and after a protective insulating film is formed over the source electrode and the drain electrode.

20 [0165]

Further, the step of forming the contact hole in the gate insulating layer 402 may be performed either before or after the oxide semiconductor film 430 is subjected to dehydration or dehydrogenation treatment.

[0166]

25 Note that the etching of the oxide semiconductor film may be dry etching, without being limited to wet etching.

[0167]

As an etching gas for dry etching, a gas containing chlorine (chlorine-based gas such as chlorine (Cl_2), boron chloride (BCl_3), silicon chloride ($SiCl_4$), or carbon
30 tetrachloride (CCl_4)) is preferably used.

[0168]

Alternatively, a gas containing fluorine (fluorine-based gas such as carbon

tetrafluoride (CF_4), sulfur fluoride (SF_6), nitrogen fluoride (NF_3), or trifluoromethane (CHF_3)); hydrogen bromide (HBr); oxygen (O_2); any of these gases to which a rare gas such as helium (He) or argon (Ar) is added; or the like can be used.

[0169]

5 As the dry etching method, a parallel plate reactive ion etching (RIE) method or an inductively coupled plasma (ICP) etching method can be used. In order to etch the oxide semiconductor film into a desired shape, the etching condition (the amount of electric power applied to a coil-shaped electrode, the amount of electric power applied to an electrode on a substrate side, the temperature of the electrode on the substrate side, 10 or the like) is adjusted as appropriate.

[0170]

As an etchant used for wet etching of the oxide semiconductor film, a solution obtained by mixing phosphoric acid, acetic acid, and nitric acid, an ammonia peroxide mixture (hydrogen peroxide water at 31 wt%: ammonia water at 28 wt%: water = 5:2:2), 15 or the like can be used. Alternatively, ITO07N (produced by KANTO CHEMICAL CO., INC.) may be used.

[0171]

The etchant used in the wet etching is removed by cleaning together with the material which is etched off. The waste liquid containing the etchant and the material 20 etched off may be purified and the material may be reused. When a material such as indium contained in the oxide semiconductor layer is collected from the waste liquid after the etching and reused, the resources can be efficiently reused and the cost can be reduced.

[0172]

25 The etching conditions (such as an etchant, etching time, and temperature) are appropriately adjusted depending on the material so that the material can be etched into a desired shape.

[0173]

Next, a metal conductive film is formed over the gate insulating layer 402 and 30 the oxide semiconductor layers 431 and 432. The metal conductive film may be formed by a sputtering method or a vacuum evaporation method. As a material of the metal conductive film, there are an element selected from Al, Cr, Cu, Ta, Ti, Mo, and W;

an alloy containing any of the above elements as its component; an alloy film containing a combination of any of these elements; and the like. Further, one or more materials selected from manganese, magnesium, zirconium, beryllium, and thorium may be used. The metal conductive film may have a single-layer structure or a stacked-layer structure of two or more layers. For example, a single-layer structure of an aluminum film containing silicon, a two-layer structure in which a titanium film is stacked over an aluminum film, a three-layer structure in which a Ti film, an aluminum film, and a Ti film are stacked in the order presented, and the like can be given. Alternatively, a film, an alloy film, or a nitride film of a combination of Al and one or plurality of elements selected from the followings may be used: titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), and scandium (Sc).

[0174]

If heat treatment is performed after formation of the metal conductive film, it is preferable that the metal conductive film have heat resistance enough to withstand the heat treatment.

[0175]

A third photolithography step is performed. A resist mask is formed over the metal conductive film and selective etching is performed, so that a source electrode layer 415a, a drain electrode layer 415b, a source electrode layer 425a, and a drain electrode layer 425b are formed. Then, the resist mask is removed (see FIG. 4C).

[0176]

Note that materials and etching conditions are adjusted as appropriate so that the oxide semiconductor layers 431 and 432 are not removed by etching of the metal conductive film.

[0177]

In this embodiment, a Ti film is used as the metal conductive film, an In-Ga-Zn-O-based metal oxide is used as the oxide semiconductor layers 431 and 432, and an ammonia peroxide mixture (31 wt% hydrogen peroxide in water: 28 wt% ammonia water: water = 5:2:2) is used as the etchant for the Ti film.

[0178]

Note that in the third photolithography step, parts of the oxide semiconductor layers 431 and 432 are etched, whereby oxide semiconductor layers each having a groove (a depressed portion) might be formed. The resist mask used for forming the source electrode layer 415a, the drain electrode layer 415b, the source electrode layer 425a, and the drain electrode layer 425b may be formed by an inkjet method. When the resist mask is formed by an inkjet method, a photomask is not used; therefore, manufacturing costs can be reduced.

[0179]

In order to reduce the number of photomasks and steps in photolithography steps, etching may be performed with the use of a resist mask formed using a multi-tone mask which is a light-exposure mask through which light is transmitted so as to have a plurality of intensities. Since a resist mask formed with the use of a multi-tone mask has a plurality of film thicknesses and further can be changed in shape by performing etching on the resist mask, the resist mask can be used in a plurality of etching steps of making different patterns. Therefore, a resist mask corresponding at least two or more kinds of different patterns can be formed using one multi-tone mask. Thus, the number of light-exposure masks can be reduced and the number of corresponding photolithography steps can be also reduced, whereby simplification of a process can be realized.

[0180]

Then, plasma treatment with a gas such as N_2O, N_2, or Ar is performed. By this plasma treatment, water adsorbed to surfaces of exposed portions of the oxide semiconductor layers, and the like are removed. Alternatively, plasma treatment may be performed using a mixed gas of oxygen and argon.

[0181]

After the plasma treatment, an oxide insulating layer 416 which serves as a protective insulating film and is in contact with parts of the oxide semiconductor layers 431 and 432 is formed without exposure to the air.

[0182]

The oxide insulating layer 416 can be formed to a thickness of at least 1 nm by a method in which impurities such as water and hydrogen do not enter the oxide insulating layer 416, such as a sputtering method. When hydrogen is contained in the

oxide insulating layer 416, entry of the hydrogen to the oxide semiconductor layers 431 and 432 or abstraction of oxygen in the oxide semiconductor layers by the hydrogen is caused, thereby making backchannels of the oxide semiconductor layers 431 and 432 have a lower resistance (have n-type conductivity) and forming parasitic channels. 5 Therefore, it is important that a film formation method in which hydrogen is not used is employed in order to form the oxide insulating layer 416 containing as little hydrogen as possible.

[0183]

In this embodiment, a silicon oxide film is formed to a thickness of 200 nm by 10 a sputtering method for the oxide insulating layer 416. The substrate temperature in deposition may be higher than or equal to a room temperature and lower than or equal to 300 °C and is 100 °C in this embodiment. The silicon oxide film can be formed by a sputtering method in a rare gas (typically argon) atmosphere, an oxygen atmosphere, or an atmosphere containing a rare gas (typically argon) and oxygen. As a target, a 15 silicon oxide target or a silicon target can be used. For example, the silicon oxide film can be formed using a silicon target by a sputtering method in an atmosphere of oxygen and nitrogen. For the oxide insulating layer 416 formed in contact with the oxide semiconductor layers 431 and 432 having reduced resistance, an inorganic insulating film that does not contain impurities such as moisture, a hydrogen ion, and OH^- and 20 blocks entry of these from the outside is used. Typically, a silicon oxide film, a silicon nitride oxide film, an aluminum oxide film, an aluminum oxynitride film, or the like is used.

[0184]

Next, second heat treatment (preferably higher than or equal to 200 °C and 25 lower than or equal to 400 °C, for example, higher than or equal to 250 °C and lower than or equal to 350 °C) is performed in an inert gas atmosphere or an oxygen gas atmosphere. For example, the second heat treatment is performed in a nitrogen atmosphere at 250 °C for one hour. In the second heat treatment, parts of the oxide semiconductor layers 431 and 432 (the channel formation regions) are heated while in 30 contact with the oxide insulating layer 416.

[0185]

Through the above steps, the oxide semiconductor layers 431 and 432 are placed in an oxygen-deficient state and are decreased in resistance by the heat treatment for dehydration or dehydrogenation; then, parts of the oxide semiconductor layers 431 and 432 are selectively placed in an oxygen-excess state. As a result, a channel
5 formation region 413 overlapping with the gate electrode layer 411 becomes i-type, and a high-resistance source region 414a overlapping with the source electrode layer 415a and a high-resistance drain region 414b overlapping with the drain electrode layer 415b are formed in a self-aligned manner. Through the above steps, the thin film transistor 410 is formed. Similarly, a channel formation region 423 overlapping with the gate
10 electrode layer 421 becomes i-type, and a high-resistance source region 424a overlapping with the source electrode layer 425a and a high-resistance drain region 424b overlapping with the drain electrode layer 425b are formed in a self-aligned manner. Through the above steps, the thin film transistor 420 is formed.

[0186]

15 Further, heat treatment may be performed at a temperature higher than or equal to 100 °C and lower than or equal to 200 °C for greater than or equal to one hour and less than or equal to 30 hours in the air. In this embodiment, the heat treatment is performed at 150 °C for 10 hours. This heat treatment may be performed at a fixed heating temperature. Alternatively, the following temperature cycle may be applied
20 plural times repeatedly: the temperature is increased from a room temperature to a temperature higher than or equal to 100 °C and lower than or equal to 200 °C and then decreased to a room temperature. Further, this heat treatment may be performed under a reduced pressure before formation of the oxide insulating layer 416. Under a reduced pressure, the heating time can be shortened. With such heat treatment,
25 hydrogen is introduced from the oxide semiconductor layers 431 and 432 to the oxide insulating layer 416; thus, normally-off thin film transistors can be obtained. Therefore, reliability of the semiconductor device can be improved.

[0187]

Note that by forming the high-resistance drain regions 414b and 424b (or the
30 high-resistance source regions 414a and 424a) in the oxide semiconductor layers 431 and 432 overlapping with the drain electrode layers 415b and 425b (and the source

electrode layers 415a and 425a), reliability of the thin film transistors 410 and 420 can be improved. Specifically, by forming the high-resistance drain regions 414b and 424b, the structure can be obtained in which conductivities of the drain electrode layers 415b and 425b, the high-resistance drain regions 414b and 424b, and the channel formation regions 413 and 423 vary stepwise. Therefore, in the case where the thin film transistors 410 and 420 operate with the drain electrode layers 415b and 425b connected to a wiring for supplying a high power supply potential V_{DD}, the high-resistance drain regions 414b and 424b serve as a buffer and a high electric field is not applied locally even if the high electric field is applied between the gate electrode layer 411 and the drain electrode layer 415b and between the gate electrode layer 421 and the drain electrode layer 425b; thus, the withstand voltage of the thin film transistor can be increased.

[0188]

Further, the high-resistance source regions 414a and 424a or the high-resistance drain regions 414b and 424b in the oxide semiconductor layers 431 and 432 are formed in the entire thickness direction in the case where the thickness of the oxide semiconductor layers 431 and 432 is less than or equal to 15 nm. In the case where the thickness of the oxide semiconductor layer is greater than or equal to 30 nm and less than or equal to 50 nm, parts of the oxide semiconductor layers 431 and 432, that is, regions in contact with the source electrode layers 415a and 425a or the drain electrode layers 415b and 425b and the vicinity thereof are reduced in resistance and become a high-resistance source regions 414a and 424a or a high-resistance drain regions 414b and 424b, while regions in the oxide semiconductor layers 431 and 432 which are close to the gate insulating layer 402 can be made to be i-type.

[0189]

A protective insulating layer 403 may be additionally formed over the oxide insulating layer 416. For example, a silicon nitride film is formed by an RF sputtering method. An RF sputtering method is preferable as a formation method of the protective insulating layer because of high productivity. The protective insulating layer 403 is formed using an inorganic insulating film which does not contain impurities such as moisture, a hydrogen ion, and OH^- and blocks entry of these from the outside; for example, a silicon nitride film, an aluminum nitride film, a silicon nitride oxide film,

an aluminum oxynitride film, or the like is used. In this embodiment, the protective insulating layer 403 is formed using a silicon nitride film (see FIG. 4D).

[0190]

A planarization insulating layer for planarization may be provided over the 5 protective insulating layer 403. As illustrated in FIG. 4E, a planarization insulating layer 404 is formed in this embodiment.

[0191]

The planarization insulating layer 404 can be formed using an organic material having heat resistance, such as a polyimide, an acrylic resin, a benzocyclobutene-based 10 resin, a polyamide, or an epoxy resin. Other than such organic materials, it is also possible to use a low-dielectric constant material (a low-k material), a siloxane-based resin, phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), or the like. The planarization insulating layer 404 may be formed by stacking plural insulating films formed using any of these materials.

15 [0192]

Note that the siloxane-based resin corresponds to a resin containing a Si-O-Si bond formed using a siloxane-based material as a starting material. The siloxane-based resin may contain as a substituent an organic group (e.g., an alkyl group or an aryl group) or a fluoro group. In addition, the organic group may contain a 20 fluoro group.

[0193]

There is no particular limitation on the method for forming the planarization insulating layer 404, and the planarization insulating layer 404 can be formed, depending on the material, by a method such as a sputtering method, an SOG method, 25 spin coating, dip coating, spray coating, or a droplet discharge method (e.g., an inkjet method, screen printing, or offset printing), or a tool (equipment) such as a doctor knife, a roll coater, a curtain coater, or a knife coater.

[0194]

A fourth photolithography step is performed. A resist mask is formed and 30 selective etching is performed to remove parts of the oxide insulating layer 416, the protective insulating layer 403, and the planarization insulating layer 404, so that an opening reaching the drain electrode layer 425b is formed.

[0195]

Next, a light-transmitting conductive film is formed. The light-transmitting conductive film is formed using an indium oxide (In_2O_3), an indium oxide-tin oxide mixed oxide (In_2O_3-SnO_2, abbreviated as ITO), or the like by a sputtering method, a vacuum evaporation method, or the like. Alternatively, an Al-Zn-O-based film containing nitrogen, that is, an Al-Zn-O-N-based film, a Zn-O-N-based film, or a Sn-Zn-O-N-based film may be used. Note that the composition (at.%) of zinc in the Al-Zn-O-N-based film is less than or equal to 47 at.% and is higher than that of aluminum in the film; the composition (at.%) of aluminum in the film is higher than that of nitrogen in the film. Such a material is etched with a hydrochloric acid-based solution. However, since an etching residue is easily precipitated and left over the substrate particularly in etching ITO, an indium oxide-zinc oxide mixed oxide (In_2O_3-ZnO) may be used to improve etching processability.

[0196]

Note that the unit of the composition of components in the light-transmitting conductive film is atomic percent (at.%), and the composition of components is evaluated by analysis using an electron probe X-ray microanalyzer (EPMA).

[0197]

Next, a fifth photolithography step is performed. A resist mask is formed and an unnecessary portion of the light-transmitting conductive film is removed by etching to form a pixel electrode layer 427 and a conductive layer 417. Then, the resist mask is removed (see FIG. 4E).

[0198]

In this embodiment, the step of forming the opening in the gate insulating layer is not illustrated in a drawing; however, the step of forming an opening in the gate insulating layer may be performed in either the same photolithography step as that of the oxide insulating layer and the protective insulating layer or another photolithography step. When the opening is formed in another photolithography step, the number of photolithography steps is six.

[0199]

This embodiment can be implemented in appropriate combination with any of

the other embodiments.

[0200]

As described above, a semiconductor device which includes a thin film transistor formed using an oxide semiconductor layer and consumes less power can be
5 provided.

[0201]

Further, a semiconductor device which includes a thin film transistor formed using an oxide semiconductor layer and has high reliability can be provided.

[0202]

10 [Embodiment 5]

In this embodiment, another example of a thin film transistor which is applicable to the semiconductor device disclosed in this specification is described. Thin film transistors 450 and 460 which are described in this embodiment can be used as the driver circuit thin film transistor 1223 and the pixel thin film transistor 1211 in
15 Embodiment 1, and the thin film transistor 320 in Embodiment 2.

[0203]

One embodiment of a semiconductor device and a manufacturing method of the semiconductor device of this embodiment is described with reference to FIGS. 5A to 5E.

20 [0204]

FIGS. 5A to 5E illustrate cross-sectional structures of a semiconductor device. The thin film transistors 450 and 460 in FIG. 5D each have one of the bottom-gate structures called a channel-protection type (also referred to as a channel-stop type) and are also referred to as an inverted-staggered thin film transistor.

25 [0205]

Although description is given using single-gate thin film transistors as the thin film transistors 450 and 460, multi-gate thin film transistors each including a plurality of channel formation regions may be formed as needed.

[0206]

30 A process of manufacturing the thin film transistors 450 and 460 over the substrate 400 is described below with reference to FIGS. 5A to 5E.

[0207]

First, a conductive film is formed over the substrate 400 having an insulating surface, and then, gate electrode layers 451 and 461 are formed in a first photolithography step. Note that a resist mask may be formed by an inkjet method. When the resist mask is formed by an inkjet method, a photomask is not used; therefore,
5 manufacturing costs can be reduced.

[0208]

The gate electrode layers 451 and 461 can each be formed to have a single-layer structure or a stacked-layer structure using any of metal materials such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium,
10 and scandium; or an alloy material containing any of these metal materials as its main component.

[0209]

Next, the gate insulating layer 402 is formed over the gate electrode layers 451 and 461.

15 [0210]

In this embodiment, a silicon oxynitride layer is formed to a thickness less than or equal to 100 nm by a plasma CVD method as the gate insulating layer 402.

[0211]

Next, an oxide semiconductor film is formed over the gate insulating layer 402
20 to have a thickness greater than or equal to 2 nm and less than or equal to 200 nm and is processed into island-shaped oxide semiconductor layers in a second photolithography step. In this embodiment, the oxide semiconductor film is formed by a sputtering method with the use of an In-Ga-Zn-O-based metal oxide target.

[0212]

25 Next, the oxide semiconductor layers are subjected to dehydration or dehydrogenation. The temperature of first heat treatment for dehydration or dehydrogenation is higher than or equal to 400 °C and lower than or equal to 750 °C, preferably higher than or equal to 400 °C and lower than the strain point of the substrate. Here, the substrate is introduced into an electric furnace which is a kind of heat
30 treatment apparatus, heat treatment is performed on the oxide semiconductor layers in a nitrogen atmosphere at 450 °C for one hour, and then, the oxide semiconductor layers

are not exposed to the air so that entry of water and hydrogen into the oxide semiconductor layers is prevented. Thus, oxide semiconductor layers 431 and 432 are obtained (see FIG. 5A).

[0213]

5 Then, plasma treatment with a gas such as N_2O, N_2, or Ar is performed. By this plasma treatment, water adsorbed to surfaces of exposed portions of the oxide semiconductor layers, and the like are removed. Alternatively, plasma treatment may be performed using a mixed gas of oxygen and argon.

[0214]

10 Next, after an oxide insulating layer is formed over the gate insulating layer 402 and the oxide semiconductor layers 431 and 432, a third photolithography step is performed. A resist mask is formed and etching is performed selectively, whereby oxide insulating layers 456 and 466 are formed. After that, the resist mask is removed.

[0215]

15 In this embodiment, a silicon oxide film is formed to a thickness of 200 nm by a sputtering method as the oxide insulating layers 456 and 466. The substrate temperature in deposition may be higher than or equal to a room temperature and lower than or equal to 300 °C and is 100 °C in this embodiment. The silicon oxide film can be formed by a sputtering method in a rare gas (typically argon) atmosphere, an oxygen 20 atmosphere, or an atmosphere containing a rare gas (typically argon) and oxygen. As a target, a silicon oxide target or a silicon target can be used. For example, the silicon oxide film can be formed using a silicon target by a sputtering method in an atmosphere of oxygen and nitrogen. For the oxide insulating layers 456 and 466 formed in contact with the oxide semiconductor layers 431 and 432, an inorganic insulating film that does 25 not contain impurities such as moisture, a hydrogen ion, and OH^- and blocks entry of these from the outside is used. Typically, a silicon oxide film, a silicon nitride oxide film, an aluminum oxide film, an aluminum oxynitride film, or the like is used.

[0216]

Next, second heat treatment (preferably higher than or equal to 200 °C and 30 lower than or equal to 400 °C, for example, higher than or equal to 250 °C and lower than or equal to 350 °C) may be performed in an inert gas atmosphere or an oxygen gas

atmosphere. For example, the second heat treatment is performed in a nitrogen atmosphere at 250 °C for one hour. In the second heat treatment, parts of the oxide semiconductor layers (the channel formation regions) are heated while in contact with the oxide insulating layers 456 and 466.

5 [0217]

In this embodiment, heat treatment is further performed on the oxide semiconductor layers 431 and 432 over which the oxide insulating layers 456 and 466 are provided and thus parts of the oxide semiconductor layers 431 and 432 are exposed in an inert gas atmosphere such as nitrogen or under reduced pressure. By performing 10 heat treatment in an inert gas atmosphere such as nitrogen or under reduced pressure, regions of the oxide semiconductor layers 431 and 432, which are not covered with the oxide insulating layers 456 and 466 and are thus exposed, can be reduced in resistance. For example, heat treatment is performed in a nitrogen atmosphere at 250 °C for one hour.

15 [0218]

By the heat treatment for the oxide semiconductor layers 431 and 432 provided with the oxide insulating layers 456 and 466, respectively, in a nitrogen atmosphere, the resistance of the exposed regions of the oxide semiconductor layers 431 and 432 is reduced. Thus, oxide semiconductor layers 452 and 462 each including regions with 20 different resistances (indicated as shaded regions and white regions in FIG. 5B) are formed.

[0219]

Next, after a metal conductive film is formed over the gate insulating layer 402, the oxide semiconductor layers 452 and 462, and the oxide insulating layers 456 and 25 466, a fourth photolithography step is performed. A resist mask is formed and selective etching is performed, whereby source electrode layers 455a and 465a and drain electrode layers 455b and 465b are formed. After that, the resist mask is removed (see FIG. 5C). The source electrode layer 455a and the drain electrode layer 455b are in contact with part of the oxide insulating layer 456 and with part of the oxide 30 semiconductor layer 452. Similarly, the source electrode layer 465a and the drain electrode layer 465b are in contact with part of the oxide insulating layer 466 and with

part of the oxide semiconductor layer 462.

[0220]

As a material of the source electrode layers 455a and 465a and the drain electrode layers 455b and 465b, there are an element selected from Al, Cr, Cu, Ta, Ti, Mo, and W; an alloy containing any of these elements as its component; an alloy film containing a combination of any of these elements; and the like. Further, the metal conductive film may have a single-layer structure or a stacked-layer structure of two or more layers.

[0221]

Through the above steps, the oxide semiconductor layers 431 and 432 are placed in an oxygen-deficient state and are decreased in resistance by the heat treatment for dehydration or dehydrogenation; then, parts of the oxide semiconductor layers 431 and 432 are selectively placed in an oxygen-excess state. As a result, channel formation regions 453 and 463 overlapping with the gate electrode layers 451 and 461 become i-type, and high-resistance source regions 454a and 464a overlapping with the source electrode layers 455a and 465a and high-resistance drain regions 454b and 464b overlapping with the drain electrode layers 455b and 465b are formed in a self-aligned manner. Through the above steps, the thin film transistors 450 and 460 are formed.

[0222]

Further, heat treatment may be performed at a temperature higher than or equal to 100 °C and lower than or equal to 200 °C for greater than or equal to one hour and less than or equal to 30 hours in the air. In this embodiment, the heat treatment is performed at 150 °C for 10 hours. This heat treatment may be performed at a fixed heating temperature. Alternatively, the following temperature cycle may be applied plural times repeatedly: the temperature is increased from a room temperature to a temperature higher than or equal to 100 °C and lower than or equal to 200 °C and then decreased to a room temperature. Further, this heat treatment may be performed under a reduced pressure before formation of the oxide insulating layers 456 and 466. Under a reduced pressure, the heating time can be shortened. With such heat treatment, hydrogen is introduced from the oxide semiconductor layers 452 and 462 to the oxide insulating layers 456 and 466; thus, normally-off thin film transistors can be obtained.

Therefore, reliability of the semiconductor device can be improved.

[0223]

Note that by forming the high-resistance drain regions 454b and 464b (or the high-resistance source regions 454a and 464a) in the oxide semiconductor layers 452 and 462 overlapping with the drain electrode layers 455b and 465b (and the source electrode layers 455a and 465a), reliability of the thin film transistors 450 and 460 can be improved. Specifically, by forming the high-resistance drain regions 454b and 464b, the structure can be obtained in which conductivities of the drain electrode layers 455b and 465b, the high-resistance drain regions 454b and 464b, and the channel formation regions 453 and 463 vary stepwise. Therefore, in the case where the thin film transistors operate with the drain electrode layers 455b and 465b connected to a wiring for supplying a high power supply potential V_{DD}, the high-resistance drain regions 454b and 464b serve as a buffer and a high electric field is not applied locally even if the high electric field is applied between the gate electrode layer 451 and the drain electrode layer 455b and between the gate electrode layer 461 and the drain electrode layer 465b; thus, the withstand voltage of the transistor can be increased.

[0224]

A protective insulating layer 403 is formed over the source electrode layers 455a and 465a, the drain electrode layers 455b and 465b, and the oxide insulating layers 456 and 466. In this embodiment, the protective insulating layer 403 is formed using a silicon nitride film (see FIG. 5D).

[0225]

Alternatively, an oxide insulating layer may be further formed over the source electrode layers 455a and 465a, the drain electrode layers 455b and 465b, and the oxide insulating layers 456 and 466, and the protective insulating layer 403 may be stacked over the oxide insulating layer. In this embodiment, the planarization insulating layer 404 is formed over the protective insulating layer 403.

[0226]

Next, a fifth photolithography step is performed. A resist mask is formed and selective etching is performed to remove parts of the planarization insulating layer 404 and the protective insulating layer 403, so that an opening reaching the drain electrode layer 465b is formed.

[0227]

Next, a light-transmitting conductive film is formed, and a sixth photolithography step is performed. A resist mask is formed and an unnecessary portion is removed by etching, whereby a pixel electrode layer 467 and a conductive layer 457 are formed. Then, the resist mask is removed (see FIG. 5E).

[0228]

In this embodiment, the step of forming the opening in the gate insulating layer is not illustrated in a drawing; however, the step of forming an opening in the gate insulating layer may be performed in either the same photolithography step as that of the oxide insulating layer and the protective insulating layer or another photolithography step. When the opening is formed in another photolithography step, the number of photolithography steps is seven.

[0229]

This embodiment can be implemented in appropriate combination with any of the other embodiments.

[0230]

As described above, a semiconductor device which includes a thin film transistor formed using an oxide semiconductor layer and consumes less power can be provided.

[0231]

Further, a semiconductor device which includes a thin film transistor formed using an oxide semiconductor layer and has high reliability can be provided.

[0232]

[Embodiment 6]

In this embodiment, another example of a thin film transistor which is applicable to the semiconductor device disclosed in this specification is described. Thin film transistors 240 and 260 which are described in this embodiment can be used as the driver circuit thin film transistor 1223 and the pixel thin film transistor 1211 in Embodiment 1, and the thin film transistor 320 in Embodiment 2.

[0233]

One embodiment of a semiconductor device and a manufacturing method of the semiconductor device of this embodiment is described with reference to FIGS. 6A to

6E.

[0234]

Although description is given using single-gate thin film transistors as the thin film transistors 240 and 260, multi-gate thin film transistors each including a plurality of channel formation regions may be formed as needed.

[0235]

A process of manufacturing the thin film transistors 240 and 260 over a substrate 290 is described below with reference to FIGS. 6A to 6E.

[0236]

First, a conductive film is formed over the substrate 290 having an insulating surface, and then, gate electrode layers 241 and 261 are formed in a first photolithography step. In this embodiment, as the gate electrode layers 241 and 261, a tungsten film is formed to a thickness of 150 nm by a sputtering method.

[0237]

Next, a gate insulating layer 292 is formed over the gate electrode layers 241 and 261. In this embodiment, a silicon oxynitride layer is formed to a thickness less than or equal to 100 nm by a plasma CVD method as the gate insulating layer 292.

[0238]

Next, a metal conductive film is formed over the gate insulating layer 292, and a second photolithography step is performed. A resist mask is formed over the metal conductive film and selective etching is performed, whereby source electrode layers 245a and 265a and drain electrode layers 245b and 265b are formed. After that, the resist mask is removed (see FIG. 6A).

[0239]

Next, an oxide semiconductor film 295 is formed (see FIG. 6B). In this embodiment, the oxide semiconductor film 295 is formed by a sputtering method with the use of an In-Ga-Zn-O-based metal oxide target. The oxide semiconductor film 295 is processed into island-shaped oxide semiconductor layers in a third photolithography step.

[0240]

Next, the oxide semiconductor layers are subjected to dehydration or dehydrogenation. The temperature of first heat treatment for dehydration or

dehydrogenation is higher than or equal to 400 °C and lower than or equal to 750 °C, preferably higher than or equal to 400 °C and lower than the strain point of the substrate. Here, the substrate is introduced into an electric furnace which is a kind of heat treatment apparatus, heat treatment is performed on the oxide semiconductor layers in a
5 nitrogen atmosphere at 450 °C for one hour, and then, the oxide semiconductor layers are not exposed to the air so that entry of water and hydrogen into the oxide semiconductor layers is prevented. Thus, oxide semiconductor layers 296 and 297 are obtained (see FIG. 6C).

[0241]

10 As the first heat treatment, GRTA may be performed as follows. The substrate is placed in an inert gas which has been heated to a high temperature of 650 °C to 700 °C, heated for several minutes, and transferred and taken out from the heated inert gas. With GRTA, high-temperature heat treatment for a short period of time can be achieved.

15 [0242]

An oxide insulating layer 246 to be a protective insulating film is formed in contact with the oxide semiconductor layers 296 and 297.

[0243]

The oxide insulating layer 246 can be formed to a thickness of at least 1 nm by
20 a method in which impurities such as water and hydrogen do not enter the oxide insulating layer 246, such as a sputtering method. When hydrogen is contained in the oxide insulating layer 246, entry of the hydrogen to the oxide semiconductor layers 296 and 297 or abstraction of oxygen in the oxide semiconductor layers 296 and 297 by the hydrogen is caused, thereby making backchannels of the oxide semiconductor layers
25 296 and 297 have a lower resistance (have n-type conductivity) and forming parasitic channels. Therefore, it is important that a film formation method in which hydrogen is not used is employed in order to form the oxide insulating layer 246 containing as little hydrogen as possible.

[0244]

30 In this embodiment, a silicon oxide film is formed to a thickness of 200 nm as the oxide insulating layer 246 by a sputtering method. The substrate temperature in

deposition may be higher than or equal to a room temperature and lower than or equal to 300 °C and is 100 °C in this embodiment. The silicon oxide film can be formed by a sputtering method in a rare gas (typically argon) atmosphere, an oxygen atmosphere, or an atmosphere containing a rare gas (typically argon) and oxygen. As a target, a
5 silicon oxide target or a silicon target can be used. For example, the silicon oxide film can be formed using a silicon target by a sputtering method in an atmosphere of oxygen and nitrogen. For the oxide insulating layer 246 formed in contact with the oxide semiconductor layers 296 and 297 having reduced resistance, an inorganic insulating film that does not contain impurities such as moisture, a hydrogen ion, and OH^- and
10 blocks entry of these from the outside is used. Typically, a silicon oxide film, a silicon nitride oxide film, an aluminum oxide film, an aluminum oxynitride film, or the like is used.

[0245]

Next, second heat treatment (preferably higher than or equal to 200 °C and
15 lower than or equal to 400 °C, for example, higher than or equal to 250 °C and lower than or equal to 350 °C) is performed in an inert gas atmosphere or an oxygen gas atmosphere. For example, the second heat treatment is performed in a nitrogen atmosphere at 250 °C for one hour. In the second heat treatment, parts (channel formation regions) of the oxide semiconductor layers 296 and 297 are heated while in
20 contact with the oxide insulating layer 246.

[0246]

Through the above steps, the oxide semiconductor layers 296 and 297 are placed in an oxygen-deficient state, are decreased in resistance by the heat treatment for dehydration or dehydrogenation, and are placed in an oxygen-excess state. As a result,
25 i-type oxide semiconductor layers 242 and 262 are formed. Through the above steps, the thin film transistors 240 and 260 are formed.

[0247]

Further, heat treatment may be performed at a temperature higher than or equal to 100 °C and lower than or equal to 200 °C for greater than or equal to one hour and
30 less than or equal to 30 hours in the air. In this embodiment, the heat treatment is performed at 150 °C for 10 hours. This heat treatment may be performed at a fixed

heating temperature. Alternatively, the following temperature cycle may be applied plural times repeatedly: the temperature is increased from a room temperature to a temperature higher than or equal to 100 °C and lower than or equal to 200 °C and then decreased to a room temperature. Further, this heat treatment may be performed under
5 a reduced pressure before formation of the oxide insulating layer. Under a reduced pressure, the heating time can be shortened. With such heat treatment, hydrogen is introduced from the oxide semiconductor layers to the oxide insulating layer; thus, normally-off thin film transistors can be obtained. Therefore, reliability of the semiconductor device can be improved.

10 [0248]

A protective insulating layer 293 may be additionally formed over the oxide insulating layer 246. For example, a silicon nitride film is formed by an RF sputtering method. In this embodiment, the protective insulating layer 293 is formed using a silicon nitride film (see FIG. 6D).

15 [0249]

A planarization insulating layer 294 for planarization may be provided over the protective insulating layer 293. In this embodiment, the planarization insulating layer 294 is formed over the protective insulating layer 293.

[0250]

20 Next, a fourth photolithography step is performed. A resist mask is formed and selective etching is performed to remove parts of the planarization insulating layer 294, the protective insulating layer 293, and the oxide insulating layer 246, whereby an opening reaching the drain electrode layer 265b is formed.

[0251]

25 Next, a light-transmitting conductive film is formed, and a fifth photolithography step is performed. A resist mask is formed and an unnecessary portion is removed by etching, so that a pixel electrode layer 267 and a conductive layer 247 are formed. Then, the resist mask is removed (see FIG. 6E).

[0252]

30 In this embodiment, the step of forming the opening in the gate insulating layer is not illustrated in a drawing; however, the step of forming an opening in the gate insulating layer may be performed in either the same photolithography step as that of

the oxide insulating layer and the protective insulating layer or another photolithography step. When the opening is formed in another photolithography step, the number of photolithography steps is six.

[0253]

5 This embodiment can be implemented in appropriate combination with any of the other embodiments.

[0254]

As described above, a semiconductor device which includes a thin film transistor formed using an oxide semiconductor layer and consumes less power can be 10 provided.

[0255]

Further, a semiconductor device which includes a thin film transistor formed using an oxide semiconductor layer and has high reliability can be provided.

[0256]

15 [Embodiment 7]

In this embodiment, another example of a thin film transistor which is applicable to the semiconductor device disclosed in this specification is described. Thin film transistors 210 and 220 which are described in this embodiment can be used as the driver circuit thin film transistor 1223 and the pixel thin film transistor 1211 in 20 Embodiment 1, and the thin film transistor 320 in Embodiment 2.

[0257]

In this embodiment, an example of a manufacturing process of a semiconductor device including a thin film transistor, part of which is different from that in Embodiment 4, is described with reference to FIGS. 8A to 8E. FIGS. 8A to 8E are the 25 same as FIGS. 4A to 4E except that part of the process in FIGS. 8A to 8E is different from that in FIGS. 4A to 4E; thus, detailed description of the same portions as those in FIGS. 4A to 4E is omitted. In this embodiment, a mask layer formed using a multi-tone mask is used in photolithography steps.

[0258]

30 Since a mask layer formed with the use of a multi-tone mask has a plurality of film thicknesses and further can be changed in shape by performing etching on the mask layer, the mask layer can be used in a plurality of etching steps of making different

patterns. Therefore, a mask layer corresponding to two or more kinds of different patterns can be formed using one multi-tone mask. Thus, the number of light-exposure masks can be reduced and the number of corresponding photolithography steps can be also reduced, whereby simplification of a process can be realized.

5 [0259]

In accordance with Embodiment 1, gate electrode layers 211 and 221 are formed over the substrate 200 in a first photolithography step and then, a gate insulating layer 202 is stacked thereover. An oxide semiconductor film is formed over the gate insulating layer 202. In this embodiment, the oxide semiconductor film is formed by a

10 sputtering method with the use of an In-Ga-Zn-O-based metal oxide target.

[0260]

The substrate is introduced into an electric furnace which is a kind of heat treatment apparatus, and first heat treatment for dehydration or dehydrogenation is performed on the oxide semiconductor film in a nitrogen atmosphere at 450 °C for one

15 hour. Then, the oxide semiconductor film is not exposed to the air so that entry of water and hydrogen into the oxide semiconductor film is prevented. Thus, an oxide semiconductor film 230 is obtained.

[0261]

Next, a metal conductive film 237 is formed over the oxide semiconductor film

20 230 by a sputtering method or a vacuum evaporation method (see FIG. 8A).

[0262]

The metal conductive film 237 is a conductive film to be source and drain electrode layers. As a material of the metal conductive film, there are an element selected from Al, Cr, Cu, Ta, Ti, Mo, and W; an alloy containing any of the above

25 elements as its component; an alloy film containing a combination of any of these elements; and the like. Further, one or more materials selected from manganese, magnesium, zirconium, beryllium, and thorium may be used.

[0263]

In a second photolithography step, resist masks 231a and 231b are formed over

30 the oxide semiconductor film 230 and the metal conductive film 237.

[0264]

In this embodiment, an example is described in which light exposure is

performed using a multi-tone (high-tone) mask for forming the resist masks 231a and 231b. First, a resist is formed in order to form the resist masks 231a and 231b. As the resist, a positive resist or a negative resist can be used. Here, a positive resist is used. The resist may be formed by a spin coating method or may be selectively formed by an inkjet method. When the resist is selectively formed by an inkjet method, a resist can be prevented from being formed in an unintended portion, which results in reducing waste of the material.

[0265]

Next, the resist is irradiated with light with the use of a multi-tone mask 81 as a light-exposure mask, so that the resist is exposed to light.

[0266]

Here, light exposure using the multi-tone mask 81 is described with reference to FIGS. 9A to 9D.

[0267]

A multi-tone mask is a mask capable of light exposure of three levels to provide an exposed region, a half-exposed region, and an unexposed region. A multi-tone mask is a light-exposure mask through which light is transmitted to have a plurality of intensities. One-time light exposure and development process allow a resist mask with plural thicknesses (typically, two kinds of thicknesses) to be formed. Therefore, with the use of a multi-tone mask, the number of light-exposure masks can be reduced.

[0268]

Typical examples of the multi-tone mask include a gray-tone mask 81a illustrated in FIG. 9A and a half-tone mask 81b illustrated in FIG. 9C.

[0269]

As illustrated in FIG. 9A, the gray-tone mask 81a includes a light-transmitting substrate 83, and a light-blocking portion 84 and a diffraction grating 85 which are formed on the light-transmitting substrate 83. The light transmittance of the light-blocking portion 84 is 0 %. Meanwhile, the diffraction grating 85 has a light-transmitting portion in a slit form, a dot form, a mesh form, or the like with intervals that are less than or equal to the resolution limit of light used for the exposure, whereby the light transmittance can be controlled. Note that the diffraction grating 85

can be in a slit form, a dot form, or a mesh form with regular intervals; or in a slit form, a dot form, or a mesh form with irregular intervals.

[0270]

As the light-transmitting substrate 83, a light-transmitting substrate such as a quartz substrate can be used. The light-blocking portion 84 and the diffraction grating 85 can be formed using a light-blocking material that absorbs light, such as chromium or a chromium oxide.

[0271]

When the gray-tone mask 81a is irradiated with light for exposure, a light transmittance 86 of the light-blocking portion 84 is 0 % and the light transmittance 86 of a region where neither the light-blocking portion 84 nor the diffraction grating 85 is provided is 100 %, as illustrated in FIG. 9B. The light transmittance 86 of the diffraction grating 85 can be controlled in the range of 10 % to 70 %. The light transmittance of the diffraction grating 85 can be controlled by adjusting the interval or pitch of slits, dots, or meshes of the diffraction grating.

[0272]

As illustrated in FIG. 9C, the half-tone mask 81b includes the light-transmitting substrate 83 provided with a semi-light-transmitting portion 87 and a light-blocking portion 88. The semi-light-transmitting portion 87 can be formed using MoSiN, MoSi, MoSiO, MoSiON, CrSi, or the like. The light-blocking portion 88 can be formed using a light-blocking material that absorbs light, such as chromium or a chromium oxide.

[0273]

When the half-tone mask 81b is irradiated with light for exposure, a light transmittance 89 of the light-blocking portion 88 is 0 % and the light transmittance 89 of a region where neither the light-blocking portion 88 nor the semi-light-transmitting portion 87 is provided is 100 %, as illustrated in FIG. 9D. The light transmittance 89 of the semi-light-transmitting portion 87 can be controlled in the range of 10 % to 70 %. The light transmittance of the semi-light-transmitting portion 87 can be controlled with the material of the semi-light-transmitting portion 87.

[0274]

After the light exposure using the multi-tone mask, development is performed, whereby the resist masks 231a and 231b each with regions having different thicknesses can be formed as illustrated in FIG. 8B.

[0275]

5 Next, a first etching step is performed using the resist masks 231a and 231b, so that the oxide semiconductor film 230 and the metal conductive film 237 are etched to have island shapes. As a result, oxide semiconductor layers 233 and 235 and metal conductive layers 232 and 234 can be formed (see FIG. 8B).

[0276]

10 Next, the resist masks 231a and 231b are subjected to ashing. Consequently, the areas (the volume, considering three dimensions) and the thicknesses of the resist masks are reduced. At that time, resists of the resist masks in regions with small thicknesses (a region overlapping with part of the gate electrode layer 211 and a region overlapping with part of the gate electrode layer 221) is removed so that separated resist
15 masks 236a, 236b, 236d, and 236e can be formed.

[0277]

Unnecessary portions are removed by etching with the use of the separated resist masks 236a, 236b, 236d, and 236e, so that the source electrode layers 215a and 225a and the drain electrode layers 215b and 225b are formed (see FIG. 8C).

20 [0278]

Note that materials and etching conditions are adjusted as appropriate so that the oxide semiconductor layers 233 and 235 are not removed by etching of the metal conductive layers 232 and 234.

[0279]

25 In this embodiment, a Ti film is used as the metal conductive layers 232 and 234, an In-Ga-Zn-O-based metal oxide is used for the oxide semiconductor layers 233 and 235, and an ammonia hydrogen peroxide solution (31 wt% hydrogen peroxide in water: 28 wt% ammonia water: water = 5:2:2) is used as an etchant for the Ti film.

[0280]

30 Note that the etching of the metal conductive film and the oxide semiconductor film may be dry etching, without being limited to wet etching.

[0281]

As an etching gas for dry etching, a gas containing chlorine (chlorine-based gas such as chlorine (Cl_2), boron chloride (BCl_3), silicon chloride ($SiCl_4$), or carbon tetrachloride (CCl_4)) is preferably used.

5 [0282]

Alternatively, a gas containing fluorine (fluorine-based gas such as carbon tetrafluoride (CF_4), sulfur fluoride (SF_6), nitrogen fluoride (NF_3), or trifluoromethane (CHF_3)); hydrogen bromide (HBr); oxygen (O_2); any of these gases to which a rare gas such as helium (He) or argon (Ar) is added; or the like can be used.

10 [0283]

As the dry etching method, a parallel plate reactive ion etching (RIE) method or an inductively coupled plasma (ICP) etching method can be used. In order to etch the films into desired shapes, the etching conditions (the amount of electric power applied to a coil-shaped electrode, the amount of electric power applied to an electrode 15 on the substrate side, the temperature of the electrode on the substrate side, and the like) are adjusted as appropriate.

[0284]

As an etchant used for wet etching, a solution obtained by mixing phosphoric acid, acetic acid, and nitric acid, or the like can be used. Alternatively, ITO07N 20 (produced by KANTO CHEMICAL CO., INC.) may be used.

[0285]

The etchant used in the wet etching is removed by cleaning together with the material which is etched off. The waste liquid containing the etchant and the material etched off may be purified and the material may be reused. When a material such as 25 indium contained in the oxide semiconductor layer is collected from the waste liquid after the etching and reused, the resources can be efficiently reused and the cost can be reduced.

[0286]

The etching conditions (such as an etchant, etching time, and temperature) are 30 appropriately adjusted depending on the material so that the material can be etched to have a desired shape.

[0287]

Next, the separated resist masks 236a, 236b, 236d, and 236e are removed and an oxide insulating layer 216 to be a protective insulating film is formed in contact with the oxide semiconductor layers 233 and 235. In this embodiment, a silicon oxide film is formed to a thickness of 200 nm by a sputtering method as the oxide insulating layer 5 216.

[0288]

Next, second heat treatment (preferably higher than or equal to 200 °C and lower than or equal to 400 °C, for example, higher than or equal to 250 °C and lower than or equal to 350 °C) is performed in an inert gas atmosphere or an oxygen gas 10 atmosphere. For example, the second heat treatment is performed in a nitrogen atmosphere at 250 °C for one hour. In the second heat treatment, parts of the oxide semiconductor layers (channel formation regions) are heated while in contact with the oxide insulating layer 216.

[0289]

15 Through the above steps, the oxide semiconductor layers 233 and 235 are placed in an oxygen-deficient state and are decreased in resistance by the heat treatment for dehydration or dehydrogenation; then, parts of the oxide semiconductor layers 233 and 235 are selectively placed in an oxygen-excess state. As a result, a channel formation region 213 overlapping with the gate electrode layer 211 becomes i-type and 20 a high-resistance source region 214a overlapping with the source electrode layer 215a and a high-resistance drain region 214b overlapping with the drain electrode layer 215b are formed in a self-aligned manner. Through the above steps, the thin film transistor 210 is formed. In a similar manner, a channel formation region 223 overlapping with the gate electrode layer 221 becomes i-type and a high-resistance source region 224a 25 overlapping with the source electrode layer 225a and a high-resistance drain region 224b overlapping with the drain electrode layer 225b are formed in a self-aligned manner. Through the above steps, the thin film transistor 220 is formed.

[0290]

Further, heat treatment may be performed at a temperature higher than or equal 30 to 100 °C and lower than or equal to 200 °C for greater than or equal to one hour and less than or equal to 30 hours in the air. In this embodiment, the heat treatment is

performed at 150 °C for 10 hours. This heat treatment may be performed at a fixed heating temperature. Alternatively, the following temperature cycle may be applied plural times repeatedly: the temperature is increased from a room temperature to a temperature higher than or equal to 100 °C and lower than or equal to 200 °C and then decreased to a room temperature. Further, this heat treatment may be performed under a reduced pressure before formation of the oxide insulating layer 216. Under a reduced pressure, the heating time can be shortened. With such heat treatment, hydrogen is introduced from the oxide semiconductor layers 233 and 235 to the oxide insulating layer 216; thus, normally-off thin film transistors can be obtained. Therefore, reliability of the semiconductor device can be improved.

[0291]

A protective insulating layer 203 is formed over the oxide insulating layer 216. In this embodiment, the protective insulating layer 203 is formed using a silicon nitride film (see FIG. 8D).

[0292]

A planarization insulating layer for planarization may be provided over the protective insulating layer 203. In this embodiment, a planarization insulating layer 204 is formed over the protective insulating layer 203.

[0293]

Next, a third photolithography step is performed. A resist mask is formed and selective etching is performed to remove parts of the planarization insulating layer 204, the protective insulating layer 203, and the oxide insulating layer 216, so that an opening reaching the drain electrode layer 225b is formed.

[0294]

Next, a light-transmitting conductive film is formed, and a fourth photolithography step is performed. A resist mask is formed and an unnecessary portion is removed by etching, whereby a pixel electrode layer 227 and a conductive layer 217 are formed. Then, the resist mask is removed (see FIG. 8E).

[0295]

In this embodiment, the step of forming the opening in the gate insulating layer is not illustrated in a drawing; however, the step of forming an opening in the gate

insulating layer may be performed in either the same photolithography step as that of the oxide insulating layer and the protective insulating layer or another photolithography step. When the opening is formed in another photolithography step, the number of photolithography steps is four.

5 [0296]

This embodiment can be implemented in appropriate combination with any of the other embodiments.

[0297]

As described above, a semiconductor device which includes a thin film
10 transistor formed using an oxide semiconductor layer and consumes less power can be provided.

[0298]

Further, a semiconductor device which includes a thin film transistor formed using an oxide semiconductor layer and has high reliability can be provided.

15 [0299]

[Embodiment 8]

In this embodiment, an example of a thin film transistor which is applicable to the semiconductor device disclosed in this specification is described. Thin film transistors 270 and 280 which are described in this embodiment can be used as the
20 driver circuit thin film transistor 1223 and the pixel thin film transistor 1211 in Embodiment 1, and the thin film transistor 320 in Embodiment 2.

[0300]

This embodiment describes an example in which a gate electrode layer, a source electrode layer, and a drain electrode layer are formed using a light-transmitting
25 conductive material with reference to FIG. 7. Except the gate electrode layer, the source electrode layer, and the drain electrode layer, this embodiment can be implemented in a manner similar to those in the above embodiments; accordingly, repetitive description of the same portions as those of the above embodiments or portions having functions similar to those of the above embodiments and repetitive
30 description of steps similar to those of the above embodiments are omitted.

[0301]

The thin film transistors 270 and 280 illustrated in FIG. 7 are channel-etched

thin film transistors and include, over a substrate 250 having an insulating surface, gate electrode layers 271 and 281; a gate insulating layer 252; an oxide semiconductor layer 272 including at least a channel formation region 273, a high-resistance source region 274a, and a high-resistance drain region 274b; an oxide semiconductor layer 282 including at least a channel formation region 283, a high-resistance source region 284a, and a high-resistance drain region 284b; and source and drain electrode layers 275a, 275b, 285a, and 285b. In addition, an oxide insulating layer 256 is provided so as to cover the thin film transistors 270 and 280 and be in contact with the channel formation regions 273 and 283. Moreover, a protective insulating layer 253 and a planarization insulating layer 254 are formed over the oxide insulating layer 256.

[0302]

In a pixel portion, an opening (contact hole) reaching the source or drain electrode layer 285b is formed so as to penetrate the oxide insulating layer 256, the protective insulating layer 253, and the planarization insulating layer 254, and a pixel electrode layer 287 is formed in and over the opening. On the other hand, in a driver circuit portion, a conductive layer 277 is formed over the planarization insulating layer 254 so as to overlap with the gate electrode layer 271 and the oxide semiconductor layer 272.

[0303]

The source and drain electrode layers 275a, 275b, 285a, and 285b are formed using a thin metal conductive film and thus can have light-transmitting properties.

[0304]

In FIG. 7, light-transmitting conductive films are used for the gate electrode layers 271 and 281 and the source and drain electrode layers 275a, 275b, 285a, and 285b of the thin film transistors 270 and 280.

[0305]

As materials of the gate electrode layers 271 and 281 and the source and drain electrode layers 275a, 275b, 285a, and 285b, any of the following conductive materials which transmit visible light can be used: for example, an In-Sn-O-based metal oxide, an In-Sn-Zn-O-based metal oxide, an In-Al-Zn-O-based metal oxide, a Sn-Ga-Zn-O-based metal oxide, an Al-Ga-Zn-O-based metal oxide, a Sn-Al-Zn-O-based metal oxide, an In-Zn-O-based metal oxide, a Sn-Zn-O-based metal oxide, an Al-Zn-O-based metal

oxide, an In-O-based metal oxide, a Sn-O-based metal oxide, and a Zn-O-based metal oxide. The thicknesses of the gate electrode layers 271 and 281 and the source and drain electrode layers 275a, 275b, 285a, and 285b are set as appropriate in the range greater than or equal to 50 nm and less than or equal to 300 nm. As a deposition
5 method of the light-transmitting conductive materials used for the gate electrode layers 271 and 281 and the source and drain electrode layers 275a, 275b, 285a, and 285b, a sputtering method, a vacuum evaporation method (such as an electron beam evaporation method), an arc discharge ion plating method, or a spray method is used. When a sputtering method is used, it is preferable that a target containing SiO_2 at greater than or
10 equal to 2 wt% and less than or equal to 10 wt% is used for deposition and the light-transmitting conductive films are made to contain SiO_x ($x > 0$) which suppresses crystallization, so that crystallization by the heat treatment for dehydration or dehydrogenation performed in a later step is prevented.

[0306]

15 Thus, the thin film transistors 270 and 280 can be light-transmitting thin film transistors.

[0307]

In the pixel provided with the thin film transistor 280, a conductive film which transmits visible light is used for the pixel electrode layer 287, another electrode layer
20 (such as a capacitor electrode layer), or a wiring layer (such as a capacitor wiring layer), whereby a display device having a high aperture ratio is realized. It is needless to say that the gate insulating layer 252, the oxide insulating layer 256, the protective insulating layer 253, and the planarization insulating layer 254 are each also preferably formed using a film which transmits visible light.

25 [0308]

In this specification, a film which transmits visible light refers to a film with a visible light transmittance of 75 % to 100 % and in the case where the film has a conductive property, it is also referred to as a transparent conductive film. Further, a conductive film which is semi-transparent to visible light may be used for a material
30 used for the gate electrode layer, the source electrode layer, the drain electrode layer, the pixel electrode layer, any other electrode layer, or a wiring layer. Being

semi-transparent to visible light means that a transmittance of visible light is 50 % to 75 %.

[0309]

Since the thin film transistor 280 has a light transmitting property, the aperture ratio can be increased. For small liquid crystal display panels of 10 inches or smaller in particular, a high aperture ratio can be achieved even when the size of pixels is decreased in order to realize higher resolution of display images by increasing the number of gate wirings, for example. Moreover, wide viewing angle is realized by using a light-transmitting film for components in the thin film transistor 280, so that a high aperture ratio can be achieved even when one pixel is divided into a plurality of subpixels. That is, high aperture ratio can be maintained even when thin film transistors are densely arranged, and the display region can have a sufficient area. For example, even when one pixel includes two to four subpixels, the aperture ratio can be increased because the thin film transistor has a light transmitting property. When a storage capacitor is formed using the same steps and the same materials as those of the thin film transistor, the storage capacitor can also have a light-transmitting property; therefore, the aperture ratio can be further increased.

[0310]

This embodiment can be implemented in appropriate combination with any of the other embodiments.

[0311]

[Embodiment 9]

In this embodiment, a liquid crystal display device is described as an example of a semiconductor device disclosed in this specification.

[0312]

There is no particular limitation on the semiconductor device disclosed in this specification, and a liquid crystal display device including a TN liquid crystal, an OCB liquid crystal, an STN liquid crystal, a VA liquid crystal, an ECB liquid crystal, a GH liquid crystal, a polymer dispersed liquid crystal, a discotic liquid crystal, or the like can be used. Among them, a normally black liquid crystal panel such as a transmissive liquid crystal display device utilizing a vertical alignment (VA) mode is preferable.

Some examples are given as a vertical alignment mode. For example, a multi-domain vertical alignment (MVA) mode, a patterned vertical alignment (PVA) mode, an ASV mode, or the like can be employed.

[0313]

5 An example of a VA liquid crystal display device is described below.

[0314]

A vertical alignment (VA) is a mode for controlling alignment of liquid crystal molecules of a liquid crystal display panel. In the VA liquid crystal display device, liquid crystal molecules are aligned in a vertical direction with respect to a panel surface 10 when no voltage is applied. In this embodiment, in particular, a pixel is divided into some regions (subpixels), and liquid crystal molecules are aligned in different directions in their respective regions. This is referred to as multi-domain or multi-domain design. Liquid crystal display devices of the multi-domain design are described below.

[0315]

15 FIG. 10 and FIG. 11 illustrate a pixel structure of a VA liquid crystal display panel formed on a substrate 600. FIG. 11 is a top view of the substrate 600. FIG. 10 is a view of a cross-sectional structure taken along section line Y-Z in FIG. 11. The following description is made with reference to these views.

[0316]

20 In this pixel structure, a plurality of pixel electrode layers are provided in one pixel, and a TFT is connected to each of the pixel electrode layers. The plurality of TFTs are driven by different gate signals. In other words, signals applied to individual pixel electrode layers in a multi-domain pixel are controlled independently.

[0317]

25 A pixel electrode layer 624 is connected to a source or drain electrode layer 618 of a TFT 628 through a contact hole 623. A pixel electrode layer 626 is connected to a source or drain electrode layer 619 of a TFT 629 through a contact hole 627 penetrating an insulating layer 620, an insulating layer 621 covering the insulating layer 620, and an insulating layer 622 covering the insulating layer 621. A gate wiring 602 of the TFT 30 628 is separated from a gate wiring 603 of the TFT 629 so that different gate signals can be supplied. On the other hand, a source or drain electrode layer 616 serving as a data line is shared by the TFTs 628 and 629. The thin film transistor described in any of

Embodiments 3 to 8 can be used as appropriate as each of the TFTs 628 and 629.

[0318]

Further, a storage capacitor is formed using a capacitor wiring 690, a gate insulating layer 606 as a dielectric, and a pixel electrode layer or a capacitor electrode electrically connected to the pixel electrode layer.

[0319]

The shape of the pixel electrode layer 624 is different from that of the pixel electrode layer 626, and the pixel electrode layer 624 and the pixel electrode layer 626 are separated from each other by a slit. The pixel electrode layer 626 is formed so as to surround the external side of the pixel electrode layer 624 which spreads into a V shape. The timings at which voltages are applied to the pixel electrode layers 624 and 626 are made to be different in TFTs 628 and 629, whereby alignment of liquid crystals is controlled. FIG. 13 illustrates an equivalent circuit of this pixel structure. The TFT 628 is connected to the gate wiring 602, and the TFT 629 is connected to the gate wiring 603. When different gate signals are supplied to the gate wirings 602 and 603, the timings of the operations of the TFTs 628 and 629 can vary.

[0320]

A counter substrate 601 is provided with a light-blocking film 632, a coloring film 636, and a counter electrode layer 640. A planarization film 637 which is also called an overcoat film is formed between the coloring film 636 and the counter electrode layer 640 to prevent alignment disorder of the liquid crystals. An alignment film 648 is formed over the pixel electrode layers 624 and 626, and an alignment film 646 is formed on the counter electrode layer 640. FIG. 12 illustrates a structure on the counter substrate side. The counter electrode layer 640 is an electrode shared by different pixels and slits 641 are formed. The slits 641 and the slits on the pixel electrode layers 624 and 626 side are alternately arranged in an engaging manner so that an oblique electric field is effectively generated, whereby the alignment of the liquid crystals can be controlled. Accordingly, the direction of the alignment of the liquid crystals can vary dependent on the location, which leads to a wider viewing angle.

[0321]

The counter electrode layer 640 having a pattern with an opening is a first counter electrode layer provided in a pixel portion and has a potential different from that

of a second counter electrode layer provided in a driver circuit portion. By providing the second counter electrode layer over the driver circuit portion, highly reliable semiconductor device with an improved resistance to static electricity can be formed.

[0322]

5 The pixel electrode layer 624, a liquid crystal layer 650, and the counter electrode layer 640 overlap with one another to form a first liquid crystal element. The pixel electrode layer 626, the liquid crystal layer 650, and the counter electrode layer 640 overlap with one another to form a second liquid crystal element. The pixel structure is a multi-domain structure in which the first liquid crystal element and the 10 second liquid crystal element are provided in one pixel.

[0323]

This embodiment can be implemented in appropriate combination with any of the other embodiments.

[0324]

15 [Embodiment 10]

A semiconductor device disclosed in this specification can be applied to a variety of electronic appliances (including game machines). Examples of such electronic devices are a television set (also referred to as a television or a television receiver), a monitor of a computer or the like, a camera such as a digital camera or a 20 digital video camera, a digital photo frame, a mobile phone handset (also referred to as a mobile phone or a mobile phone device), a portable game machine, a portable information terminal, an audio reproducing device, a large-sized game machine such as a pachinko machine, and the like.

[0325]

25 In this embodiment, examples of an electronic appliance on which a liquid crystal display device obtained in any one of Embodiments 1 to 9 is mounted are described with reference to FIGS. 14A to 14E.

[0326]

FIG. 14A illustrates a laptop personal computer which is manufactured by 30 mounting at least a liquid crystal display device as a component and which includes a main body 3001, a housing 3002, a display portion 3003, a keyboard 3004, and the like. Note that this laptop personal computer includes the liquid crystal display device

described in Embodiment 1.

[0327]

FIG. 14B illustrates a portable information terminal device (which is also referred to as a personal digital assistant (PDA)) which is manufactured by mounting at least a liquid crystal display device as a component. A main body 3021 is provided with a display portion 3023, an outside interface 3025, an operation button 3024, and the like. In addition, the portable information terminal device has a stylus 3022 as an accessory for operation. Note that this portable information terminal device includes the liquid crystal display device described in Embodiment 1.

[0328]

FIG. 14C illustrates an e-book reader manufactured by mounting at least a liquid crystal display device as a component. For example, an e-book reader 2700 includes two housings, a housing 2701 and a housing 2703. The housing 2701 and the housing 2703 are combined with a hinge 2711 so that the e-book reader 2700 can be opened and closed with the hinge 2711 as an axis. With such a structure, the e-book reader 2700 can operate like a paper book.

[0329]

A display portion 2705 and a display portion 2707 are incorporated in the housing 2701 and the housing 2703, respectively. The display portion 2705 and the display portion 2707 may display one image or different images. In the structure where different images are displayed on different display portions, for example, the right display portion (the display portion 2705 in FIG. 14C) displays text and the left display portion (the display portion 2707 in FIG. 14C) displays images.

[0330]

FIG. 14C illustrates an example in which the housing 2701 is provided with an operation portion and the like. For example, the housing 2701 is provided with a power switch 2721, an operation key 2723, a speaker 2725, and the like. With the operation key 2723, pages can be turned. Note that a keyboard, a pointing device, or the like may also be provided on the surface of the housing, on which the display portion is provided. Furthermore, an external connection terminal (an earphone terminal, a USB terminal, a terminal that can be connected to various cables such as an AC adapter and a USB cable, or the like), a recording medium insertion portion, and the

like may be provided on the back surface or the side surface of the housing. Moreover, the e-book reader 2700 may have a function of an electronic dictionary.

[0331]

The e-book reader 2700 may have a configuration capable of wirelessly transmitting and receiving data. Through wireless communication, desired book data or the like can be purchased and downloaded from an electronic book server. Note that the e-book reader 2700 includes the liquid crystal display device described in Embodiment 1.

[0332]

FIG. 14D illustrates a mobile phone which is manufactured by mounting at least a liquid crystal display device as a component and which includes two housings, a housing 2800 and a housing 2801. The housing 2801 includes a display panel 2802, a speaker 2803, a microphone 2804, a pointing device 2806, a camera lens 2807, an external connection terminal 2808, and the like. The housing 2800 includes a solar cell 2810 for charging the mobile phone, an external memory slot 2811, and the like. Further, an antenna is incorporated in the housing 2801.

[0333]

Further, the display panel 2802 is provided with a touch panel. A plurality of operation keys 2805 which is displayed as images is illustrated by dashed lines in FIG. 14D. Note that a boosting circuit by which a voltage output from the solar cell 2810 is increased to be sufficiently high for each circuit is also included.

[0334]

In the display panel 2802, the direction of display is changed appropriately depending on an application mode. Further, the mobile phone is provided with the camera lens 2807 on the same surface as the display panel 2802, and thus can be used as a video phone. The speaker 2803 and the microphone 2804 can be used for videophone, recording, playback, and the like without being limited to verbal communication. Moreover, the housings 2800 and 2801 in a state where they are developed as illustrated in FIG. 14D can shift so that one is lapped over the other by sliding; therefore, the size of the portable information terminal can be reduced, which makes the mobile phone suitable for being carried.

[0335]

The external connection terminal 2808 can be connected to an AC adapter and various types of cables such as a USB cable, and charging and data communication with a personal computer are possible. Moreover, a large amount of data can be stored by inserting a storage medium into the external memory slot 2811 and can be moved.

5 [0336]

Further, in addition to the above functions, an infrared communication function, a television reception function, or the like may be provided. Note that this mobile phone includes the liquid crystal display device described in Embodiment 1.

[0337]

10 FIG. 14E illustrates a digital camera which is manufactured by mounting at least a liquid crystal display device as a component and which includes a main body 3051, a display portion (A) 3057, an eyepiece 3053, an operation switch 3054, a display portion (B) 3055, a battery 3056, and the like. Note that this digital camera includes the liquid crystal display device described in Embodiment 1.

15 [0338]

This embodiment can be combined with any of Embodiments 1 to 9.

This application is based on Japanese Patent Application serial no. 2009-250909 filed with Japan Patent Office on October 30, 2009, the entire contents of
20 which are hereby incorporated by reference.

CLAIMS

1. A semiconductor device comprising:

a first electrode layer and a second electrode layer over a first substrate;

5 a liquid crystal layer over the first electrode layer and the second electrode layer;

a first counter electrode layer and a second counter electrode layer over the liquid crystal layer; and

a second substrate over the first counter electrode layer and the second counter 10 electrode layer,

wherein the first electrode layer is a pixel electrode formed in a position overlapping with the first counter electrode layer with the liquid crystal layer therebetween; and

wherein the second electrode layer is an electrode layer of a driver circuit 15 formed in a position overlapping with the second counter electrode layer with the liquid crystal layer therebetween.

2. The semiconductor device according to claim 1, wherein a potential of the first counter electrode layer is different from a potential of the second counter electrode 20 layer.

3. The semiconductor device according to claim 1, wherein the first electrode layer is electrically connected to a thin film transistor in a pixel portion.

25 4. The semiconductor device according to claim 1, wherein the second electrode layer is a gate electrode layer of a thin film transistor of the driver circuit.

5. The semiconductor device according to claim 1 further comprising:

a third electrode layer over the first substrate; and

30 a conductive particle between the third electrode layer and the first counter electrode layer,

wherein the third electrode layer is electrically connected to the first counter

electrode layer through the conductive particle.

6. The semiconductor device according to claim 1 further comprising:

a fourth electrode layer over the first substrate; and

5 a conductive particle between the fourth electrode layer and the second counter electrode layer,

wherein the fourth electrode layer is electrically connected to the second counter electrode layer through the conductive particle.

10 7. A semiconductor device comprising:

a first electrode layer, a second electrode layer, a third electrode layer, and a fourth electrode layer over a first substrate;

a liquid crystal layer over the first electrode layer and the second electrode layer;

15 a first counter electrode layer and a second counter electrode layer over the liquid crystal layer; and

a second substrate over the first counter electrode layer and the second counter electrode layer,

wherein the third electrode layer is electrically connected to the first counter

20 electrode layer through a first conductive particle,

wherein the fourth electrode layer is electrically connected to the first counter electrode layer through a second conductive particle,

wherein the first electrode layer is a pixel electrode formed in a position overlapping with the first counter electrode layer with the liquid crystal layer

25 therebetween; and

wherein the second electrode layer is an electrode layer of a driver circuit formed in a position overlapping with the second counter electrode layer with the liquid crystal layer therebetween.

30 8. The semiconductor device according to claim 7, wherein a potential of the first counter electrode layer is different from a potential of the second counter electrode layer.

9. The semiconductor device according to claim 7, wherein the first electrode layer is electrically connected to a thin film transistor in a pixel portion.

5 10. The semiconductor device according to claim 7, wherein the second electrode layer is a gate electrode layer of a thin film transistor of the driver circuit.

11. The semiconductor device according to claim 7 further comprising:

a fifth electrode layer over the first substrate; and

10 a third conductive particle between the fourth electrode layer and the second counter electrode layer,

wherein the fifth electrode layer is electrically connected to the second counter electrode layer through the third conductive particle.

FIG. 1A

1210 1204 1235 1243 E F 1205 1242 1202 1280 1241 1201 H G 1240 1208 1200 1246

FIG. 1B

1204 1295 1270 1291 1205 1241 1208 G 1240 1210 1290 1235 H

FIG. 1C

1204 1295 1292 1293 1207 1255 1291 1280 1205 1243 1242 E 1210 1290 1223 1214 1211 1206 1250 F 1240 1200 1202

FIG. 2A

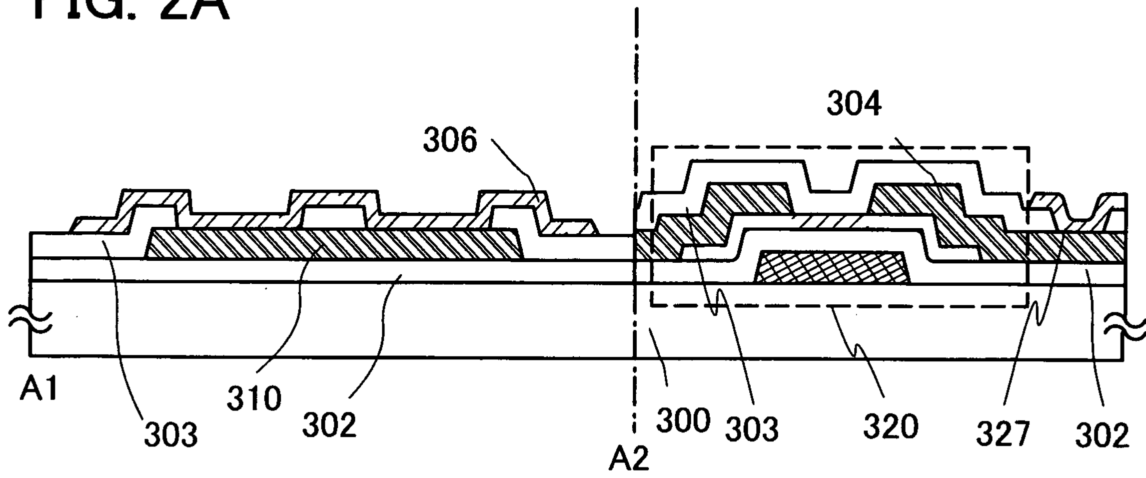


FIG. 2B

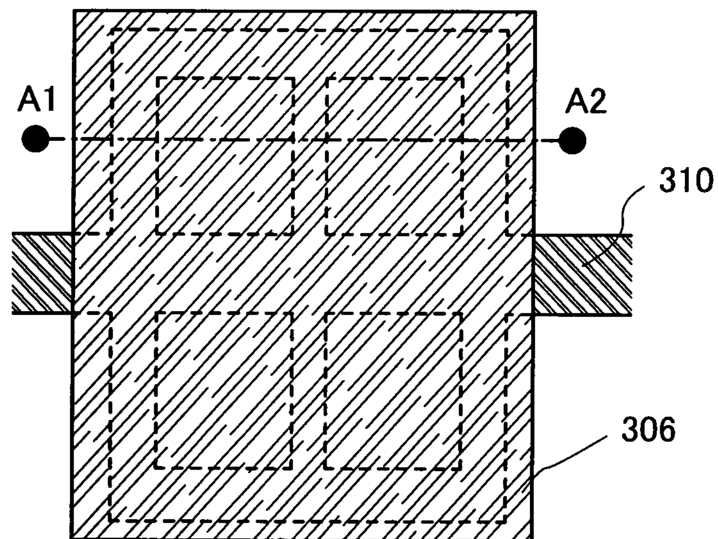


FIG. 3A

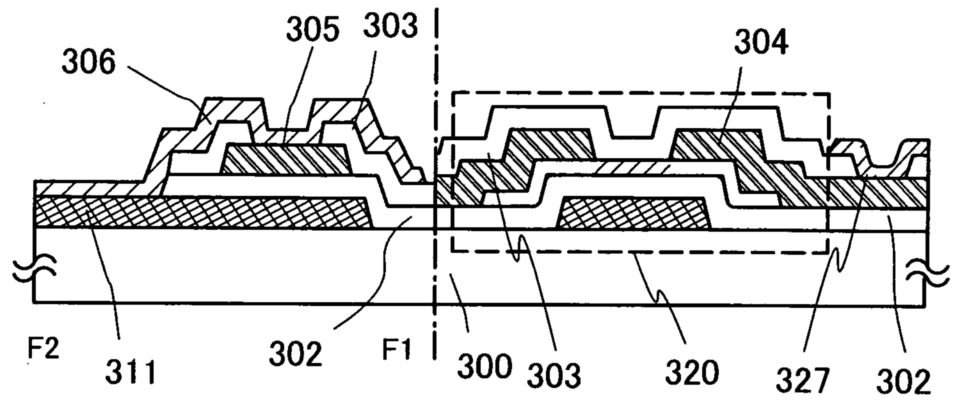


FIG. 3B

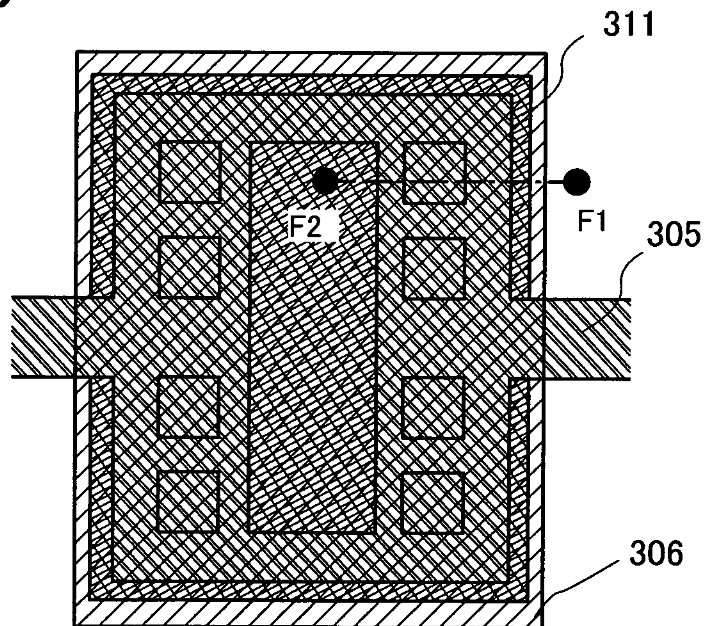


FIG. 4A

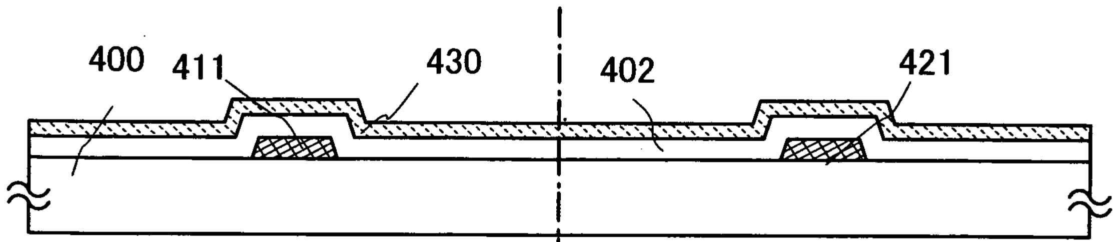


FIG. 4B

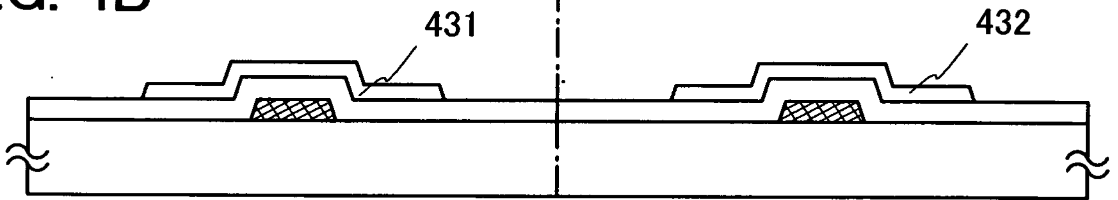


FIG. 4C

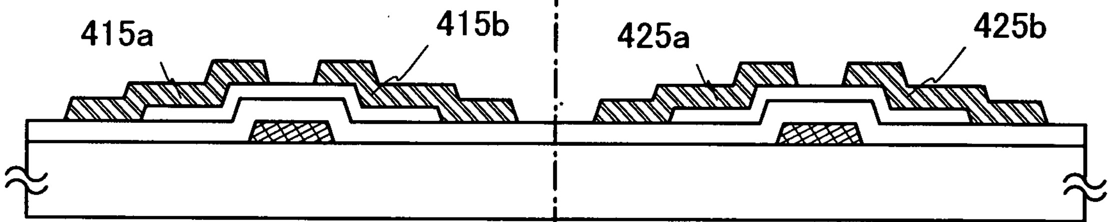


FIG. 4D

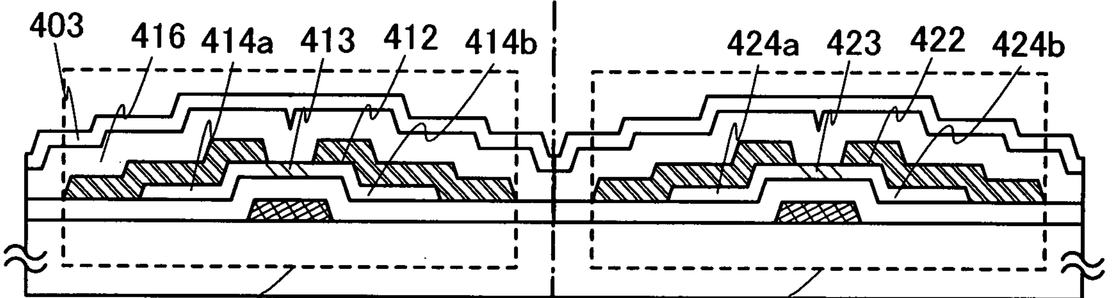


FIG. 4E

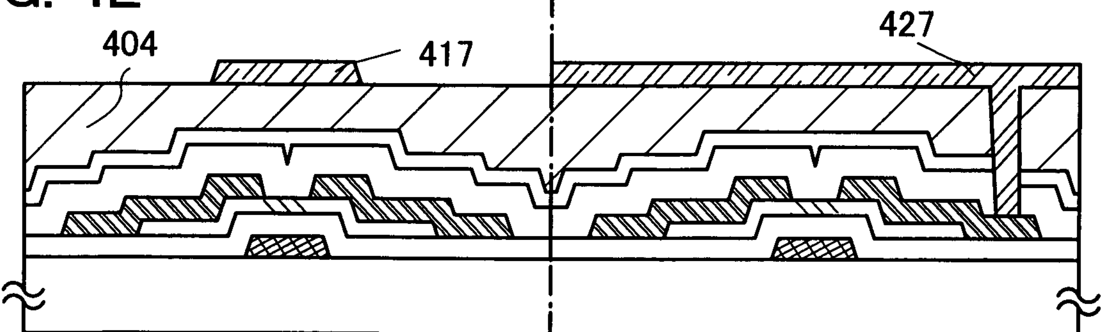


FIG. 5A

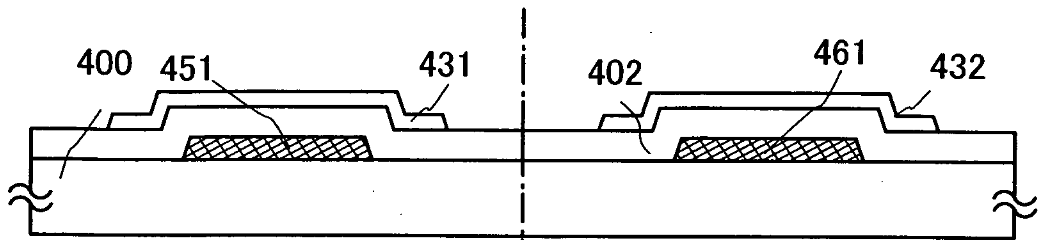


FIG. 5B

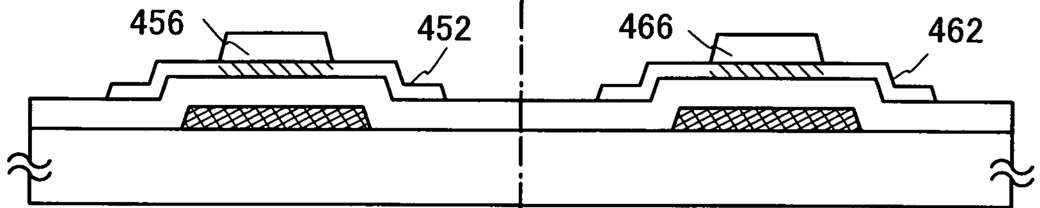


FIG. 5C

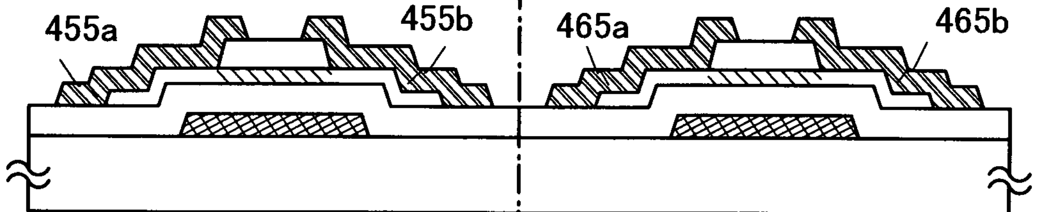


FIG. 5D

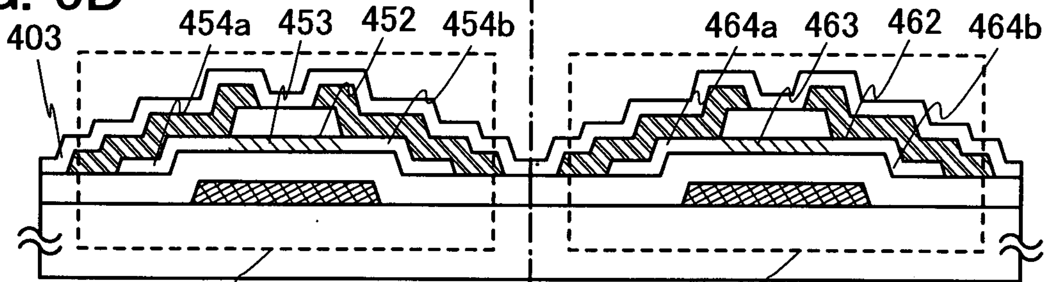


FIG .5E

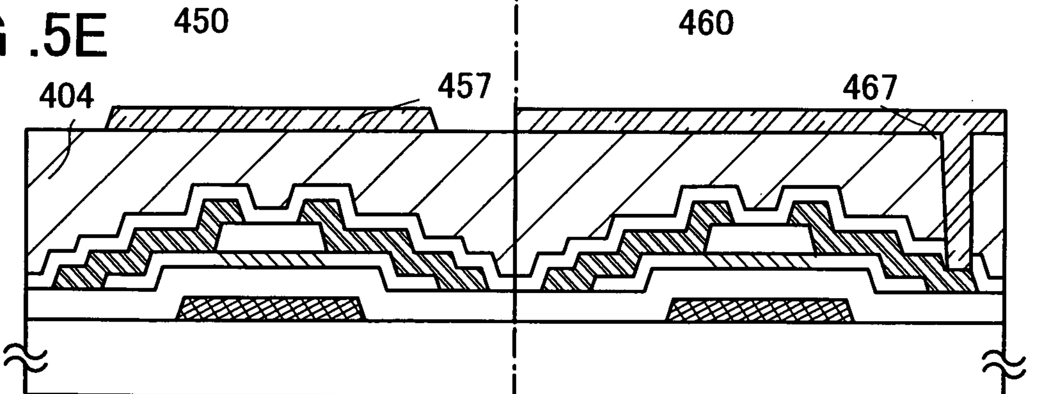


FIG. 6A

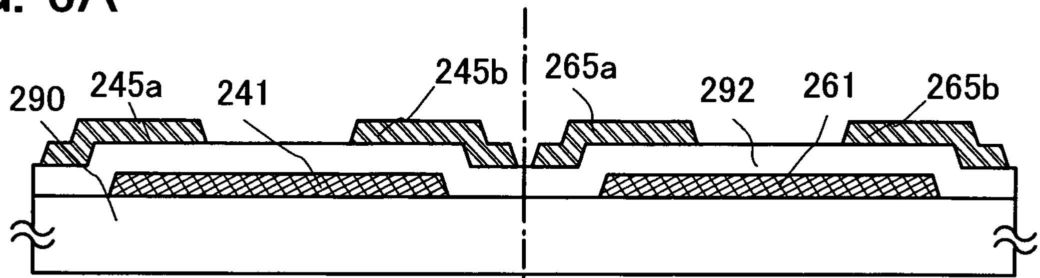


FIG. 6B

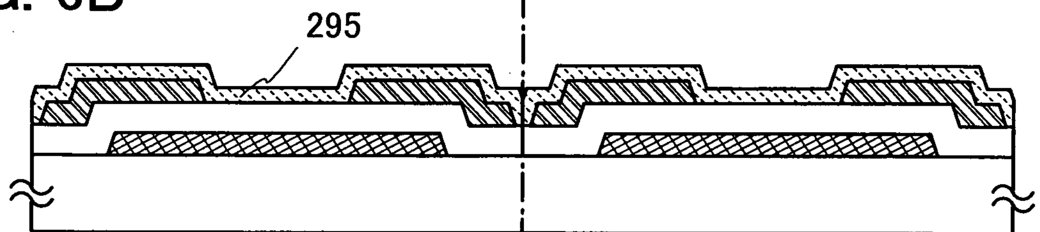


FIG. 6C

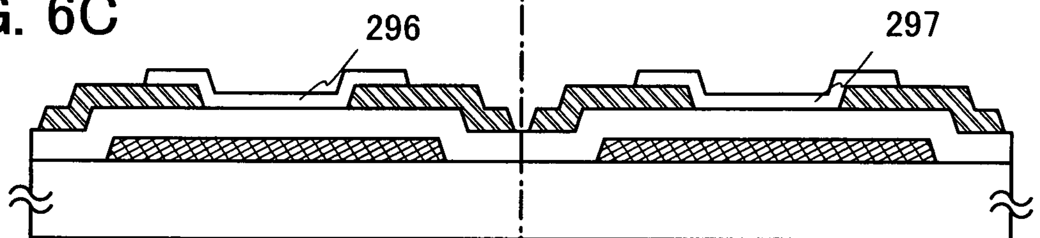


FIG. 6D

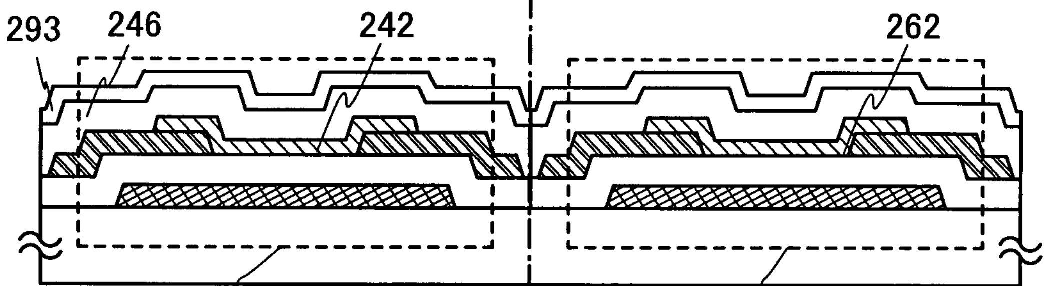


FIG. 6E

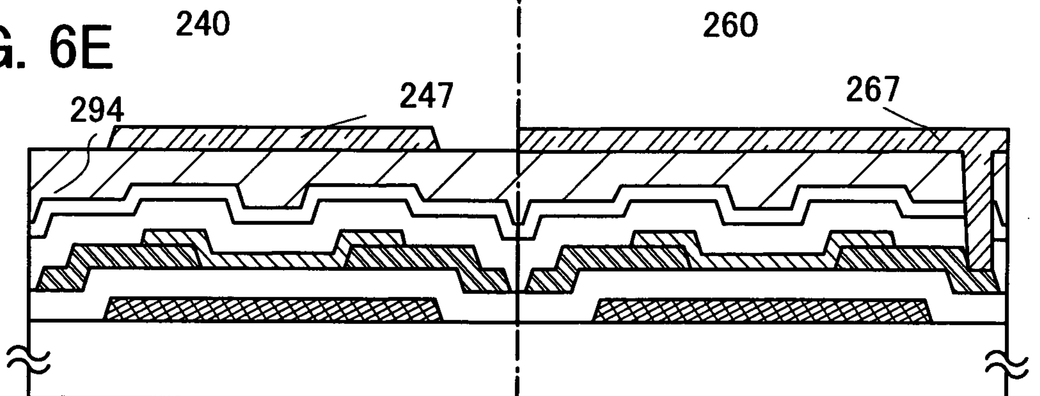


FIG. 7

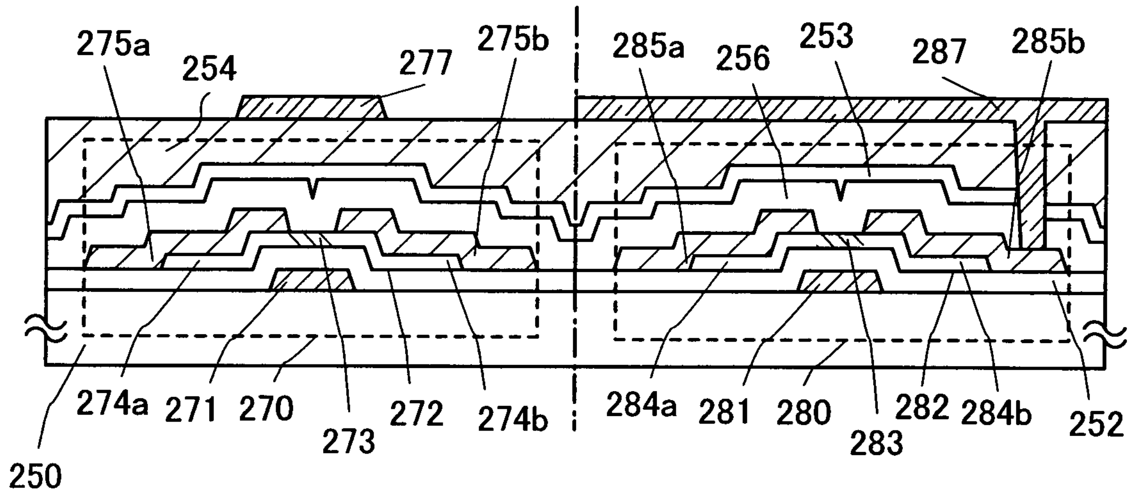


FIG. 8A

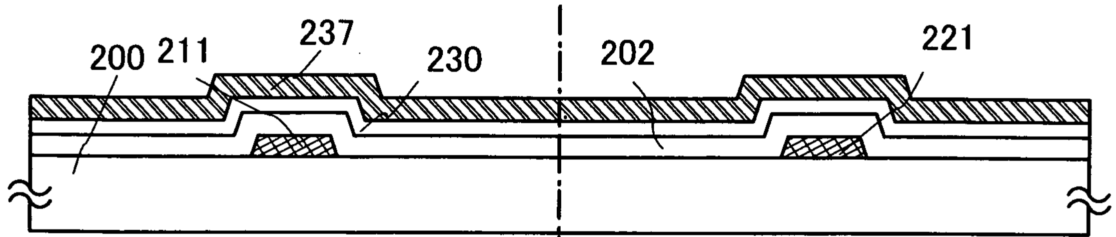


FIG. 8B

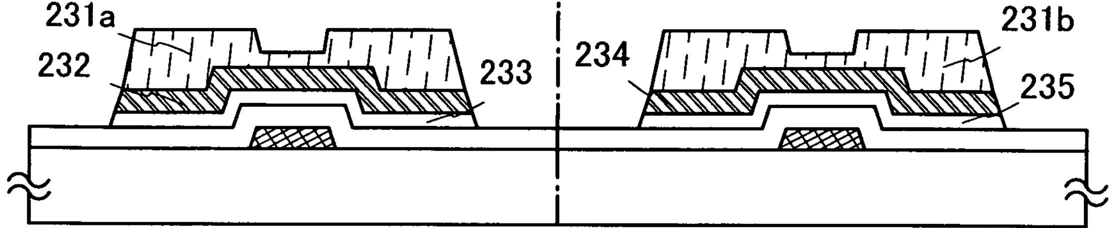


FIG. 8C

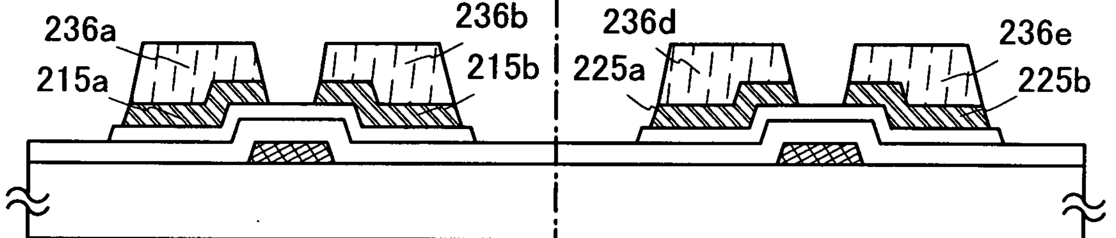


FIG. 8D

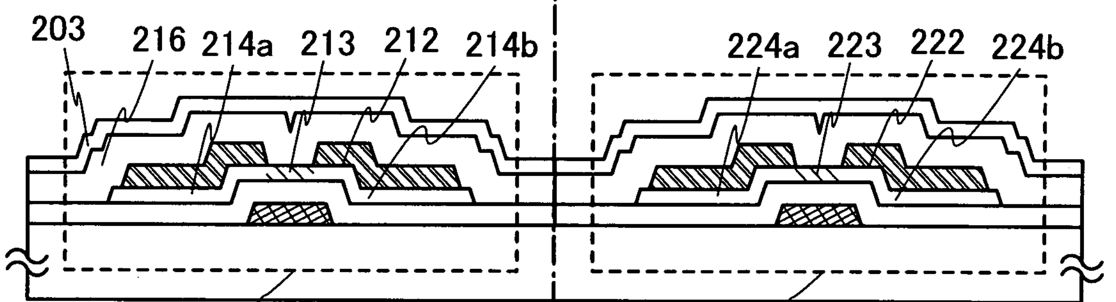


FIG. 8E

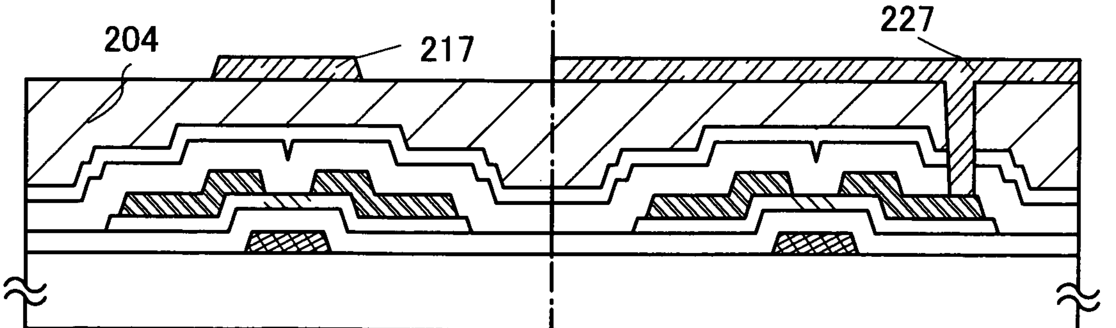


FIG. 9A

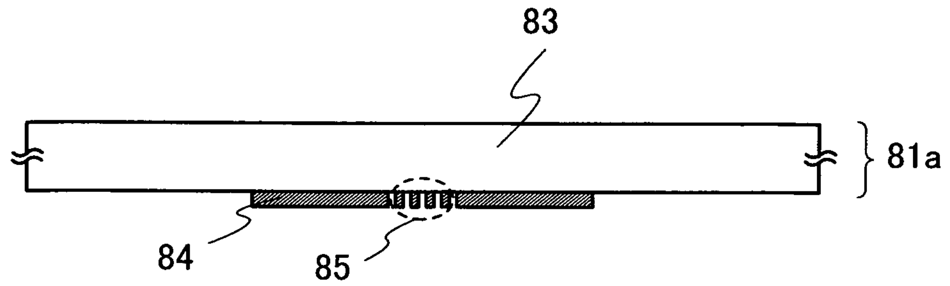


FIG. 9B

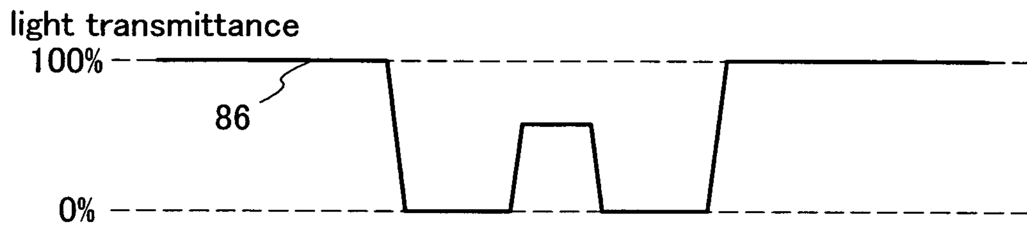


FIG. 9C

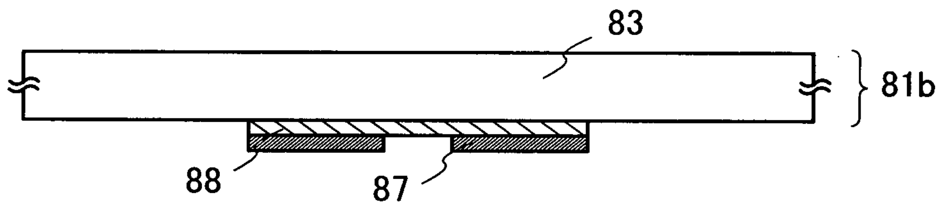
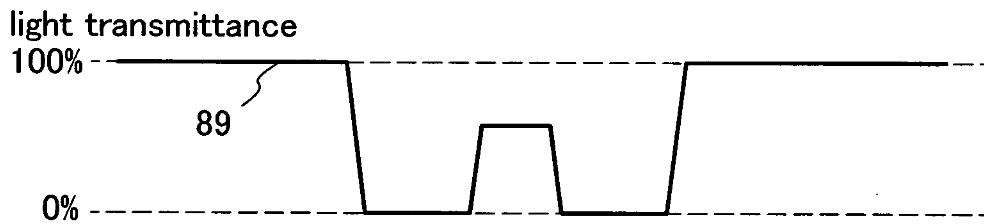


FIG. 9D



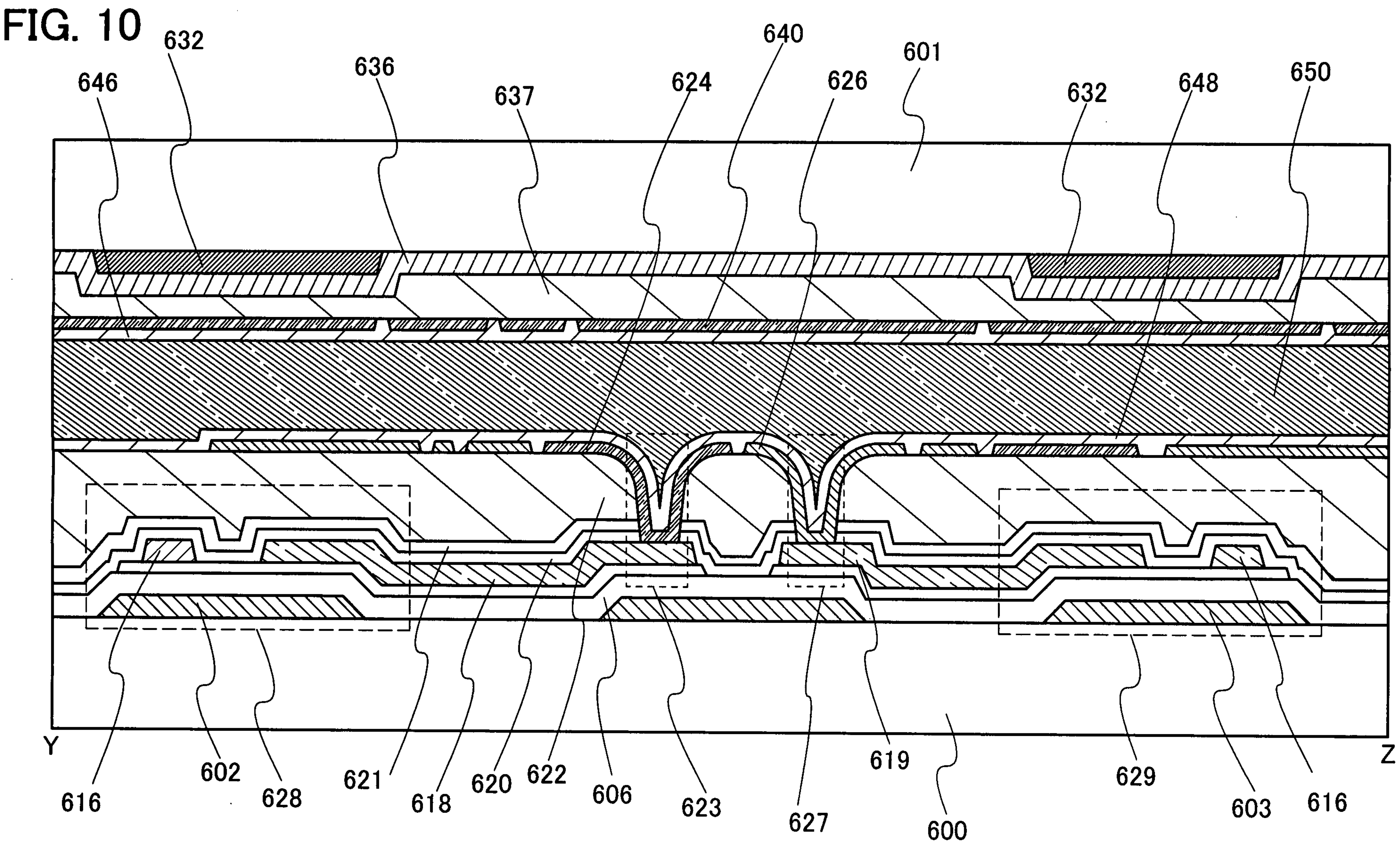


FIG. 10
646
632
636
637
624
640
626
601
632
648
650
Y
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621
618
620
622
606
623
627
619
600
629
603
616
Z

FIG. 11

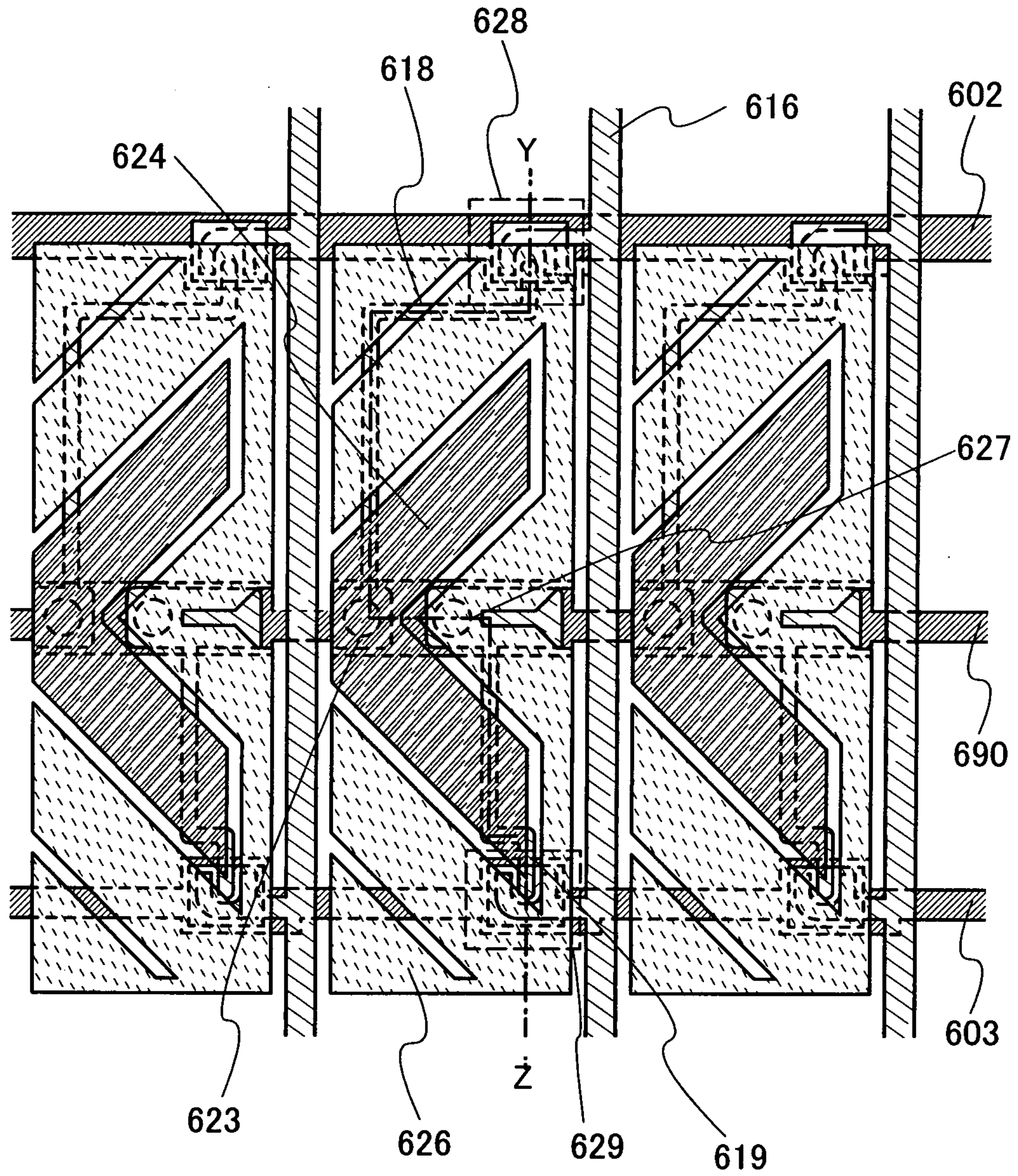


FIG. 12

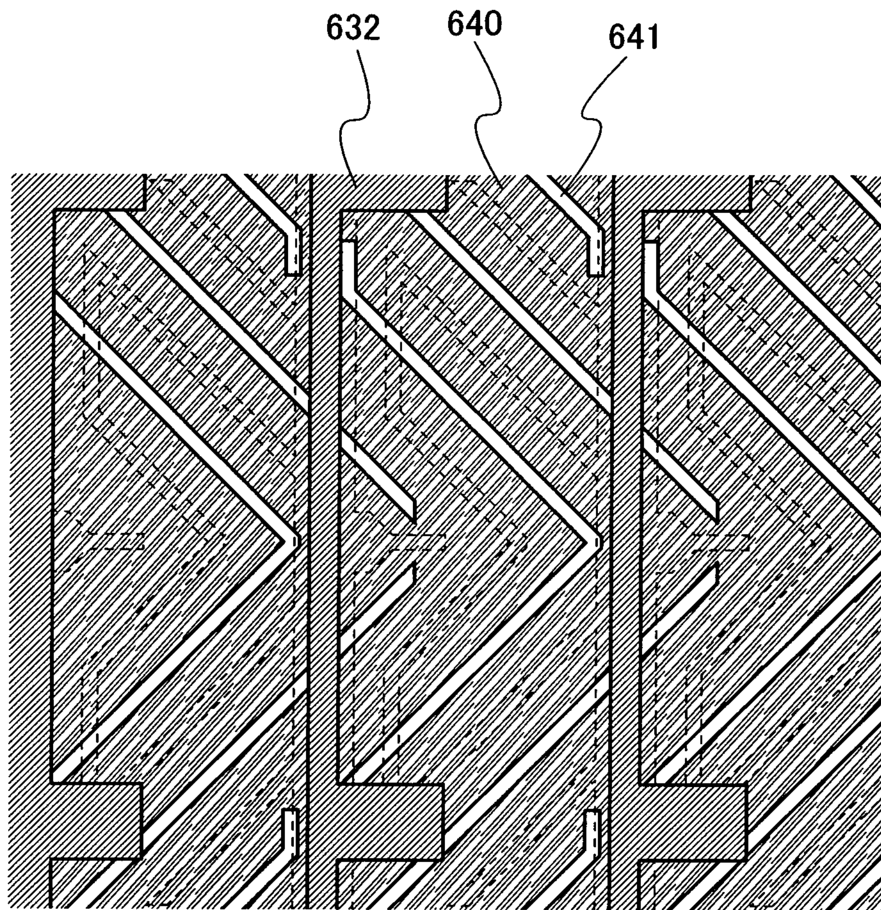


FIG. 13

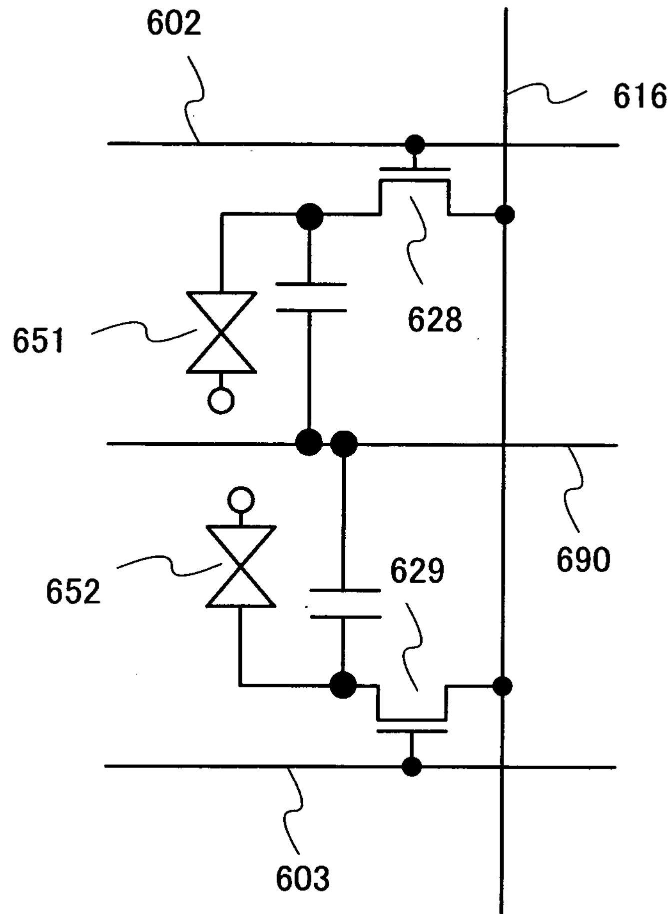


FIG. 14A

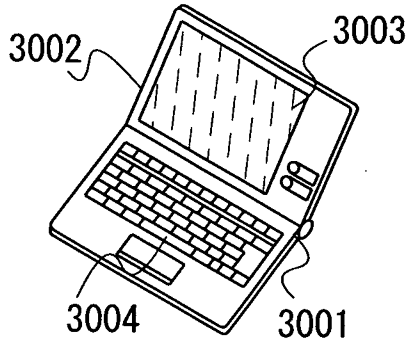


FIG. 14D

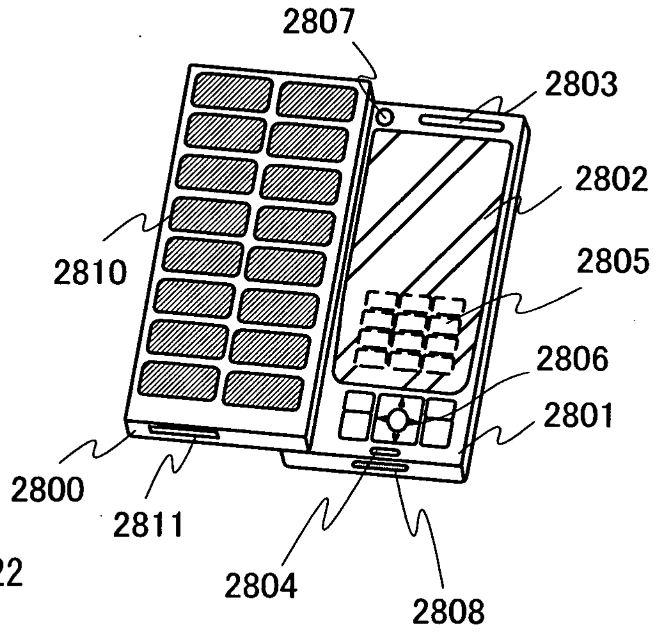


FIG. 14B

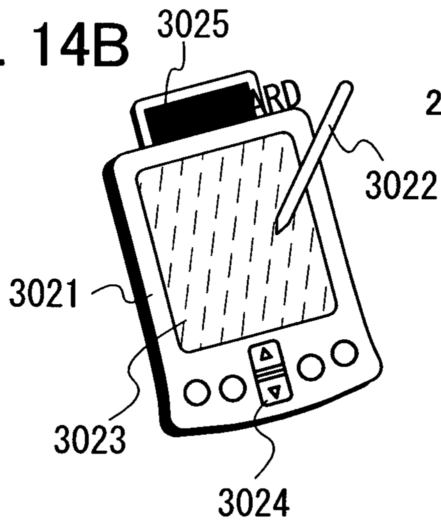


FIG. 14E

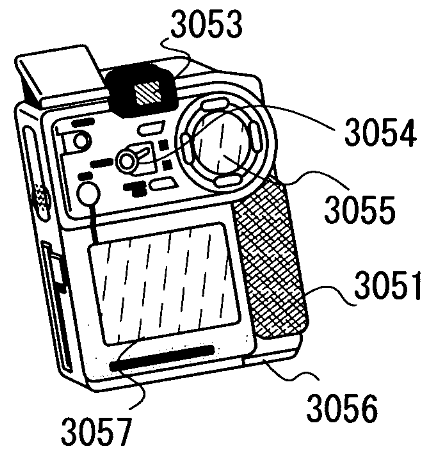


FIG. 14C

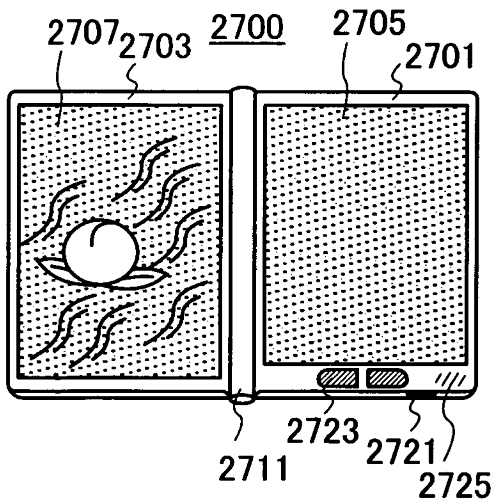


FIG. 15

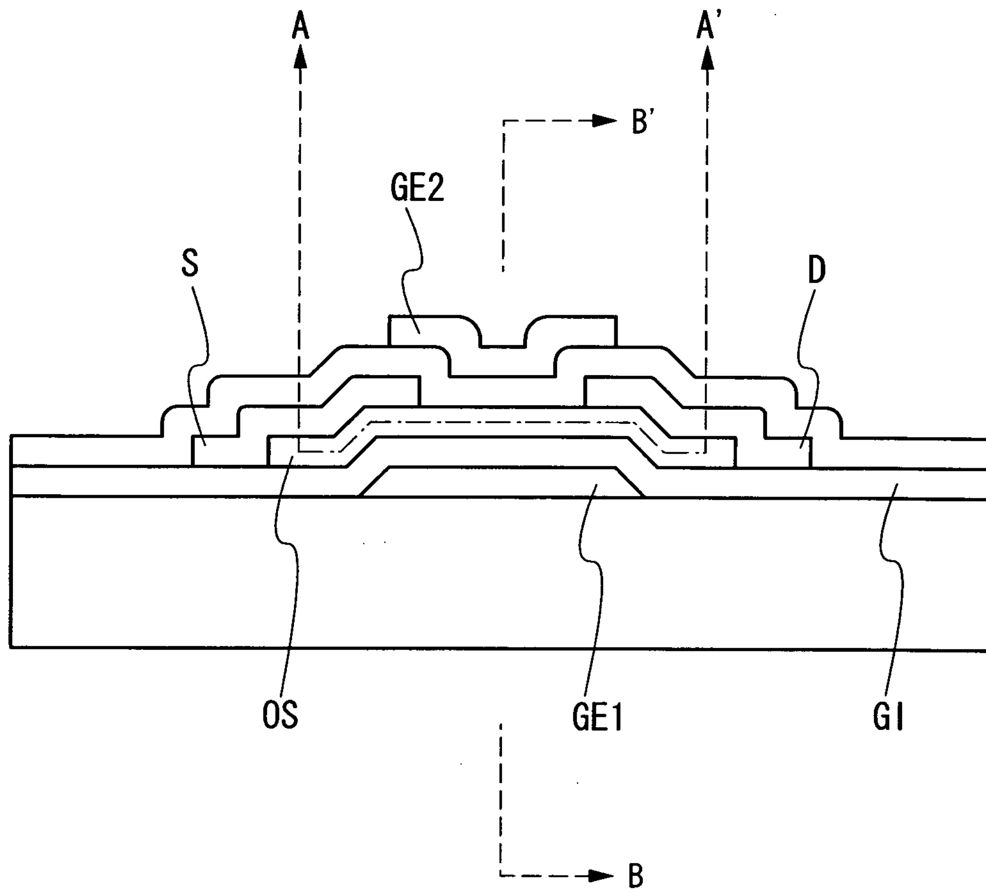


FIG. 16A

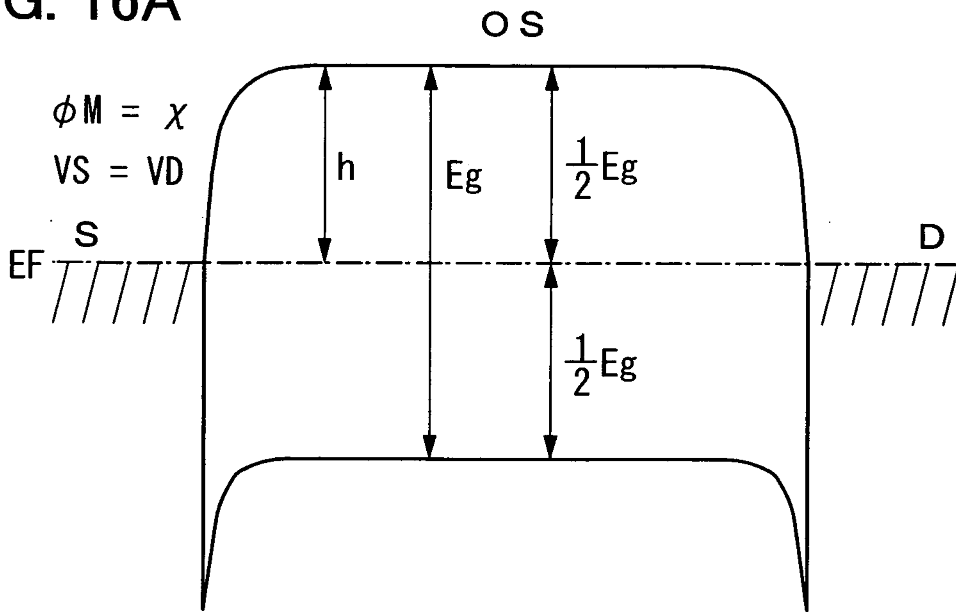


FIG. 16B

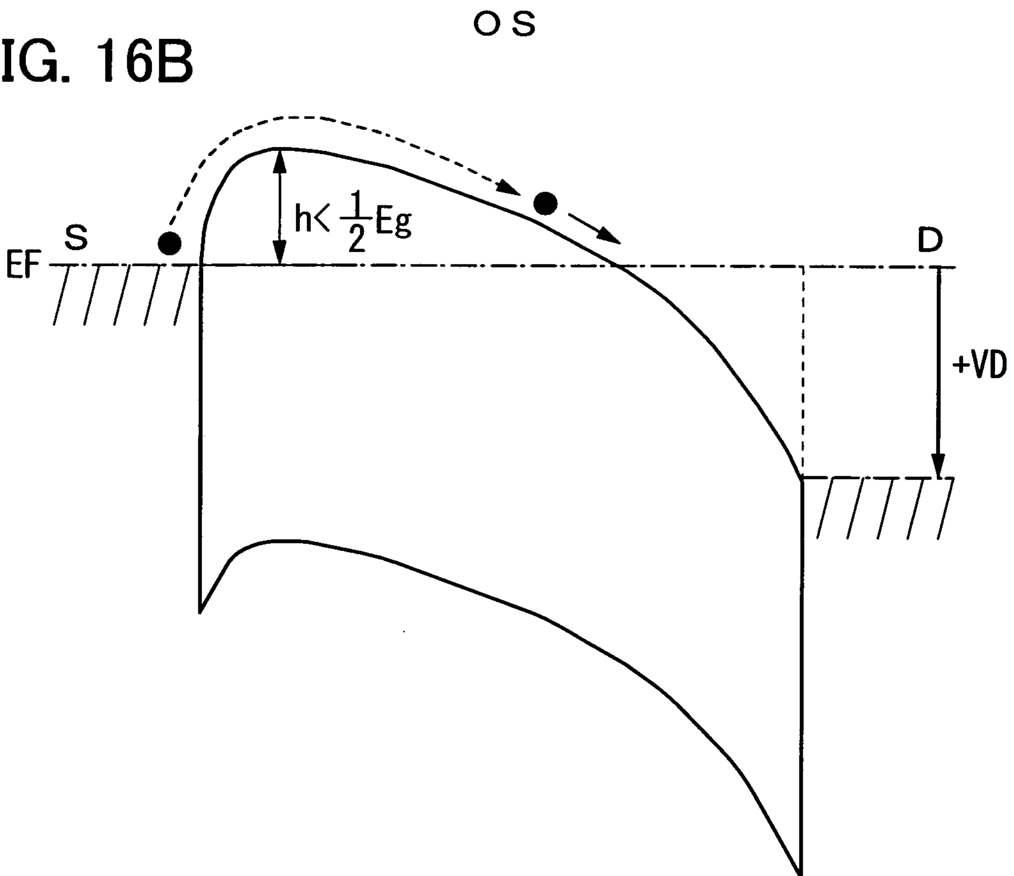


FIG. 17A

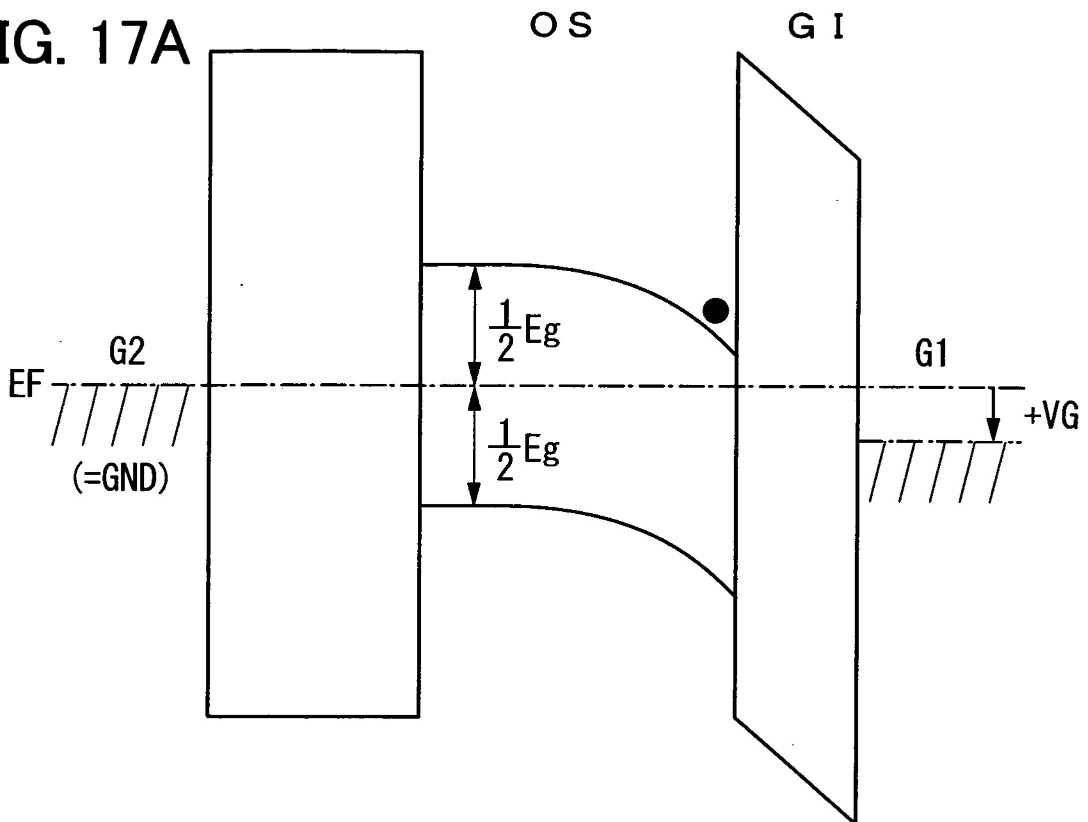


FIG. 17B

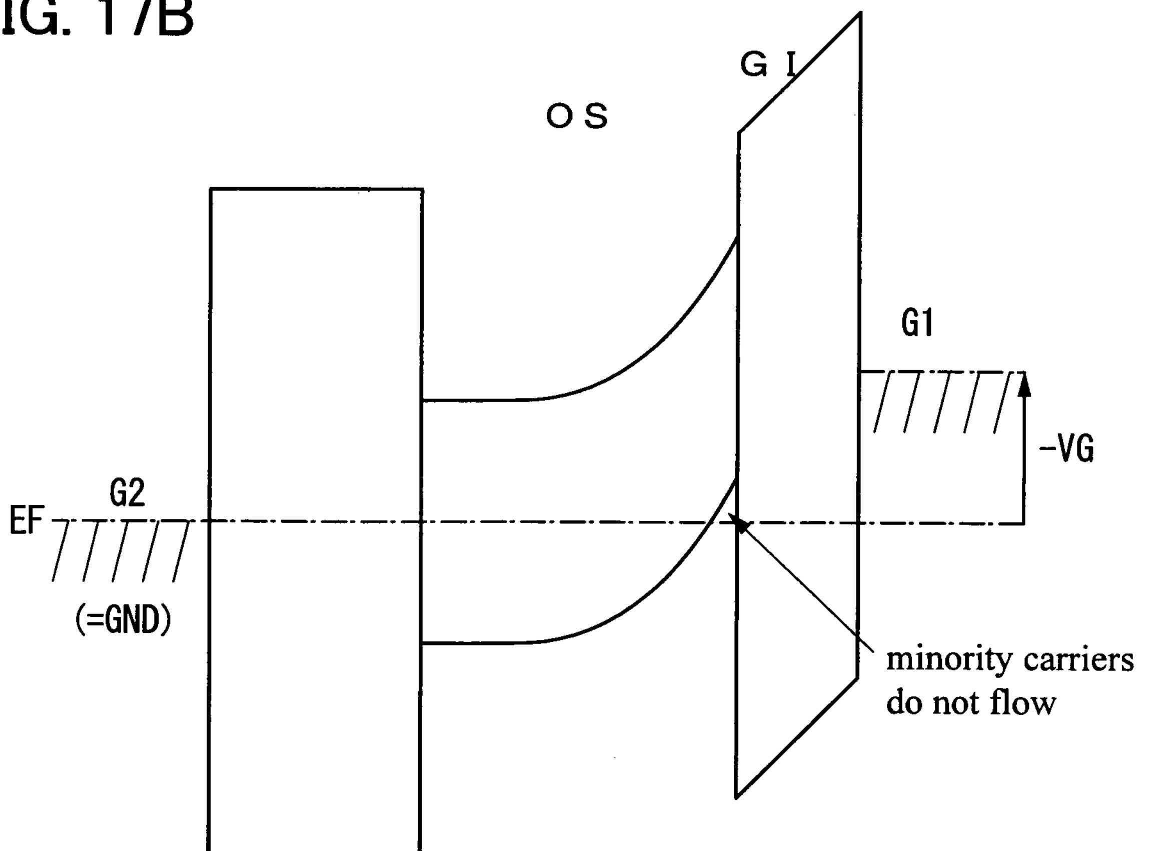
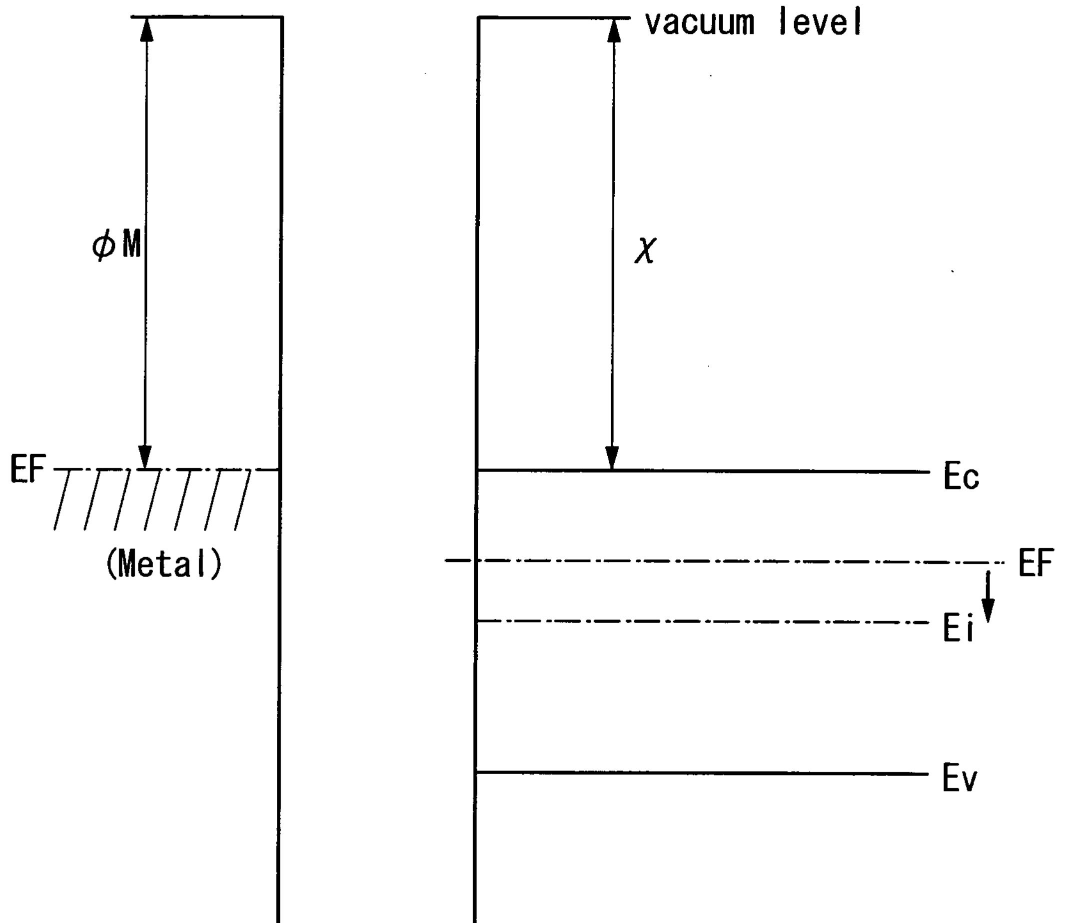


FIG. 18



EXPLANATION OF REFERENCE

81: multi-tone mask, 81a: gray-tone mask, 81b: half-tone mask, 83: light-transmitting substrate, 84: light-blocking portion, 85: diffraction grating, 87: semi-light-transmitting portion, 88: light-blocking portion, 200: substrate, 202: gate insulating layer, 203: protective insulating layer, 204: planarization insulating layer, 210: thin film transistor, 211: gate electrode layer, 213: channel formation region, 214a: high-resistance source region, 214b: high-resistance drain region, 215a: source electrode layer, 215b: drain electrode layer, 216: oxide insulating layer, 217: conductive layer, 220: thin film transistor, 221: gate electrode layer, 223: channel formation region, 224a: high-resistance source region, 224b: high-resistance drain region, 225a: source electrode layer, 225b: drain electrode layer, 227: pixel electrode layer, 230: oxide semiconductor layer, 231a: resist mask, 231b: resist mask, 232: metal conductive layer, 233: oxide semiconductor layer, 236a: resist mask, 236b: resist mask, 236d: resist mask, 236e: resist mask, 237: metal conductive film, 240: thin film transistor, 241: gate electrode layer, 242: oxide semiconductor layer, 245a: source electrode layer, 245b: drain electrode layer, 246: oxide insulating layer, 247: conductive layer, 250: substrate, 252: gate insulating layer, 253: protective insulating layer, 254: planarization insulating layer, 256: oxide insulating layer, 261: gate electrode layer, 265a: source electrode layer, 265b: drain electrode layer, 267: pixel electrode layer, 270: thin film transistor, 271: gate electrode layer, 272: oxide semiconductor layer, 273: channel formation region, 274a: high-resistance source region, 274b: high-resistance drain region, 275a: source or drain electrode layer, 275b: source or drain electrode layer, 277: conductive layer, 280: thin film transistor, 282: oxide semiconductor layer, 283: channel formation region, 284a: high-resistance source region, 284b: high-resistance drain region, 285a: source or drain electrode layer, 285b: source or drain electrode layer, 287: pixel electrode layer, 290: substrate, 292: gate insulating layer, 293: protective insulating layer, 294: planarization insulating layer, 295: oxide semiconductor film, 296: oxide semiconductor layer, 300: first substrate, 302: gate insulating layer, 303: protective insulating layer, 304: drain electrode, 305: common potential line, 306: common electrode layer, 310: common potential line, 311:

common electrode, 320: thin film transistor, 327: pixel electrode layer, 400: substrate, 402: gate insulating layer, 403: protective insulating layer, 404: planarization insulating layer, 410: thin film transistor, 411: gate electrode layer, 413: channel formation region, 414a: high-resistance source region, 414b: high-resistance drain region, 415a: source electrode layer, 415b: drain electrode layer, 416: oxide insulating layer, 420: thin film transistor, 421: gate electrode layer, 423: channel formation region, 424a: high-resistance source region, 424b: high-resistance drain region, 425a: source electrode layer, 425b: drain electrode layer, 427: pixel electrode layer, 430: oxide semiconductor film, 431: oxide semiconductor layer, 450: thin film transistor, 451: gate electrode layer, 452: oxide semiconductor layer, 453: channel formation region, 454a: high-resistance source region, 454b: high-resistance drain region, 455a: source electrode layer, 455b: drain electrode layer, 456: oxide insulating layer, 457: conductive layer, 461: gate electrode layer, 465a: source electrode layer, 465b: drain electrode layer, 466: oxide insulating layer, 467: pixel electrode layer, 600: substrate, 601: counter substrate, 602: gate wiring, 603: gate wiring, 606: gate insulating layer, 616: drain electrode layer, 618: drain electrode layer, 619: drain electrode layer, 620: insulating layer, 621: insulating layer, 622: insulating layer, 623: contact hole, 624: pixel electrode layer, 626: pixel electrode layer, 627: contact hole, 628: TFT, 629: TFT, 632: light-blocking film, 636: coloring film, 637: planarization film, 640: counter electrode layer, 641: slit, 646: alignment film, 648: alignment film, 650: liquid crystal layer, 663: wiring, 690: capacitor wiring, 1200: signal line driver circuit portion, 1201: scan line driver circuit portion, 1202: pixel portion, 1204: substrate, 1205: sealing material, 1206: first alignment film, 1207: second alignment film, 1208: connection wiring, 1210: substrate, 1211: pixel thin film transistor, 1214: insulating layer, 1223: driver circuit thin film transistor, 1235: resin layer, 1240: terminal portion, 1241: connection terminal, 1242: connection wiring, 1243: connection terminal, 1246: connection wiring, 1250: pixel electrode layer, 1255: pillar spacer, 1270: conductive particle, 1280: liquid crystal, 1290: first polarizing plate, 1291: counter electrode layer, 1292: counter electrode layer, 1293: conductive layer, 1295: second polarizing plate, 2700: e-book reader, 2701: housing, 2703: housing, 2705: display portion, 2707: display portion, 2711: hinge, 2721: power switch, 2723: operation key, 2725: speaker, 2800: housing,

2801: housing, 2802: display panel, 2803: speaker, 2804: microphone, 2805: operation key, 2806: pointing device, 2807: camera lens, 2808: external connection terminal, 2810: solar cell, 2811: external memory slot, 3001: main body, 3002: housing, 3003: display portion, 3004: keyboard, 3021: main body, 3022: stylus, 3023: display portion, 3024: operation button, 3025: outside interface, 3051: main body, 3053: eyepiece, 3054: operation switch, 3055: display portion (B), 3056: battery, 3057: display portion (A).

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2010/067995

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. G02F1/1368(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. G02F1/1368

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2010
Registered utility model specifications of Japan 1996-2010
Published registered utility model applications of Japan 1994-2010

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2005-519344 A (Koninklijke Philips Electronics N. V.) 2005.06.30, [0015]-[0032], Figure1, Figure2 & US 2005/0088589 A1 & EP 1485753 A & WO 2003/077021 A1	1-11
A	JP 11-202366 A (SEIKO EPSON CORPORATION) 1999.07.30, [0056], Figure5 No family	1-11
A	JP 2004-4526 A (SEIKO EPSON CORPORATION) 2004.01.08, [0019], Figure3 No family	1-11

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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Date of the actual completion of the international search: 11.11.2010

Date of mailing of the international search report: 22.11.2010

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2010/067995

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 6-258661 A (SEIKO EPSON CORPORATION) 1994.09.16, [0009], Figure2 No family	1-11