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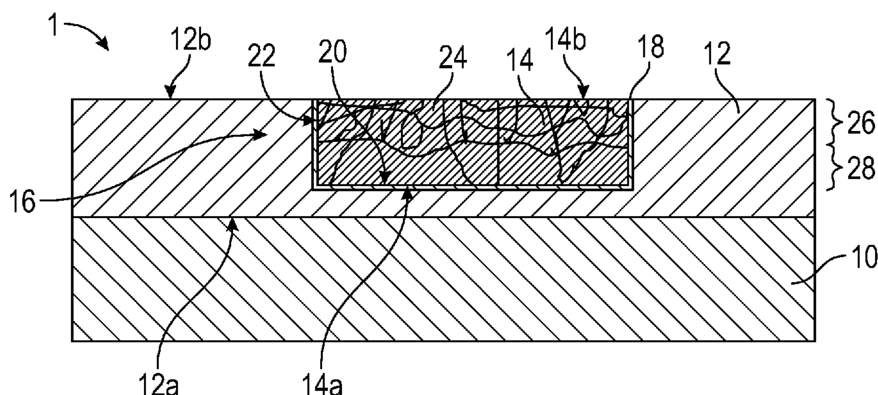


FIG. 1

(57) **Abstract:** An element is disclosed. The element can include a non-conductive structure having a non-conductive bonding surface, a cavity at least partially extending through a portion of a thickness of the non-conductive structure from the non-conductive bonding surface, and a conductive pad disposed in the cavity. The cavity has a bottom side and a sidewall. The conductive pad has a bonding surface and a back side opposite the bonding surface. An average size of the grains at the bonding surface is smaller than an average size of the grains adjacent the bottom side of the cavity. The conductive pad can include a crystal structure with grains oriented along a 111 crystal plane. The element can be bonded to another element to form a bonded structure. The element and the other element can be directly bonded to one another without an intervening adhesive.

WO 2022/147459 A1

STRUCTURE WITH CONDUCTIVE FEATURE AND METHOD OF FORMING SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Provisional Patent Application No. 63/132,334, filed December 30, 2020, titled "STRUCTURE WITH CONDUCTIVE FEATURE AND METHOD OF FORMING SAME," the entire contents of each of which are hereby incorporated herein by reference.

BACKGROUND

Field of the Invention

[0002] The field relates to structures with features, such as surface contact pads, and methods for forming the same, and in particular to structures with conductive features having engineered metal grains, methods for forming the same and for directly bonding such features to conductive features on other elements.

Description of the Related Art

[0003] Semiconductor elements, such as integrated device dies or chips, may be mounted or stacked on other elements. For example, a semiconductor element can be mounted to a carrier, such as a package substrate, an interposer, a reconstituted wafer or element, etc. As another example, a semiconductor element can be stacked on top of another semiconductor element, *e.g.*, a first integrated device die can be stacked on a second integrated device die. Each of the semiconductor elements can have conductive pads for mechanically and electrically bonding the semiconductor elements to one another. There is a continuing need for improved methods for forming the conduct pads.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Specific implementations will now be described with reference to the following drawings, which are provided by way of example, and not limitation.

[0005] Figure 1 illustrates a schematic cross-sectional view of an element, according to an embodiment.

[0006] Figure 2A shows a step in a manufacturing process for forming the element illustrated in Figure 1, according to an embodiment.

[0007] Figure 2B shows another step in the manufacturing process for forming the element illustrated in Figure 1.

[0008] Figure 2C shows another step in the manufacturing process for forming the element illustrated in Figure 1.

[0009] Figure 2D shows another step in the manufacturing process for forming the element illustrated in Figure 1.

[0010] Figure 2E shows another step in the manufacturing process for forming the element illustrated in Figure 1.

[0011] Figure 2F shows another step in the manufacturing process for forming the element illustrated in Figure 1.

[0012] Figure 2G shows another step in the manufacturing process for forming the element illustrated in Figure 1.

[0013] Figure 2H illustrates a schematic cross-sectional view of the element being in contact with another element.

[0014] Figure 2I illustrates a schematic cross-sectional view of a bonded structure.

[0015] Figure 3A shows a step in another manufacturing process for forming the element illustrated in Figure 1, according to an embodiment.

[0016] Figure 3B shows another step in the manufacturing process for forming the element illustrated in Figure 1.

[0017] Figure 3C shows another step in the manufacturing process for forming the element illustrated in Figure 1.

[0018] Figure 3D shows another step in the manufacturing process for forming the element illustrated in Figure 1.

[0019] Figure 3E shows another step in the manufacturing process for forming the element illustrated in Figure 1.

[0020] Figure 3F shows another step in the manufacturing process for forming the element illustrated in Figure 1.

[0021] Figure 3G shows another step in the manufacturing process for forming the element illustrated in Figure 1.

DETAILED DESCRIPTION

[0022] The present disclosure describes methods of engineering metallic grain structures for conductive pads in microelectronic elements. Such engineering can be advantageous for direct metal bonding, such as direct hybrid bonding. For example, two or more semiconductor elements (such as integrated device dies, wafers, etc.) may be stacked on or bonded to one another to form a bonded structure. Conductive contact pads of one element may be electrically connected to corresponding conductive contact pads of another element. Any suitable number of elements can be stacked in the bonded structure. The methods and bond pad structures described herein can be useful in other contexts as well.

[0023] In some embodiments, the elements are directly bonded to one another without an adhesive. In various embodiments, a non-conductive (e.g., semiconductor or inorganic dielectric) material of a first element can be directly bonded to a corresponding non-conductive (e.g., semiconductor or inorganic dielectric) field region of a second element without an adhesive. In various embodiments, a conductive region (e.g., a metal pad) of the first element can be directly bonded to a corresponding conductive region (e.g., a metal pad) of the second element without an adhesive. The non-conductive material can be referred to as a nonconductive bonding region or bonding layer of the first element. In some embodiments, the non-conductive material of the first element can be directly bonded to the corresponding non-conductive material of the second element using bonding techniques without an adhesive using the direct bonding techniques disclosed at least in U.S. Patent Nos. 9,564,414; 9,391,143; and 10,434,749, the entire contents of each of which are incorporated by reference herein in their entirety and for all purposes. In other applications, in a bonded structure, a non-conductive material of a first element can be directly bonded to a conductive material of a second element, such that a conductive material of the first element is intimately mated with a non-conductive material of the second element. Suitable dielectric materials for direct bonding include but are not limited to inorganic dielectrics, such as silicon oxide, silicon nitride, or silicon oxynitride, or can include carbon, such as silicon carbide, silicon oxycarbonitride, silicon carbonitride or diamond-like carbon. Such carbon-containing ceramic materials can be considered inorganic, despite the inclusion of carbon. Additional examples of hybrid direct

bonding may be found throughout US 11,056,390, the entire contents of which are incorporated by reference herein in their entirety and for all purposes.

[0024] In various embodiments, direct bonds can be formed without an intervening adhesive. For example, semiconductor or dielectric bonding surfaces can be polished to a high degree of smoothness. The bonding surfaces can be cleaned and exposed to a plasma to activate the surfaces. In some embodiments, the surfaces can be terminated with a species after activation or during activation (e.g., during the plasma processes). Without being limited by theory, in some embodiments, the activation process can be performed to break chemical bonds at the bonding surface, and the termination process can provide additional chemical species at the bonding surface that improves the bonding energy during direct bonding. In some embodiments, the activation and termination are provided in the same step, e.g., a plasma or wet etchant to activate and terminate the surfaces. In other embodiments, the bonding surface can be terminated in a separate treatment to provide the additional species for direct bonding. In various embodiments, the terminating species can comprise nitrogen. Further, in some embodiments, the bonding surfaces can be exposed to fluorine. For example, there may be one or multiple fluorine peaks near layer and/or bonding interfaces. Thus, in the directly bonded structures, the bonding interface between two non-conductive materials can comprise a very smooth interface with higher nitrogen content and/or fluorine peaks at the bonding interface. Additional examples of activation and/or termination treatments may be found throughout U.S. Patent Nos. 9,564,414; 9,391,143; and 10,434,749, the entire contents of each of which are incorporated by reference herein in their entirety and for all purposes.

[0025] In various embodiments, conductive contact pads of the first element can also be directly bonded to corresponding conductive contact pads of the second element. For example, a direct hybrid bonding technique can be used to provide conductor-to-conductor direct bonds along a bond interface that includes covalently direct bonded dielectric-to-dielectric surfaces, prepared as described above. In various embodiments, the conductor-to-conductor (e.g., contact pad to contact pad) direct bonds and the dielectric-to-dielectric hybrid bonds can be formed using the direct bonding techniques disclosed at least in U.S. Patent Nos. 9,716,033 and 9,852,988, the entire contents of each of which are incorporated by reference herein in their entirety and for all purposes. The bond structures described herein can also be

useful for direct metal bonding without non-conductive region bonding, or for other bonding techniques.

[0026] In some embodiments, inorganic dielectric bonding surfaces can be prepared and directly bonded to one another without an intervening adhesive as explained above. Conductive contact pads (which may be surrounded by nonconductive dielectric field regions) may also directly bond to one another without an intervening adhesive. In some embodiments, the respective contact pads can be recessed below exterior (e.g., upper) surfaces of the dielectric field or nonconductive bonding regions, for example, recessed by less than 30 nm, less than 20 nm, less than 15 nm, or less than 10 nm, for example, recessed in a range of 2 nm to 20 nm, or in a range of 4 nm to 10 nm. The nonconductive bonding regions can be directly bonded to one another without an adhesive at room temperature in some embodiments and, subsequently, the bonded structure can be annealed. Upon annealing, the contact pads can expand with respect to the nonconductive bonding regions and contact one another to form a metal-to-metal direct bond. Beneficially, the use of hybrid bonding techniques, such as Direct Bond Interconnect, or DBI®, available commercially from Xperi of San Jose, CA, can enable high density of pads connected across the direct bond interface (e.g., small or fine pitches for regular arrays). In various embodiments, the contact pads can comprise copper or copper alloys, although other metals may be suitable.

[0027] Thus, in direct bonding processes, a first element can be directly bonded to a second element without an intervening adhesive. In some arrangements, the first element can comprise a singulated element, such as a singulated integrated device die. In other arrangements, the first element can comprise a carrier or substrate (e.g., a wafer) that includes a plurality (e.g., tens, hundreds, or more) of device regions that, when singulated, form a plurality of integrated device dies. Similarly, the second element can comprise a singulated element, such as a singulated integrated device die. In other arrangements, the second element can comprise a carrier or substrate (e.g., a wafer).

[0028] As explained herein, the first and second elements can be directly bonded to one another without an adhesive, which is different from a deposition process. The first and second elements can accordingly comprise non-deposited elements. Further, directly bonded structures, unlike deposited layers, can include a defect region along the bond interface in which nanovoids are present. The nanovoids may be formed due to activation of the bonding

surfaces (e.g., exposure to a plasma). As explained above, the bond interface can include concentration of materials from the activation. For example, in embodiments that utilize a nitrogen plasma for activation, a nitrogen peak can be formed at the bond interface. In embodiments that utilize an oxygen plasma for activation, an oxygen peak can be formed at the bond interface. In some embodiments, the bond interface can comprise a nitrogen-terminated inorganic non-conductive material, such as nitrogen-terminated silicon, silicon oxide, silicon nitride, silicon oxynitride, silicon carbide, silicon oxycarbide, silicon oxycarbonitride, etc. Thus, the surface of the bonding layer can comprise silicon nitride, silicon oxynitride, silicon oxycarbonitride, or silicon carbonitride, with levels of nitrogen present at the bonding interface that are indicative of nitrogen termination of at least one of the elements prior to direct bonding. In some embodiments, nitrogen and nitrogen related moieties may not be present at the bonding interface. As explained herein, the direct bond can comprise a covalent bond, which is stronger than van Der Waals bonds. The bonding layers can also comprise polished surfaces that are planarized to a high degree of smoothness.

[0029] In various embodiments, the metal-to-metal bonds between the contact pads can be joined such that copper grains grow into each other across the bond interface. In some embodiments, the copper can have grains oriented vertically along the 111 crystal plane for improved copper diffusion across the bond interface. In some embodiments, the misorientation of 111 crystal plane in the conductive material may be in a range of $\pm 30^{\circ}$ with respect to the vertical direction from the surface of the conductive material. In some embodiments, the crystal misorientation can be in a range of $\pm 20^{\circ}$, or in a range of $\pm 15^{\circ}$, with respect to the vertical direction. The bond interface can extend substantially entirely to at least a portion of the bonded contact pads, such that there is substantially no gap between the nonconductive bonding regions at or near the bonded contact pads. In some embodiments, a barrier layer may be provided under the contact pads (e.g., which may include copper). In other embodiments, however, there may be no barrier layer under the contact pads, for example, as described in US 2019/0096741, which is incorporated by reference herein in its entirety and for all purposes.

[0030] Annealing temperatures and annealing durations for forming the metal-to-metal direct bond can affect the consumption of thermal budget by the annealing. It may be desirable to lower the annealing temperature and/or annealing duration to minimize consumption of the thermal (energy) budget. Surface diffusion of atoms along the 111 crystal

plane (<111>) can be 3 to 4 orders of magnitude faster than along the 100 or 110 crystal planes. Also, a metal (e.g., Cu) with grains oriented along a 111 crystal plane can have a higher surface mobility as compared to conventional back end of line (BEOL) copper. Further, low-temperature direct metal-to-metal bonding is enabled by creep on the 111 planes of Cu. Therefore, it can be advantageous to have the 111 crystal plane on the bonding surface in order to shorten the annealing time and/or reduce the annealing temperature for direct bonding (e.g., direct hybrid bonding). The advantage to have the 111 crystal plane can be pronounced especially at lower temperatures because the metal surface diffusion (e.g., Cu surface diffusion) also slows down when the annealing temperature is reduced. Accordingly, in various embodiments disclosed herein, a crystal structure can have grains oriented vertically along the 111 crystal plane to enhance metal diffusion (e.g., copper diffusion) during direct bonding.

[0031] A metal layer can be formed with a process selected to plate a copper (Cu) layer having Cu in the 111 crystal orientation at or near the bonding surface of the conductive layer or bonding pad. The Cu layer may be deposited from a non-superfilling or super-filling electroplating bath, for example, with plating chemistry selected to optimize efficient filling of voids or embedded cavities (e.g., vias, trenches) in the substrate, rather than to optimize the direct metal-to-metal bonding to occur during direct hybrid bonding. Subsequent metal treatment, described hereinbelow, can facilitate subsequent bonding such that any desirable plating chemistry can be employed to optimize for other considerations, such as filling noted above. The microstructure (e.g., a grain size) of the deposited or coated metal layer is typically less than 50 nm and may need to be stabilized, for example by an annealing step (at temperature typically lower than 300°C). After the plated metal stabilization step, the coated metal can be planarized by CMP methods to remove unwanted materials (excess plated metal, barrier layer, and/or portion of the non-conductive layer) to form the planar bond surface. The bonding surface can include a planar non-conductive portion that surrounds an adequately dispersed planar conductive portion.

[0032] Various embodiments disclosed herein relate to forming an element with a conductive pad that has a direct bonding surface having a 111 crystal plane orientation independent of plating chemistry. The direct bonding surface can have a cold worked surface with nano-grains that is independent of a metal coating method such as electroplating,

electroless, physical vapor deposition (PVD) amongst others. Therefore, various embodiments disclosed herein provide greater flexibility for the design of plating processes and/or more efficient conductive material filling, as compared to conventional plating processes tuned for forming a 111 crystal plane orientation. In some embodiments, the conductive pad (e.g., plated Cu in a damascene cavity) can be treated by a cold work process at room temperature and/or below room temperature. In some embodiments, the surface of the coated conductive material including the conductive pad can be treated by way of peening in which the conductive pad is bombarded with a stream of particles, such as metal, glass, or ceramic. In some embodiments, the cold work process may comprise, for example, cold rolling a coated conductive material to reduce the grain size of the coated conductive material. A lubricating fluid with and/or without colloidal particles may be used in the cold rolling process. In some embodiments, grain boundaries of the deformed grains of conductive pad can comprise subgrains, high angle grain boundaries, twins massive dislocations and/or dislocation networks. In some embodiments, nano-spaced nano-twinned grains and/or nano-laminates can be formed within the conductive pad.

[0033] In some embodiments, a texture gradient and a grain-size gradient within the conductive pad can be formed by the cold work process. For example, smaller grains and/or a lower percentage of 111 oriented crystals can be achieved near the surface of the pad as compared to deeper within the pad. The cold worked coated conductive material or layers deform plastically. Most of the mechanical energy expended in the deformation process can be converted into heat and the remainder can be stored in the deformed structure with the creation of lattice imperfections. The lattice imperfections can include fine grains, high angle grain boundaries, mechanical twins and/or nano-twins, dislocations, vacancies etc. In the deformed conductive layer (pads and traces), the dominant contribution to the stored energy of the cold work process can be the energy associated with the formation of the additional lattice imperfections present relative to those in an undeformed portion of the annealed conductive layer. The deformation process can induce residual compressive stress in the conductive pad. This residual compressive stress may vary from the surface of the pad to the bottom of the pad. Depending on the energy imparted to the metal in the cold working process, upper portions of the pad may have a higher residual stress compared to the lower portions of the pad.

[0034] Various embodiments disclosed herein allows for relatively low temperature annealing for metal-to-metal direct bonding while being independent of electroplating baths, electroplating methods and/or other conductive layer coating or forming method. In some embodiments, stored energy in a portion of the cold-worked conductive layer can contribute to enabling a relatively low temperature annealing. In some embodiments, the annealing temperature for bonding can be, for example, between about 50°C and about 250°C, between about 100°C and about 200°C, 125°C and about 170°C or between about 50°C and about 180°C. Depending on the annealing temperature or temperatures, the annealing time may range between 45 minutes to 180 minutes. The annealing time may increase when the annealing temperature is lower. However, the embodiments disclosed herein can still lower consumption of the thermal (energy) budget relative to conventional structures, such that anneal durations can remain low despite lower anneal temperatures.

[0035] Figure 1 illustrates a schematic cross-sectional view of an element 1, according to an embodiment. The element 1 can comprise a semiconductor element, either before singulation, such as a semiconductor substrate or wafer, or after singulation, such as an interposer, electronic component, integrated circuit (IC) die or chip. The element 1 can include a substrate 10 (e.g., bulk semiconductor material), a non-conductive layer (e.g., a dielectric layer 12, such as silicon oxide or other low k material) over the substrate 10, a conductive pad 14 disposed in a cavity 16 formed in the dielectric layer 12, and a barrier layer 18 disposed between the dielectric layer 12 and the conductive pad 14. While for simplicity a single dielectric layer 12 is illustrated, the skilled artisan will understand that the dielectric layer 12 and conductive pad 14 can comprise part of a back-end-of-line (BEOL) structure or redistribution layer (RDL) structure over a BEOL structure, which typically includes vias and trenches or traces (not shown). In some embodiment, the conductive pad or via or trace may comprise an alloy of copper, nickel, gold, or other metal alloys.

[0036] In some embodiments, the substrate 10 can comprise a semiconductor substrate or wafer. In some embodiments, the substrate 10 can comprise a glass substrate, a dielectric substrate, or a ceramic substrate.

[0037] The dielectric layer 12 can comprise a relatively low k (e.g., $k < 4$) dielectric material. In some embodiments, the dielectric layer 12 can comprise an inorganic material. The dielectric layer 12 can have a lower side 12a that faces the substrate 10 and an upper side

12b opposite the lower side 12a. The upper side 12b can define a bonding surface of the dielectric layer 12, and can thus include, for example, a higher concentration of nitrogen and/or fluorine compared to the bulk material of the layer, as described above. In some embodiments, the bonding surface at the upper side can be defined by a barrier or etch stop layer (not shown) over the low k dielectric layer 12. The dielectric layer 12 can have the cavity 16 that at least partially extends through a thickness of the dielectric layer 12 from the upper side 12b. The cavity 16 has a bottom side 20 and sidewalls 22.

[0038] The conductive pad 14 can have a lower side 14a that faces the bottom side 20 of the cavity and an upper side 14b opposite the lower side 14a. The upper side 14b can define a bonding surface of the conductive pad 14. The conductive pad 14 can comprise a metal such as copper (Cu). The conductive pad 14 can comprise copper with grains oriented along a 111 crystal plane. In some embodiments, the conductive pad 14 can comprise a cold worked or mechanically or optically deformed pad.

[0039] Sizes of the grains 24 in the element 1 can vary in deformed conductive pads 14. A size of the grain 24 used herein may refer the maximum dimension of the grain 24. In some embodiments, the grains 24 at or near the upper side 14b can be smaller on average than the grains 24 at or near the lower side 14a. In some embodiments, the grains can have a small grain region 26 at or near the upper side 14b of the conductive pad 14 and a large grain region 28 at or near the lower side 14a of the conductive pad 14. In some embodiments, the small grain region 26 can be arbitrarily selected to be a region of the conductive pad 14 from the upper side 14b to 1000 nm deep into the conductive pad 14 for a shallow conductive pad 14, or to 3000 nm in a deeper conductive pad 14 (e.g., pads of thickness greater than 5000 nm), for purposes of comparing grain sizes above and below this level. In some embodiments, an average grain size in the small grain region 26 at or near the upper side 14b can be about 10 nanometers (nm) to 200 nm, or about 30 nm to 200 nm. In some embodiments, an average grain size in the large grain region 28 at or near the lower side 14a can be about 0.5 microns (μm) to 5 μm. In some embodiments the average grain size can vary depending on the width and depth of the conductive pad 14. In some embodiments, the average size of the grain 24 at or near the lower side 14a can be at least five times greater than the average size of the grains 24 at or near the upper side 14b. For example, the average size of the grain 24 at or near the lower side 14a can be about 3 to 100, 10 to 100, 20 to 100, 30 to 100, 40 to 100, or 40 to 100,

times greater than the average size of the grains 24 at or near the upper side 14b of the deformed conductive pad 14. In some embodiments, the grains 24 can have graded grain sizes through the depth of the conductive pad 14 as a result of the gradation of lattice imperfections from the upper side 14b to the lower side 14a. In some embodiments, the conductive pad 14 can be measurably harder at or near the upper side 14b than at or near the lower side 14a. In some embodiments, the average size of 3 contiguous grains 24 at or near the lower side 14a can be about 3 to 100, 10 to 100, 20 to 100, 30 to 100, 40 to 100, or 40 to 100, times greater than the average size of 3 contiguous grains 24 at or near the upper side 14b of the deformed conductive pad 14. Similarly, the average grain size of 2 contiguous grains 24 at or near the upper side 14b of the deformed conductive pad 14 can be at least 2 times smaller than the average of 2 contiguous grain in an interconnect layer below the barrier layer 18 (not shown) of the deformed conductive pad 14. In some embodiments, at a higher determined deformation of the coated conductive layer, the grain size of 3 contiguous grains 24 near the upper side 14b of the conductive pad 14 and lower side 14a of the conductive pad 14 are similar, and can be at least 3 times smaller than grain size at corresponding locations in undeformed conductive pads 14.

[0040] Upon thermal annealing after cold working, such as during bonding the conductive pad 14 to another conductive pad of another element, to release the stored energy in the deformed conductive pad 14 (deformed due to compressive stress induced by mechanical or optical peening) and to enhance grain recovery and growth, the recovered grains of the upper side 14b region of the conductive pad 14 can be larger than the recovered grains of the lower side 14a region beneath (see Figure 2I). The grain sizes at the upper side 14b can exceed the sizes at the lower side 14a to produce a reversed gradient from that just after the cold working process. Similarly the grain sizes at the upper side 14b can exceed the sizes of an interconnect layer below the barrier layer 18 (not shown) of the deformed conductive pad 14.

[0041] In some embodiments, the upper side 14b of the conductive pad 14 can be recessed below the upper side 12b of the dielectric layer 12. For example, the upper side 14b of the conductive pad 14 can be recessed below the upper side 12b of the dielectric layer 12 by less than about 30 nm, less than about 20 nm, less than about 15 nm, or less than about 10 nm. For example, the upper side 14b of the conductive pad 14 can be recessed below the upper side 12b of the dielectric layer 12 in a range of 2 nm to 20 nm, or in a range of 4 nm to 15 nm.

[0042] The barrier layer 18 can comprise, for example, a dielectric barrier layer, such as silicon nitride, silicon oxynitride, silicon carbonitride, diamond-like carbon, etc. The barrier layer 18 can comprise a conductive barrier, such as a metal nitride (e.g., Ta, TiN, TaN, WN, and their various combinations etc.). For example, a conductive barrier layer 18 can be deposited over the bottom side 20 and the sidewalls 22 of the cavity 16. A non-conductive barrier layer 18 may be formed on the sidewalls 22, and not at the bottom side 20 of the cavity 16. In some embodiments, the non-conductive barrier layer 18 may be discontinuous over the bottom side 20 of the cavity 16. The barrier layer 18 can intervene between the dielectric layer 12 and the conductive pad 14.

[0043] Figures 2A-2G show stages in a manufacturing process for forming the element 1 illustrated in Figure 1, according to an embodiment. Figure 2H shows the element 1 being in contact with another element (a second element 2), and Figure 2I shows a bonded structure 3 that include the element 1 and the second element 2.

[0044] In Figure 2A, a dielectric layer 12 is provided over a substrate 10. A cavity 16 is selectively formed in the dielectric layer 12, including an upper surface 12b. The cavity 16, shown with a bottom surface 20 and sidewall surfaces 22, can extend through at least a portion of a thickness of the dielectric layer 12. The cavity 16 can be formed by way of masking and etching or drilling. The cavity 16 can comprise a damascene cavity that is formed with damascene processes. The cavity 16 may comprise a thru substrate cavity (TSC) such as a through silicon via (TSV) or a through glass via (TGV). In some embodiments, the cavity 16 may be formed to be in contact with an embedded interconnect structure such as a BEOL or RDL layer (not shown).

[0045] In Figure 2B, a barrier layer 18 can be provided on the upper surface 12b of the dielectric layer, the sidewalls 22 of the cavity 16, and the bottom surface 20 of the cavity 16. As mentioned earlier the barrier layer 18 may be a non-conductive material formed on the upper surface 12b of the dielectric layer, the sidewalls 22 of the cavity 16, and not at the bottom surface 20 of the cavity16. A seed layer 30 can be provided on the barrier layer 18 over these same surfaces. In some embodiments, a conductive via or vias or one or more traces (not shown) contacting the barrier layer 18 may be disposed beneath the lower surface 20 of the cavity 16.

[0046] In Figure 2C, a conductive material 32 can be provided in the cavity 16 and over the upper side 12b of the dielectric layer 12. In some embodiments, the conductive material can comprise metal, such as copper (Cu), and can be provided, for example, by plating or other known methods. In some embodiment, the conductive material 32 may comprise an alloy of copper, nickel, gold, or other metal alloys. The conductive material 32 can have a lower side 32a and an upper side 32b. Advantageously, the plating methods and additives can be optimized for efficiently filling the cavity 16, which may be just one of many vias and/or trenches across the substrate, and which can have high aspect ratios. In some embodiments, the conductive material 32 can comprise an electroplating coating formed at or below room temperature. The room temperature can be defined as temperatures in a range of, for example, 20°C to 35°C. The plated metal of the conductive material 32 can have grain sizes in a range of between 10 nm to 100 nm, or 30 nm to 100 nm in the as-plated state.

[0047] In Figure 2D, the conductive material 32 can be annealed at a temperature between room temperature and 250°C. In some embodiment, some electroplated copper films with low interstitial and non-interstitial impurities can form large grains at room temperatures due to room temperature grain growth phenomenon. The annealing process can stabilize the microstructure (e.g., a grain size) of grains 24 in the conductive material 32. The annealing process can form relatively large grains 24 in the conductive material 32. For relatively large pads greater than 5 microns across, the grain size of the conductive material after annealing can be in a range of, for example, 0.3 microns to 3 microns. For conductive traces with width less than 1 microns, the grain structure may exhibit a bamboo type grain structure extending along the trace axes.

[0048] In Figure 2E, the conductive material 32 can be treated with a cold work process. The cold work process can take place at room temperature and/or below room temperature. For example, the substrate temperature during the cold work process may range from – 196°C (77K), the temperature of liquid nitrogen, to about 30°C or 50°C, or from 0°C to about 25°C, and in one example at about ambient clean room temperature. The conductive material 32 can be treated from the upper side 32b. In some embodiments, the conductive material 21 can be treated with a strain hardening process. For example, the conductive material 32 can be treated by a shot peening process, cold rolling or laser peening process to induce plastic deformation in the conductive material 32. As noted above, shot peening can

include bombardment by particles, such as metal, sand, glass, or ceramic. For example, the mechanical peening may include bombarding the surface (e.g., the upper side 32b) of the conductive material 32 with ceramic or steel shots. For example, s diameter of the shots may range between 0.1 mm and 2 mm, a velocity of the shots can be between 1 to 5 meters per second, and a bombardment time can be between 30s to 180s. In some embodiments, the substrate 10 may rotate between 10 to 60 rpm and preferably between 15 to 45 rpm during the peening operation. In some embodiments, the element 1 can be static during the peening operation. The plastic deformation can induce residual compressive stresses in the grains 24 at the surface and below the surface of the conductive material 32 and/or tensile stresses at an interior or bulk of the conductive material 32. The conductive material 32 after the cold work process can have stored energy from compressive residual stress. In some embodiments, a portion of the conductive material 32 at or near the upper side 32b can have higher stored energy from the cold work process than the lower side 32a. In some embodiment, the conductive material 32 can be uniformly deformed from the top surface 32b to the bottom surface 32a, including a portion of the conductive material 32 at the bottom of the cavity 20 adjacent to the barrier layer 18. The conductive material 32 may be heavily deformed such that it is challenging to distinguish the individual metal grains because of the massive structural defects such as stacking faults, mechanical twins, slips, vacancies, and/or dislocation networks induced by the deformation process. As a result of the structural defects and very small grain sizes (e.g., 5 nm to 30 nm), it may be challenging to index the individual grains 24 for their orientation. Regardless of the method of applying compressive force or forces to the conductive material 32, the applied force should degrade the substrate 1. Degrading the element 1 may, for example, comprise applying excessive force so as to induce delamination of the barrier layer 18 or induce defects or cracks in the dielectric layer 12 and/or the substrate 10. The stored energy can contribute to achieving a relatively low temperature annealing bonding (see Figure 2I).

[0049] Figure 2F shows the grains 24 after the treatment in Figure 2E. Sizes of the grains 24 in the conductive material 32 can vary. In some embodiments, the grains 24 at or near the upper side 32b can be smaller than the grains 24 at or near the lower side 32a. In some embodiments, an average size of the grains 24 at or near the upper side 32b can be about 10 nanometers (nm) to 200 nm, or about 50 nm to 200 nm. In some embodiments, an average

size of the grains 24 at or near the lower side 32a or at the interior of the cavity can be about 0.5 microns (μm) to 1 μm. In some embodiments, the average size of the grains 24 at or near the lower side 32a can be at least about five times greater than the average size of the grains 24 at or near the upper side 32b. For example, the average size of the grain 24 at or near the lower side 32a can be about 10 to 100, 20 to 100, 30 to 100, 40 to 100, or 40 to 100, times greater than the average size of the grains 24 at or near the upper side 32b. In some embodiments, because of the top to bottom variation in the compressive residual stress in the conductive material, the grains 24 can have gradient grain sizes. For example, the grain sizes of the grains 24 can gradually increase from the upper side 32b to the lower side 32a or in the interior of the conductive cavity or layer. In some embodiments, the conductive material 32 can be harder at or near the upper side 32b than at or near the lower side 32a. As compared to the deeper or bulk material near the lower side 32a, the conductive material 32 near the upper side 32b can have a lower percentage of grains 24 with vertically oriented 111 crystal planes and comparatively higher percentage of 220 crystal planes (<220>) from the deformation process. In some embodiments, especially when laser peening method is applied to the conductive material 32, the cold working of the conductive layer can be sufficiently deep, such that the smaller grains at the upper surface 32b are similar to those at lower side 32a or at the interior of the cavity.

[0050] In some applications, the conductive material 32 may comprise a portion of a through substrate pad (not shown), such as a through-silicon via (TSV) or through-glass via (TGV). Here, a portion of the conductive material 32 at or near the upper surface 32b may exhibit lattice imperfections from the cold working step.

[0051] In Figure 2G, the element 1 is formed and prepared for direct bonding, such as by a high degree of polishing and activation (e.g., nitrogen termination). At least a portion of the conductive material 32 can be removed, such as by polishing. Portions of the barrier layer 18 and the seed layer 30 can also be removed. Although the slurry chemistry for chemical mechanical planarization (CM) can be selective to stop on the dielectric layer 12, a portion of the dielectric layer 12 can also be removed to form a bonding surface. The bonding surface can include highly polished surfaces of the non-conductive layer 12b and the upper surface 14b of the planar conductive material. In some embodiments, the portions of the conductive material, barrier layer 18, seed layer 30, and the dielectric layer 12 can be removed by

polishing, such as chemical mechanical polishing (CMP), in one or multiple stages with one or multiple different slurry compositions to form the bonding surface. The upper side 12b of the dielectric layer 12 can be polished to a high degree of smoothness to prepare for direct bonding, followed by very slight etching and/or surface activation, such as by exposure to nitrogen-containing plasma. The activated bonding surface is cleaned with a suitable solvent such as deionized water (DI) water to remove unwanted particles. The cleaned surface may be spun dried to remove cleaning solvent residues prior to a bonding operation and subsequent annealing step.

[0052] In some embodiments, the highly polished bonding surfaces of the non-conductive layer 12b and the upper surface 14b of the planar conductive material of the substrate 10 may be coated with a protective layer (not shown), typically with an organic resist layer. The coated substrate can be mounted on a dicing frame for singulation. The singulation process may be formed by any known process, for example, saw dicing, laser singulation, reactive ion etching (RIE), wet etching or any suitable combination of these singulation steps. Regardless of the singulation step, the protective layer and singulation particulates can be cleaned off from the singulated dies and from the dicing frame. The bonding surfaces of the cleaned dies may ashed to remove unwanted organic residues and cleaned for direct bonding to another prepared bonding surface of another substrate. In some embodiments, the cleaned bonding surface of the singulated dies may be activated by known methods, cleaned of unwanted particles and material prior to directly bonding the bonding surfaces of the activated die to another prepared bonding surface of a second substrate. The bonded elements can be annealed to mechanically and electrically interconnect the opposing conductive pads of the bonded substrates (see Figure 2I). In some embodiments, the second substrate with bonded singulated dies may further be singulated to form directly bonded die stacks.

[0053] Sizes of the grains 24 in the element 1 can vary. In some embodiments, the grains 24 at or near the upper side 14b can be smaller on average than the grains 24 at or near the lower side 14a. In some embodiments, the grains can have a small grain region at or near the upper side 14b of the conductive pad 14 and a large grain region at or near the lower side 14a of the conductive pad 14. In some embodiments, the small grain region can be a region of the conductive pad 14 from the upper side 14b to 1000 nm, or to 3000 nm for a deeper pad, into the conductive pad 14. In some embodiments, an average size of the grains 24 in the small

grain region at or near the upper side 14b can be about 10 nanometers (nm) to 200 nm, or about 30 nm to 200 nm. In some embodiments, an average size of the grain 24 in the large grain region at or near the lower side 14a can be about 0.2 microns (μm) to 1 μm, or 0.2 μm to 0.5 μm. In some embodiments, the average size of the grain 24 at or near the lower side 14a can be at least five times greater than the average size of the grains 24 at or near the upper side 14b. For example, the average size of the grain 24 at or near the lower side 14a can be about 10 to 100, 20 to 100, 30 to 100, 40 to 100, or 40 to 100, times greater than the average size of the grains 24 at or near the upper side 14b. In some embodiments, the grains 24 can have gradient grain sizes. For example, the grain sizes of the grains 24 can gradually increase from the upper side 14b to the lower side 14a. In some embodiments, the conductive pad 14 can be harder at or near the upper side 14b than at or near the lower side 14a. In some embodiments, the cold working of the conductive pad 14 is sufficiently deep such that an average size of the smaller grains at or near the upper surface 14b is similar to an average size of the grains at or near lower side 14a or at the interior of the cavity.

[0054] In Figure 2H, the element 1 is brought into contact with the second element 2. In some embodiments, the second element can comprise an identical or generally similar element as the element 1. In some embodiments, the second element 2 can comprise a carrier, such as a package substrate, an interposer, a reconstituted wafer or element, etc. In some embodiments, the second element 2 can also be prepared for direct bonding as in element 1. A dashed line shown in Figure 2H indicates a bond interface 56 between the element 1 and the second element 2. The second element 2 can include a second substrate 50, a second dielectric layer 52, and a second conductive pad 54. The conductive pad 54 can have grains 64. In some embodiments, upon contacting the dielectric layer 12 and the second dielectric layer 52, the dielectric layers 12 and 52 can bond to one another. In some embodiments, the dielectric layer 12 and the second dielectric layer 52 can be bonded to one another directly without an intervening adhesive. The dielectric layer 12 and the second dielectric layer 52 can be directly bonded at room temperature without external pressure. Although not shown in Figure 2H, the conductive pads 14, 54 can be recessed from the surfaces of the dielectric layers 12, 52, respectively, at the time of contact, such that a small gap is present between the opposing bond pads 14, 54 or other conductive elements at the surface.

[0055] In Figure 2I, the conductive pad 14 and the second conductive pad 54 are bonded to one another. In some embodiments, the conductive pad 14 and the second conductive pad 54 can be bonded to one another directly without an intervening adhesive. The bonded structure can be annealed. Upon annealing, the conductive pads 14, 54 can expand and contact one another to form a metal-to-metal direct bond. A dashed line shown in Figure 2I indicates the bond interface 56 between the element 1 and the second element 2.

[0056] As described above, prior to anneal, the crystal structure of the conductive material 32 can have grains 24 including a lower percentage of vertically oriented 111 crystal planes near the interface, as compared to the bottom regions of the conductive pads 14, 54. The conductive pad 14 after the cold work process in Figures 2G and 2H has stored energy in the cold worked conductive pad 14. The cold worked conductive pad 14 may comprise very fine non-oriented grain sizes (with massive lattice imperfections, high angle grain boundaries, twins, dislocations, vacancies etc.) exhibiting high creep in the pad 14. The combination of higher creep and grain stored energy can enable the bridging of the recess between the pads 14 and 54.at relatively low temperature annealing. Therefore, the conductive pads 14, 54 can be sufficiently bonded to one another directly with a relatively low temperature and/or short anneal. In some embodiments, the conductive pad 14 and the second conductive pads 54 can be annealed at a temperature less than 250°C, less than 200°C, or less than 150°C, for example about 100°C to 250°C, about 125°C to 200°C, or about 125°C to 180°C.

[0057] After the conductive pad 14 and the second conductive pad 54 are annealed and bonded, the grain sizes can change relative to before bonding. In some embodiments, a size of a grain 24, 64 at or near the bonding interface 56 can be on average more than about 1.2 or 2 times larger than a size of a grain 24 at or near the lower side 14a of the conductive pad 14. For example, the size of a grain 24, 64 at or near the bonding interface 56 can be on average more than about 2 to 10, 2 to 7, 2 to 5, 1.2 to 10, 1.2 to 7, or 1.2 to 5 times larger than a size of a grain 24 at or near the lower side 14a of the conductive pad 14. In some embodiment, a grain size of the grain 24, 64 at or near the bonding interface 56 may be at least 20% to 50% larger than a grain size of the grain 24 at or near the lower side 14a of the conductive pad 14.

[0058] In some embodiments, an average dimension of the grains 24, 64 at the bonding interface 56 is about 3 to 8 times, 3 to 6 times, 4 to 8 times, or 4 to 6 times greater than an average dimension of the grains 24 closer to the lower side 14a of the conductive pad

14. In some embodiments, the grains 24, 64 at or near the bonding interface of the bonded conductive pads 14, 54 can have a higher percentage of 111 planes and annealing twins than that of the grains 24 at or near the lower side 14a of the conductive pad 14. The stored energy in the surface grain structure facilitates greater grain growth and re-orientation during the anneal for bonding, as compared to deeper parts of the pad structure that are less affected by the cold working process.

[0059] Figures 3A-3G show steps in a manufacturing process for forming the element 1 illustrated in Figure 1, according to another embodiment. The process illustrated in Figures 3A-3G is different from the process illustrated in Figures 2A-2G in that the conductive material 32 is thinned prior to peening in the process illustrated in Figures 2A-2G. The components shown in Figures 3A-3G can be the same as or generally similar to like components shown in Figures 1-2I, and like reference numerals are used to refer to like parts.

[0060] In Figure 3A, a dielectric layer 12 is provided over a substrate 10. A cavity 16 is formed in the dielectric layer 12. The cavity 16 can extend through at least a portion of a thickness of the dielectric layer 12. The cavity 16 can be formed by way of selective etching or drilling. The cavity 16 can comprise a damascene cavity that is formed with damascene processes. In Figure 3A, an insulating or conductive barrier layer 18 can be provided on an upper side 12b of the dielectric layer 12, sidewalls 22 of the cavity 16, and the bottom side 20 of the cavity 16. A seed layer 30 can be provided on the barrier layer 18 over the same surfaces.

[0061] In Figure 3B, a conductive material 32 can be provided in the cavity 16 and over the upper side 12b of the dielectric layer 12. In some embodiments, the conductive material can comprise metal, such as copper (Cu). The conductive material 32 can have a lower side 32a and an upper side 32b. As shown in Figure 3C, the conductive material 32 can be annealed. The annealing process can stabilize the microstructure (e.g., grain structure) of grains 24 in the conductive material 32. The annealing process can form relatively large grains in the conductive material 32.

[0062] In Figure 3D, the conductive material 32 can be thinned from the upper side 32b. In some embodiments, the conductive material 32 can be thinned by way of polishing, such as chemical mechanical polishing (CMP). Figure 3D illustrates that a portion of the conductive material 32 is disposed on the upper side 12b of the dielectric layer 12. However, in some embodiments, the conductive material 32 positioned over the upper side 12b of the

dielectric layer 12 can be removed completely and expose the barrier layer 18. In some other embodiments, the barrier layer 18 over the upper side 12b of the dielectric layer 12 can be removed completely and expose the upper side 12b of the dielectric layer 12.

[0063] In Figure 3E, the conductive material 32 can be treated with a cold work process as described above with respect to Figure 2E. The cold work process can take place at room temperature and/or below room temperature. For example, the substrate temperature during the cold work process may range from – 196°C (77K), the temperature of liquid nitrogen, to about 50°C, or from 0°C to about 25°C, and in one example at about ambient clean room temperature. The conductive material 32 can be treated from the upper side 32b. In some embodiments, the conductive material 21 can be treated with a strain hardening process. For example, the conductive material 32 can be treated by a shot peening process or laser peening process to induce plastic deformation in the conductive material 32. As noted above, shot peening can include bombardment by particles, such as metal, sand, glass, or ceramic. The plastic deformation can induce residual compressive stresses in the grains 24 at a surface and below surface of the conductive material 32 and/or tensile stresses at an interior of the conductive material 32. As discussed herein, regardless of the method of applying compressive force or forces to the conductive material 32, the applied force should degrade the substrate 1. Degrading the element 1 may, for example, comprise applying excessive force so as to induce delamination of the barrier layer 18 for the surface of the substrate or induce defects or cracks in the dielectric layer 12 and/or the substrate 10.

[0064] Figure 3F shows the grains 24 after the treatment in Figure 3E. Sizes of the grains 24 in the conductive material 32 can vary. In some embodiments, the grains 24 at or near the upper side 32b can be smaller than the grains 24 at or near the lower side 32a. In some embodiments, an average size of the grains 24 at or near the upper side 32b can be about 5 nanometers (nm) to 200 nm, or about 30 nm to 200 nm. Depending upon the thickness of remaining metal over field regions (upper surface of the dielectric layer 12), an average size of the grain 24 at or near the lower side 32a can be about 0.5 microns (μm) to 3 μm or larger. In some embodiments, the average size of the grain 24 at or near the lower side 32a or in the regions of the bottom of the conductive pad can be at least about two times greater than the average size of the grains 24 at or near the upper side 32b to the average size of the grain 24 at or near the lower side 32a. For example, the average size of the grain 24 at or near the lower

side 32a can be about 2 to 100, 20 to 100, 30 to 100, 40 to 100, or 40 to 100, times greater than the average size of the grains 24 at or near the upper side 32b. In some embodiments, the grains 24 can have 1 gradient grain sizes. For example, the grain sizes of the grains 24 can gradually increase from the upper side 32b to the lower side 32a. In some embodiments, the conductive material 32 can be harder at or near the upper side 32b than at or near the lower side 32a. Due to the plastic deformation, reduced grain sizes, increased lattice imperfections and a reduced percentage of 111 oriented crystal planes are left at or near the upper side 32b of the conductive pad 32. In some embodiments, due to the reduced thickness of the metal left by the planarization shown in Figure 3E, the plastic deformation may extend from the upper side 32b of the conductive pad 32 to the lower side 32a of the conductive pads 32.

[0065] In Figure 3G, the element 1 is formed. At least a portion of the conductive material 32 can be removed. Portions of the barrier layer 18 and the seed layer 30 can also be removed to form a highly polished planar bonding surface. A portion of the dielectric layer 12 can also be removed. In some embodiments, the portions of the conductive material, barrier layer 18, seed layer 30, and the dielectric layer 12 can be removed by polishing, such as chemical mechanical polishing (CMP) in one or multiple stages to form a highly polished bonding surface. The bonding surface comprising a planar top surface of the dielectric layer 12 and a planar polished surface of the conductive pad 14. The upper side 12b of the dielectric layer 12 can be polished to a high degree of smoothness and can be activated to prepare for direct bonding.

[0066] As described above with respect to Figures 2H and 2I, the structure shown in Figure 3G can then be directly hybrid bonded to another element, which may or may not have received similar treatment. As also noted above with respect to Figures 2H and 2I, the prepared bonding surface can first be protected with a protective layer, such as an organic resist layer, for intervening singulation or other processing prior to bonding.

[0067] The conductive pad 14 after the cold work process in Figures 2E and 3E have stored energy in conductive pad 14. The stored energy can enable a relatively low temperature annealing for bonding the element (the first element 1) to another element (the second element 2). The conductive pads 14, 54 can be directly bonded to one another sufficiently with a relatively low temperature and/or a relatively short anneal duration. In some embodiments, the conductive pad 14 and the second conductive pad 54 can be annealed at a

temperature less than 250°C, less than 200°C, or less than 150°C, for example about 100°C to 250°C, or about 125°C to 180°C.

[0068] After the conductive pad 14 and the second conductive pad 54 are annealed and bonded, the grain sizes can change relative to the grain sizes before bonding. In some embodiments, a size of a grain 24, 64 at or near the bonding interface 56 can be on average more than about 1.2 or 2 times larger than a size of a grain 24 at or near the lower side 14a of the conductive pad 14. For example, the size of a grain 24, 64 at or near the bonding interface can be on average more than about 2 to 10, 2 to 7, 2 to 5, 1.2 to 10, 1.2 to 7, or 1.2 to 5 times larger than a size of a grain 24, 64 at or near the lower side of the conductive pad 14, 54. In some embodiment, a grain size of the grain 24, 64 at or near the bonding interface may be at least 20% to 50% larger than a grain size of the grain 24, 64 at or near the lower side of the conductive pad 14, 54. In general, the larger the stored energy from the applied compressive force, the larger the grain size in the annealed bonded conductive pads.

[0069] In some embodiments, a third conductive material (not shown) may be disposed in a cavity 16 in the dielectric material 12, beneath the barrier layer 18 (see Figures 2B and 3A) as typical in multilayer BEOL or redistribution layer (RDL) within the element 1. After the bonding and annealing operation(s), as a result of the mechanical and thermal treatment(s) to the conductive material 32 in the cavity 16, an average size of the grain 24 in the regions of the conductive pad 32 of cavity 16 can be at least about 20% greater than the average size of the grains 24 of the third conductive material beneath the barrier layer 18 compared to a third conductive material that was exposed to only thermal treatment. For example, the average size of the grain 24 of conductive pad 32 can be about 1.2 to 20 times greater than the average size of the grains 24 of the third conductive material beneath the barrier layer 18 or subsequent conductive pads (not shown) beneath the third conductive pads.

[0070] Referring back to Figure 2I, in some embodiment, after annealing the mechanically or optically cold worked conductive material, the annealed grains are elongated along a direction generally parallel to the dielectric bonding surface or the bonding surface of the conductive material. A horizontal dimension (length *l*) of a grain of the annealed conductive material 24 may be at least 20% larger than a vertical dimension (thickness *t*) of the same grain about a direction perpendicular to the dielectric bonding surface or the bonding surface of the conductive material. For example, the length of a grain of the conductive material generally

parallel to the bonding interface can be, on average, more than about 1.5 to 10 times larger than the thickness of the grain in a direction generally perpendicular to the bonding interface. In some embodiment, the length of the columnar grain a bonded elements (e.g., the bonded elements 3 shown in Figure 2I) may be at least 20% to 300% longer than the thickness of columnar grain of the conductive material in bonded element 3. In some embodiments, an aspect ratio of a grain (the maximum longitudinal dimension (length *l*) of a grain/the maximum perpendicular dimension (thickness *t*) of the same grain), can be greater than 1.2, 1.5, or 3.

[0071] In one aspect, an element is disclosed. The element can include a non-conductive structure that has a non-conductive bonding surface, a cavity that at least partially extends through a portion of a thickness of the non-conductive structure from the non-conductive bonding surface, and a conductive pad that is disposed in the cavity. The cavity has a bottom side and a sidewall. The conductive pad has a bonding surface and a back side opposite the bonding surface. An average size of the grains at the bonding surface is smaller than an average size of the grains that are adjacent the bottom side of the cavity.

[0072] In one embodiment, the non-conductive structure includes a dielectric layer. The non-conductive bonding surface of the non-conductive layer can be prepared for direct bonding.

[0073] The conductive bonding surface of the conductive pad can be prepared for direct bonding.

[0074] The conductive pad comprises can be a copper (Cu) pad.

[0075] The conductive pad can include a lower percentage of grains with 111 crystal planes at the bonding surface compared with adjacent to the bottom side.

[0076] The conductive pad can include a higher percentage of grains with 220 crystal planes at the bonding surface compared with adjacent to the bottom side

[0077] In one embodiment, the average size of the grains adjacent the bottom side of the cavity is at least 3 times greater than the average size of the grains at the bonding surface.

[0078] In one embodiment, the average size of the grains adjacent the bottom side of the cavity is at least 20 times greater than the average size of the grains at the bonding surface.

[0079] In one embodiment, the average size of the grains adjacent the bottom side of the cavity is between 0.2 microns (μm) to 1 μm.

[0080] In one embodiment, the average size of the grains at the bonding surface is between 30 nanometer (nm) to 200 nm.

[0081] In one embodiment, the element further includes a barrier layer disposed between the non-conductive layer and the conductive pad.

[0082] In one aspect, a bonded structure is disclosed. The bonded structure can include a first element that includes a non-conductive structure that has a non-conductive bonding surface, a cavity that extends at least partially through a thickness of the non-conductive structure from the non-conductive bonding surface, and a conductive pad that is disposed in the cavity. The cavity has a bottom side and a sidewall. The conductive pad has a bonding surface and a back side opposite the bonding surface. An average size of the grains at the bonding interface is at least 20% greater than an average size of the grains adjacent the bottom side of the cavity. The bonded structure can include a second element that has a second conductive pad. The conductive pad of the first element and the second conductive pad of the second element are directly bonded to one another without an intervening adhesive along a bonding interface.

[0083] In one embodiment, the second element further includes a second non-conductive structure that has a second non-conductive bonding surface that is directly bonded to the non-conductive bonding surface of the first element without an intervening adhesive.

[0084] In one embodiment, an average size of the grains at the bonding interface is at least 50% greater than an average size of the grains closer to the back side.

[0085] In one embodiment, an average size of the grains at the bonding interface is at least two times greater than an average size of the grains adjacent the bottom side of the cavity.

[0086] An average size of the grains at the bonding interface can be at least three times greater than an average size of the grains adjacent the bottom side of the cavity.

[0087] In one aspect, a method for forming an element is disclosed. The method can include providing a non-conductive structure that has a first side and a second side opposite the first side. The method can include forming a cavity in the non-conductive structure. The method can include providing a conductive material in the cavity and on a portion of the first side of the non-conductive layer. The conductive material has a lower side facing a bottom side of the cavity and an upper side opposite the lower side. The method can include cold

working the upper side of the conductive material to modify a grain structure of the conductive material. The cold working is conducted between about -196°C and 50°C. The method can include removing at least a portion of the conductive material to define a conductive pad that has a conductive bonding surface.

[0088] In one embodiment, the cold working includes mechanical peening or laser peening.

[0089] In one embodiment, the cold working includes bombarding the upper side of the conductive material with metal particles, glass particles, or ceramic particles.

[0090] In one embodiment, the cold working includes decreasing a percentage of 111 crystal planes in the conductive material.

[0091] The cold working includes inducing plastic deformation in the conductive material, and causing grain sizes of the conductive material at least at the upper side to be reduced compared to prior to the cold working.

[0092] In one embodiment, the cold working produces smaller grains sizes at the upper side of the conductive material compared to at the lower side of the conductive material.

[0093] In one embodiment, the method further includes annealing the conductive material to stabilize grain sizes of the conductive material prior to cold working.

[0094] In one embodiment, the removing includes at least partially removing the portion of the conductive material prior to cold working.

[0095] The method can further include preparing the conductive bonding surface of the conductive pad and the first side of the non-conductive structure for direct bonding.

[0096] In one embodiment, the method further includes providing a barrier layer between the non-conductive structure and the conductive material.

[0097] In one embodiment, a method for forming a bonded structure includes bonding the element to a second element having a second non-conductive structure and a second conductive pad.

[0098] The bonding can include directly bonding the non-conductive structure and the second non-conductive structure.

[0099] The bonding can further include annealing the conductive pad and the second conductive pad at a temperature between 50°C and 250°C.

[0100] The annealing can include annealing the conductive pad and the second conductive pad at a temperature between 50°C and 150°C.

[0101] The annealing the conductive pad and the second conductive pad can cause an average grain size of the conductive material at the upper side to be larger as compared to prior to the annealing.

[0102] The annealing the conductive pad and the second conductive pad can cause an average grain size of the conductive material at the upper side to be larger than an average grain size of the conductive material at the lower side.

[0103] In one aspect, an element is disclosed. The element can include a non-conductive structure that has a non-conductive bonding surface, a cavity that at least partially extends through a portion of a thickness of the non-conductive structure from the non-conductive bonding surface, and a conductive pad that is disposed in the cavity. The cavity has a bottom side and a sidewall. The conductive pad has a bonding surface and a back side opposite the bonding surface. The conductive pad includes a lower percentage of grains with vertically oriented 111 crystal planes at the bonding surface as compared with grains adjacent to the bottom side.

[0104] In one aspect, an element is disclosed. The element can include a non-conductive structure that has a non-conductive bonding surface, a cavity that at least partially extends through a portion of a thickness of the non-conductive structure from the non-conductive bonding surface, and a conductive feature that is disposed in the cavity. The cavity has a bottom side and a sidewall. The conductive feature has a bonding surface and a back side opposite the bonding surface. An average size of grains in a portion of the conductive feature near the bonding surface is less than 200 nanometer (nm).

[0105] In one embodiment, the average size of the grains in the portion of the conductive feature near the bonding surface is at least 50 nm.

[0106] In one aspect, a bonded structure is disclosed. The bonded structure can include a first element that includes a non-conductive structure that has a non-conductive bonding surface, a cavity that extends at least partially through a thickness of the non-conductive structure from the non-conductive bonding surface, and a conductive pad that is disposed in the cavity. The cavity has a bottom side and a sidewall. The conductive pad has a bonding surface and a back side opposite the bonding surface. The conductive pad includes

a crystal structure with grains oriented along a 111 crystal plane. An average grain size of the conductive pad at the bonding surface is greater than an average grain size of the conductive pad at the back side. The bonded structure can include a second element that has a second conductive pad. The conductive pad of the first element and the second conductive pad of the second element are directly bonded to one another without an intervening adhesive along a bonding interface.

[0107] In one aspect, a method for forming an element is disclosed. the method can include providing a non-conductive structure that has a first side and a second side opposite the first side. The method can include forming a cavity in the first side of the non-conductive structure. The method can include providing a conductive material in the cavity and over the first side of the non-conductive structure. The method can include increasing a grain size of the conductive material by thermal annealing. The method can include forming lattice imperfections in the annealed conductive material. The method can include forming a planar bonding surface comprising a non-conductive bonding surface and a conductive bonding surface. The conductive bonding surface includes the lattice imperfections.

[0108] In one embodiment, the method further includes providing a barrier layer between the non-conductive structure and the conductive material.

[0109] In one embodiment, the method further includes singulating the element on a dicing frame.

[0110] The method can further include providing a protective layer over the element and further cleaning off the protective layer particles from singulation from the bonding surface of the singulated element and the dicing frame.

[0111] The method can further include directly bonding a cleaned singulated element to a prepared bonding surface of a second substrate to form a bonded structure.

[0112] The method can further include annealing the bonded structure at a temperature below 200ºC to electrically bond the singulated element to the second substrate.

[0113] In one embodiment, the forming the lattice imperfections comprises cold working a surface of the annealed conductive material.

[0114] In one aspect, a bonded structure is disclosed. The bonded structure can include a first element that includes a non-conductive structure that has a non-conductive bonding surface, a cavity extending at least partially through a thickness of the nonconductive

structure from the non-conductive bonding surface, and a conductive pad that is disposed in the cavity. The cavity has a bottom side and a sidewall. The conductive pad has a bonding surface and a back side opposite the bonding surface. The conductive pad includes a longitudinal columnar grain structure oriented generally parallel to the non-conductive bonding surface. The bonded structure can include a second element that has a second conductive pad. The conductive pad of the first element and the second conductive pad of the second element are directly bonded to one another without an intervening adhesive along a bonding interface.

[0115] In one aspect, a bonded structure is disclosed. the bonded structure can include a first element that includes a planar conductive structure embedded in the surface of a non-conductive material that has a non-conductive bonding surface. The conductive structure has a longitudinal columnar grain structure oriented generally parallel to the non-conductive bonding surface. The bonded structure can include a second element that has a planar bonding surface. The bonding surface of the first element and the second element are directly bonded to one another without an intervening adhesive along a bonding interface.

[0116] In one aspect, a bonded structure is disclosed. The bonded structure can include a first element that includes a first conductive feature and a first non-conductive region. the bonded structure can include a second element that includes a second conductive feature that is directly bonded to the first conductive feature without an intervening adhesive and a second non-conductive region that is bonded to the first non-conductive region. The bonded first and second conductive features include grains. Each grain of the grains has a length along an bonding interface between the first and second element and a thickness perpendicular to the bonding interface. The grains have an average length that is at least 1.5 times larger than an average thickness of the grains.**[0069]** Unless the context clearly requires otherwise, throughout the description and the claims, the words “comprise,” “comprising,” “include,” “including” and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of “including, but not limited to.” The word “coupled”, as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Likewise, the word “connected”, as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally,

the words "herein," "above," "below," and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Moreover, as used herein, when a first element is described as being "on" or "over" a second element, the first element may be directly on or over the second element, such that the first and second elements directly contact, or the first element may be indirectly on or over the second element such that one or more elements intervene between the first and second elements. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word "or" in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[0117] Moreover, conditional language used herein, such as, among others, "can," "could," "might," "may," "e.g.," "for example," "such as" and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments.

[0118] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel apparatus, methods, and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. For example, while blocks are presented in a given arrangement, alternative embodiments may perform similar functionalities with different components and/or circuit topologies, and some blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these blocks may be implemented in a variety of different ways. Any suitable combination of the elements and acts of the various embodiments described above can be combined to provide further embodiments. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

WHAT IS CLAIMED IS:

1. An element comprising:

a non-conductive structure having a non-conductive bonding surface;

a cavity at least partially extending through a portion of a thickness of the non-conductive structure from the non-conductive bonding surface, the cavity having a bottom side and a sidewall; and

a conductive pad disposed in the cavity, the conductive pad having a bonding surface and a back side opposite the bonding surface, an average size of grains of the conductive pad at the bonding surface being smaller than an average size of the grains adjacent the bottom side of the cavity.

2. The element of Claim 1, wherein the non-conductive structure comprises a dielectric layer, and the non-conductive bonding surface of the non-conductive structure is prepared for direct bonding.

3. The element of Claim 2, wherein the conductive bonding surface of the conductive pad is prepared for direct bonding.

4. The element of Claim 2, wherein the conductive pad comprises is a copper (Cu) pad.

5. The element of Claim 4, wherein the conductive pad includes a lower percentage of grains with 111 crystal planes at the bonding surface compared with adjacent to the bottom side.

6. The element of Claim 4, wherein the conductive pad includes a higher percentage of grains with 220 crystal planes at the bonding surface compared with adjacent to the bottom side.

7. The element of Claim 1, wherein the average size of the grains adjacent the bottom side of the cavity is at least 3 times greater than the average size of the grains at the bonding surface.

8. The element of Claim 1, wherein the average size of the grains adjacent the bottom side of the cavity is at least 20 times greater than the average size of the grains at the bonding surface.

9. The element of Claim 1, wherein the average size of the grains adjacent the bottom side of the cavity is between 0.2 microns (μm) to 1 μm.

10. The element of Claim 1, wherein the average size of the grains at the bonding surface is between 30 nanometer (nm) to 200 nm.

11. The element of Claim 1, further comprising a barrier layer disposed between the non-conductive structure and the conductive pad.

12. A bonded structure comprising:

a first element including;

a non-conductive structure having a non-conductive bonding surface,

a cavity extending at least partially through a thickness of the non-conductive structure from the non-conductive bonding surface, the cavity having a bottom side and a sidewall, and

a conductive pad disposed in the cavity, the conductive pad having a bonding surface and a back side opposite the bonding surface, wherein an average size of grains of the conductive pad at the bonding interface is at least 20% greater than an average size of the grains adjacent the bottom side of the cavity, and

a second element having a second conductive pad,

wherein the conductive pad of the first element and the second conductive pad of the second element are directly bonded to one another without an intervening adhesive along a bonding interface.

13. The bonded structure of Claim 12, wherein the second element further includes a second non-conductive structure having a second non-conductive bonding surface that is

directly bonded to the non-conductive bonding surface of the first element without an intervening adhesive.

14. The bonded structure of Claim 12, wherein an average size of the grains at the bonding interface is at least 50% greater than an average size of the grains closer to the back side.

15. The bonded structure of Claim 12, wherein an average size of the grains at the bonding interface is at least two times greater than an average size of the grains adjacent the bottom side of the cavity.

16. The bonded structure of Claim 15, wherein an average size of the grains at the bonding interface is at least three times greater than an average size of the grains adjacent the bottom side of the cavity.

17. A method for forming an element, the method comprising:

providing a non-conductive structure having a first side and a second side opposite the first side;

forming a cavity in the non-conductive structure;

providing a conductive material in the cavity and on a portion of the first side of the non-conductive structure, the conductive material having a lower side facing a bottom side of the cavity and an upper side opposite the lower side;

cold working the upper side of the conductive material to modify a grain structure of the conductive material, wherein the cold working is conducted between about -196°C and 50°C; and

removing at least a portion of the conductive material to define a conductive pad having a conductive bonding surface.

18. The method of Claim 17, wherein the cold working comprises mechanical peening or laser peening.

19. The method of Claim 17, wherein the cold working comprises bombarding the upper side of the conductive material with metal particles, glass particles, or ceramic particles.

20. The method of Claim 17, wherein the cold working comprises decreasing a percentage of 111 crystal planes in the conductive material.

21. The method of Claim 20, wherein the cold working comprises inducing plastic deformation in the conductive material, and causing grain sizes of the conductive material at least at the upper side to be reduced compared to prior to the cold working.

22. The method of Claim 17, wherein the cold working produces smaller grains sizes at the upper side of the conductive material compared to at the lower side of the conductive material.

23. The method of Claim 17, further comprising annealing the conductive material to stabilize grain sizes of the conductive material prior to cold working.

24. The method of Claim 17, wherein the removing comprises at least partially removing the portion of the conductive material prior to cold working.

25. The method of Claim 24, further comprising preparing the conductive bonding surface of the conductive pad and the first side of the non-conductive structure for direct bonding.

26. The method of Claim 17, further comprising providing a barrier layer between the non-conductive structure and the conductive material.

27. A method for forming a bonded structure, the method comprising bonding the element of Claim 17 to a second element having a second non-conductive structure and a second conductive pad.

28. The method of Claim 27, wherein the bonding comprises directly bonding the non-conductive structure and the second non-conductive structure.

29. The method of Claim 28, wherein the bonding further comprises annealing the conductive pad and the second conductive pad at a temperature between 50°C and 250°C.

30. The method of Claim 29, wherein the annealing comprises annealing the conductive pad and the second conductive pad at a temperature between 50°C and 150°C.

31. The method of Claim 27, wherein annealing the conductive pad and the second conductive pad causes an average grain size of the conductive material at the upper side to be larger as compared to prior to the annealing.

32. The method of Claim 27, wherein annealing the conductive pad and the second conductive pad causes an average grain size of the conductive material at the upper side to be larger than an average grain size of the conductive material at the lower side.

33. An element comprising:

a non-conductive structure having a non-conductive bonding surface;

a cavity at least partially extending through a portion of a thickness of the non-conductive structure from the non-conductive bonding surface, the cavity having a bottom side and a sidewall; and

a conductive pad disposed in the cavity, the conductive pad having a bonding surface and a back side opposite the bonding surface, the conductive pad including a lower percentage of grains with vertically oriented 111 crystal planes at the bonding surface as compared with grains adjacent to the bottom side.

34. An element comprising:

a non-conductive structure having a non-conductive bonding surface;

a cavity at least partially extending through a portion of a thickness of the non-conductive structure from the non-conductive bonding surface, the cavity having a bottom side and a sidewall; and

a conductive feature disposed in the cavity, the conductive feature having a bonding surface and a back side opposite the bonding surface,

wherein an average size of grains in a portion of the conductive feature near the bonding surface is less than 200 nanometer (nm).

35. The element of Claim 34, wherein the average size of the grains in the portion of the conductive feature near the bonding surface is at least 50 nm.

36. A bonded structure comprising:

a first element including;

a non-conductive structure having a non-conductive bonding surface,

a cavity extending at least partially through a thickness of the non-conductive structure from the non-conductive bonding surface, the cavity having a bottom side and a sidewall, and

a conductive pad disposed in the cavity, the conductive pad having a bonding surface and a back side opposite the bonding surface, the conductive pad including a crystal structure with grains oriented along a 111 crystal plane, an average grain size of the conductive pad at the bonding surface being greater than an average grain size of the conductive pad at the back side, and

a second element having a second conductive pad,

wherein the conductive pad of the first element and the second conductive pad of the second element are directly bonded to one another without an intervening adhesive along a bonding interface.

37. A method for forming an element, the method comprising:

providing a non-conductive structure having a first side and a second side opposite the first side;

forming a cavity in the first side of the non-conductive structure;

providing a conductive material in the cavity and over the first side of the non-conductive structure;

increasing a grain size of the conductive material by thermal annealing;

forming lattice imperfections in the annealed conductive material; and

forming a planar bonding surface comprising a non-conductive bonding surface and a conductive bonding surface, and

wherein the conductive bonding surface comprises the lattice imperfections.

38. The method of Claim 37, further comprising providing a barrier layer between the non-conductive structure and the conductive material.

39. The method of Claim 37, further comprising singulating the element on a dicing frame.

40. The method of Claim 39, further comprising providing a protective layer over the element and further cleaning off protective layer particles from singulation from the bonding surface of the singulated element and the dicing frame.

41. The method of Claim 40, further comprising directly bonding a cleaned singulated element to a prepared bonding surface of a second substrate to form a bonded structure.

42. The method of Claim 41, further comprising annealing the bonded structure at a temperature below 200ºC to electrically bond the singulated element to the second substrate.

43. The method of Claim 37, wherein forming the lattice imperfections comprises cold working a surface of the annealed conductive material.

44. A bonded structure comprising:

a first element including;

a non-conductive structure having a non-conductive bonding surface,

a cavity extending at least partially through a thickness of the non-conductive structure from the non-conductive bonding surface, the cavity having a bottom side and a sidewall, and

a conductive pad disposed in the cavity, the conductive pad having a bonding surface and a back side opposite the bonding surface, the conductive pad including a longitudinal columnar grain structure oriented generally parallel to the non-conductive bonding surface, and

a second element having a second conductive pad,

wherein the conductive pad of the first element and the second conductive pad of the second element are directly bonded to one another without an intervening adhesive along a bonding interface.

45. A bonded structure comprising:

a first element including;

a planar conductive structure embedded in a surface of a non-conductive material having a non-conductive bonding surface,

the conductive structure having a longitudinal columnar grain structure oriented generally parallel to the non-conductive bonding surface, and

a second element having a planar bonding surface,

wherein the bonding surface of the first element and the second element are directly bonded to one another without an intervening adhesive along a bonding interface.

46. A bonded structure comprising:

a first element including a first conductive feature and a first non-conductive region, and

a second element including a second conductive feature directly bonded to the first conductive feature without an intervening adhesive and a second non-conductive region bonded to the first non-conductive region,

wherein the bonded first and second conductive features include grains each having a length along an bonding interface between the first and second element and a thickness perpendicular to the bonding interface, the grains have an average length that is at least 1.5 times larger than an average thickness of the grains.

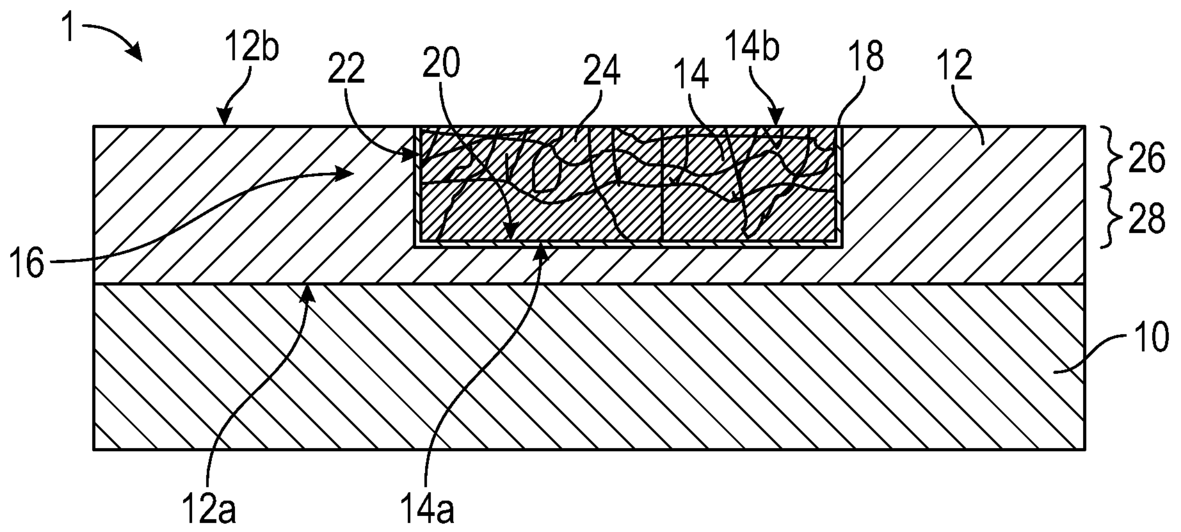


FIG. 1

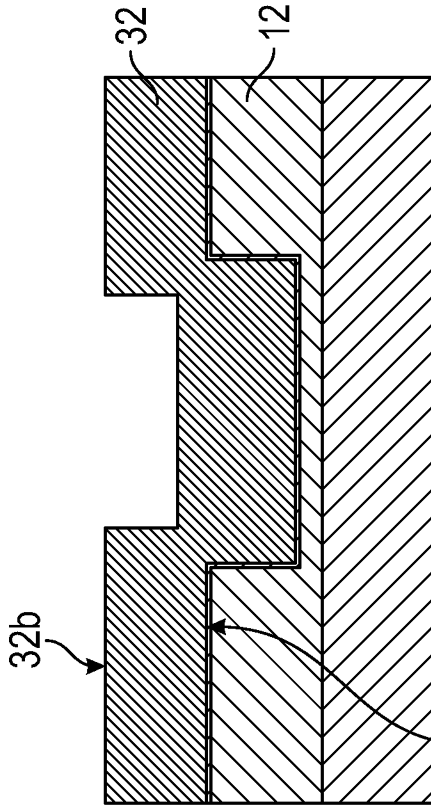


FIG. 2C

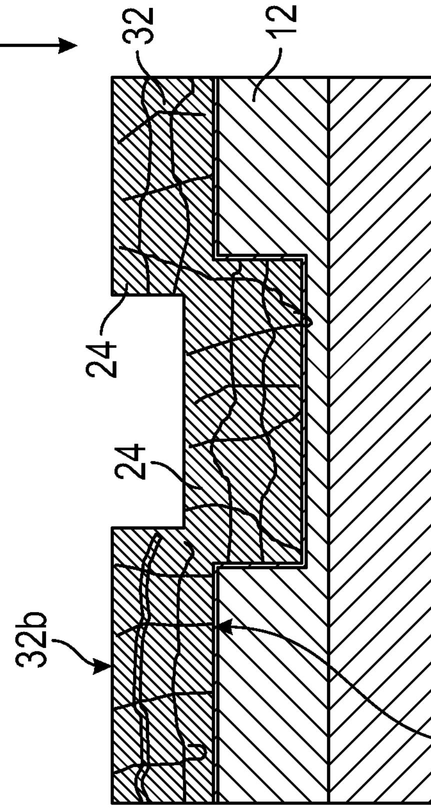


FIG. 2D

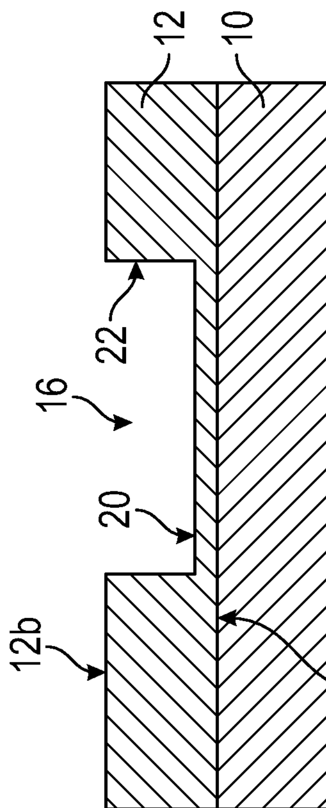


FIG. 2A

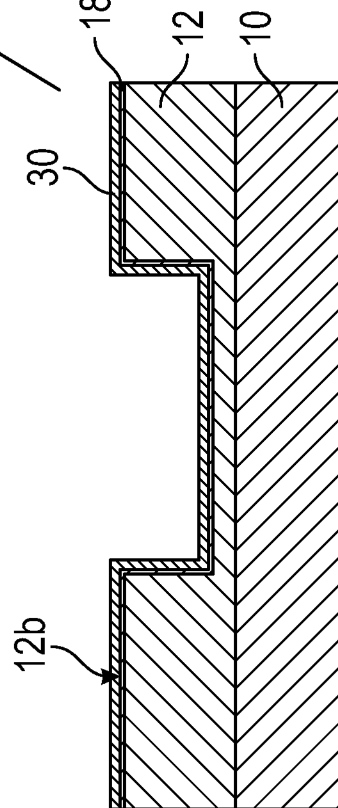


FIG. 2B

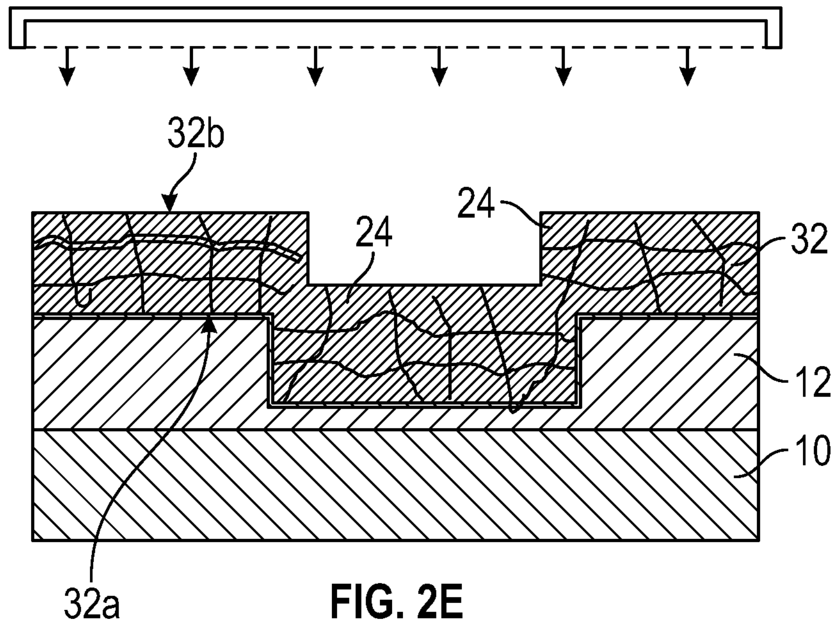


FIG. 2E

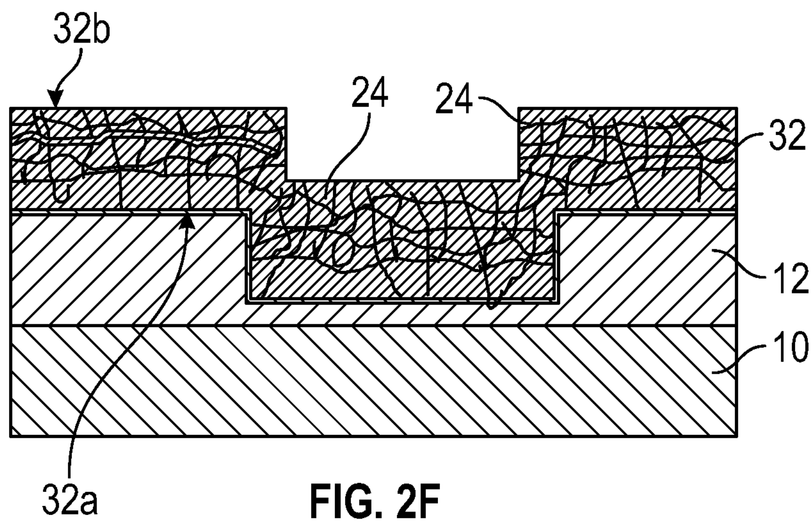


FIG. 2F

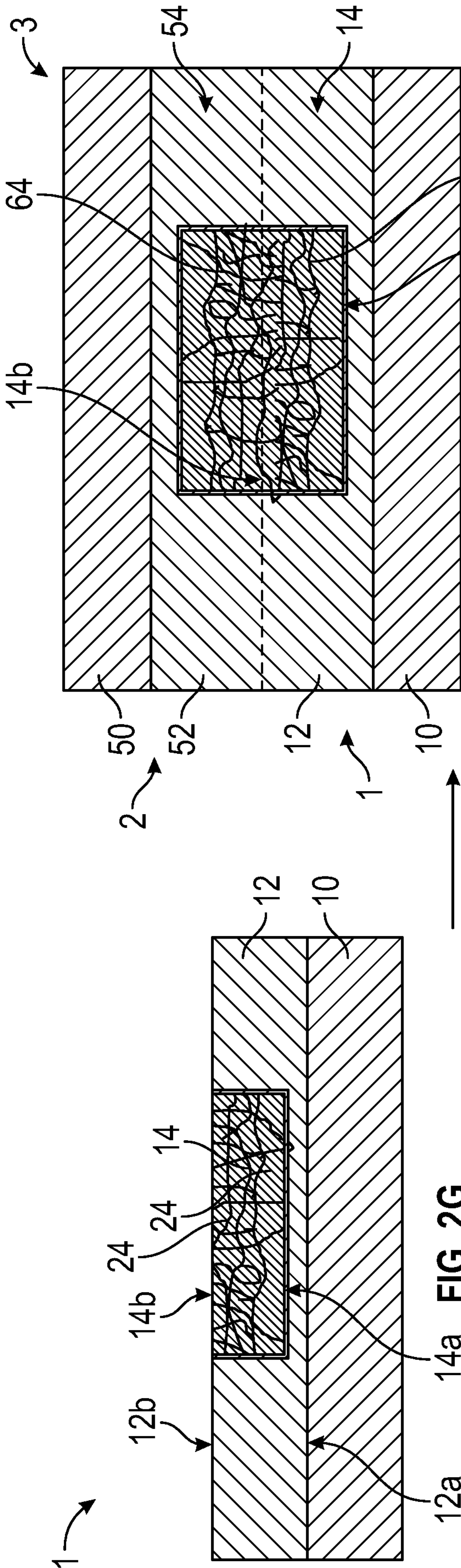


FIG. 2H

FIG. 2G

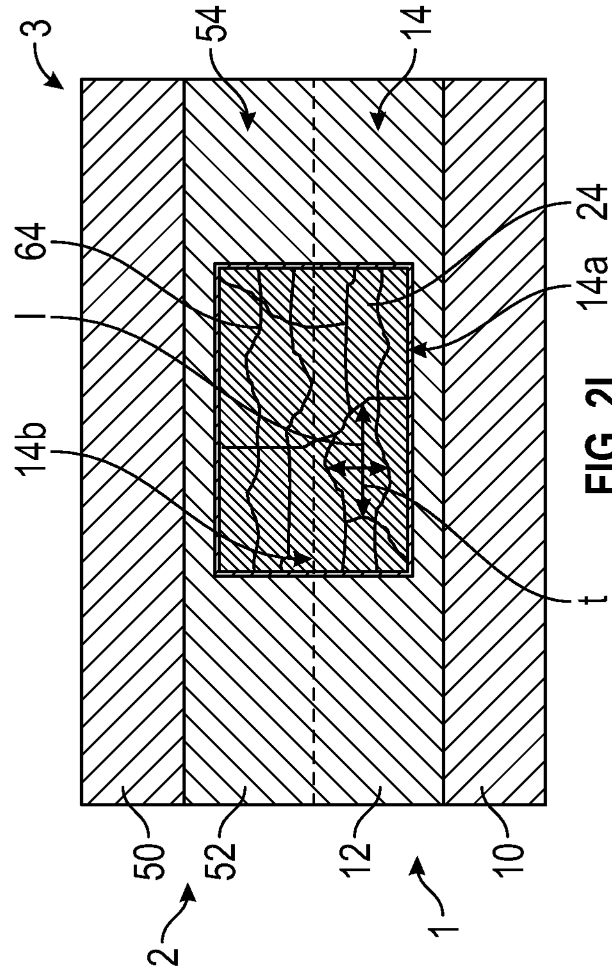


FIG. 2I

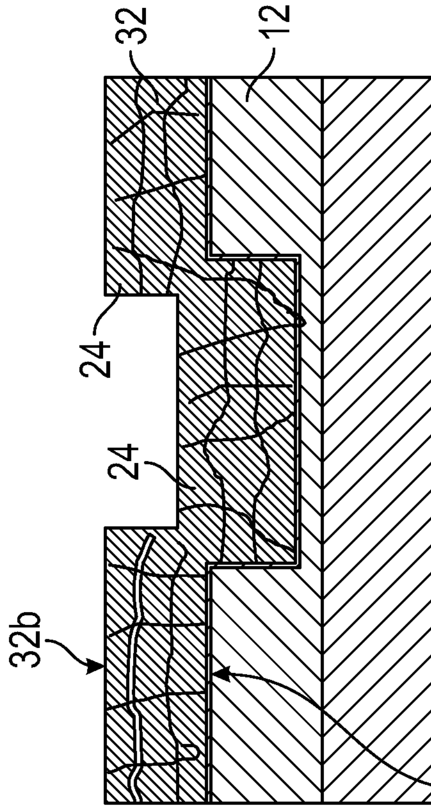


FIG. 3C

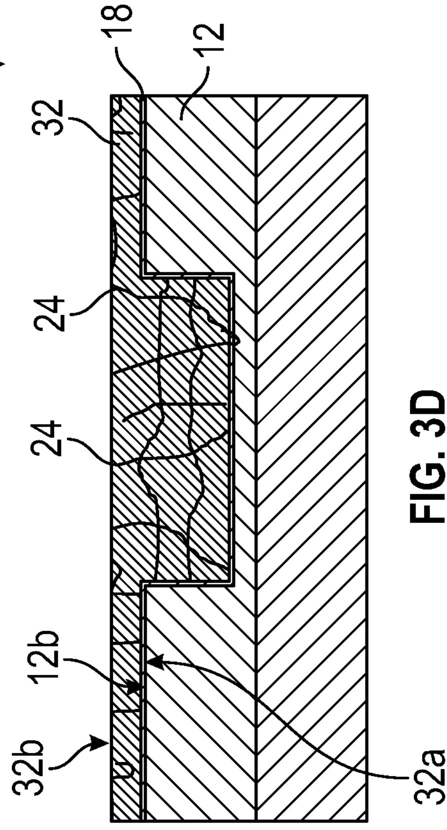
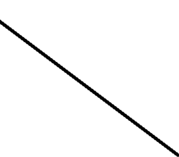


FIG. 3D



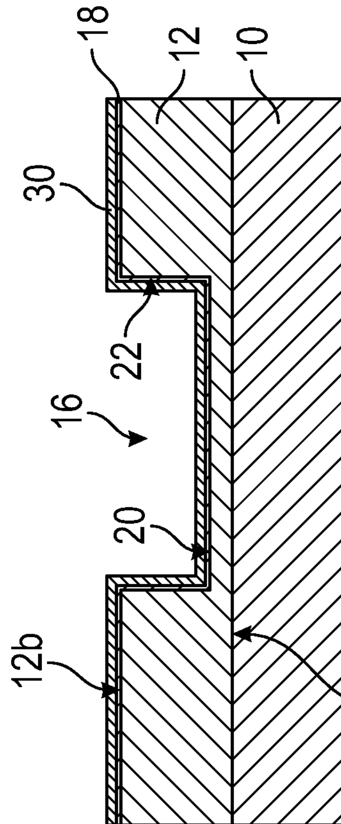


FIG. 3A

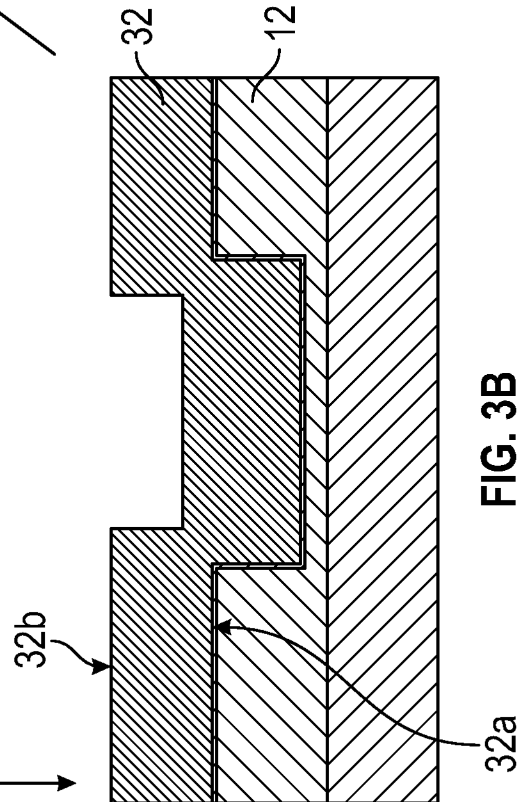


FIG. 3B

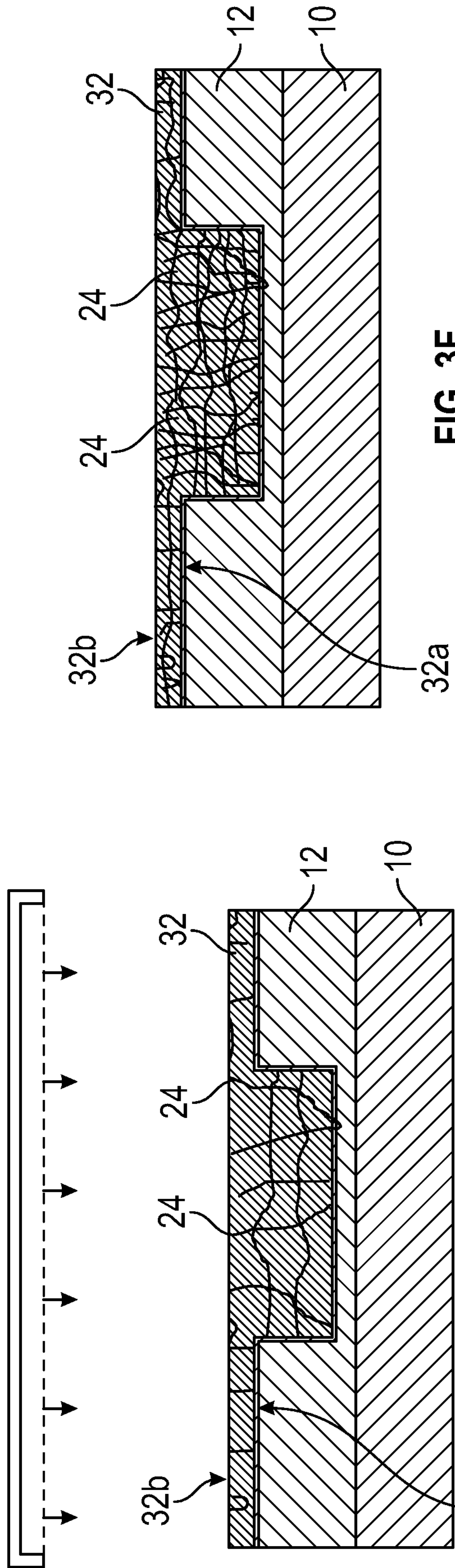


FIG. 3F

FIG. 3E

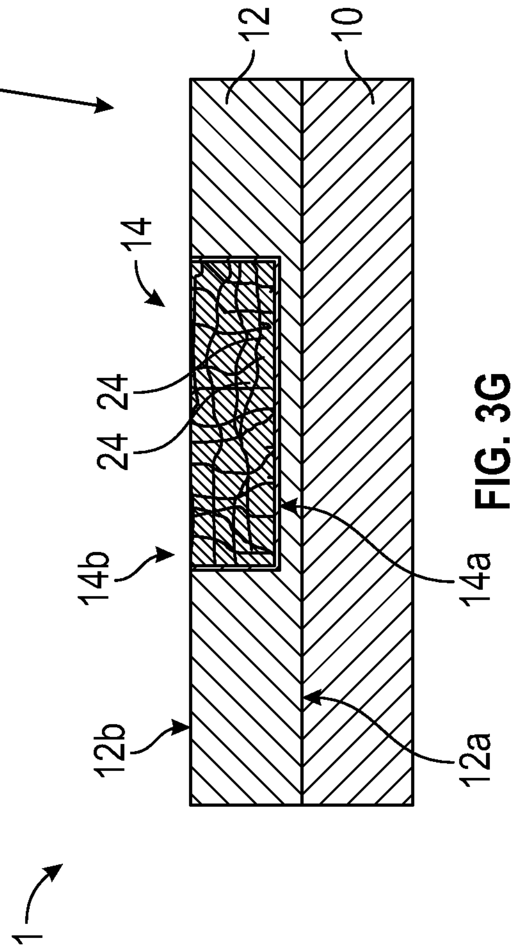


FIG. 3G

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2021/073169

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 23/00(2006.01); H01L 21/02(2006.01); H01L 25/065(2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: direct bonding, bonding pad, grain size, cold working, crystal plane

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2020-0194396 A1 (INVENSAS BONDING TECHNOLOGIES, INC.) 18 June 2020 (2020-06-18) See paragraphs [0027]-[0091] and figures 2-10.	1-46
A	US 2016-0020183 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 21 January 2016 (2016-01-21) See paragraphs [0010]-[0027] and figures 1-3B.	1-46
A	US 2020-0006280 A1 (PRIYAL SHAH et al.) 02 January 2020 (2020-01-02) See paragraphs [0044]-[0050] and figures 2-11.	1-46
A	US 2015-0380368 A1 (FUJI ELECTRIC CO., LTD.) 31 December 2015 (2015-12-31) See paragraphs [0054]-[0061] and figures 4-5.	1-46
A	US 2013-0252399 A1 (COMMISSARIAT A L`ENERGIE ATOMIQUE ET AUX ENE ALT) 26 September 2013 (2013-09-26) See paragraphs [0071]-[0087] and figures 1A-2B.	1-46

☐ Further documents are listed in the continuation of Box C.   ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 April 2022	**22 April 2022**

Name and mailing address of the ISA/KR	Authorized officer
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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2021/073169

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