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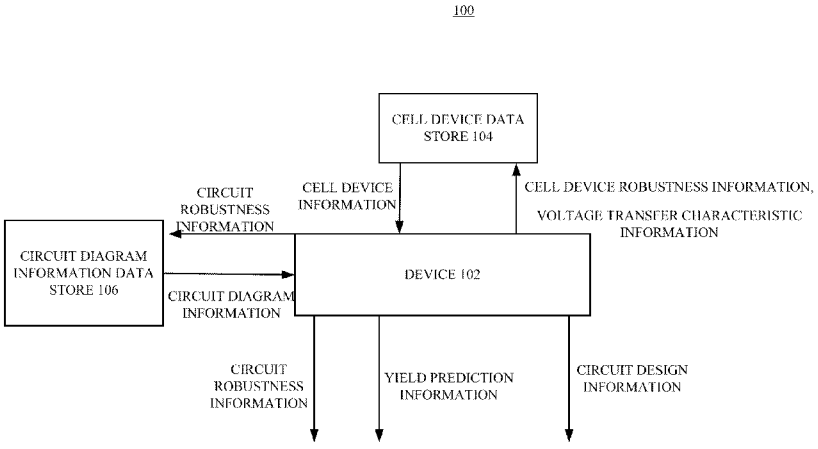

FIG. 1

(57) Abstract: Technologies are generally described that relate to analysis of circuits and that facilitate determination of electronic circuit robustness. An example method includes performing, for a cell device by a unit including a processor, statistical analysis to obtain statistical information for the cell device that is indicative of a robustness of the cell device. The robustness of the cell device pertains to a parameter variation of the cell device that is related to a noise of the cell device. The method also includes determining a characteristic of the cell device based on the statistical information.

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DETERMINATION OF ELECTRONIC CIRCUIT ROBUSTNESS

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application is related to and claims the benefit of the earliest available effective filing date from the following listed application: United States Provisional Patent Application No. 61/838,037, titled "Method for Quantifying Electronic Circuit Robustness," naming Sean J. Keller and Alain J. Martin as inventors, filed June 21, 2013, which is currently co-pending.

[0002] All subject matter of the listed application is incorporated herein by reference to the extent such subject matter is not inconsistent herewith.

TECHNICAL FIELD

[0003] The subject disclosure relates generally but not exclusively to determination of electronic circuit robustness.

BACKGROUND

[0004] Unless otherwise indicated herein, the materials described in this section are not prior art to the claims in this application and are not admitted to be prior art by inclusion of this section.

[0005] Design of efficient and robust modern binary digital systems can be an arduous task. The use of numerous levels of logical abstraction may be typically employed due to the sheer complexity of utilizing upwards of a billion, for example, devices in modern binary digital systems. Errors introduced at different levels of abstraction can result in circuits that fail to function as expected for a number of reasons (e.g., timing, logical, functional, and/or other types of failures). Understanding and quantifying these different modes of failure can be useful, but failures in the base digital assumption can supersede all other failures. If a gate cannot switch between logic values, then the gate may not be able to perform computation, for example.

[0006] With regard to static direct current (DC) analysis, logic gates in modern technologies may exhibit a number of frequency-dependent effects. Incorporating these effects can greatly increase the complexity of analysis.

SUMMARY

[0007] In various, non-limiting embodiments, systems, devices, and/or computer-readable storage media that facilitate determination of electronic circuit robustness are described herein.

[0008] In some embodiments, methods include performing, for a cell device by a unit including a processor, statistical analysis to obtain statistical information for the cell device. The statistical information can be indicative of robustness of the cell device. In these embodiments, the robustness of the cell device pertains to a parameter variation of the cell device that is related to a noise of the cell device. The methods can also include determining a characteristic of the cell device based on the statistical information.

[0009] In other embodiments, other methods are described. For example, methods can include determining, by a unit including a processor, characteristics that pertain to respective cell devices associated with circuit diagram information. The characteristics can include functions of respective robustness data for the cell devices. In these embodiments, the methods can also include determining a quantification of reliability for the circuit diagram information based on composing respective characteristics for the cell devices of the circuit diagram information.

[0010] In other embodiments, yet other methods are described. For example, methods can include determining, by a unit including a processor, characteristics that pertain to candidate cell devices that are candidates for association with a circuit. The characteristics can include functions of respective robustness data for the candidate cell devices. The respective robustness data can be associated with parameter variations of the candidate cell devices that are related to noises of the plurality of candidate cell devices. In these embodiments, the methods can also include selecting one or more cell devices of the candidate cell devices based on the determined characteristics for the candidate cell devices.

[0011] In some embodiments, devices are described. For example, some devices can include a first component configured to perform statistical analysis for a cell device to determine a robustness of the cell device. The robustness of the cell device can be associated with a parameter variation of the cell device that is related to a noise of the cell device. The devices can also include a second component coupled to the first component and configured to generate statistical information for the cell device based on the statistical analysis. The statistical information can be indicative of the robustness of the cell device. The devices can also include a third component coupled to the second component and configured to determine a characteristic of the cell device based on the statistical information.

[0012] In some embodiments, non-transitory computer-readable storage media are described. For example, non-transitory computer-readable storage media having computer-executable instructions stored thereon that, in response to execution by a processor, cause a device to perform operations are described. The operations can include determining characteristics that pertain to respective cell devices associated with circuit diagram information. The characteristics can include functions of respective robustness data for the cell devices. The respective robustness data can be based on parameter variations of the respective cell devices and noises of the respective cell devices. The operations can also include determining a quantification of reliability for the circuit diagram information based on composing the respective characteristics for the cell devices of the circuit diagram information.

[0013] The foregoing summary is illustrative only and is not intended to be in any way limiting. In addition to the illustrative aspects, embodiments, and features described above, further aspects, embodiments, and features will become apparent by reference to the drawings and the following detailed description.

BRIEF DESCRIPTION OF THE FIGURES

[0014] The foregoing and other features of this disclosure will become more fully apparent from the following description and appended claims, taken in conjunction with the accompanying drawings. Understanding that these drawings depict only several embodiments in accordance with the disclosure and are, therefore, not to be considered limiting of its scope, various non-limiting embodiments are further described with reference to the accompanying drawings in which:

[0015] **FIG. 1** illustrates an example block diagram of a system configured to facilitate determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0016] **FIG. 2** illustrates an example block diagram of cell device information stored within a cell device data store and employed by the system of **FIG. 1** to facilitate determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0017] **FIG. 3** illustrates an example block diagram of circuit diagram information stored within a circuit diagram information data store and employed by the system of **FIG. 1** to facilitate determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0018] **FIG. 4** illustrates an example block diagram of a device of the system of **FIG. 1** and configured to facilitate determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0019] **FIG. 5** illustrates an example block diagram of a robustness determination component of the device of **FIG. 4** and configured to facilitate determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0020] **FIG. 6** illustrates an example block diagram of a circuit design component of the device of **FIG. 4** and configured to generate information for circuit design based on determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0021] **FIGS. 7-10** illustrate example flowcharts of methods associated with determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0022] **FIG. 11** illustrates an example graph of statistical voltage transfer characteristics (VTCs) for 100 Monte Carlo trials of a minimum-size inverter and which may be employed for determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0023] **FIG. 12** illustrates an example circuit of a cross-coupled inverter pair and direct circuit noise voltage sources for which electronic circuit robustness can be determined in accordance with one or more embodiments described herein;

[0024] **FIG. 13** illustrates an example graph of statistical voltage transfer characteristics for a minimum-size inverter and which may be employed for determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0025] **FIGS. 14**, **15**, **16** and **17** illustrate example graphs depicting probability density distributions for input parameters for an inverter at respective values of V_{DD} values, and which may be employed for determination of electronic circuit robustness in accordance with one or more embodiments described herein

[0026] **FIG. 18** illustrates example graphs of a ratio of input VTC parameter variance to output VTC parameter variance in a complementary metal-oxide semiconductor (CMOS) for determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0027] **FIG. 19** illustrates example graphs of correlation between input parameters for determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0028] **FIGS. 20**, **21**, **22**, **23** and **24** illustrate example graphs depicting probabilities of minimum-size cross-coupled inverter-pair failure for respective noise margin threshold values for determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0029] **FIG. 25** illustrates an example of an infinite chain construct equivalent to the cross-coupled pair of **FIG. 12** for determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0030] **FIG. 26** illustrates an example of a chain of inverters for determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0031] **FIGS. 27**, **28**, **29, 30, 31** illustrate example graphs depicting probabilities of failure for minimum-size inverters in chains for determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0032] **FIG. 32** illustrates an example NAND2 circuit diagram for determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0033] **FIGS. 33** and **34** illustrate example graphs of VTCs for the minimum-size NAND2 for determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0034] **FIG. 35** illustrates an example circuit diagram of NAND2 inverter equivalence for determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0035] **FIG. 36** illustrates an example graph of NAND2 input correlation for determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0036] **FIG. 37** illustrates an example circuit diagram detailing equivalent gate pairs formed from multiple fan-in and fan-out gate networks for determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0037] **FIGS. 38** and **39** illustrate example graphs depicting probabilities of a chain of 20 alternating NAND2 and NOR2 gates failing for respective noise margin thresholds for determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0038] **FIG. 40** illustrates an example graph of maximum number of equivalent gate pairs versus V_{DD} for chains of alternating gates and combinations from a defined set of gates for determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0039] **FIG. 41** illustrates an example graph of maximum noise margin threshold versus V_{DD} for chains of alternating gates and combinations from a defined set of gates for determination of electronic circuit robustness in accordance with one or more embodiments described herein;

[0040] **FIG. 42** illustrates an example block diagram of a computing device that is arranged for quantification of circuit robustness in accordance with one or more embodiments described herein.

DETAILED DESCRIPTION

[0041] In the following detailed description, reference is made to the accompanying drawings, which form a part hereof. In the drawings, similar symbols typically identify similar components, unless context dictates otherwise. The illustrative embodiments described in the detailed description, drawings, and claims are not meant to be limiting. Other embodiments may be utilized, and other changes may be made, without departing from the spirit or scope of the subject matter presented herein. The aspects of the present disclosure, as generally described herein, and illustrated in the Figures, can be arranged, substituted, combined, separated, and designed in a wide variety of different configurations, all of which are explicitly contemplated herein.

[0042] Parameter variation can be caused by stochastic process variation and intrinsic parameter fluctuations (IPF). Parameter variation can be a reason why modern digital circuits that function at the process nominal supply voltage (for example, V_{DD}) may eventually fail as the supply is lowered. Further, parameter variation may make functional digital circuits less robust and hence less reliable. This reduction in robustness may be of little consequence at the process nominal supply voltage V_{DD}, but, as V_{DD} is lowered, the reduction in robustness may become a more substantial design concern.

[0043] In modern complementary metal oxide semiconductor (CMOS) technologies, device parameters such as channel length, oxide thickness and dopant concentration can have significant deviations from nominal values due to process-induced and/or intrinsic parameter fluctuations. Process variability may be considered a global, predictable, and gradual skew in device characteristics introduced by the complexity of manufacturing chips (e.g., from thermal gradients during fabrication). Intrinsic parameter fluctuations may be truly statistical in nature and may cause significant deviations from device to device within a chip.

[0044] Circuit noise (e.g., thermal noise) can result from physical components and/or man-made digital switching components. Possible dominant sources of noise from physical

components in modern CMOS, which may have significant impact on radio frequency (RF) CMOS circuits, may include 1/frequency (1/f) noise and thermal noise. Switching noise can be caused by the rapid full-rail voltage swings typical in digital systems, and can include cross-talk due to capacitive and inductive coupling, charge sharing, supply-rail and ground noise, and/or substrate noise.

[0045] Increasing parameter variation in circuits can tend to reduce robustness to noise. Intrinsic variations can be attributed to atomistic effects (e.g., random dopant fluctuation (RDF)) and device structure variations (e.g., line edge roughness (LER)). There may be a number of different ways to characterize and partition these effects, and the approach used herein is to consider a global component wherein all devices on a chip may be affected in the same way, and a local component wherein each device on a chip may have a number of statistical parameters drawn from distributions with mean values set by the global skew.

[0046] Considering variation in terms of a global component and a local component may simplify statistical analysis while permitting a circuit designer to choose, for example, a worst-case 3σ global corner wherein the die that fall outside of this range are assumed not to yield. The worst case 3σ global corner refers to the instance of global Process Voltage Temperature (PVT) variation at which the functional yield is minimal.

[0047] For a circuit's operating subthreshold, the local component of variation can be dominated by RDF and can be accurately modeled by a normally distributed uncorrelated device threshold, V_t, variation. Near-threshold, local variation may exhibit some degree of spatial correlation, and at the process nominal supply voltage V_{DD}, spatial correlation can be significant. This increase in the spatial correlation of local variation as a function of V_{DD} can be attributed to the fact that channel-length variation may have little effect on devices' operating subthreshold but may become the dominant effect at approximately twice the threshold voltage. Channel length variation can be spatially correlated between devices within some radius, and can be straightforward to model.

[0048] Given that one feature of the embodiments described herein is to quantify the robustness of low-power subthreshold and near-threshold circuits, local parameter variation can be treated as random and uncorrelated; however, the effects of spatial correlation can be included. Furthermore, in some embodiments, SPICE electronic circuit simulations, along with foundry-provided statistically-extracted BSIM4 models, are employed for the embodiments described herein as a basis for correctness; these models are considered accurate over the entire device operating range. Most of the figures make use of the statistical BSIM4 models (the corresponding plotted data are typically referred to as "Actual" within

the figures). These models form the base case and are assumed to be representative of actual silicon. As such, these models are referred to as "Actual" in figures throughout.

[0049] Briefly stated, technologies are generally described that relate to analysis of circuits and that facilitate determination of electronic circuit robustness. An example method may include performing, for a cell device by a unit including a processor, statistical analysis to obtain statistical information for the cell device that is indicative of a robustness of the cell device. The robustness of the cell device may pertain to a parameter variation of the cell device that is related to a noise of the cell device. The method may also include determining a characteristic of the cell device based on the statistical information. In some embodiments, determining the characteristic may include determining the statistical voltage transfer characteristics (VTC) of the cell device. In various embodiments, the parameter variation of the cell device may include at least one of the channel length variation, the oxide thickness variation or the dopant concentration variation of a component of the cell device, relative to another cell device.

[0050] In some embodiments, information indicative of a description of the cell devices from circuit diagram information can be obtained. Circuit diagram information can include information describing the function or components of a circuit for which circuit robustness is to be determined. In response to quantifying the circuit robustness, the yield of the circuit diagram information can be predicted.

[0051] In some embodiments, a circuit to be included in a device can be selected based on the prediction of yield and/or quantification of circuit robustness generally. Being able to quantify the robustness of a circuit makes it possible to predict yield and to perform new optimizations (or other customization or tailoring) that include robustness when considering gate choice and transistor sizing during cell design and optimization, circuit design and optimization, and/or place and route.

[0052] The embodiments described herein may account for parameter variation and may be therefore suitable for modern low-voltage circuit analysis. Futher, noise margin based analysis of memory cells and other devices/circuits may be described using a generalized noise margin target based analysis as opposed to a simple binary failure model (e.g., statistical noise margin (SNM) > 0 or SNM < 0).

[0053] One or more of the embodiments described herein can analyze the robustness of a circuit, or chip, in an efficient and scalable manner with any number of elements (e.g., transistors, etc.). In some examples, the circuits, or chips to which the disclosed embodiments apply may include those having one million to one billion transistors, for

example. Further, circuit robustness can be included alongside energy, delay, and area during circuit design and optimization. A computation aspect of the embodiments may be applied to a defined set of cell devices typically included in cell device libraries and memories, and the calculation of robustness cost may be generally linear in the number of instances of these cell devices.

[0054] Further, one or more of the embodiments described herein can define a method to calculate robustness in such a way that the robustness can be feasibly computed for large circuits (e.g., billions of gates), and which may also fit in with any suitable method of system design, inlcuding standard-cell hierarchical digital circuit design. As such, a new compact model for statistical robustness is described herein with parameters that can be stored alongside timing and energy data in a cell device data store (e.g., cell libraries). Moreover, the model employed by a device to determine robustness can be defined such that the compact data is composable. Compact data may be composable if the robustness of an arbitrary network of standard cells is computable by the composition of robustness data from member cell devices. In this way, the robustness of a large circuit (built out of standard cells) can be readily calculated.

[0055] Turning now to the drawings, **FIG. 1** illustrates an example block diagram of a system configured to facilitate determination of electronic circuit robustness in accordance with one or more embodiments described herein. **FIG. 2** illustrates an example block diagram of cell device information stored within a cell device data store and employed by the system of **FIG. 1** to facilitate determination of electronic circuit robustness in accordance with one or more embodiments described herein. **FIG. 3** illustrates an example block diagram of circuit diagram information stored within a circuit diagram information data store and employed by the system of **FIG. 1** to facilitate determination of electronic circuit robustness in accordance with one or more embodiments described herein.

[0056] Turning first to **FIG. 1**, system 100 can include device 102, cell device data store 104 and/or circuit diagram information data store 106. In various embodiments, device 102 can be electrically and/or communicatively coupled (or otherwise operationally coupled) to one or more of cell device data store 104 and/or circuit diagram information data store 106 to perform one or more functions or operations of device 102 and/or system 100.

[0057] System 100 can facilitate determination of cell device and/or circuit robustness in various embodiments. In some embodiments, system 100 can also facilitate generation yield prediction information for a circuit analyzed by device 102 based on robustness of the circuit. Further, in some embodiments, system 100 can facilitate generation of circuit design

information such as identification of specific cell devices and interconnections of cell devices to design circuits that satisfy defined conditions relative to robustness, probability of circuit failure or other factor(s).

[0058] As shown, device 102 can receive cell device information from cell device data store 104. In some embodiments, cell device data store 104 may be a cell device library storing information about one or more cell devices that can be selected for design of an electronic circuit. For example, in some embodiments, cell device data store 104 may be or may include an electronic design automation cell device electronic library.

[0059] With reference to **FIGS. 1** and **2**, cell device information can include any number of different types of information that describe a type of the cell device. The information indicating the type of cell device can include, but is not limited to, text, symbols, data or other information descriptive of the components or materials or interconnections of the cell device. By way of example, but not limitation, cell devices can include logic gates (e.g., NAND2 gates, NOR2 gates, or other types of gates and configurations thereof), transistors, inverters (e.g., cross-coupled inverter, chain of inverters, or other types of gates and configurations thereof), memory devices, registers or any number or type of other devices that may be employed in the design of electronic circuits. As used herein, a "NAND2" gate means a 2-input NAND gate (as opposed to a NAND gate having a number of inputs other than two inputs). As used herein, a "NOR2" gate means a 2-input NOR gate (as opposed to a NOR gate having a number of inputs other than two inputs).

[0060] Further, in the embodiment shown, cell device information may be received at device 102 from cell device data store 104. However, in various embodiments, device 102 can receive cell device information from any number of different sources including, but not limited to, as information entered or provided to device 102 via an input device (e.g., mouse, keyboard) or via network connection.

[0061] In response to receipt of the cell device information, device 102 can perform statistical analysis to generate statistical information descriptive of the robustness of the cell device. In particular, device 102 can describe the robustness of the cell device as relates to parameter variation for the cell device when noise is experienced by the cell device. The parameters for which variation can occur for a cell device can be any number of different parameters including, but not limited to, channel length variation, oxide thickness variation, dopant concentration variation of the cell device (or a component of the cell device), or other type of variation(s) and combination(s) thereof.

[0062] Device 102 can determine cell device robustness information and/or one or more VTCs for the cell device based on the cell device robustness determination, and associate the one or more VTCs with the cell device. For example, in some embodiments, information indicative of one or more VTCs for a cell device can be stored by device 102 in the cell device data store 104 with statistical noise margin information for the cell device. Accordingly, device 102 can determine a VTC for a cell device based on variation of a parameter (e.g., channel length) when noise is experienced by the cell device.

[0063] As shown in **FIG. 2**, in some embodiments, the type of cell device, statistical noise margin information and robustness information and/or VTC information can be stored (for instance by device 102) in cell device data store 104 in some embodiments. In other embodiments, information indicative of one or more VTCs for a cell device can be associated with an identifier and stored in a location other than cell device data store 104. For example, the information indicative of the one or more VTCs and the identifier can be stored in device 104 or at a data store remote from cell device data store 104.

[0064] As also shown in **FIG. 1**, device 102 can receive circuit diagram information descriptive of one or more cell devices of a circuit and, in some embodiments, interconnections between the one or more cell devices. In various embodiments, any number of different arrangements of text, cell device or other symbols, graphical information or the like can be provided to describe the composition of a circuit. In some embodiments, circuit diagram information can be a netlist. While the embodiment of **FIG. 1** illustrates the circuit diagram information being received at device 102 from circuit diagram information data store 106, in other embodiments, as with cell device information, circuit diagram information can be received from other sources such as via input devices and/or via network connection from sources remote from device 102.

[0065] Circuit diagram information can be received after, currently with or prior to determination of cell device robustness and/or VTC information; however, device 102 can determine or identify robustness information and/or VTC information for one or more cell devices of the circuit diagram prior to determining circuit robustness. For example, the information can be previously-determined by device 102 prior to receipt of circuit diagram information or determined after receipt of circuit diagram information.

[0066] Device 102 can determine information indicative of the robustness of a circuit composed of one or more cell devices for which robustness information has been generated. For example, device 102 can receive and/or access circuit diagram information for a circuit having one or more cell devices for which device 102 has generated robustness information

(or for which device 102 can generate robustness information after receipt of the circuit diagram information).

[0067] Device 102 can determine the robustness of the circuit based on an accumulation of robustness data for one or more of the cell devices of which the circuit is composed. Methods for determination of circuit robustness will be described in greater detail with reference to **FIGS. 4**. In this regard, for example when circuit diagram information is provided via a netlist, the method of determining robustness can be linear in the number of edges in a netlist graph. The edges of the netlist graph refer to the logical input to the output connections (e.g., wires) between logic gates.

[0068] In some embodiments, device 102 can store robustness information for the circuit in circuit diagram information data store 106. In other embodiments, device 102 can store the information at device 102 and/or at a data store located remote from circuit diagram information data store 106.

[0069] In some embodiments, device 102 can employ the robustness information for a circuit to predict yield of the circuit.

[0070] In some embodiments, device 102 can employ the robustness information for a circuit to generate circuit design information descriptive of a circuit design including one or more cell devices or including one or more circuits for which device 102 has generated robustness information. For example, in some embodiments, device 102 can generate circuit design information including details of particular cell devices, place and route to yield a defined desired circuit performance. For example, device 102 can select one or more of the cell devices of the candidate cell devices based on the determined characteristics or robustness data for the candidate cell devices.

[0071] As shown in **FIG. 1**, circuit robustness information can be output from device 102, and therefore can be transmitted to one or more other systems or devices for circuit design, performance evaluation, modeling, or other use(s). However, as described above, in some embodiments, device 102 can perform yield prediction based on robustness information generated for the circuit for which circuit diagram information is received by device 102.

[0072] Details associated with determination of cell device and/or circuit robustness and/or yield prediction will be described in greater detail with reference to **FIG. 4**. **FIG. 4** illustrates an example block diagram of a device of the system of **FIG. 1** and configured to facilitate determination of electronic circuit robustness in accordance with one or more embodiments described herein. **FIG. 5** illustrates an example block diagram of a robustness determination component of the device of **FIG. 4** and configured to facilitate determination

of electronic circuit robustness in accordance with one or more embodiments described herein. Repetitive description of like elements employed in respective embodiments of systems and/or apparatus described herein are omitted for sake of brevity.

[0073] Methods of computing robustness for cross-coupled inverters (for example) are provided followed by methods of computing robustness for chains of inverters (for example) and finally methods of computing robustness for gates, generally and for example. As shown in **FIG. 4**, device 102 can include communication component 400, robustness determination component 402, prediction component 404, circuit design component 406, memory 408, processor 410 and/or data storage 412. In various embodiments, one or more of communication component 400, cell device robustness determination component 402, circuit robustness component 404, circuit design component 406, memory 408, processor 410 and/or data storage 412 can be electrically and/or communicatively coupled (or otherwise operatively coupled) to one another to perform one or more functions or operations of device 102. The various elements/components of device 102 (as well as other elements/components shown in the various Figures) can be implemented in hardware, software (or other computer-readable instructions stored on a non-transitory computer readable medium and executable by one or more processors), or a combination of hardware and software (or other computer-readable instructions).

[0074] Communication component 400 can transmit and/or receive information to and/or from device 102. For example, in various embodiments, communication component 400 can receive text, alphanumeric information, symbols representative of cell devices or circuits, or other types of information and combination(s) thereof. For example, the text can be a description of a cell device or circuit. In some embodiments, communication component 400 can receive or access statistical information previously-generated by device 102 and/or stored in a cell device data store or circuit diagram information source or data store.

[0075] Communication component 400 can transmit text or other information indicative of statistical information, an identity or descriptor of a cell device, an identity and/or descriptor of a circuit, or other types of information and combination(s) thereof. Communication component 400 can transmit information to a data store (e.g., cell device data store, circuit diagram information data store).

[0076] In various embodiments, although not shown, communication component 400 can receive and/or transmit information via a network (e.g., Internet, wireless local area network (WLAN), wire line connection, etc.), and/or via a direct electrical connection between a data store and device 102. In some embodiments, communication component 400 can transmit

and/or receive information to/from an interface to which device 102 is electrically and/or communicatively coupled.

[0077] As also shown in **FIG. 4**, device 102 can include robustness determination component 402. Robustness determination component 402 can determine the robustness of a cell device and/or a circuit composed of one or more cell devices. The robustness can be based on the parameter variation and effects of noise on the cell device. In various embodiments, robustness determination component 402 can determine the robustness for an entire circuit based on robustness information for one or more of the cell devices from which the circuit is composed.

[0078] Robustness determination component 402 will be described in greater detail below and with reference to **FIG. 5**. As shown in **FIG. 5**, robustness determination component 402 can include communication component 400, statistical analysis / characterization component 500, quantification component 502, memory 408, processor 410 and/or data storage 412. In various embodiments, one or more of communication component 400, statistical analysis / characterization component 500, quantification component 502, memory 408, processor 410 and/or data storage 412 can be electrically and/or communicatively coupled (or otherwise operatively coupled) to one another to perform one or more functions or operations of robustness determination component 402.

[0079] Statistical analysis / characterization determination component 500 can perform statistical analysis based on a description of a cell device to obtain statistical information for the cell device. The statistical information generated can be indicative of the robustness of the cell device. The robustness of the cell device can be a measure that takes into account parameter variation of the cell device that is related to a noise of the cell device.

[0080] Parameter variation of the cell device can include or be a variation of any number of different aspects of the cell device and/or can depend on the particular type of cell device. For example, the parameter variation can include the channel length variation, oxide thickness variation, dopant concentration variation, or other parameter variation(s) and combination(s) thereof. Characteristics of cell devices such as channel length, oxide thickness, or dopant concentration can have significant deviations from their nominal values due to process-induced and intrinsic parameter fluctuations

[0081] Statistical analysis / characterization determination component 500 can also determine one or more VTCs to characterize the cell device. For example, statistical analysis / characterization determination component 500 can determine the characteristic based on the statistical information generated.

[0082] Quantification component 502 can generate robustness information for the cell device. In some embodiments, quantification component 502 can generate robustness information for a circuit including one or more cell devices. For example, quantification component 502 can determine or access a previously-determined robustness for the one or more cell devices. Quantification component 502 can aggregate robustness information for the different cell devices in the circuit and generate a robustness value for the entire circuit.

[0083] Robustness determination component 402 (and components thereof), statistical analysis characterization determination component 500 and quantification component 502 can be further described as noted below. In particular, robustness determination component 402 (and/or components thereof) can quantify cross-coupled inverter robustness, robustness for a chain of inverters, robustness for memory and robustness for a number of different types of gates.

DETERMINATION OF CROSS-COUPLED INVERTER ROBUSTNESS

[0084] Parameter variation and noise can have a significant impact on circuit robustness. As such, increasing parameter variation may tend to reduce robustness to noise. For example, for two circuits, C_1 and C_2, operating at the same supply voltage, C_1 may be more robust than C_2 if C_1 can tolerate more noise than C_2. Accordingly, as circuit noise increases, C_2 may fail to function before C_1 fails to function. With statistical parameter variation, the occurrence of failure can be represented in terms of probability of failure. Accordingly, robustness can be defined such that C_1 may be more robust than C_2 if, for the same quantity of noise in both circuits, the probability that C_1 fails is less than the probability that C_2 fails.

[0085] In the embodiments described herein, robustness determination component 402 can determine the probability of active device parametric failure and corresponding circuit robustness. Specifically, robustness determination component 402 can determine the probability of active device parametric failure in which a cell device (e.g., gate or memory) erroneously changes state between binary digital values due to parameter variation. Circuit noise may act to make these failures more likely.

[0086] In order to quantify functional failures due to variation and noise, a guideline can be determined that provides guideance on what it means for a gate or memory to change state. Toward this, consider the base digital assumption: the abstraction of networks of transistors as logic-gates, and logic-gates as Boolean functions over Boolean logic-values. This abstraction may use an example guideline of a mapping between logic-values and a

physical quantity: the electrical potential of charge stored on capacitive gate nodes. In the simplest mapping, nodes near the supply rail potential, V_{DD}, may represent a logic-1, and nodes near ground (GND) may represent a logic-0. As used herein, $V_{DD,}$ supply rail voltage, and supply rail potential are synonymous.

[0087] In a real CMOS circuit, no two gates may be identical. They may differ in function, topology, and sizing; and distinct instances of the same gate can differ because of parameter variation. Consider an inverter, for example. If a 0 is applied to its input, then a 1 may be typically produced on its output. Similarly, a 1 at the input may typically result in a 0 at the output. However, in some instances (e.g., intentional construction or parameter variation), two distinct inverters, INV_1 and INV_2, can have different outputs given the same inputs.

[0088] For example, for input voltages near V_{DD} or GND, INV_1 and INV_2 can behave logically identically and correctly (e.g., invert), but for some input voltage, V_X, between V_{DD} and GND, INV_1 can produce a 0 as an output while INV_2 produces a 1 as an output. In this situation, INV_1 and INV_2 interpret V_X differently. The situation can be further complicated when the notion of the output voltage level is considered. That is, for example, the output of INV_1 is really only a 0 when a subsequent gate interprets it as such, and so on down a chain of gates.

[0089] Since different gates can have different interpretations of input voltages, a mapping between voltage levels and logic values can be defined in terms of the manner in which a subsequent gate interprets the output (as opposed to using a global bound). That is, for example, if worst-case boundaries on voltages are a high voltage boundary, V_H, and a low voltage boundary, V_L (in which it is known that all gates in a circuit interpret voltages above V_H as a 1 and all voltages below V_L as 0), then the mapping of $V(G) > V_H \leftrightarrow 1$ and $V(G) < V_L \leftrightarrow 0$ can be sufficient for some notion of correct operation, but it is not necessary. As used hererein, V(G) refers to the voltage applied to the input node of a gate.

[0090] Consider an example that demonstrates the trouble with using the worst-case definitions for V_H and V_L in low-voltage applications. **FIG. 11** illustrates an example graph of statistical voltage transfer characteristics (VTCs) for 100 Monte Carlo trials of a minimum-size inverter and which may be employed for determination of electronic circuit robustness in accordance with one or more embodiments described herein. Specifically, **FIG. 11** illustrates 100 instances of a minimum-size inverter in a modern 40 nanometer (nm)

low-power bulk CMOS process with V_{DD} = 200 millivolts (mV) at 25 degrees Celsius (°C) (typical-typical) TT-Corner. The curves vary significantly due to random parameter variation. These statistical VTCs have remarkably similar shapes and are nearly identical modulo horizontal translation. As such, it can be reasonable to consider defining $V_H = 180mV$ and $V_L = 20mV$ as worst-case output high and low voltages, respectively (these boundaries are also depicted by the dash-dot and the dashed lines, respectively in **FIG. 11**). However, worst-case can result in ranges that overlap.

[0091] In some embodiments, device 102 can employ statistical noise margin (SNM) analysis to determine circuit robustness. **FIG. 12** illustrates an example circuit of a cross-coupled inverter pair and direct circuit noise voltage sources for which electronic circuit robustness can be determined in accordance with one or more embodiments described herein. The SNM of this cross-coupled pair may represent the largest DC noise voltage, V_{noise}, that can be applied between the bistable pair before the inverters switch state (e.g., between logic-0 and logic-1). If the SNM of a cross-coupled pair is less than or equal to zero (e.g., due to parametric variation), then the pair may not be bistable; is the cell may be unable to hold two distinct logic states (a functional failure). If the SNM of the pair is infinitesimally greater than zero, then the cell can hold two distinct logic states, but a diminutive noise can act to switch these states, so the cell may not be robust. Given that noise may be typically present, in some embodiments, a cross-coupled pair of inverters in a digital system may be designed to have static noise margins in excess of the system noise in order to maintain state. In some embodiments, in real memories (e.g., static random access memory (SRAM) arrays), the SNM during both reading and writing of cells may be considered. Furthermore, ensuring a SNM of greater than zero may be typical, but it may not be sufficient for ensuring read stability and write-ability.

[0092] **FIG. 13** illustrates an example graph of statistical voltage transfer characteristics for a minimum-size inverter and which may be employed for determination of electronic circuit robustness in accordance with one or more embodiments described herein, and more specifically, **FIG. 13** shows an example VTC for a minimum-size inverter in a commercial 40 nm low-power CMOS process (V_{DD} = 1.1 volts (V) at 25 °C). Device 102 can identify the unity gain points of the inverter shown in **FIG. 13** to define the statistical VTC parameters: maximum output voltage, V_{OH} , miniumum output voltage, V_{OL}, maximum input voltage, V_{1H}, and minimum input voltage, V_{IL}.

[0093] Statistical analysis / characterization determination component 500 can perform statistical analysis on the unity gain points (e.g., $|\frac{dV_{out}}{dV_{in}}|=1$) of the statistical VTCs to measure the SNMs for the inverter. As used herein, dV_{out} and dV_{in} mean the change in V_{out} and the change in V_{in}, RESPECTIVELY. For example, with reference to FIGS. 12 and 13, INV_a (INV_b) can represent a static CMOS inverter having a single negative channel field effect transistor (NFET) and positive channel field effect transistor (PFET) with the statistical VTC depicted in **FIG. 13**.

[0094] The functionality of the inverter and/or the definition of SNM can rely on two properties of the statistical VTC holding: (1) two unity gain points exist and (2) the slope between the unity gain points exceeds unity in absolute value. From these unity gain points, four properties of an inverter statistical VTC can be defined: Vo_H , V_{OL}, V_{1H}, V_{1L}, as shown in **FIG. 13**. These four points may be referred to as statistical VTC parameters throughout.

[0095] The statistical VTC parameters can identify definable boundaries between the voltages that are interpreted as a logic-1 or logic-0, and the undefined region of high-gain in between. That is, V_{1H} can be considered the lowest voltage that the inverter correctly interprets as a 1 and V_{1L} as the highest voltage that it correctly interprets as a 0 . Similarly, V_{OH} can be considered the lowest voltage that the inverter will output as a 1, and V_{OL} the highest voltage that the inverter will output as a 0.

[0096] In general, when one gate drives another gate, a static noise margin can be defined. This static noise margin can be separated into two components: a noise margin high (NM_H) and a noise margin low (NM_L) (one for each logic value). Consider a pair of inverters, with INV_x driving INV_y. The two components of the corresponding noise margin can be defined as shown in Equations 1 and 2 below:

$$NM_H(INV_x - INV_y) = V_{OH}(INV_x) - V_{IH}(INV_y) \text{ (Equation 1).}$$

$$NM_H(INV_x - INV_y) = V_{OH}(INV_x) - V_{IH}(INV_y) \text{ (Equation 2).}$$

[0097] The static noise margin can be defined as the smaller of NM_H or NM_L. Equation 3 can result.

$$SNM\ (INV_x\ ,\ INV_y) = \min(\ NM_L(INV_x,\ INV_y),\ NM_H(INV_x,\ INV_y)) \text{ (Equation 3).}$$

[0098] The relationships in Equations 1, 2 and 3 can be implicit functions of $V_{DD.}$ For cross-coupled inverters, as in **FIG. 12**, INV_a may drive INV_b , and INV_b may drive INV_a , and, as such, two different static noise margins can be defined, SNM (INV_a , INV_b) and SNM (INV_b , INV_a). Employing assumptions that the statistical VTCs may be monotonic and may

have a single inflection point, the condition that SNM (INV_a , INV_b) > V_{noise} ∩ SNM (INV_b , INV_a) > V_{noise} can be, in some embodiments, a sufficient condition for differentiation of binary logic-values by way of the electrical potential stored on the output of each inverter.

[0099] The SNM of the cross-coupled inverters, extended to incorporate parametric variability, and generalized to apply to various different types of gates, can be employed by quantification component 502 to quantify circuit robustness. In particular, statistical analysis / characterization determination component 500 and/or quantification component 500 can define a robustness metric for cross-coupled inverters that includes parameter variation and noise by way of a statistical noise margin constraint.

[00100] As described above, when considering two different circuits, C_1 and C_2, operating with the same supply voltage, C_1 may be more robust than C_2 if for the same quantity of noise in both circuits the probability that C_1 fails is less than the probability that C_2 fails. That is, for two different circuits C_1 and C_2, the relationship described by Equation 4 may be true:

$$ROB(C_1) > ROB(C_2) \leftrightarrow P(FAIL((C_1)) < P(FAIL((C_2)) \text{ (Equation 4).}$$

where ROB refers to circuit robustness and FAIL refers to circuit failure.

[00101] Switching noise in digital circuits can be estimated and reduced/optimized at some cost; e.g., spreading wires reduces coupling noise at the expense of area. As such, the circuit designer can choose a noise margin target, NM_T. Noise margin target can be the minimum noise margin constraint for all gates. A unique noise margin target can be chosen for one or more (or all) of the gates (if desired). In this way, noisy gates can be assigned larger targets than quiet gates. In the embodiments described herein, statistical analysis / characterization determination component 500 can operate according to the assumption that if any gate has a noise margin less than or equal to the NM_T, then the gate is said to fail, as is the entire circuit containing the failing gate.

[00102] Consider a cross-coupled inverter-pair, INV_a and INV_b, (as in **FIG. 12** with $V_{noise} = 0V$) operating at a particular V_{DD}. The probability of failure for a pair can then be defined as shown in Equation 5:

$$P(FAIL(INV_a, NM_T) \cup FAIL(INV_b, NM_T) = P(SNM((INV_a, INV_b) \leq NM_T \cup SNM(INV_b, INV_a) \leq NM_T) \text{ (Equation 5).}$$

[00103] For a circuit, C_a, having n cross-coupled inverter-pairs, e.g., $C_a = (INV_a^i, INV_b^i)$ for $i \in \{1, 2, ..., n\}$, Equation 6 can result:

$$P(FAIL(C_a, NM_T)) = P(\bigcup_{i\in\{1,2,\ldots,n\}} FAIL(INV_a^i, NM_T) \cup FAIL(INV_b^i, NM_T)$$

(Equation 6).

[00104] As such, robustness can be determined, by quantification component, for a cross-coupled inverter pair cell device by application of Equations 5 and 6. The relationships shown in Equations 5 and 6 can treat both the probability of failure and SNM as random variables (RVs). However, to compute the values for the variables in Equations 5 and 6, the corresponding distributions and the effects of correlation are considered below.

[00105] Distributions and effects of correlation can be determined based on an analysis of one or more statistical VTC parameters. Device parameter variation can result in variation in the SNMs of inverters, gates, etc.. The precise relationship can be based on the type of parameter variation and the device operating regime (e.g., subthreshold and above threshold). As described, the variation in SNM can be analyzed in terms of NM_H and NM_L variation (see Equation 3). Similarly, NM_H and NM_L can be considered in terms of the corresponding statistical VTC parameters, V_{OH}, V_{IH} and V_{OL} , V_{IL} associated with NM_H and NM_L (see Equations 1 and 2).

[00106] In modern bulk CMOS technologies, the output statistical VTC parameters of a gate, V_{OH} and V_{OL}, can be considered regular (not random) variables. In some embodiments, evaluating first-order effects, V_{OH} and V_{OL} can be considered global constants dependent on temperature when operating in the subthreshold regime. Including second order effects and near-threshold operation can induce a dependence on V_{DD} and gate topology, in some embodiments. As such, V_{OH} and V_{OL} may be treated as regular variables in the embodiments described herein while the input statistical VTC parameters, V_{IH} and V_{IL}, may be treated as normal random variables.

[00107] Referring to **FIG. 11** for a particular gate (an inverter) operating at a particular supply voltage (e.g., 200mV), the output statistical VTC parameters, V_{OH} and V_{OL}, may be nearly constant and close to V_{DD} and GND, respectively (consider the dash-dot and dashed lines). The horizontal translation between this family of statistical VTC curves, which can be due to random parameter variation, can correspond to shifts in the input statistical VTC parameters, V_{IH} and V_{IL}.

[00108] **FIGS. 14**, **15**, **16** and **17** illustrate example graphs depicting probability density distributions for input parameters for an inverter at respective values of V_{DD} values, and which may be employed for determination of electronic circuit robustness in accordance with one or more embodiments described herein. In **FIG. 14**, shown are example V_{IH} and V_{IL} distributions for a minimum-size inverter in a commercial 40 nm low-power CMOS process

at the TT-Corner ($V_{DD} = 200mV$ at 25 °C). In **FIG. 15**, shown are example V_{IH} and V_{IL} distributions for a minimum-size inverter in a commercial 40 nm low-power CMOS process at the TT-Corner ($V_{DD} = 600mV$ at 25 °C). In **FIG. 16**, shown are examples of the the V_{IH} and V_{IL} distributions for a minimum-size inverter in a commercial 40 nm low-power CMOS process at the TT-Corner ($V_{DD} = 1.1V$ at 25 °C). In **FIG. 17**, shown are examples of the V_{IH} distributions for a minimum-size inverter in a commercial 40 nm low-power CMOS process ($V_{DD} = 300mV$ at 25 °C). Global variation may shift the mean value for both V_{IH} and V_{IL}.

[00109] **FIG. 18** illustrates example graphs of a ratio of input VTC parameter variance to output VTC parameter variance in a CMOS for determination of electronic circuit robustness in accordance with one or more embodiments described herein. Specifically, **FIG. 18** shows an example of the ratio of input statistical VTC parameter variance to output statistical VTC parameter variance in a commercial 40 nm low-power CMOS process (25 °C, TT-Corner).

[00110] The large ratio across the entire operating range can facilitate approximation of the output statistical VTC parameters as regular variables, whereas the input statistical VTC parameters may be considered random variables.

[00111] The input statistical VTC parameters may be normally distributed with mean and standard deviation determined by the supply voltage, gate topology, temperature, and/or global corner. This may be shown by the analysis of two standard cell libraries in different technologies and from different foundries (e.g., a 40 nm low-power process and a 65-nm low-power process). Both cell libraries may contain hundreds of cell devices, and Anderson-Darling normality testing may show that neither V_{IH} nor V_{IL} have any significant departure from normality over the entire operating range. The Anderson-Darling normality test is a statistical test of whether a given sample of data is drawn from a given probability distribution. Furthermore, it can be difficult to verify that the tails of purportedly normal distributions are actually normal; as such, treating V_{IH} and V_{IL} and normal RVs can be considered an approximation.

[00112] **FIGS. 14**, **15** and **16** depict example V_{IH} and V_{IL} histograms along with corresponding normal probability density funstions (PDFs) for a minimum-size inverter operating sub-threshold, near threshold and at process nominal V_{DD}, respectively. Global variation can skew the mean value, as depicted in **FIG. 17**. **FIG. 18** further supports the treatment of the output VTC parameters as regular variables because the spread of each input VTC parameter may be several orders of magnitude greater than the corresponding output VTC parameter spread.

[00113] At any particular global corner, local parameter variation can be uncorrelated. As such, the statistical VTC parameters for distinct inverters, gates, etc. can be independent. Consider two distinct inverters, INV_x driving INV_y; INV_x and INV_y have independent normally distributed input statistical VTC parameters. From Equations 1 and 2 and the assumption that the corresponding output statistical VTC parameters may be regular variables, it follows that the corresponding NM_H and NM_L may also be normally distributed random variables (RVs) with mean and standard deviation given by Equations 7 and 8 shown below:

$$\mu(NM_H(INV_x, INV_y) = V_{OH}(INV_x) - \mu(V_{IH}(INV_y)), \sigma(NM_H(INV_x, INV_y)) = \sigma(V_{IH}(INV_y))$$

(Equation 7).

$$\mu(NM_L(INV_x, INV_y) = \mu(V_{IL}(INV_y) - V_{OL}(INV_x)), \sigma(NM_L(INV_x, INV_y)) = \sigma(V_{IL}(INV_y))$$

(Equation 8).

where for any RV Z, $\mu(Z)$ and $\sigma(Z)$ denote the mean value of the random variable and the standard deviation of the random variable, respectively. However, the statistical SNM may not follow directly from Equation 3 (due to the min function). If $NM_H(INV_x, INV_y)$ and $NM_L(INV_x, INV_y)$ are independent, order statistics can be used by quantification component 502 to directly calculate $SNM(INV_a, INV_b)$. However, in some embodiments, $NM_H(INV_x, INV_y)$ and $NM_L(INV_x, INV_y)$ may not be independent.

[00114] **FIG. 19** illustrates example graphs of correlation between input parameters for determination of electronic circuit robustness in accordance with one or more embodiments described herein. Specifically, **FIG. 19** shows an example correlation between V_{IH} and V_{IL} in a commercial 40 nm low-power CMOS process (25 °C, TT-Corner). These input statistical VTC parameters may be highly positively correlated across V_{DD} for a wide variety of gates. From **FIG. 19**, it is clear that the input statistical VTC parameters may be highly positively correlated, and it follows from this and Equations 7 and 8 that NM_H and NM_L may be highly negatively correlated, which can make the direct calculation of SNM difficult.

[00115] In embodiments described herein, quantification component 502 can employ NM_H and NM_L directly to calculate the probability that a circuit fails, thus avoiding the need to compute SNM. In this way, the effects of correlation can be accounted for, and a general method for failure analysis is made possible.

[00116] The failure probability, and thus robustness, of a cross-coupled inverter pair can be computed by quantification component 502 as follows. Again, consider a cross-coupled

inverter-pair, INV_a and INV_b, (as in **FIG. 12** with $V_{noise} = 0V$) operating at a particular V_{DD} and with a noise margin target of NM_T.

[00117] Quantification component 502 can calculate the probability of failure from Equation 5 by evaluation of $P(SNM(INV_a, INV_b) \leq NM_T \cup SNM(INV_b, INV_a) \leq NM_T)$. Assuming statistical independence, the disjunction can be treated as an addition, and Equation 5 reduces to Equation 9 shown below:

$$P(FAIL(INV_a, NM_T) \cup FAIL(INV_b, NM_T) = P(SNM((INV_a, INV_b) \leq NM_T + P(SNM(INV_b, INV_a) \leq NM_T) \quad \text{(Equation 9)}.$$

[00118] To calculate this quantity in closed-form, Equation 9 can be re-termed by using NM_H and NM_L in lieu of SNM. In order to do this, upper and lower bounds on failure may be determined, and then an approximation may be given.

[00119] The upper bound on failure for a cross-coupled inverter pair can be determined as follows. If $SNM(INV_a, INV_b) \leq NM_T$, then $NM_H(INV_a, INV_b) \leq NM_T$ and/or $NM_L(INV_a, INV_b) \leq NM_T$ (following directly from Equation 3). This can be stated in terms of probabilities as shown in Equation 10 below:

$$P(SNM(INV_a, INV_b) \leq NM_T) \leq P(NM_H(INV_a, INV_b) \leq NM_T \cup NM_L(INV_a, INV_b) \leq NM_T) \quad \text{(Equation 10)}.$$

[00120] Due to the high degree of anti-correlation between NM_H and NM_L, the disjunction can be approximated as an addition as shown in Equation 11 below:

$$P(SNM(INV_a, INV_b) \leq NM_T) \leq P(NM_H(INV_a, INV_b) \leq NM_T + P(NM_L(INV_a, INV_b) \leq NM_T) \quad \text{(Equation 11)}.$$

[00121] Due to symmetry, a similar argument can hold for $SNM(INV_b, INV_a)$, so combining Equations 9 and 11 can yield an upper bound on the probability of failure for cross-coupled inverters. That is, the upper bound on the probability for failure for a cross-coupled inverter pair can be as shown in Equation 12:

$$P(FAIL(INV_a, NM_T) \cup FAIL(INV_b, NM_T) \leq P(NM_H(INV_a, INV_b) \leq NM_T) + P(NM_L(INV_a, INV_b) \leq NM_T) + P(NM_H(INV_b, INV_a) \leq NM_T) + P(NM_L(INV_b, INV_a) \leq NM_T) \quad \text{(Equation 12)}.$$

[00122] The lower bound on failure for a cross-coupled inverter pair can be determined as follows. If $NM_H(INV_a, INV_b) \leq NM_T$ and $NM_L(INV_a, INV_b) \leq NM_T$, then $SNM(INV_a, INV_b) \leq NM_T$ (following directly from Equation 3). This can be stated in terms of probabilities as shown in Equation 13 shown below:

$$P(SNM(INV_a, INV_b) \leq NM_T) > P(NM_H(INV_a, INV_b) \leq NM_T \cap NM_L(INV_a, INV_b) \leq NM_T) \text{ (Equation 13).}$$

[00123] Due to the high degree of anti-correlation between NM_H and NM_L, the conditional probability of each event ($NM_H(INV_a, INV_b) \leq NM_T$, and $NM_L(INV_a, INV_b) \leq NM_T$) may be less than the unconditional probability, so Equation 14 results and is shown below:

$$P(SNM(INV_a, INV_b) \leq NM_T) > P(NM_H(INV_a, INV_b) \leq NM_T) * P(NM_L(INV_a, INV_b) \leq NM_T) \text{ (Equation 14).}$$

[00124] Due to symmetry, a similar argument can hold for $SNM(INV_b, INV_a)$. As such, combining Equations 9 and 14 can yield a lower bound on the probability of failure for cross-coupled inverters. That is, the lower bound on the probability for failure for a cross-coupled inverter pair can be as shown in Equation 15:

$$P(FAIL(INV_a, NM_T) \cup FAIL(INV_b, NM_T)) > P(NM_H(INV_a, INV_b) \leq NM_T) * P(NM_L(INV_a, INV_b) \leq NM_T) + P(NM_H(INV_b, INV_a) \leq NM_T) * P(NM_L(INV_b, INV_a) \leq NM_T) \text{ (Equation 15).}$$

[00125] A heuristic approximation of the probability of failure for a cross-coupled inverter pair can be determined as follows. One way to approximate the probability of failure comes from the consideration of the cross-coupled inverter pair as a whole. If INV_A is skewed such that it can barely interpret a logical-0 and INV_B is skewed such that is can barely interpret a logical-1 (or vice versa), then a failure may be likely. That is, if $NM_H(INV_a, INV_b) \leq NM_T$ and $NM_L(INV_b, INV_a) \leq NM_T$, or if $NM_H(INV_b, INV_a) \leq NM_T$ and $NM_L(INV_a, INV_b) \leq NM_T$, then it may be likely that $SNM(INV_a, INV_b) \leq NM_T$ or $SNM(INV_b, INV_a) \leq NM_T$. Empirically, with a small shift, δ, the lower bound approximation (given by Equation 15) may lead to an accurate heuristic over a wide range of NM_T and V_{DD}. That is, Equation 16 results and is shown below:

$$P(FAIL(INV_a, NM_T) \cup FAIL(INV_b, NM_T)) \approx P(NM_H(INV_a, INV_b) \leq NM_T + \delta) * P(NM_L(INV_b, INV_a) \leq NM_T + \delta) + P(NM_H(INV_b, INV_a) \leq NM_T + \delta) \text{ (Equation 16).}$$

[00126] Quantification component 502 can employ the Gauss error function, erf, and the cumulative distribution function (CDF) of the normal distribution to compute the probability of failure. If Z is a normal random variable with mean μ and standard deviation σ, and c a constant, then Equation 17 results and is shown below:

$$P(Z \le c) = \frac{1}{2}\left(1 + erf\left(\frac{c-\mu}{\sigma\sqrt{2}}\right)\right) \text{(Equation 17).}$$

[00127] Consider an inverter INV_x driving another inverter INV_y, combining Equations 7, 8 and 17 yields Equation 18 shown below:

$$P((INV_x, INV_y) \le) = \frac{1}{2}\left[1 + erf\left(\frac{-((INV_x) - \mu((INV_y)))}{\sigma((INV_y))\sqrt{2}}\right)\right]$$

and (Equation 18).

$$P((INV_x, INV_y) \le) = \frac{1}{2}\left[1 + erf\left(\frac{-(\mu((INV_y)) - (INV_x))}{\sigma((INV_y))\sqrt{2}}\right)\right]$$

[00128] Quantification component 502 can apply Equation 18 directly to Equations 12, 15 and 16, thus yielding close-form equations for the probability of cross-coupled inverter failure. Accordingly, quantification component 502 can perform a method of computation that applies the variable values and relationships of Equation 18 to Equations 12, 15 and 16 to quantify robustness of a cross-coupled inverter pair.

[00129] Equations 18, 12, 15 and 16 may provide expressions for failure likelihood that use an extremely compact set of real numbers: $V_{OH}(INV_{x,y})$, $V_{OL}(INV_{x,y})$, $\mu(V_{IH}(INV_{x,y}))$, $\mu(V_{IL}(INV_{x,y}))$, $\sigma(V_{IH}(INV_{x,y}))$, $\sigma(V_{IL}(INV_{x,y}))$. That is, these are the parameters that may be employed in order to calculate the probability of failure, and hence robustness of a circuit.

[00130] Accordingly, for a cell device, quantification component 502 of robustness determination component 402 can generate VTC information and compute robustness based on performing a method based at least in part on Equations 18, 12, 15 and 16.

[00131] **FIGS. 20**, **21**, **22**, **23** and **24** illustrate example graphs depicting probabilities of minimum-size cross-coupled inverter-pair failure for respective noise margin threshold values for determination of electronic circuit robustness in accordance with one or more embodiments described herein. Specifically, **FIGS. 20**, **21** and **22** illustrate an example of the probability of failure for a crossed-coupled inverter pair against V_{DD}.

[00132] In particular, **FIG. 20** illustrates an example of the probability of minimum-size cross-coupled inverter-pair failure for $NM_T = 0mV$ in a commercial 40 nm low-power CMOS process (25 °C, TT-Corner). For the heuristic approximation, the mean absolute error may be 13% , and the maximum absolute error may be 20% with $\delta = 4.2\%\ V_{DD}$.

[00133] **FIG. 21** illustrates an example of the probability of minimum-size cross-coupled inverter-pair failure for $NM_T = 10\%\ V_{DD}$ in a commercial 40 nm low-power CMOS process (25 °C, TT-Corner). For the heuristic approximation, the mean absolute error may be 12%, and the maximum absolute error may be 20% with $\delta = 3.2\%\ V_{DD}$.

[00134] **FIG. 22** illustrates an example of the probability of minimum-size cross-coupled inverter-pair failure for $NM_T = 20\%\ V_{DD}$ in a commercial 40 nm low-power CMOS process (25 °C, TT-Corner). For the heuristic approximation, the mean absolute error may be 5.2%, and the maximum absolute error may be 17% with $\delta = 2.2\%\ V_{DD}$.

[00135] **FIG. 23** illustrates an example of the probability of minimum-size cross-coupled inverter-pair failure for $V_{DD} = 150mV$ in a commercial 40 nm low-power CMOS process (25 °C, TT-Corner). For the heuristic approximation, the mean absolute error may be 2.5%, and the maximum absolute error may be 5.5% with $\delta = 4.3\%\ V_{DD}$.

[00136] **FIG. 24** illustrates an example of the probability of cross-coupled inverter failure versus NM_T for a fixed supply voltage of $150mV$. Digital noise may tend to be proportional to V_{DD}, so the NM_T may be reported as a percentage of V_{DD}. Each of these figures depicts the upper bound, lower bound, and approximation for cross-coupled inverter failure probability, in addition to the actual (empirical) failure rate. Actual failures may be calculated via Monte Carlo SPICE simulations with foundry provided statistical BSIM4 models. These models are statistical models provided by the foundry for the process being used/analyzed.

[00137] **FIGS. 20**, **21**, **22** and **23** also serve to exemplify why an accurate and simple closed-form approximation for the probability of failure may be useful. In particular, in each of these plots, as V_{DD} increases linearly, the probability of failure may decrease exponentially, and the size of the Monte Carlo simulations employed to generate accurate failure rates may increase exponentially. With an NMT of 10% and V_{DD} at $300mV$, the probability of failure may be already less than 10^{-5}, so millions of Monte Carlo trials may need to be performed. A million such trials on modern computers with modern tools may involve several core-hours of compute time. Furthermore, it is not uncommon for a modern microprocessor design to contain millions of cross-coupled inverters, so higher supply voltages with lower failure rates on the order of 10^{-9} or lower may need to be considered. This corresponds to at least a four order of magnitude increase in computational time for a single temperature and V_{DD} of interest. To ensure reliability, multiple supply voltages and temperatures may be considered, thereby increasing the computation requirement by yet another order of magnitude. Optimization of transistor sizing can easily increase the

computation requirement by another order of magnitude, thereby resulting in a computational requirement in the realm of millions of core-hours. Finally, this type of analysis may extend to arbitrary gates (typical standard cell device data stores/libraries containing hundreds of cell devices). This analysis may push the computation requirement to billions of core-hours. A closed-form approximation may be more practical.

[00138] In some embodiments, quantification component 502 can compute the probability of failure of a circuit C_a having n cross-coupled inverter pairs ($C_a = (INV_a^i, INV_b^i)$ for $i \in \{1,2,...,n\}$) as shown in Equation 19. Equation 6 can be re-written in terms of a global conjunction instead of disjunction and is shown as Equation 19

$$P(FAIL(C_{a,} NM_T)) = 1 - P(\bigcup_{i\in\{1,2,...,n\}} - FAIL(INV_a^i, NM_T) \cup FAIL(INV_b^i, NM_T)))$$

(Equation 19).

[00139] Given the assumption of statistical VTC parameter independence between gate pairs, the global conjunction can be treated as a product, given a readily computable compact expression for the probability of failure and hence robustness of a circuit, one of the goals of this section. That is, Equation 20 results and is shown below:

$$P(FAIL(C_{a,} NM_T)) = 1 - P(\prod_{i\in\{1,2,...,n\}} FAIL\ (INV_a^i, NM_T) \cup FAIL(INV_b^i, NM_T)))$$

(Equation 20).

[00140] **FIG. 24** illustrates the probability of failure for $2e^{28}$ minimum-size cross-coupled inverter-pairs with $NM_T = 20\%\ V_{DD}$ in a commercial 40 nm low-power CMOS process (25 °C, TT-Corner, and $\delta = 2.2\%\ V_{DD}$). **FIG. 24** gives the probability of failure for $2e^{28}$ independent cross-coupled inverter pairs (e.g., a 32MB memory).

[00141] With Equation 20, quantification component 502 can quantify the probability of failure, and hence robustness, for an entire memory. In some embodiments, δ may be taken from the considerably smaller experiments depicted in **FIG. 22** to perform the analysis.

DETERMINATION OF CHAIN OF INVERTERS ROBUSTNESS

[00142] The preceding analysis that can be performed by statistical analysis / characterization determination component 500 and quantification component 502 employing noise margins and circuit robustness can be extended to arbitrary networks of inverters. In some embodiments, the probability of failure of a linear chain of n inverters can differ significantly from that of n cross-coupled inverters. In particualr, a cross-coupled pair of identical inverters can be modeled as, and can be mathematically equivalent to, an infinite chain of identical inverters. Moreover, alternating worst-case noise sources between a cross-

coupled pair can be modeled as alternating noise in an infinite chain, as depicted in **FIG. 25.** **FIG. 25** illustrates an example of an infinite chain construct equivalent to the cross-coupled pair of **FIG. 12** for determination of electronic circuit robustness in accordance with one or more embodiments described herein.

[00143] One idea behind this equivalence is that an infinite chain can be viewed as the unrolling of the loop that is a cross-coupled pair. When a bistable cross-coupled pair in steady state is perturbed by some voltage δV, the bistable pair may either change digital state, or the inverters may act as a restorative filter, successively removing the δV disturbance one iteration at a time in the same exact way that a chain of inverters may filter a δV disturbance. As used herein, δV means a change voltage of magnitude, dV. When the inverters are not identical, the two circuits may no longer behave in the same way, and equivalence can be lost.

[00144] Consider a cross-coupled inverter pair (INV_a, INV_b), where INV_a and INV_b may behave differently due to parameter variation. With the infinite chain construct, this pair can be modeled as a never-ending alternating linear chain of INV_a driving INV_b driving INV_a driving INV_b, etc. (see FIG. 15). Suppose that this inverter pair may not be robust, e.g., the static noise margin may be just slightly larger than $0mV$ due to INV_a being skewed such that INV_a can barely interpret a logical-0 and INV_b being skewed such that INV_b can barely interpret a logical-1. Consider the state where the input of INV_a is a logical-0 and its output (the input of INV_b) is a logical-1. A small DC noise can raise the input voltage, thus causing INV_a to no longer interpret its input as a logical-0, thus resulting in a lowering of its output node voltage. This, in turn, can result in INV_b no longer interpreting its input as a logical-1, thus resulting in INV_b raising its output node voltage. This result, in turn, pushes INV_a even further away from interpreting its input as a logical-0, and so on down the infinite chain until the bistable pair changes digital state.

[00145] **FIG. 26** illustrates an example of a chain of inverters for determination of electronic circuit robustness in accordance with one or more embodiments described herein. Consider an actual linear chain of inverters, as in **FIG. 26**. Due to parameter variation, each inverter in the chain may behave differently. Suppose that the chain begins with the identical sequence of skewed INV_a driving a skewed INV_b, but INV_b now drives a different inverter INV_c. Again, consider the same state and event where the input of INV_a is a logical-0 and its

output (the input of INV_b) is a logical-1, and a small DC noise raises the input voltage, thus causing INV_a to no longer interpret its input as a logical-0, resulting in a lowering of its output node voltage. This, in turn, results in INV_b no longer interpreting its input as a logical-1, resulting in INV_b raising output node voltage. Suppose, however, that INV_c is a robust inverter and completely restores the rather poor logical-0 generated by INV_B to approximately $0mV$. That is, the condition that causes INV_a and INV_b to change state if configured as a cross-coupled pair may not cause a failure with INV_a and INV_b in a linear chain.

[00146] In order to determine equations/methods for quantification component 502 to calculate the probability of failure for a chain of inverters, the notion of what it means for a chain to fail is defined. However, cross-coupled inverter static noise margin analysis may avoid the definition of failure of an individual inverter by considering a bistable loop. Analogously, consider a chain of an even number, $n > 2$, of inverters. If the output of the last inverter in the chain is connected to the input of the first inverter, then the chain may become a state-holding ring (loop). The definition of failure naturally follows as a failure of the ring to maintain state. Informally, the requirement of an even number of stages may not result in a loss of generality, as it is possible to calculate a tight upper and lower bound on failure rate by considering a chain with one extra and one fewer inverters respectively.

[00147] As with the cross-coupled inverter pair analysis, the NM_H and NM_L can be used to generate an upper bound, a lower bound, and an approximation for the probability of failure for chains of inverters. For a chain of inverters, the worst-case, demonic, DC noise can include alternating positive and negative voltage sources acting contrary to the desired state of each inverter input. That is, if the desired input to a gate is logical-1, e.g., V_{DD}, then a voltage source that acts to lower this electrical potential may be said to act contrary to the desired state. In steady-state, a linear chain of n functional inverters may include alternating sequences of 0 and 1 at the input of each inverter. As such, there may be two possible digital states for such a chain: the sequence either begins with a 1 or it begins with a 0. Correspondingly, there may be two states for alternating demonic noise sources; the first DC noise source may be either positive or negative.

[00148] Consider a linear chain, CH_a, of n inverters with demonic noise sources, as in **FIG. 26** (with the constraint that n is an even integer greater than 2). The chain may be said to fail if the corresponding ring, created by connecting the output of the last inverter to the

input of the first inverter, fails to maintain state when all inverter inputs are properly initialized with alternating values of 0 and 1. The chain and ring may fail with respect to a noise margin target, NM_T, when the ring fails to maintain state with demonic noise sources with $V_{noise} = NM_T$ or $V_{noise} = -NM_T$. Given the assumption of statistical independence between the noise margins of different gates pairs (as discussed with reference to FIGs. 7 and 8), the probability of chain failure can be analyzed and computed in terms of the NM_H and NM_L of pairs of gates.

[00149] A heuristic upper bound can be determined as follows. Consider a labeling of inverters in the chain CH_a such that the first inverter is labeled as INV_1, the second inverter as INV_2, and so on with the last inverter being INV_n. If the chain fails, then it follows that there may exist some inverter pair in the chain, INV_i driving INV_{i+1}, with $NM_H(INV_i, INV_{i+1}) \leq NM_T$ and/or $NM_L(INV_i, INV_{i+1}) \leq NM_T$, which leads to the same probabilistic upper bound for cross-coupled pairs. For chains, however, this may not not be a tight upper bound. Empirically, the cross-coupled pair heuristic approximation can lead to a tighter upper bound for chains of gates.

[00150] Consider two connected pairs of inverters, the set (INV_i, INV_{i+1}, INV_{i+2}); if the chain fails, then it may be likely that either (1) $NM_L(INV_i, INV_{i+1}) \leq NM_T$ and $NM_H(INV_{i+1}, INV_{i+2}) \leq NM_T$), and/or (2) $NM_H(INV_i, INV_{i+1}) \leq NM_T$) and $NM_L(INV_{i+1}, INV_{i+2}) \leq NM_T$). With the assumption of statistical independence, the upper bound on the probability of failure for the chain can be approximated as shown in Equation 21 below:

$$P(FAIL(CH_a, NM_T) \leq P(\cup_{i\in\{1,2,\ldots,n-2\}}((NM_H(INV_i, INV_{i+1}) \leq NM_T + \delta u \cap NM_L(INV_{i+1}, INV_{i-2}) \leq NM_T + \delta u) \cup (NM_L(INV_i, INV_{i+1}) \leq NM_T + \delta u \cap NM_H(INV_{i+1}, INV_{i+2}) \leq NM_T + \delta u)))$$

(Equation 21).

[00151] In Equation 21, δu is a small constant used to maintain the boundary over a wide range of NM_T and V_{DD}. Sample values for δu are typcially on the order of +-2%.

[00152] A heuristic for the lower bound may have the same form, but a small constant δl may be subtracted from the NM_T and is shown in Equation 22 below:

$$P(FAIL(CH_a, NM_T) \geq P(\cup_{i\in\{1,2,\ldots,n-2\}}((NM_H(INV_i, INV_{i+1}) \leq NM_T - \delta l \cap NM_L(INV_{i+1}, INV_{i-2}) \leq NM_T - \delta l) \cup (NM_L(INV_i, INV_{i+1}) \leq NM_T - \delta l \cap NM_H(INV_{i+1}, INV_{i+2}) \leq NM_T - \delta l)))$$

(Equation 22).

[00153] The value for δl is typically +=2%. The heuristic approximation may follow from the upper and lower bound heuristics. In particular, Equation 23 results and is shown below:

$$P(FAIL(CH_a, NM_T) \approx P(\bigcup_{i\in\{1,2,...,n-2\}}((NM_H(INV_i, INV_{i+1}) \leq NM_T + \delta \cap$$
$$NM_L(INV_{i+1}, INV_{i-2}) \leq NM_T + \delta) \cup (NM_L(INV_i, INV_{i+1}) \leq NM_T + \delta \cap$$
$$NM_H(INV_{i+1}, INV_{i+2}) \leq NM_T + \delta))) \text{ (Equation 23).}$$

[00154] Empirically, δu and δl can be defined in terms of δ. For the devices: INV, NAND2, NOR3, NAND3, NOR3, AOI21, each of which may be static CMOS gates, and for noise margin targets between 0% V_{DD} and 20% V_{DD}, a relative offset of 3% V_{DD} may be sufficient. That is, $\delta u = \delta l = \delta + 3\%\ V_{DD}$.

[00155] **FIGS. 27**, **28**, **29, 30, 31** illustrate example graphs depicting probabilities of failure for minimum-size inverters in chains for determination of electronic circuit robustness in accordance with one or more embodiments described herein. In particular, **FIGS. 27, 28, and 29** depict the upper bound, lower bound, and approximations for a chain of 20 inverters.

[00156] **FIG. 27** illustrates an example probability of a chain of 20 inverters failing with $NM_T = 0\%\ V_{DD}$ in a commercial 40 nm low-power CMOS process (25 °C, TT-Corner). For the heuristic approximation, the mean absolute error may be 17%, and the maximum absolute error may be 43% with $\delta = -3.2\%\ V_{DD}$. **FIG. 28** illustrates an example probability of a chain of 20 inverters failing with $NM_T = 10\%$ in a commercial 40 nm low-power CMOS process (25 °C, TT-Corner). For the heuristic approximation, the mean absolute error may be 13%, and the maximum absolute error may be 38% with $\delta = -2.3\%\ V_{DD}$. **FIG. 29** illustrates an example probability of a chain of 20 inverters failing with $NM_T = 20\%$ in a commercial 40 nm low-power CMOS process (25 °C, TT-Corner). For the heuristic approximation, the mean absolute error may be 6.8%, and the maximum absolute error may be 24% with $\delta = -1.8\%\ V_{DD}$.

[00157] A circuit, C_a, composed of n chains of inverters, may be said to fail if any chain fails. That is, with chain labeled as $CH_1, CH_2, ..., CH_n$, Equation 24 results and is shown below.

$$P(FAIL(CH_a, NM_T) = P(\bigcup_{i\in\{1,2,...,n\}}(FAIL(CH_i, NM_T)) \text{ (Equation 24).}$$

[00158] As with the cross-coupled inverter analysis, Equation 24 can be re-written in terms of a global conjunction instead of disjunction as shown in Equation 25:

$$P(FAIL(CH_a, NM_T) = 1 - P(\bigcap_{i\in\{1,2,...,n\}} - FAIL(CH_i, NM_T)) \text{ (Equation 25).}$$

[00159] Given the assumption of statistical VTC parameter independence between gate pairs, and hence chains, the global conjunction can be treated as a product, giving a readily computable compact expression for the probability of failure and hence robustness of a circuit having chains of inverters. For example, Equation 26 results and is shown below:

$$P(FAIL(CH_a, NM_T) = 1 - P(\prod_{i\in\{1,2,\ldots,n\}} - FAIL(CH_i, NM_T)) \text{ (Equation 26).}$$

[00160] **FIG. 30** illustrates an example probability of failure for $2*2e^{28}$ minimum-size inverters in chains with $NM_T = 20\%\ V_{DD}$ in a commercial 40 nm low-power CMOS process (25 °C, TT-Corner, and $\delta = -1.8\%\ V_{DD}$). **FIG. 31** illustrates an example probability of failure for $2*2e^{28}$ minimum-size inverters in chains compared to that of $2e^{28}$ minimum size cross-coupled pairs with $NM_T = 20\%\ V_{DD}$ in a commercial 40 nm low-power CMOS process (25 °C, TT-Corner). As used herein, $2*2e^{28}$ means 2 multiplied by 2 e^{28}.

[00161] Quantification component 502 can perform methods to compute a value for robustness for a chain of inverters based on applying Equation 26. **FIG. 30** gives an example of the probability of failure for $2*2e^{28}$ independent inverters in the form of chains. δ may be based on what is depicted in **FIG. 29**. In the drawing shown, δ is a fitting constant determined by analysis smaller sample size 20-chains (instead of 2e28 chains).

[00162] The probability of failure of chains of inverters may be considerably lower than that of cross-coupled pairs (with the same number of devices, noise-margin target, and V_{DD}), as depicted in **FIG. 31**. The failure probabilities may be similar for cross-coupled pairs of inverters operating $50-100mV$ above the inverter chain supply voltage.

[00163] The analysis described above for a chain of inverters and cross-coupled inverter pairs can be extended to a larger gate set than that of inverters alone. Employing the following methods, quantification component 502 can generate a composable robustness metric for a wide variety of gates so that the robustness of an arbitrary network of standard cell devices can be easily computed.

ROBUSTNESS OF LOGIC GATES

[00164] **FIG. 32** illustrates an example NAND2 circuit diagram for determination of electronic circuit robustness in accordance with one or more embodiments described herein. **FIGS. 33** and **34** illustrate example graphs of VTCs for the minimum-size NAND2 for determination of electronic circuit robustness in accordance with one or more embodiments described herein.

[00165] Specifically, **FIG. 32** illustrates an example of a NAND2 device, and **FIG. 33** illustrates example voltage transfer characteristic for the minimum-size NAND2 depicted in **FIG. 32**, in a commercial 40 nm low-power CMOS process ($V_{DD} = 1.1V$, 25 °C , TT-Corner). **FIG. 34** illustrates example voltage transfer characteristic for the minimum-size NAND2

depicted in **FIG. 32** in a commercial 40 nm low-power CMOS process ($V_{DD} = 1.1V$, 25 °C, TT-Corner).

[00166] The term "NAND2" can represent a combinational CMOS 2-input NAND gate with nodes labeled as shown in **FIG. 32**. If the input nodes, $in1$ and $in2$, are treated independently, then the statistical VTC may describe V_{out} as a function of both V_{in1} and V_{in2}, as depicted in **FIGS. 33** and **34**. **FIGS. 33** and **34** illustrate example graphs of VTCs for the minimum-size NAND2 for determination of electronic circuit robustness in accordance with one or more embodiments described herein, and more specifically, **FIG. 33** provides a three dimensional view and, **FIG. 34** plots the statistical VTC in the $V_{in1} \times V_{in2}$ plane with V_{out} encoded by hatching. The partial derivatives $\frac{\partial V_{out}}{\partial V_{in1}}$ and $\frac{\partial V_{out}}{\partial V_{in2}}$ may describe two continuums of unity gain points depicted by triangles and squares, respectively, in **FIG. 34**.

[00167] The gradient is given by Equation 27 below:

$$\nabla V_{out} = \frac{\partial V_{out}}{\partial V_{in1}}\mathbf{i} + \frac{\partial V_{out}}{\partial V_{in2}}\mathbf{j}, \quad \text{(Equation 27)}$$

where $\mathbf{i}$ and $\mathbf{j}$ are the unit vectors in the $V_{in1} \times V_{in2}$ plane. The two continuums of unity gain points defined by $|\nabla V_{out}| = 1$ (depicted by a black line in **FIG. 34**) may be analogous to an inverter's two unity gain points given by $|\frac{dV_{out}}{dV_{in}}| = 1$ above for the cross-coupled inverter pair. For an inverter, the two measures can be identical: $|\nabla V_{out}| \equiv |\frac{dV_{out}}{dV_{in}}|$.

[00168] Moreover, the magnitude of ∇V_{out} may be the most general measure for determining unity gain points, as it may be applicable to any gate regardless of the number of inputs. For noise margin analysis, choosing individual unity gain points as representative approximations can be provided, and individual points can be chosen by considering slices of the statistical VTC (planes orthogonal to $V_{in1} \times V_{in2}$). Three slices of the NAND2 statistical VTC are depicted by dashed lines in **FIG. 34**. These three slices may be notable for two reasons. First, they may give the upper and lower unity-gain bounds in terms of V_{in1} and V_{in2}. Second, they may correspond to a logical reduction of the NAND2 to that of an inverter. That is, if either input is tied to logical-1 or if both inputs are tied together, then the NAND2 may be functionally equivalent to an inverter.

[00169] In **FIG. 34**, the three possible inverter-equivalent slices are depicted by: (1) a first dashed line along the rightmost edge of the graph labeled (1) and corresponding to tying $in1$

to V_{DD} and sweeping $in2$ from GND to V_{DD}; a second dashed line along the top edge of the graph labeled (2) and corresponding to tying $in2$ to V_{DD} and sweeping $in1$ from GND to V_{DD}; and a third dashed line running diagonal from the upper right corner of the graph to the lower left corner of the graph labeled (3) and generated by tying $in1$ to $in2$ and sweeping them together.

[00170] **FIG. 35** illustrates an example circuit diagram of NAND2 inverter equivalence for determination of electronic circuit robustness in accordance with one or more embodiments described herein. The idea of inverter-equivalence can be used to generate the boundary unity-gain points for arbitrary gates. Consider an inverting binary CMOS gate, G, with n inputs and a single output. Gate G can be made to act logically as a single input/output inverter for some assignment of inputs where inputs can be tied together, tied to 1, or tied to 0. Since G may be an inverting CMOS gate, one or more inverter-equivalent input assignments may exist, and the assignments may depend on the topology of G. The three inverter-equivalent slices from **FIG. 34** are depicted at the gate level in **FIG. 35**.

[00171] A general notion of an inverter equivalent assignment is helpful. Let G be an inverting binary CMOS gate with k inputs labeled as $in1, in2, ..., ink$, a single output, out, and with functionality defined by $V_{out} = G(V_{in1}, V_{in2}, ..., V_{ink})$. The set of inverter equivalent input assignments to G, denoted $IE(G)$, may be a set of k-tuples, $(ie_1, ie_2, ..., ie_k)$, where ie $\in$ (1,0,in) and $(ie_1, ie_2, ..., ie_k) \in IE(G)$ if and only if $G(ie_1, ie_2, ..., ie_k)$ is functionally equivalent to an inverter with input in, and output out. For the NAND2, the three inverter equivalent input assignments may be (1) (1, in), (2) (in, 1) and (3) (in, in). In order to work with inverter equivalent input assignments, it may be convenient to define F, a simple mapping function between real voltages and elements of (1, 0, in). That is, the following relationships may result: $F(V_i) = 0$, if V_i = GND; $F(V_i) = 1$, if $V_i = V_{DD}$; $F(V_i) = in$, otherwise.

[00172] With a notion of inverter equivalence, it is possible to define a representative set of unity gain points for a gate. Let G be an inverting binary CMOS gate with k inputs labeled as $in1, in2, ..., ink$, and a single output, out. The gradient of V_{out} is defined as shown in Equation 29:

$$\nabla V_{out} = \frac{\partial V_{out}}{\partial V_{in1}}\mathbf{i}_1 + \frac{\partial V_{out}}{\partial V_{in2}}\mathbf{i}_2 + ... + \frac{\partial V_{out}}{\partial V_{ink}}\mathbf{i}_k, \text{(Equation 29)}$$

[00173] where $\mathbf{i}_1$, $\mathbf{i}_2$, ..., $\mathbf{i}_k$ are the corresponding unit vectors. The representative set of unity gain points for G, $RS(G)$, is defined such that Equations 30 and 31 result and are shown below:

$$(V_{in1},V_{in2},...,V_{ink},V_{out}) \in RS(G) \text{ ifandonlyif } |\nabla V_{out}(V_{in1},V_{in2},...,V_{ink})| = 1 \text{ ,and}$$

$$(F(V_{in1}),F(V_{in2}),...,F(V_{ink})) \in IE(G) \text{ ,and forall} x, y \in (1,2,...,k) \quad \text{(Equation 30)}$$

$$\text{if} F(V_{inx}) = \text{and} F(V_{iny}) = \text{then} V_{inx} = V_{iny}. \quad \text{(Equation 31).}$$

[00174] For the NAND2, the representative set of unity gain points are depicted in **FIG. 34** as shaded circles, shaded diamonds and unshaded circles with annotated values. The values for each slice $(V_{in1},V_{in2},V_{out})$ may be (1): (1100,470,1066), (1100,626,42) (2): (445,1100,1063), (630,1100,40), (3): (540,540,1062), (674,674,51). These representative points can be mapped back to simple pairs of the form (V_{in},V_{out}) by using the inverter equivalent input assignment to remove the references to V_{DD}, GND, and shared inputs. For the NAND2, this reduced representative set of unity gain points may be (1): (470,1066), (626,42) (2): (445,1063), (630,40), (3): (540,1062), (674,51).

[00175] The statistical VTC parameters can be defined using the reduced set of unity gain points. The usual mapping of unity gain points to statistical VTC parameters can be employed, so for the NAND2, (1): $V_{IL} = 470$, $V_{OH} = 1066$, $V_{IH} = 626$, $V_{OL} = 42$, (2): $V_{IL} = 445$, $V_{OH} = 1063$, $V_{IH} = 630$, $V_{OL} = 40$, and (3): $V_{IL} = 540$, $V_{OH} = 1062$, $V_{IH} = 674$, $V_{OL} = 51$. Statistical analysis may be greatly simplified when a single set of representative statistical VTC parameters is chosen, but the parameters---as measured with (1), (2), and (3)---may differ. V_{OH} and V_{OL} may be nearly constant. The two inverter equivalent input assignments where a single input is tied to V_{DD} ((1) and (2)) may be highly symmetric and may have only slightly different values for V_{IH} and V_{IL}, respectively. The input assignment wherein both inputs are tied together, (3), may differ significantly in terms of V_{IH} and V_{IL} from (1) and (2).

[00176] Consider the measurement of V_{IL} performed by sweeping the input(s) from GND to V_{DD} using (1) as compared to (3). The value of V_{IL} may correspond to the greatest input voltage that still results in the output being pulled-up to a logical-1. The NAND2 may contain 2 parallel PFETs with gates connected to $in1$ and $in2$, respectively. With input assignment (1), $in1$ is tied to V_{DD}, causing the corresponding PFET to effectively turn off, e.g., it contributes only sub-threshold leakage current to the pull-up network as $in2$ is swept from GND to V_{DD}. As V_{in2} is increased, the corresponding PFET begins to turn off and the NFETs

begin to turn on, thus transitioning the output towards a logic-0; V_{IL} is the input voltage at which this transition occurs. With (3), both inputs are tied together, and the parallel PFETs actively pull up the output node together as the input is swept. The parallel PFETs in (3) continue to actively pull up the output node as the input voltage is increased beyond the V_{IL} from (1). As such, V_{IL} as measured with (3) is greater than V_{IL} as measured with (1). An analogous, but reciprocal explanation can be given for V_{IH}. That is, V_{IH} as measured with (1) is greater than V_{IH} as measured with (3).

[00177] In order to provide an upper bound on the robustness, the representative set of statistical VTC parameters may be chosen so as to overestimate the probability of failure of a gate. This corresponds to underestimating both NM_H and NM_L; this, in turn, may involve underestimating V_{IH} and overestimating V_{IL} assuming that the corresponding variances are approximately equal.

[00178] Since V_{OH} and V_{OL} may be approximately constant across inverter equivalent input assignment slices, the smallest V_{IH} and the largest V_{IL} may be chosen from the reduced representative set of unity gain points. For the NAND2, this may correspond to selecting the statistical VTC parameters from different slices: V_{IH} from (1) and V_{IL} from (3). In a similar manner, the smallest V_{OH} and largest V_{OL} could be chosen as representative statistical VTC parameters; however, the output statistical VTC parameters may be approximately constant, so they can also be chosen arbitrarily or by convenience.

[00179] In the embodiments described herein, the statistical VTC parameters from (1) may be chosen as the representative set, despite the fact that this simplifying choice slightly underestimates V_{IL}. In terms of calculating the probability of failure, this simplification has little impact.

[00180] The statistical VTC parameters for an arbitrary gate can be defined. Let G be an inverting binary CMOS gate with m inputs and a single output, out, and let $RS(G)$ be the reduced representative set of unity gain points for G. Assume that $RS(G)$ has cardinality n, and elements labeled as (V_{in_i}, V_{out_i}) for $i \in \{1,2,...,n\}$. The statistical VTC parameters for G may be defined as $(G) = min(V_{in_i})$ $(G) = max(V_{in_j})$ $(G) = min(V_{out_k})$ $(G) = max(V_{out_l})$, for $i, j, k, l \in \{1,2,...,n\}$.

[00181] To provide general definitions for NM_H and NM_L, the input statistical VTC parameter correlation between multiple inputs of the same gate may be considered. **FIG. 36** illustrates an example graph of NAND2 input correlation for determination of electronic

circuit robustness in accordance with one or more embodiments described herein. **FIG. 36** illustrates an example NAND2 input correlation in a commercial 40 nm low-power CMOS process ($V_{DD} = 1.1V$, 25 °C, TT-Corner).

[00182] As shown in **FIG. 36**, the input statistical VTC parameters may be highly uncorrelated over a wide range of V_{DD}. Given this and the treatment of output statistical VTC parameters as regular variables, arbitrary networks of combinational gates with fan-in and fan-out greater than unity can be broken apart into equivalent gate-pairs, and ultimately, into inverter-equivalent pairs for statistical analysis; e.g., for the purpose of computing the probability of circuit failure.

[00183] **FIG. 37** illustrates an example circuit diagram detailing equivalent gate pairs formed from multiple fan-in and fan-out gate networks for determination of electronic circuit robustness in accordance with one or more embodiments described herein. Gate pairs GP_1 and GP_2 may be formed for each input of the NAND gate, and gate pairs GP_3 and GP_4 may be due to the inverter fan-out.

[00184] Consider a circuit, C_a, that includes a network of n combinational gates in an array of simple linear chains; C_a may be said to fail if any chain of gates within the circuit fails (see Equation 24). In general, digital circuits include networks of combinational gates organized as interconnecting chains, wherein some gates drive multiple gates, some gates may be driven by multiple gates, or both. Consider a circuit, C_b, that includes a network of n combinational gates with interconnecting chains, e.g., some gates within C_b may drive multiple gates and some gates may have multiple inputs. Consider a gate, $G_x \in C_b$ that drives k gates in C_b, labeled as G_1, G_2, ..., G_k. Since the output statistical VTC parameters of G_x may not be stochastic in nature, these gates can be treated as k equivalent gate-pairs (G_x, G_i) for $i \in \{1,2,...,k\}$. As an example, consider GP_3 and GP_4 in **FIG. 37**. Similarly, consider k gates in C_b, labeled as G_3, G_4, ..., G_k that drive (fan-in) to a multi-input gate, $G_x \in C_b$.

[00185] Given that the input statistical VTC parameters of G_x may be independent, each pair, (G_i, G_x) for $i \in \{1,2,...,k\}$, can be considered as components of independent equivalent gate-pairs, as illustrated in **FIG. 37** by GP_1 and GP_2. As discussed above, equivalent gate-pairs can be analyzed as inverter equivalent pairs, and the robustness of a circuit having arbitrary connections of combinational gates can be computed by way of the methods described herein.

[00186] **FIGS. 38** and **39** illustrate example graphs depicting probabilities of a chain of 20 alternating NAND2 and NOR2 gates failing for respective noise margin thresholds for determination of electronic circuit robustness in accordance with one or more embodiments described herein. **FIG. 38** illustrates an example probability of a chain of 20 combinational gates failing (the chain includes alternating NAND2, NOR2 gates) with $NM_T = 10\% V_{DD}$ in a commercial 40 nm low-power CMOS process (25 °C, TT-Corner). For the heuristic approximation, the mean absolute error may be 16% , and the maximum absolute error may be 36% with $\delta = -1.2\% V_{DD}$. **FIG. 39** shows an example of the probability of a chain of 20 combinational gates failing (the chain includes alternating NAND3, NOR3 gates) with $NM_T = 20\% V_{DD}$ in a commercial 40 nm low-power CMOS process ($25C$, TT-Corner). For the heuristic approximation, the mean absolute error may be 16% , and the maximum absolute error may be 67% with $\delta = -1.3\% V_{DD}$.

[00187] Accordingly, the embodiments described herein can facilitate determination of robustness for one or more different types of cell devices (and corresponding circuits composed from the one or more cell devices). For example, the cell devices can include, but are not limited to, inverters and gates. That is, for some circuit, C_a, and a target noise margin, NM_T, Equation 26 gives the probability that some gate chain in C_a may have a noise margin less than the target, e.g., a probability of failure, P(FAIL). This quantity can instead be considered as a passing probability P(PASS) by subtracting it from unity, and this passing probability can be thought of as a parametric yield.

[00188] Prediction component 404 of **FIG. 4** can be configured to determine a yield of a parameter, or parametric yield. That is, prediction component 404 can determine the probability of passing (as opposed to failure) for a defined cell device (and correspondingly, for a defined circuit that includes one or more cell devices for which parametric yield has been determined by prediction component 404). In some embodiments, for example, if P(PASS) = 95%, then in 95% of instances of C_a, all gates may exceed the noise margin target constraint (this is definitionally a parametric yield). If the circuit under consideration, C_a, is an entire microprocessor, then this parametric yield can be included as a part of the die yield calculation.

[00189] In Equation 26, the circuit under consideration, C_a, may be an independent variable, and P(FAIL) may be a dependent variable. The circuit C_a may instead be treaed as dependent on P(FAIL). In this way, circuit design component 406 can calculate a maximum number of gates that can satisfy a defined constraint for a circuit (e.g., how large a circuit can

be built). For example, for a defined NM_T and a yield, circuit design component 406 can calculate a maximum number of gates for the circuit.

[00190] **FIG. 40** illustrates an example graph of maximum number of equivalent gate pairs versus V_{DD} for chains of alternating gates and combinations from a defined set of gates for determination of electronic circuit robustness in accordance with one or more embodiments described herein. **FIG. 41** illustrates an example graph of maximum noise margin threshold versus V_{DD} for chains of alternating gates and combinations from a defined set of gates for determination of electronic circuit robustness in accordance with one or more embodiments described herein.

[00191] Specifically, **FIG. 40** illustrates an example maximum number of equivalent gate-pairs vs. V_{DD} with $NM_T = 20\%$ V_{DD} and $yield = 95\%$ in a commercial 40 nm low-power CMOS process (25 °C, TT-Corner). Chains may include alternating gates, and all combinations from the set $(INV, NAND2, NOR2, AOI21, NAND3, NOR3)$ may be considered. The gate choice may have only a small impact on how large of circuit can be constructed, and the most important constraint may be supply voltage; e.g., the maximum circuit size is exponential in V_{DD}.

[00192] **FIG. 41** illustrates an example maximum NM_T vs. V_{DD} for $1M$ equivalent gate-pairs and $yield = 95\%$ in a commercial 40 nm low-power CMOS process (25 °C, TT-Corner). Chains include alternating gates, and all combinations from the set $(INV, NAND2, NOR2, AOI21, NAND3, NOR3)$ may be considered. Specifically, **FIG. 41** may plot the maximum NM_T that can be guaranteed (for 1M equivalent gate-pairs in chains and a yield of 95%) versus V_{DD}.

[00193] **FIG. 6** illustrates an example block diagram of a circuit design component of the device of **FIG. 4** and configured to generate information for circuit design based on determination of electronic circuit robustness in accordance with one or more embodiments described herein. Circuit design component 406 can include communication component 400, circuit device selection component 600, circuit device place and route component 602, memory 408, processor 410 and/or data store 412. In various embodiments, one or more of communication component 400, circuit device selection component 600, circuit device place and route component 602, memory 408, processor 410 and/or data store 412 can be electrically and/or communicatively coupled to one another to perform one or more operations of circuit design component 406.

[00194] As noted above, in some embodiments, circuit design component 406 can determine a number of gates that can satisfy defined constraints for a circuit. For example,

circuit device selection component 600 can select a number of gates and/or types of gates that satisfy the constraint. Circuit device place and route component 602 can determine the arrangement of the selected gates relative to one another to meet the defined constraint.

[00195] In some embodiments, circuit design component 406 can generate information that can be employed to identify one or more cell devices and/or place/route for connection of the one or more cell devices. The information can be determined based on a desired performance of the generated circuit and information indicative of the robustness of one or more of the cell devices of the circuit.

[00196] Turning back to **FIG. 4**, memory 408 can be a non-transitory computer-readable storage medium storing computer-executable instructions and/or information for performing the operations described herein with reference to device 102 (or any component of device 102). For example, memory 408 can store computer-executable instructions that can be executed by processor 410 to perform communication, quantification of robustness, generation of information for selection of gates/route/placement and/or prediction of yield information or other types of operations executed by device 102.

[00197] Processor 410 can perform or cause to be performed one or more of the operations described herein with reference to device 102 (or any component of device 102). For example, processor 410 can evaluate parameter variation and/or noise for a cell device and/or perform analysis to determine robustness of the cell device in view of parameter variation and noise. As another example, processor 410 can determine robustness of a circuit composed of one or more cell devices. As another example, processor 410 can predict the yield of a circuit composed of one or more cell devices. As another example, processor 410 can generate information indicative of components and place/route for a design of a circuit based on the robustness information determined by processor 410.

[00198] Data storage 412 can store various information for use in the methods performed by device 102 including, but not limited to, statistical noise margin, noise margin threshold, probability of pass, probability of failure and/or VTCs for one or more cell devices or circuits and/or computer-executable instructions that can be executed to perform one or more methods dictated by the equations described herein.

[00199] **FIGS. 7-10** illustrate example flowcharts of methods associated with determination of electronic circuit robustness in accordance with one or more embodiments described herein. An example method may include one or more operations, actions, or functions as illustrated by one or more of blocks shown in **FIGS. 7-10**. Although illustrated as discrete blocks, various blocks may be divided into additional blocks, combined into fewer

blocks, or eliminated, depending on the particular implementation. Blocks may be supplemented with additional blocks representing other operations, actions, or functions. Turning first to **FIG. 7**, at block 702, method 700 can include storing cell device information at a data store (e.g., using communication component 400).

[00200] At block 704, method 700 can include computing one or more statistical VTCs for a cell device represented by the cell device information (e.g., using statistical analysis / characteristic determination component 500 of robustness determination component 402).

[00201] At block 706, method 700 can include accessing statistical noise margin data store for the cell device (e.g., using communication component 400). At block 708, method 700 can include accessing circuit diagram information (e.g., using communication component 400).

[00202] At block 710, method 700 can include composing one or more statistical VTCs for one or more cell devices represented by the circuit diagram information (e.g., using statistical analysis / characteristic determination component 500 of robustness determination component 402). At block 712, method 700 can include generating information indicative of robustness of the circuit (e.g., using quantification component 502).

[00203] Turning now to **FIG. 8**, at block 802, method 800 can include performing, for a cell device by a unit comprising a processor, statistical analysis to obtain statistical information for the cell device that is indicative of a robustness of the cell device, wherein the robustness of the cell device pertains to a parameter variation of the cell device that is related to a noise of the cell device (e.g., using statistical analysis / characteristic determination component 500 of robustness determination component 402).

[00204] At block 804, method 800 can include determining a characteristic of the cell device based on the statistical information (e.g., using statistical analysis / characteristic determination component 500 of robustness determination component 402).

[00205] At block 806, method 800 can include associating the characteristic of the cell device with statistical noise margin information for the cell device (e.g., using communication component 400).

[00206] Turning now to **FIG. 9**, at block 902, method 900 can include determining, by a unit comprising a processor, one or more characteristics that pertain to respective cell devices associated with a circuit design, wherein the characteristics include functions of respective robustness data for the cell devices (e.g., using statistical analysis / characteristic determination component 500 of robustness determination component 402).

[00207] At block 904, method 900 can include determining a quantification of reliability for the circuit based on composing respective characteristics for the cell devices of the circuit (e.g., using quantification component 502). At block 906, method 900 can include predicting a yield of the circuit based on the quantification of the reliability for the circuit (e.g., using prediction component 404).

[00208] Turning now to **FIG. 10**, at block 1002, method 1000 can include determining, by a unit comprising a processor, characteristics that pertain to candidate cell devices that are candidates for association with a circuit, wherein the characteristics include functions of respective robustness data for the candidate cell devices, and wherein the respective robustness data is associated with parameter variations of the candidate cell devices that are related to noises of the plurality of candidate cell devices, respectively (e.g., using statistical analysis / characteristic determination component 500 of robustness determination component 402).

[00209] At block 1004, method 1000 can include selecting one or more cell devices of the candidate cell devices based on the determined characteristics for the candidate cell devices (e.g., using circuit design component 406). At block 1006, method 1000 can include determining a design for the circuit based on the selected one or more cell devices (e.g., using circuit design component 406).

[00210] **FIG. 42** is a block diagram illustrating an example computing device 4200 that is arranged for determination of circuit robustness in accordance with the present disclosure. In a very basic configuration 4202, computing device 4200 typically includes one or more processors 4204 and a system memory 4206. A memory bus 4208 can be used for communicating between processor 4204 and system memory 4206.

[00211] Depending on the desired configuration, processor 4204 can be of any type including but not limited to a microprocessor (μP), a microcontroller (μC), a digital signal processor (DSP), or any combination thereof. Processor 4204 can include one more levels of caching, such as a level one cache 4210 and a level two cache 4212, a processor core 4214, and registers 4216. An example processor core 4214 can include an arithmetic logic unit (ALU), a floating point unit (FPU), a digital signal processing (DSP) core, or any combination thereof. An example memory controller 4218 can also be used with processor 4204, or in some implementations memory controller 4218 can be an internal part of processor 4204.

[00212] Depending on the desired configuration, system memory 4206 can be of any type including but not limited to volatile memory (such as RAM), non-volatile memory (such as

ROM, flash memory, etc.) or any combination thereof. System memory 4206 can include an operating system 4220, one or more applications 4222, and program data 4224. Application 4222 can include a robustness determination component 4226 that is arranged to determine statistical information about one or more VTCs for a cell device, and determine robustness for a circuit composed of one or more of the cell devices for which the VTCs are determined. In some embodiments, computing device 4200 can be or be included in device 102. Program data 4224 can include, for example, voltage transfer characteristic data 4228 that can be useful for quantification of robustness of a circuit as is described herein. In some embodiments, application 4222 can be arranged to operate with program data 4224 on operating system 4220 such that generation of circuit robustness information, prediction of yields and/or circuit design can be performed as described herein. This described basic configuration 4202 is illustrated in **FIG. 42** by those components within the inner dashed line.

[00213] Computing device 4200 can have additional features or functionality, and additional interfaces to facilitate communications between basic configuration 4202 and any required devices and interfaces. For example, a bus/interface controller 4230 can be used to facilitate communications between basic configuration 4202 and one or more data storage devices 4232 via a storage interface bus 4234. Data storage devices 4232 can be removable storage devices 4236, non-removable storage devices 4238, or a combination thereof. Examples of removable storage and non-removable storage devices include magnetic disk devices such as flexible disk drives and hard-disk drives (HDDs), optical disk drives such as compact disk (CD) drives or digital versatile disk (DVD) drives, solid state drives (SSDs), and tape drives to name a few. Example computer storage media can include volatile and nonvolatile, removable and non-removable media implemented in any method or technology for storage of information, such as computer readable instructions, data structures, program modules, or other data.

[00214] System memory 4206, removable storage devices 4236 and non-removable storage devices 4238 are examples of computer storage media. Computer storage media includes, but is not limited to, RAM, ROM, EEPROM, flash memory or other memory technology, CD-ROM, digital versatile disks (DVDs) or other optical storage, magnetic cassettes, magnetic tape, magnetic disk storage or other magnetic storage devices, or any other medium which can be used to store the desired information and which can be accessed by computing device 4200. Any such computer storage media can be part of computing device 4200.

[00215] Computing device 4200 can also include an interface bus 4240 for facilitating communication from various interface devices (e.g., output devices 4242, peripheral interfaces 4244, and communication devices 4246) to basic configuration 4202 via bus/interface controller 4230. Example output devices 4242 include a graphics processing unit 4248 and an audio processing unit 4250, which can be configured to communicate to various external devices such as a display or speakers via one or more A/V ports 4252. Example peripheral interfaces 4244 include a serial interface controller 4254 or a parallel interface controller 4256, which can be configured to communicate with external devices such as input devices (e.g., keyboard, mouse, pen, voice input device, touch input device, etc.) or other peripheral devices (e.g., printer, scanner, etc.) via one or more I/O ports 4258. An example communication device 4246 includes a network controller 4260, which can be arranged to facilitate communications with one or more other computing devices 4262 over a network communication link via one or more communication ports 4264.

[00216] Computing device 4200 can be implemented as a portion of a small-form factor portable (or mobile) electronic device such as a cell phone, a personal data assistant (PDA), a personal media player device, a wireless web-watch device, a personal headset device, an application specific device, or a hybrid device that include any of the above functions. Computing device 4200 can also be implemented as a personal computer including both laptop computer and non-laptop computer configurations.

[00217] A network communication link can be one example of a communication media. Communication media can typically be embodied by computer readable instructions, data structures, program modules, or other data in a modulated data signal, such as a carrier wave or other transport mechanism, and can include any information delivery media. A "modulated data signal" can be a signal that has one or more of its characteristics set or changed in such a manner as to encode information in the signal. By way of example, and not limitation, communication media can include wired media such as a wired network or direct-wired connection, and wireless media such as acoustic, radio frequency (RF), microwave, infrared (IR) and other wireless media. The term computer readable media as used herein can include both storage media and communication media.

[00218] In an illustrative embodiment, any of the operations, processes, etc. described herein can be implemented as computer-readable instructions stored on a computer-readable medium. The computer-readable instructions can be executed by a processor of a mobile unit, a network element, and/or any other computing device.

[00219] The use of hardware or software may be generally (but not always, in that in certain contexts the choice between hardware and software can become significant) a design choice representing cost vs. efficiency tradeoffs. There are various vehicles by which processes and/or systems and/or other technologies described herein can be effected (e.g., hardware, software, and/or firmware), and that the preferred vehicle will vary with the context in which the processes and/or systems and/or other technologies are deployed. For example, if an implementer determines that speed and accuracy are paramount, the implementer can opt for a mainly hardware and/or firmware vehicle; if flexibility is paramount, the implementer can opt for a mainly software implementation; or, yet again alternatively, the implementer can opt for some combination of hardware, software, and/or firmware.

[00220] The foregoing detailed description has set forth various embodiments of the devices and/or processes via the use of block diagrams, flowcharts, and/or examples. Insofar as such block diagrams, flowcharts, and/or examples contain one or more functions and/or operations, each function and/or operation within such block diagrams, flowcharts, or examples can be implemented, individually and/or collectively, by a wide range of hardware, software, firmware, or virtually any combination thereof. In one embodiment, several portions of the subject matter described herein can be implemented via Application Specific Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs), digital signal processors (DSPs), or other integrated formats. However, some aspects of the embodiments disclosed herein, in whole or in part, can be equivalently implemented in integrated circuits, as one or more computer programs running on one or more computers (e.g., as one or more programs running on one or more computer systems), as one or more programs running on one or more processors (e.g., as one or more programs running on one or more microprocessors), as firmware, or as virtually any combination thereof, and that designing the circuitry and/or writing the code for the software and or firmware would be possible in light of this disclosure. In addition, the mechanisms of the subject matter described herein are capable of being distributed as a program product in a variety of forms, and that an illustrative embodiment of the subject matter described herein applies regardless of the particular type of signal bearing medium used to actually carry out the distribution. Examples of a signal bearing medium include, but are not limited to, the following: a recordable type medium such as a floppy disk, a hard disk drive, a CD, a DVD, a digital tape, a computer memory, etc.; and a transmission type medium such as a digital and/or an analog

communication medium (e.g., a fiber optic cable, a waveguide, a wired communications link, a wireless communication link, etc.).

[00221] Those skilled in the art will recognize that it is common within the art to describe devices and/or processes in the fashion set forth herein, and thereafter use engineering practices to integrate such described devices and/or processes into data processing systems. That is, at least a portion of the devices and/or processes described herein can be integrated into a data processing system via a reasonable amount of experimentation. A typical data processing system may generally include one or more of a system unit housing, a video display device, a memory such as volatile and non-volatile memory, processors such as microprocessors and digital signal processors, computational entities such as operating systems, drivers, graphical user interfaces, and applications programs, one or more interaction devices, such as a touch pad or screen, and/or control systems including feedback loops and control motors (e.g., feedback for sensing position and/or velocity; control motors for moving and/or adjusting components and/or quantities). A typical data processing system can be implemented utilizing any suitable commercially available components, such as those typically found in data computing/communication and/or network computing/communication systems.

[00222] The herein described subject matter sometimes illustrates different components contained within, or connected with, different other components. Such depicted architectures are merely examples, and many other architectures can be implemented which achieve the same functionality. In a conceptual sense, any arrangement of components to achieve the same functionality is effectively "associated" such that the desired functionality is achieved. Hence, any two components herein combined to achieve a particular functionality can be seen as "associated with" each other such that the desired functionality is achieved, irrespective of architectures or intermediate components. Likewise, any two components so associated can also be viewed as being "operably connected", or "operably coupled", to each other to achieve the desired functionality, and any two components capable of being so associated can also be viewed as being "operably coupleable", to each other to achieve the desired functionality. Specific examples of operably coupleable include but are not limited to physically mateable and/or physically interacting components and/or wirelessly interactable and/or wirelessly interacting components and/or logically interacting and/or logically interactable components.

[00223] With respect to the use of substantially any plural and/or singular terms herein, those having skill in the art can translate from the plural to the singular and/or from the singular to the plural as is appropriate to the context and/or application. The various singular/plural permutations can be expressly set forth herein for sake of clarity.

[00224] It will be understood by those within the art that, in general, terms used herein, and especially in the appended claims (e.g., bodies of the appended claims) are generally intended as "open" terms (e.g., the term "including" should be interpreted as "including but not limited to," the term "having" should be interpreted as "having at least," the term "includes" should be interpreted as "includes but is not limited to," etc.). It will be further understood by those within the art that if a specific number of an introduced claim recitation is intended, such an intent will be explicitly recited in the claim, and in the absence of such recitation no such intent is present. For example, as an aid to understanding, the following appended claims can contain usage of the introductory phrases "at least one" and "one or more" to introduce claim recitations. However, the use of such phrases should not be construed to imply that the introduction of a claim recitation by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim recitation to embodiments containing only one such recitation, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an" (e.g., "a" and/or "an" should be interpreted to mean "at least one" or "one or more"); the same holds true for the use of definite articles used to introduce claim recitations. In addition, even if a specific number of an introduced claim recitation is explicitly recited, those skilled in the art will recognize that such recitation should be interpreted to mean at least the recited number (e.g., the bare recitation of "two recitations," without other modifiers, means at least two recitations, or two or more recitations). Furthermore, in those instances where a convention analogous to "at least one of A, B, and C, etc." is used, in general such a construction is intended in the sense one having skill in the art would understand the convention (e.g., " a system having at least one of A, B, and C" would include but not be limited to systems that have A alone, B alone, C alone, A and B together, A and C together, B and C together, and/or A, B, and C together, etc.). In those instances where a convention analogous to "at least one of A, B, or C, etc." is used, in general such a construction is intended in the sense one having skill in the art would understand the convention (e.g., " a system having at least one of A, B, or C" would include but not be limited to systems that have A alone, B alone, C alone, A and B together, A and C together, B and C together, and/or A, B, and C together, etc.). It will be further understood by those within the art that virtually any disjunctive word and/or phrase

presenting two or more alternative terms, whether in the description, claims, or drawings, should be understood to contemplate the possibilities of including one of the terms, either of the terms, or both terms. For example, the phrase "A or B" will be understood to include the possibilities of "A" or "B" or "A and B."

[00225] In addition, where features or aspects of the disclosure are described in terms of Markush groups, those skilled in the art will recognize that the disclosure is also thereby described in terms of any individual member or subgroup of members of the Markush group.

[00226] As will be understood by one skilled in the art, for any and all purposes, such as in terms of providing a written description, all ranges disclosed herein also encompass any and all possible subranges and combinations of subranges thereof. Any listed range can be easily recognized as sufficiently describing and enabling the same range being broken down into at least equal halves, thirds, quarters, fifths, tenths, etc. As a non-limiting example, each range discussed herein can be readily broken down into a lower third, middle third and upper third, etc. As will also be understood by one skilled in the art all language such as "up to," "at least," and the like include the number recited and refer to ranges which can be subsequently broken down into subranges as discussed above. Finally, as will be understood by one skilled in the art, a range includes each individual member. Thus, for example, a group having 1-3 cells refers to groups having 1, 2, or 3 cells. Similarly, a group having 1-5 cells refers to groups having 1, 2, 3, 4, or 5 cells, and so forth.

[00227] The present disclosure is not to be limited in terms of the particular embodiments described in this application, which are intended as illustrations of various aspects. Many modifications and variations can be made without departing from its spirit and scope. Functionally equivalent methods and devices within the scope of the disclosure, in addition to those enumerated herein, are possible from the foregoing descriptions. Such modifications and variations are intended to fall within the scope of the appended claims. The present disclosure is to be limited only by the terms of the appended claims, along with the full scope of equivalents to which such claims are entitled. This disclosure is not limited to particular methods, computer-readable storage devices, systems or apparatus disclosed, which can, of course, vary. The terminology used herein is for the purpose of describing particular embodiments only, and is not intended to be limiting.

CLAIMS

What is claimed is:

1. A method, comprising:

performing, for a cell device by a unit comprising a processor, statistical analysis to obtain statistical information for the cell device that is indicative of a robustness of the cell device, wherein the robustness of the cell device pertains to a parameter variation of the cell device that is related to a noise of the cell device; and

determining a characteristic of the cell device based on the statistical information.

2. The method of claim 1, wherein determining the characteristic comprises determining a voltage transfer characteristic of the cell device.

3. The method of claim 1, wherein the parameter variation of the cell device comprises at least one of a channel length variation, an oxide thickness variation, or a dopant concentration variation of a component of the cell device, relative to another cell device.

4. The method of claim 1, further comprising:

associating the characteristic of the cell device with statistical noise margin information for the cell device.

5. The method of claim 4, wherein the associating comprises storing the characteristic in a data store that stores statistical noise margin information for the cell device.

6. The method of claim 1, wherein the cell device comprises at least one of an inverter, a memory device, a transistor, a logic gate, or a register.

7. A method, comprising:

determining, by a unit comprising a processor, characteristics that pertain to respective cell devices associated with circuit diagram information, wherein the characteristics include functions of respective robustness data for the cell devices; and

determining a quantification of reliability for the circuit diagram information based on composing respective characteristics for the cell devices of the circuit diagram information.

8. The method of claim 7, wherein the respective robustness data represents respective functions of parameter variations of the respective cell devices that are related to respective noises of the respective cell devices.

9. The method of claim 7, further comprising:

obtaining information indicative of a description of the cell devices from the circuit diagram information.

10. The method of claim 7, further comprising:

predicting a yield of the circuit diagram information based on the quantification of the reliability for the circuit diagram information.

11. A method, comprising:

determining, by a unit comprising a processor, characteristics that pertain to candidate cell devices that are candidates for association with a circuit, wherein the characteristics include functions of respective robustness data for the candidate cell devices, and wherein the respective robustness data is associated with parameter variations of the candidate cell devices that are related to noises of the plurality of candidate cell devices, respectively;

selecting one or more cell devices of the candidate cell devices based on the determined characteristics for the candidate cell devices; and

determining a design for the circuit based on the selected one or more cell devices.

12. The method of claim 11, further comprising:

predicting a yield of the circuit based on the determined characteristics of the one or more cell devices.

13. The method of claim 11, further comprising:

obtaining information indicative of a description of the candidate cell devices from circuit diagram information.

14. An apparatus, comprising:

a first component configured to perform statistical analysis for a cell device to determine a robustness of the cell device, wherein the robustness of the cell device is associated with a parameter variation of the cell device that is related to a noise of the cell device;

a second component coupled to the first component and configured to generate statistical information for the cell device based on the statistical analysis, wherein the statistical information is indicative of the robustness of the cell device; and

a third component coupled to the second component and configured to determine a characteristic of the cell device based on the statistical information.

15. The apparatus of claim 14, wherein the characteristic comprises a voltage transfer characteristic of the cell device.

16. The apparatus of claim 14, wherein the parameter variation of the cell device comprises at least one of a channel length variation, an oxide thickness variation, or a dopant concentration variation of a component of the cell device, relative to another cell device.

17. The apparatus of claim 14, further comprising:

a fourth component coupled to the third component and configured to associate the characteristic of the cell device with statistical noise margin information for the cell device.

18. A non-transitory computer-readable storage medium including computer-executable instructions stored thereon that, in response to execution by a processor, cause a device to perform operations, comprising:

determining characteristics that pertain to respective cell devices associated with a circuit design, wherein the characteristics include functions of respective robustness data for the cell devices, and wherein the respective robustness data are based on parameter variations of the respective cell devices and noises of the respective cell devices; and

determining a quantification of reliability for the circuit design based on composing the respective characteristics for the cell devices of the circuit design.

19. The non-transitory computer-readable storage medium of claim 18, wherein the operations further comprise:

predicting a yield of the circuit design based on the quantification of the reliability for the circuit design.

20. The non-transitory computer-readable storage medium of claim 18, wherein the characteristics comprise a voltage transfer characteristic of the respective cell devices.

21. The non-transitory computer-readable storage medium of claim 18, wherein the parameter variations comprise variations of at least one of channel length, oxide thickness, or dopant concentration for a component of the respective cell devices.

22. The non-transitory computer-readable storage medium of claim 18, wherein the operations further comprise storing the characteristics along with statistical noise margin information for the cell devices.

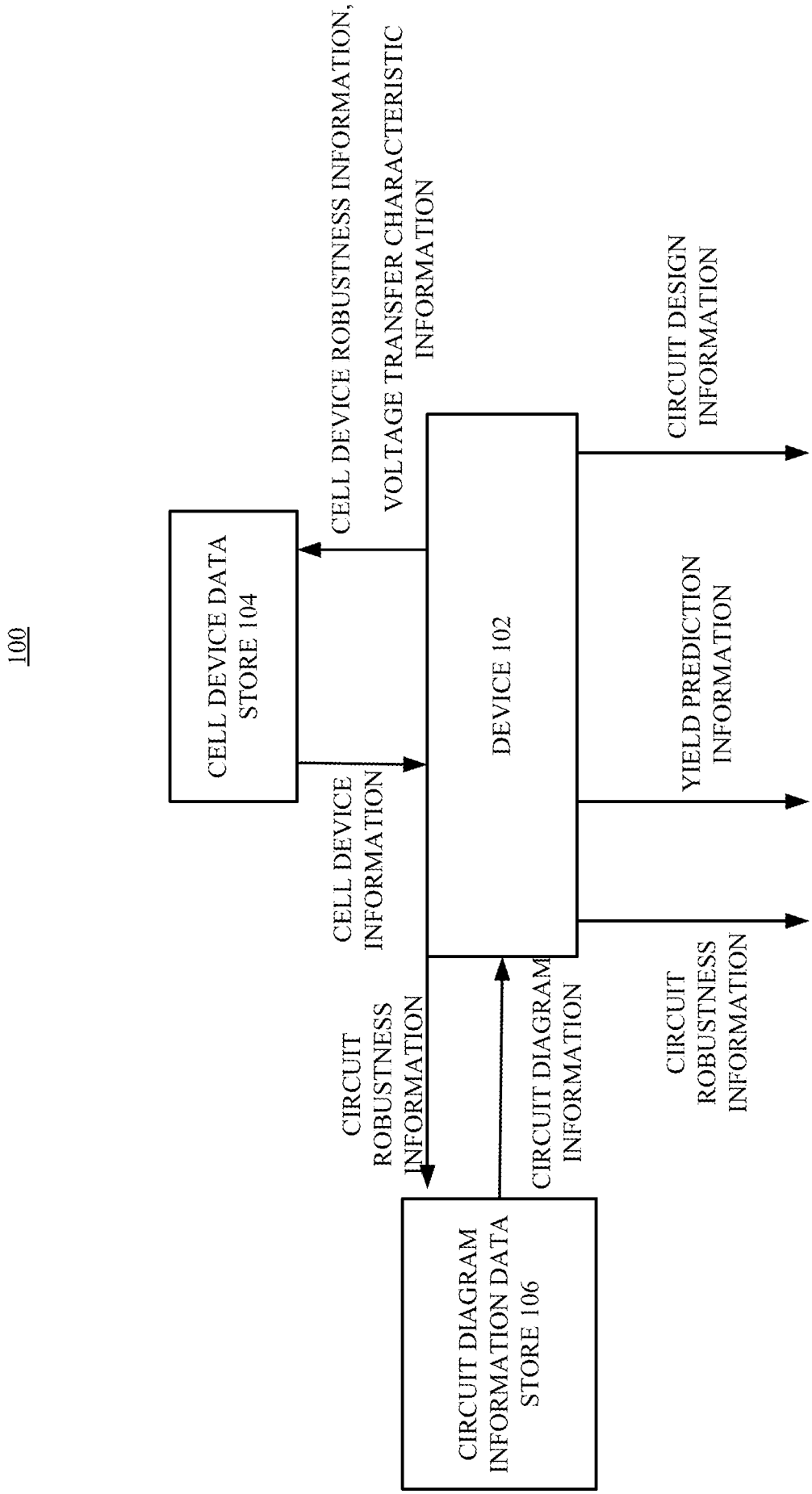
100
CELL DEVICE DATA STORE 104
CELL DEVICE ROBUSTNESS INFORMATION, VOLTAGE TRANSFER CHARACTERISTIC INFORMATION
CELL DEVICE INFORMATION
DEVICE 102
CIRCUIT DESIGN INFORMATION
YIELD PREDICTION INFORMATION
CIRCUIT ROBUSTNESS INFORMATION
CIRCUIT ROBUSTNESS INFORMATION
CIRCUIT DIAGRAM INFORMATION
CIRCUIT DIAGRAM INFORMATION DATA STORE 106

FIG. 1

CELL DEVICE DATA STORE 104		
CELL DEVICE TYPE 1 INFORMATION	CELL DEVICE TYPE 1 STATISTICAL NOISE MARGIN INFORMATION	CELL DEVICE TYPE 1 ROBUSTNESS INFORMATION / VTC INFORMATION
CELL DEVICE TYPE 2 INFORMATION	CELL DEVICE TYPE 2 STATISTICAL NOISE MARGIN INFORMATION	CELL DEVICE TYPE 2 ROBUSTNESS INFORMATION / VTC INFORMATION
CELL DEVICE TYPE 3 INFORMATION	CELL DEVICE TYPE 3 STATISTICAL NOISE MARGIN INFORMATION	CELL DEVICE TYPE 3 ROBUSTNESS INFORMATION / VTC INFORMATION

FIG. 2

CIRCUIT DIAGRAM INFORMATION DATA STORE 106		
CIRCUIT DIAGRAM 1 INFORMATION	CELL DEVICE TYPE 1 ROBUSTNESS INFORMATION	CELL DEVICE TYPE 1 YIELD PREDICTION INFORMATION
CIRCUIT DIAGRAM 2 INFORMATION	CELL DEVICE TYPE 2 ROBUSTNESS INFORMATION	CELL DEVICE TYPE 2 YIELD PREDICTION INFORMATION
CIRCUIT DIAGRAM 3 INFORMATION	CELL DEVICE TYPE 3 ROBUSTNESS INFORMATION	CELL DEVICE TYPE 3 YIELD PREDICTION INFORMATION

FIG. 3

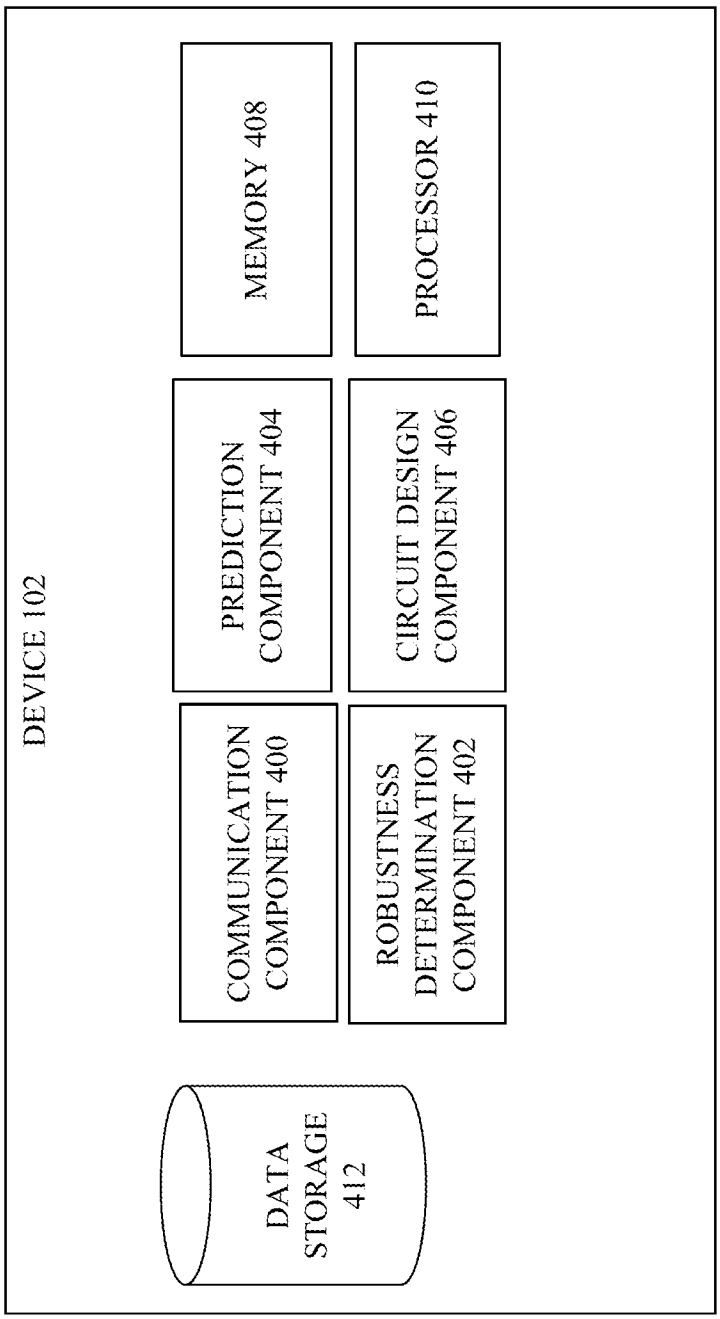
DEVICE 102
COMMUNICATION COMPONENT 400
PREDICTION COMPONENT 404
MEMORY 408
ROBUSTNESS DETERMINATION COMPONENT 402
CIRCUIT DESIGN COMPONENT 406
PROCESSOR 410
DATA STORAGE 412

FIG. 4

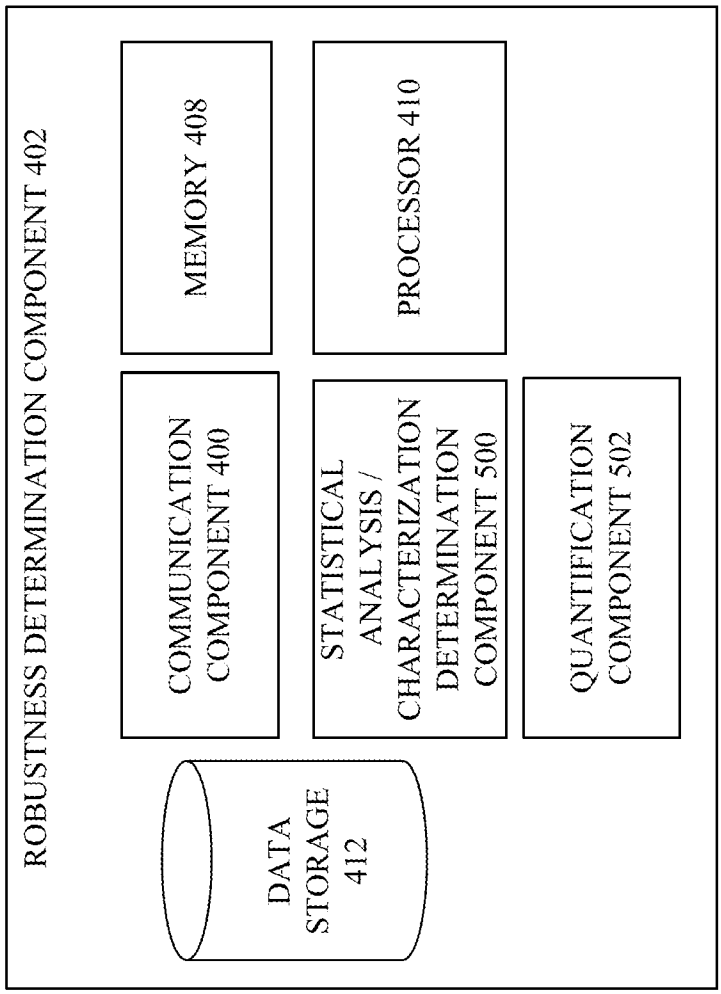
ROBUSTNESS DETERMINATION COMPONENT 402
COMMUNICATION COMPONENT 400
MEMORY 408
PROCESSOR 410
STATISTICAL ANALYSIS / CHARACTERIZATION DETERMINATION COMPONENT 500
QUANTIFICATION COMPONENT 502
DATA STORAGE 412

FIG. 5

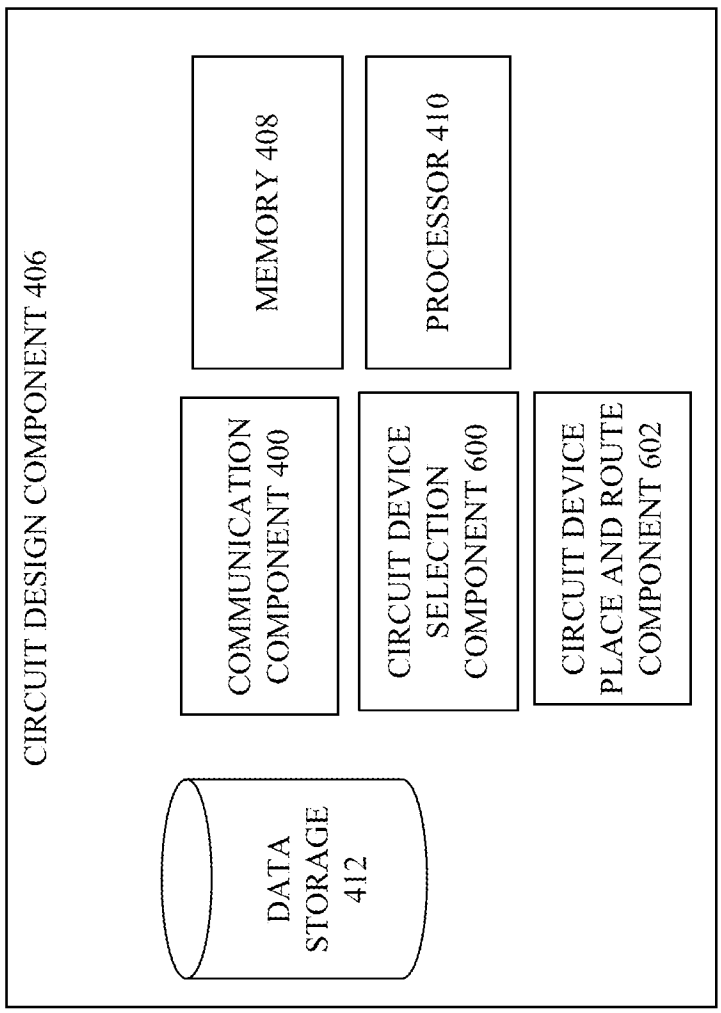
CIRCUIT DESIGN COMPONENT 406
MEMORY 408
PROCESSOR 410
COMMUNICATION COMPONENT 400
CIRCUIT DEVICE SELECTION COMPONENT 600
CIRCUIT DEVICE PLACE AND ROUTE COMPONENT 602
DATA STORAGE 412

FIG. 6

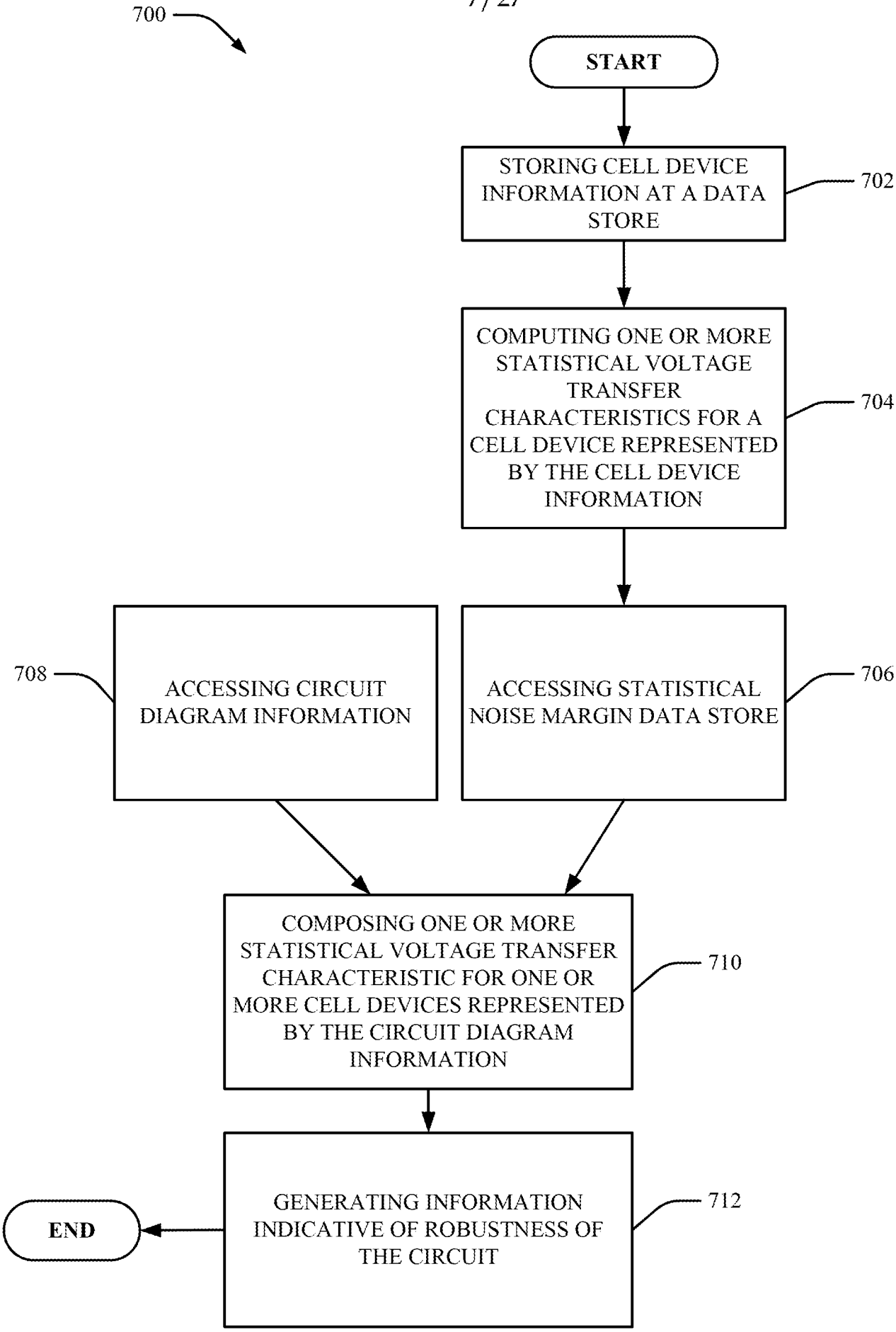
700
START
STORING CELL DEVICE INFORMATION AT A DATA STORE
702
COMPUTING ONE OR MORE STATISTICAL VOLTAGE TRANSFER CHARACTERISTICS FOR A CELL DEVICE REPRESENTED BY THE CELL DEVICE INFORMATION
704
708
ACCESSING CIRCUIT DIAGRAM INFORMATION
ACCESSING STATISTICAL NOISE MARGIN DATA STORE
706
COMPOSING ONE OR MORE STATISTICAL VOLTAGE TRANSFER CHARACTERISTIC FOR ONE OR MORE CELL DEVICES REPRESENTED BY THE CIRCUIT DIAGRAM INFORMATION
710
GENERATING INFORMATION INDICATIVE OF ROBUSTNESS OF THE CIRCUIT
712
END

FIG. 7

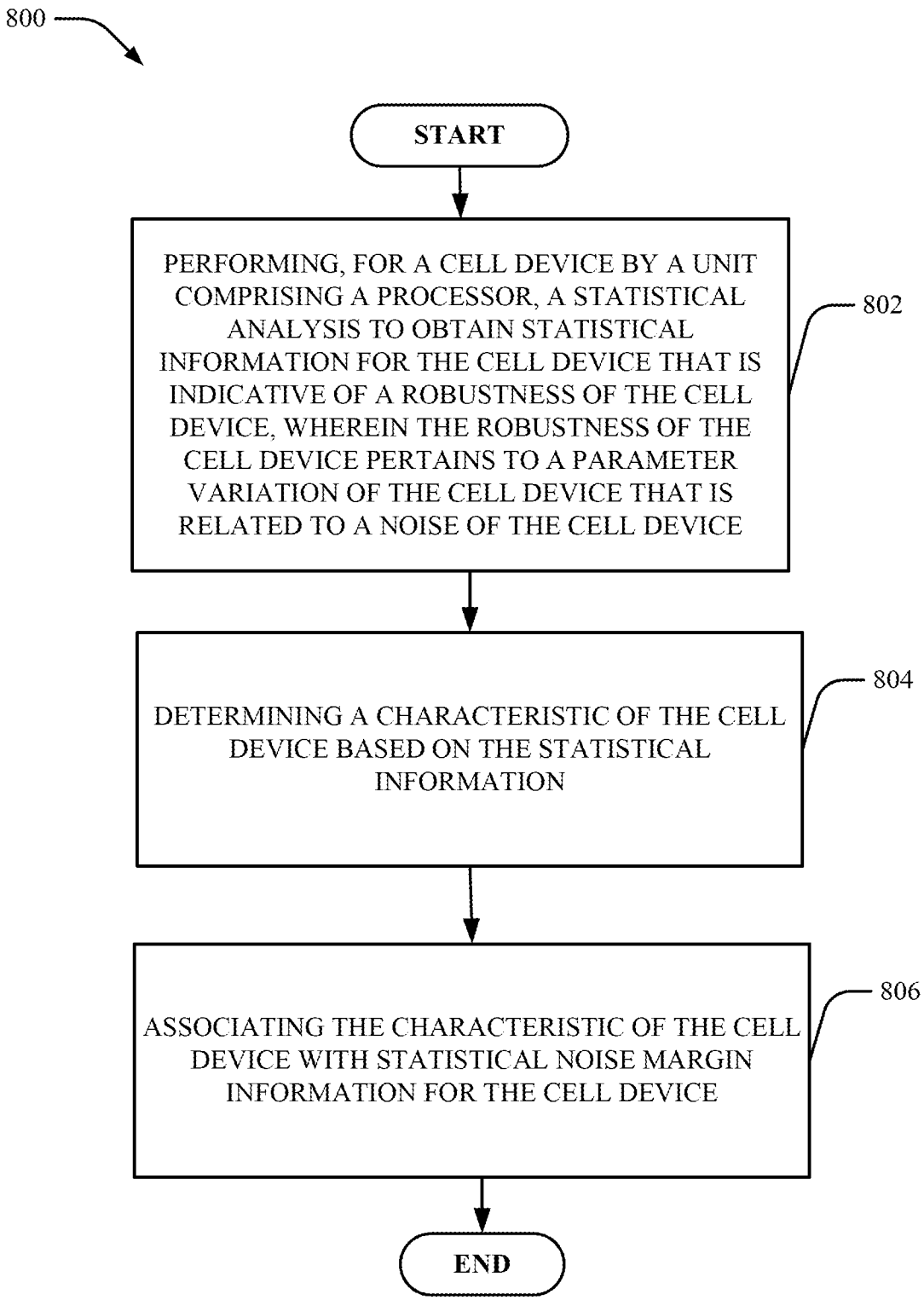
800
START
PERFORMING, FOR A CELL DEVICE BY A UNIT COMPRISING A PROCESSOR, A STATISTICAL ANALYSIS TO OBTAIN STATISTICAL INFORMATION FOR THE CELL DEVICE THAT IS INDICATIVE OF A ROBUSTNESS OF THE CELL DEVICE, WHEREIN THE ROBUSTNESS OF THE CELL DEVICE PERTAINS TO A PARAMETER VARIATION OF THE CELL DEVICE THAT IS RELATED TO A NOISE OF THE CELL DEVICE
802
DETERMINING A CHARACTERISTIC OF THE CELL DEVICE BASED ON THE STATISTICAL INFORMATION
804
ASSOCIATING THE CHARACTERISTIC OF THE CELL DEVICE WITH STATISTICAL NOISE MARGIN INFORMATION FOR THE CELL DEVICE
806
END

FIG. 8

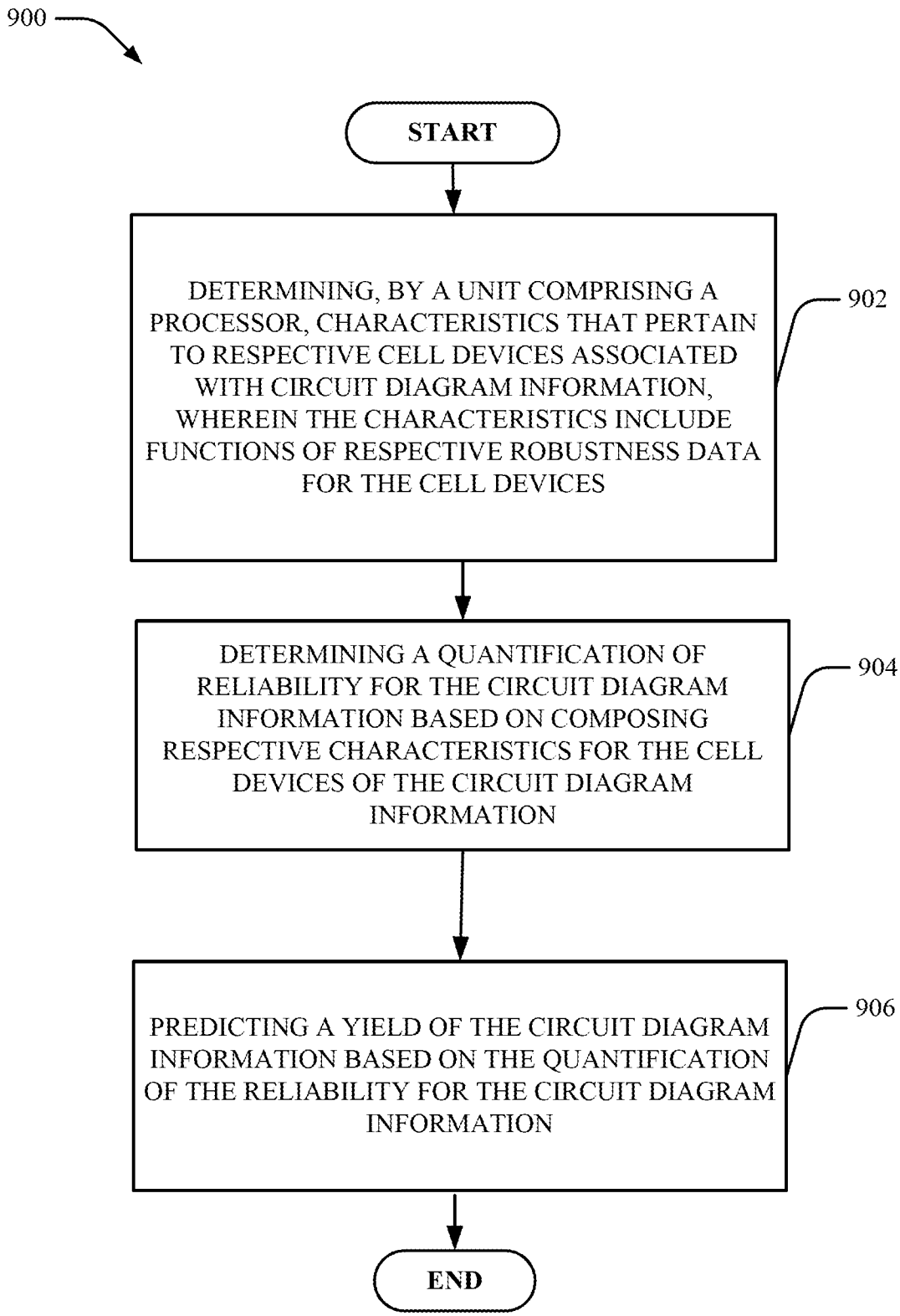
900
START
DETERMINING, BY A UNIT COMPRISING A PROCESSOR, CHARACTERISTICS THAT PERTAIN TO RESPECTIVE CELL DEVICES ASSOCIATED WITH CIRCUIT DIAGRAM INFORMATION, WHEREIN THE CHARACTERISTICS INCLUDE FUNCTIONS OF RESPECTIVE ROBUSTNESS DATA FOR THE CELL DEVICES
902
DETERMINING A QUANTIFICATION OF RELIABILITY FOR THE CIRCUIT DIAGRAM INFORMATION BASED ON COMPOSING RESPECTIVE CHARACTERISTICS FOR THE CELL DEVICES OF THE CIRCUIT DIAGRAM INFORMATION
904
PREDICTING A YIELD OF THE CIRCUIT DIAGRAM INFORMATION BASED ON THE QUANTIFICATION OF THE RELIABILITY FOR THE CIRCUIT DIAGRAM INFORMATION
906
END

FIG. 9

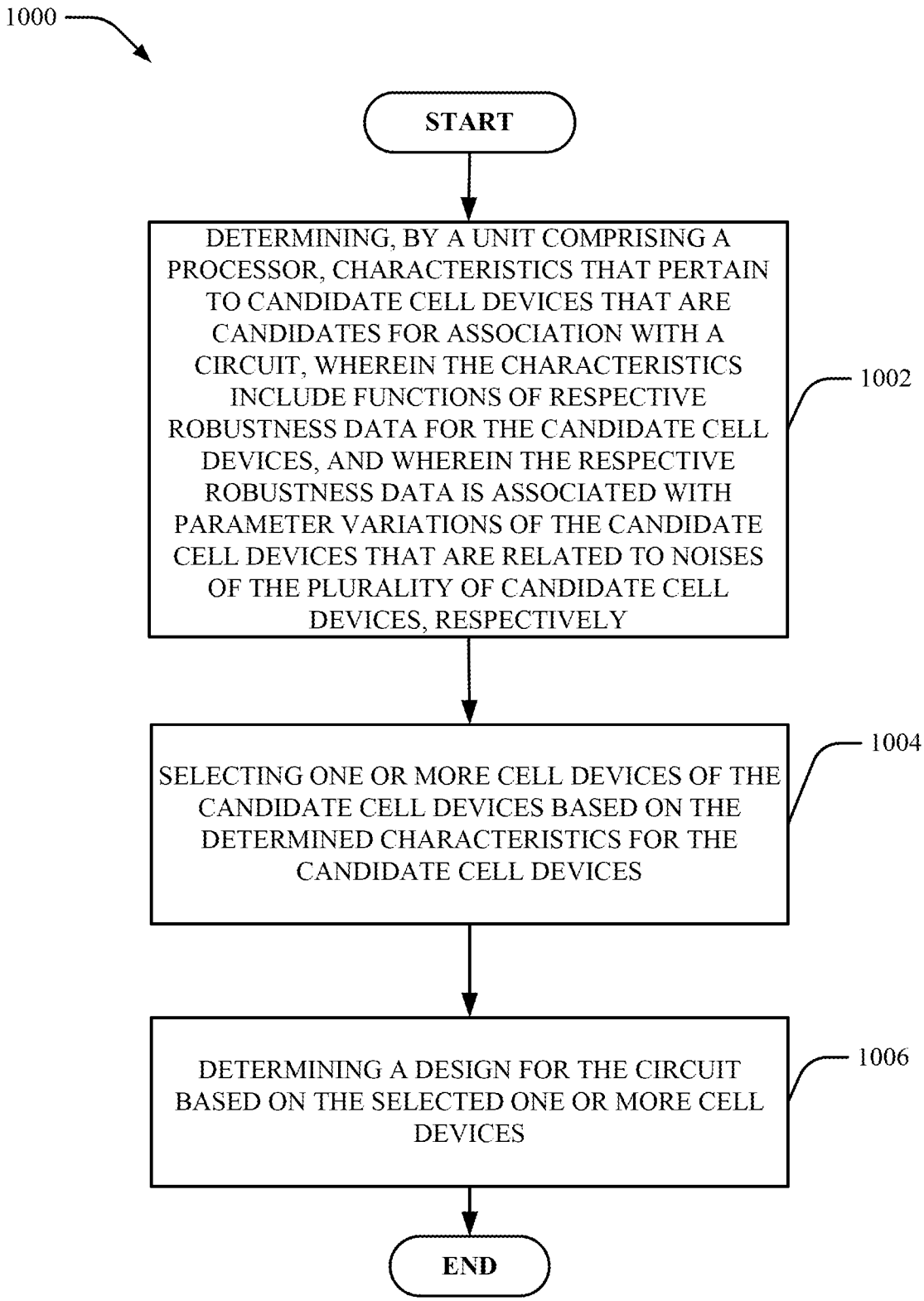
1000
START
DETERMINING, BY A UNIT COMPRISING A PROCESSOR, CHARACTERISTICS THAT PERTAIN TO CANDIDATE CELL DEVICES THAT ARE CANDIDATES FOR ASSOCIATION WITH A CIRCUIT, WHEREIN THE CHARACTERISTICS INCLUDE FUNCTIONS OF RESPECTIVE ROBUSTNESS DATA FOR THE CANDIDATE CELL DEVICES, AND WHEREIN THE RESPECTIVE ROBUSTNESS DATA IS ASSOCIATED WITH PARAMETER VARIATIONS OF THE CANDIDATE CELL DEVICES THAT ARE RELATED TO NOISES OF THE PLURALITY OF CANDIDATE CELL DEVICES, RESPECTIVELY
1002
SELECTING ONE OR MORE CELL DEVICES OF THE CANDIDATE CELL DEVICES BASED ON THE DETERMINED CHARACTERISTICS FOR THE CANDIDATE CELL DEVICES
1004
DETERMINING A DESIGN FOR THE CIRCUIT BASED ON THE SELECTED ONE OR MORE CELL DEVICES
1006
END

FIG. 10

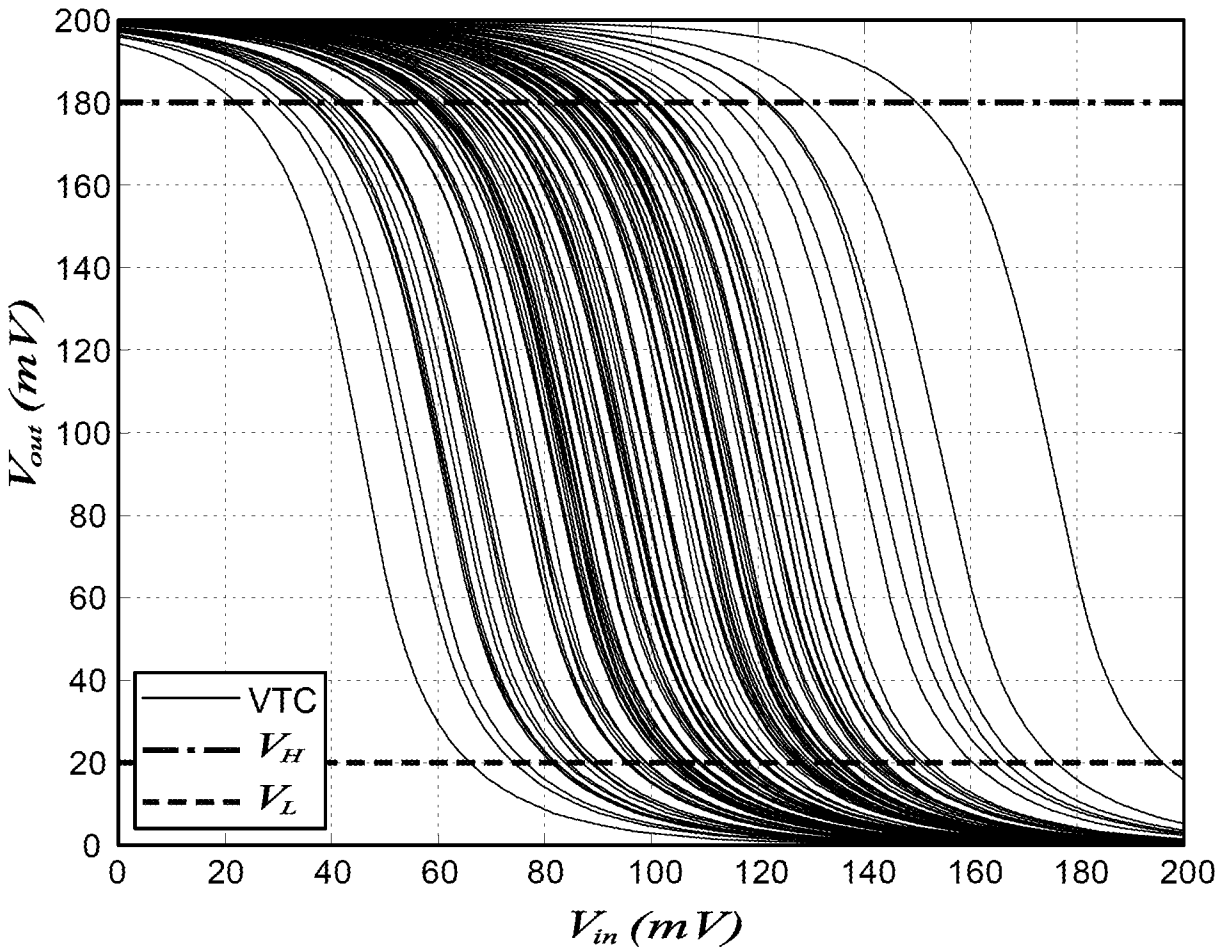
200
180
160
140
120
100
80
60
40
20
0
0
20
40
60
80
100
120
140
160
180
200
V_{out} (mV)
V_{in} (mV)
VTC
V_H
V_L

FIG. 11

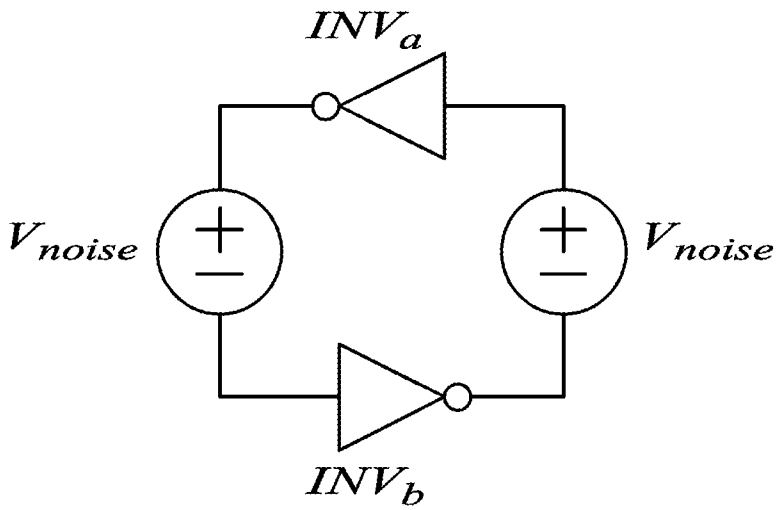
INV_a
V_{noise}
V_{noise}
INV_b

FIG. 12

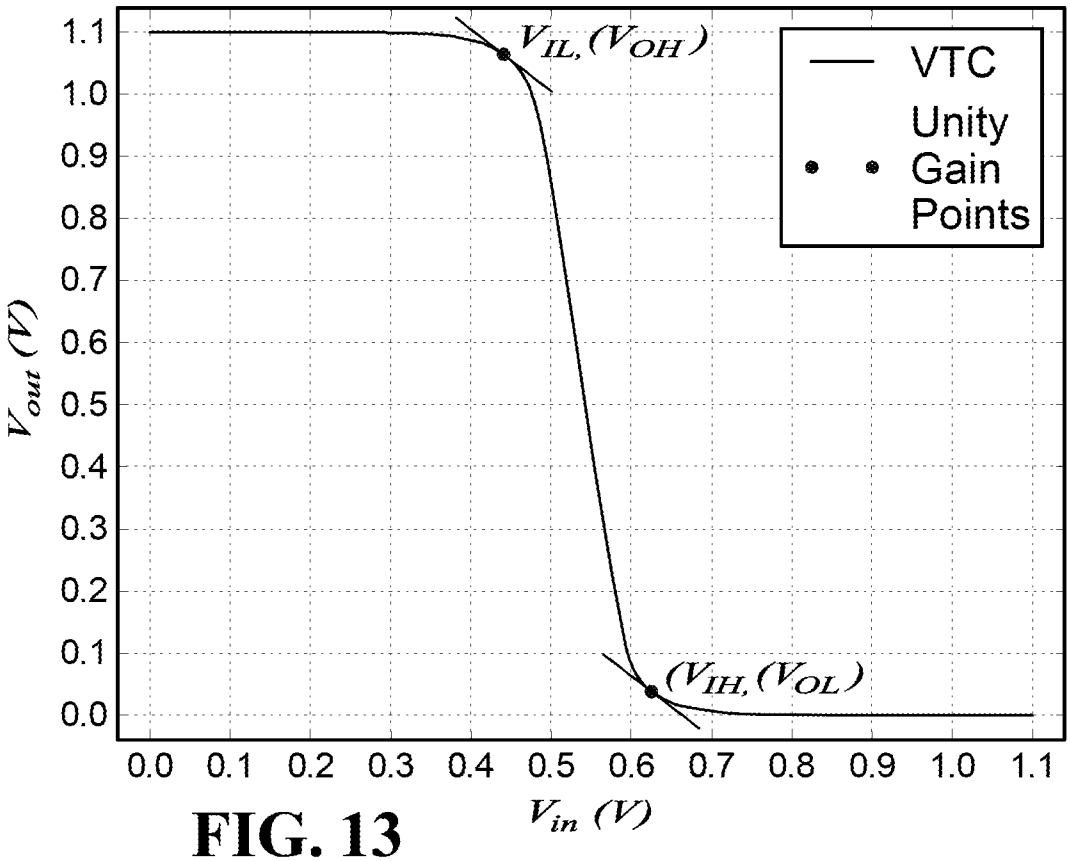
VTC
Unity Gain Points
$V_{IL}, (V_{OH})$
$(V_{IH}, (V_{OL})$
V_{out} (V)
V_{in} (V)
0.0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0 1.1

FIG. 13

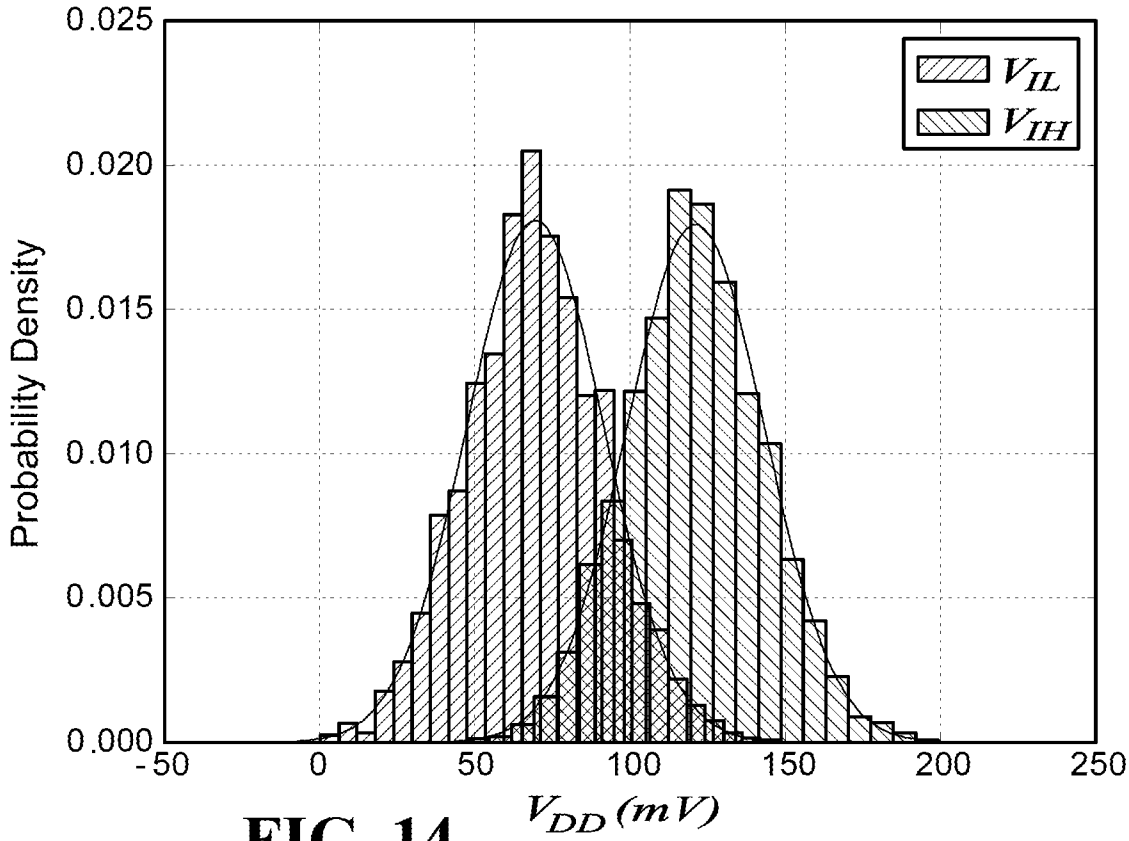
V_{IL}
V_{IH}
Probability Density
V_{DD} (mV)
0.000 0.005 0.010 0.015 0.020 0.025
-50 0 50 100 150 200 250

FIG. 14

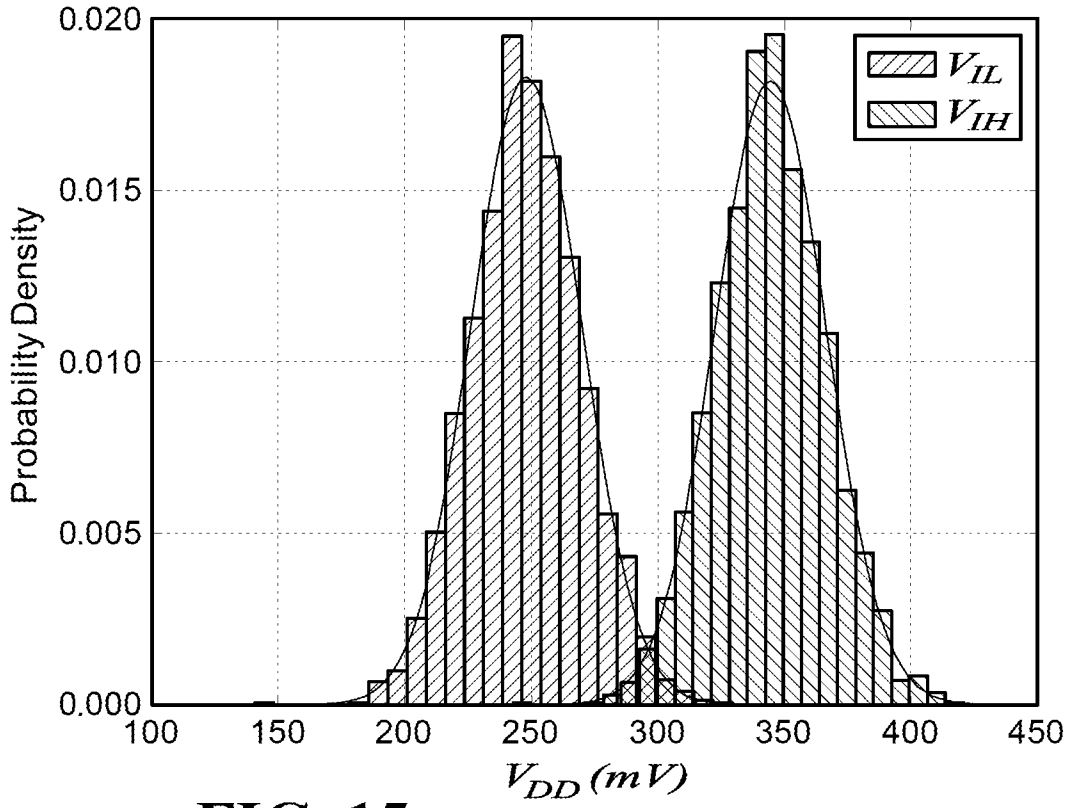
0.020
0.015
0.010
0.005
0.000
Probability Density
100
150
200
250
300
350
400
450
V_{DD} (mV)
V_{IL}
V_{IH}

FIG. 15

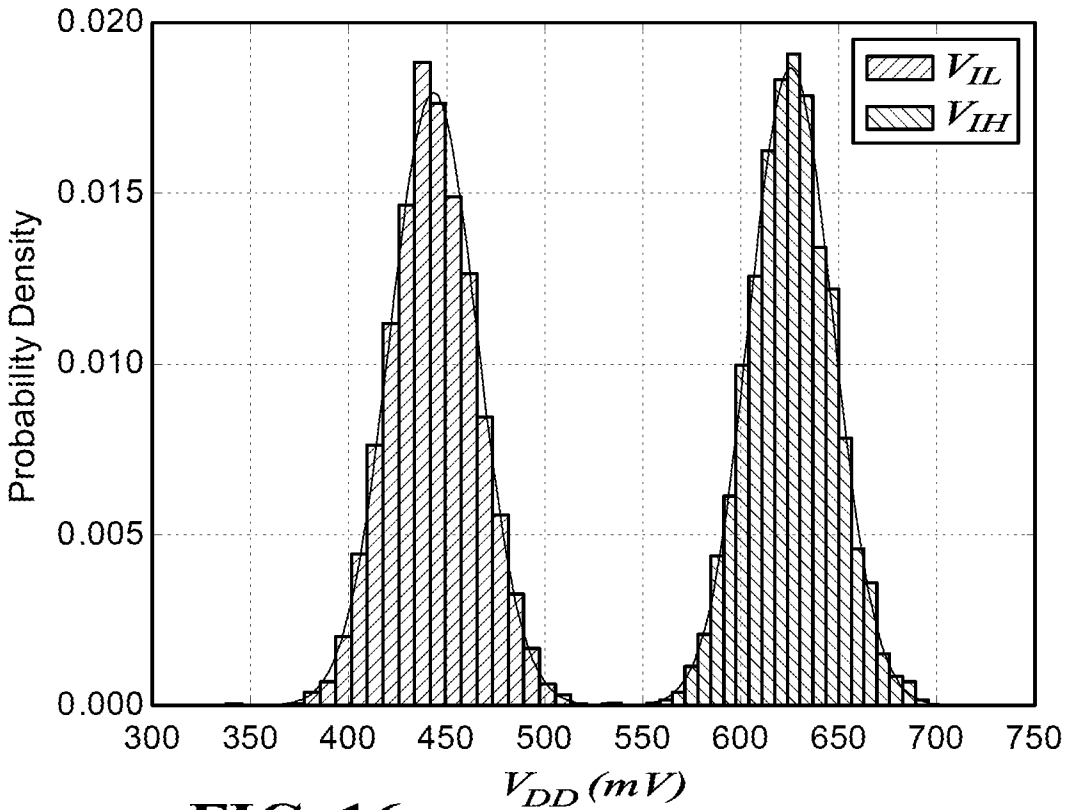
0.020
0.015
0.010
0.005
0.000
Probability Density
300
350
400
450
500
550
600
650
700
750
V_{DD} (mV)
V_{IL}
V_{IH}

FIG. 16

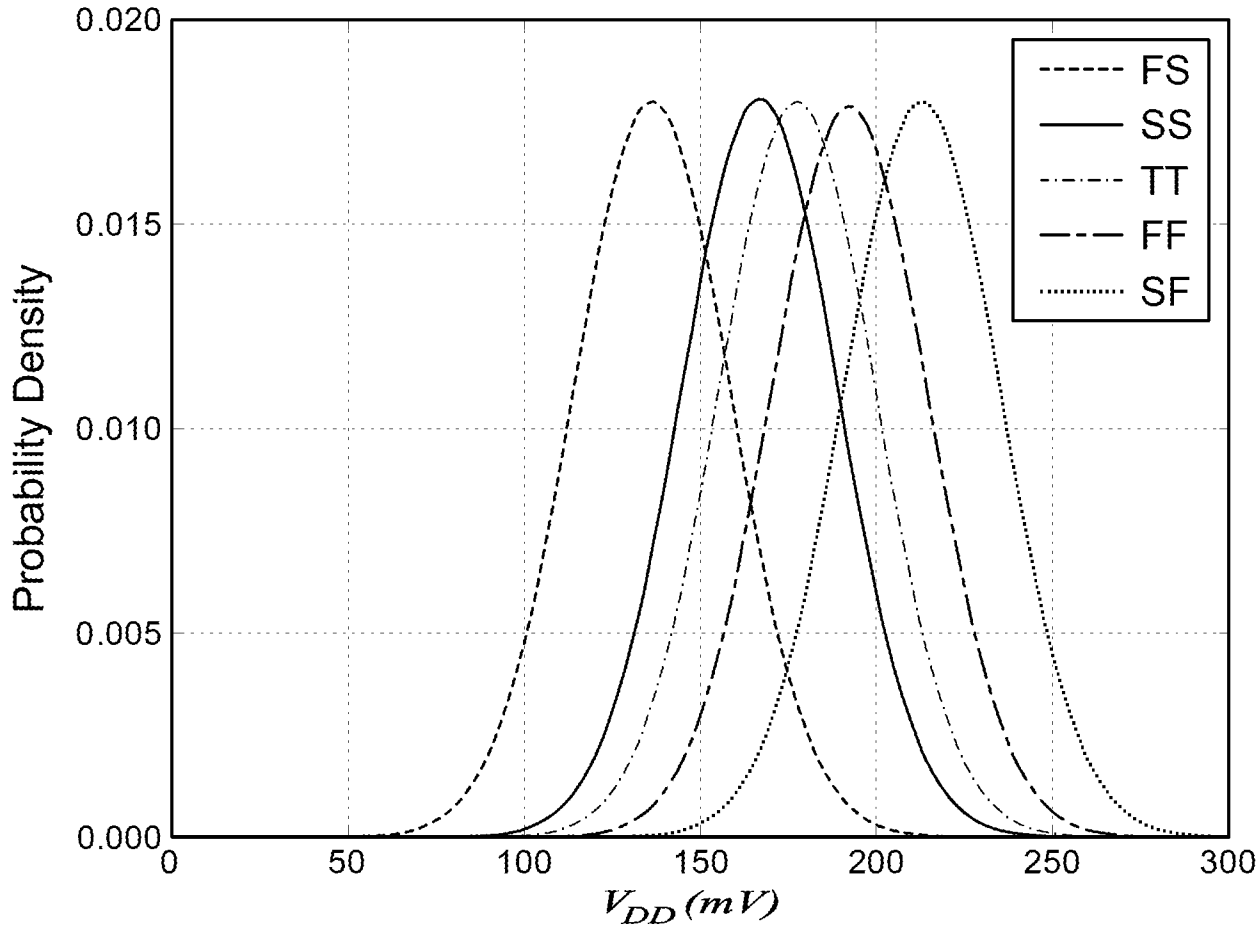
0.020
0.015
0.010
0.005
0.000
Probability Density
0
50
100
150
200
250
300
V_{DD} (mV)
FS
SS
TT
FF
SF

FIG. 17

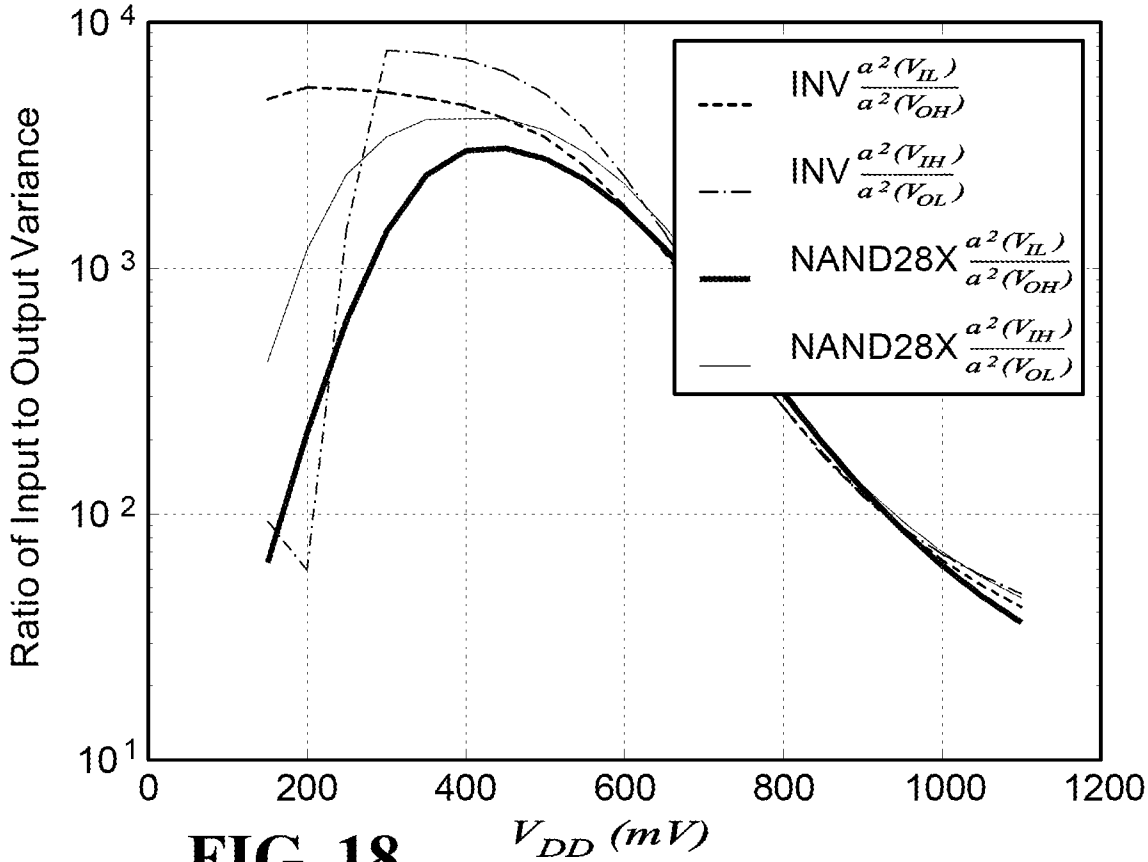
Ratio of Input to Output Variance
10^4
10^3
10^2
10^1
0
200
400
600
800
1000
1200
V_{DD} (mV)
INV $\frac{a^2(V_{IL})}{a^2(V_{OH})}$
INV $\frac{a^2(V_{IH})}{a^2(V_{OL})}$
NAND28X $\frac{a^2(V_{IL})}{a^2(V_{OH})}$
NAND28X $\frac{a^2(V_{IH})}{a^2(V_{OL})}$

FIG. 18

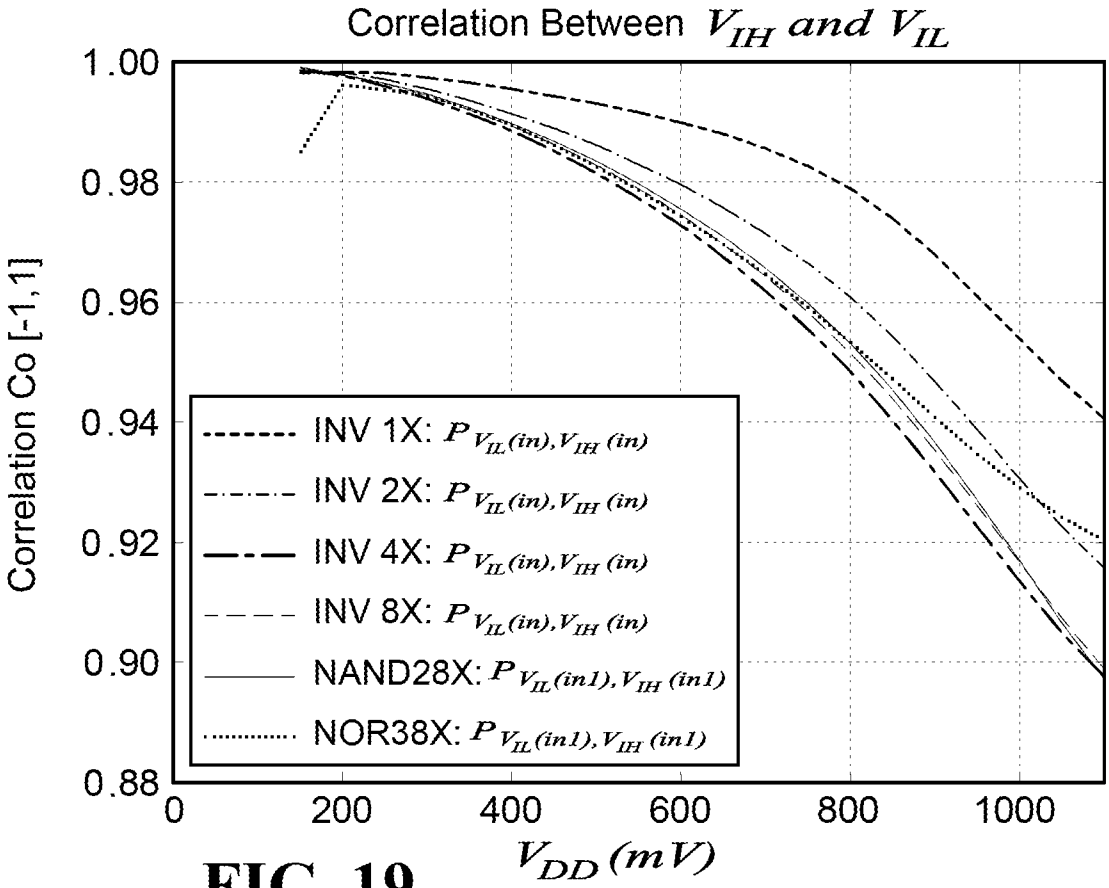
Correlation Between V_{IH} and V_{IL}
Correlation Co [-1,1]
1.00
0.98
0.96
0.94
0.92
0.90
0.88
0
200
400
600
800
1000
V_{DD} (mV)
INV 1X: $P_{V_{IL}(in),V_{IH}(in)}$
INV 2X: $P_{V_{IL}(in),V_{IH}(in)}$
INV 4X: $P_{V_{IL}(in),V_{IH}(in)}$
INV 8X: $P_{V_{IL}(in),V_{IH}(in)}$
NAND28X: $P_{V_{IL}(in1),V_{IH}(in1)}$
NOR38X: $P_{V_{IL}(in1),V_{IH}(in1)}$

FIG. 19

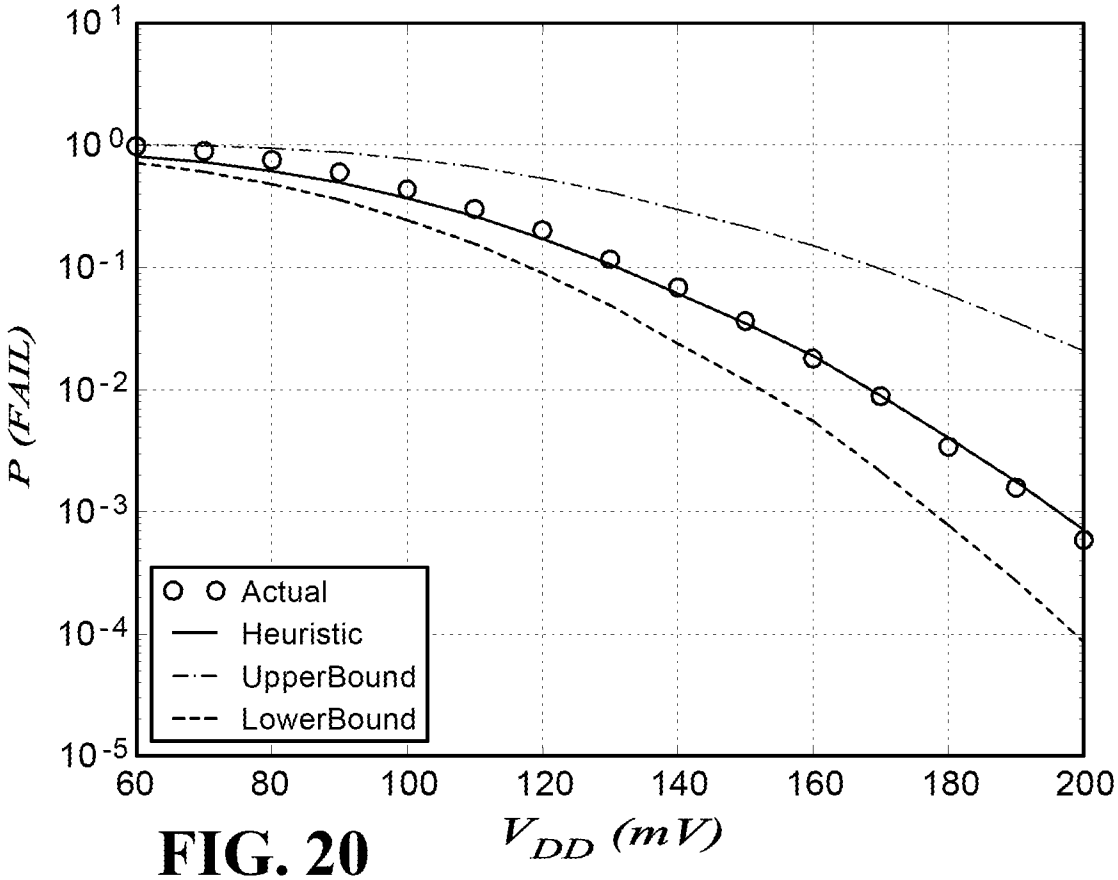
10 1
10 0
10-1
10-2
10-3
10-4
10-5
P (FAIL)
Actual
Heuristic
UpperBound
LowerBound
60
80
100
120
140
160
180
200
V_{DD} (mV)

FIG. 20

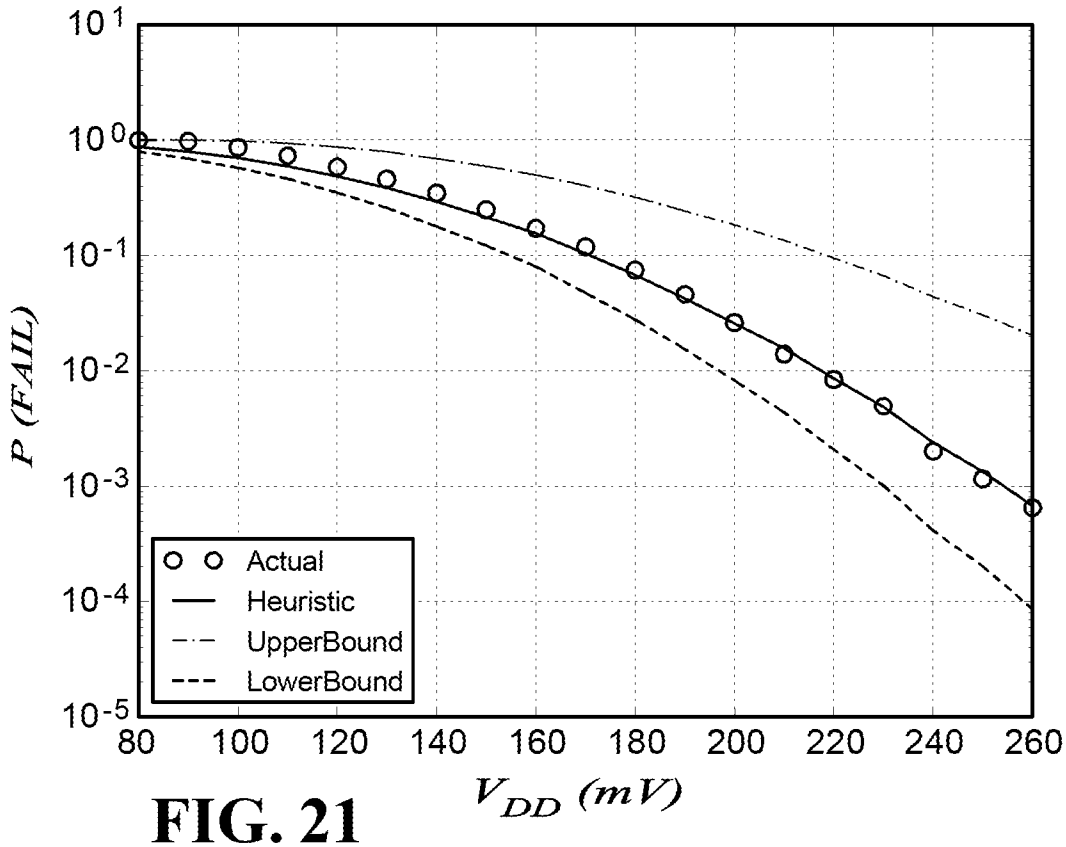
10 1
10 0
10-1
10-2
10-3
10-4
10-5
P (FAIL)
Actual
Heuristic
UpperBound
LowerBound
80
100
120
140
160
180
200
220
240
260
V_{DD} (mV)

FIG. 21

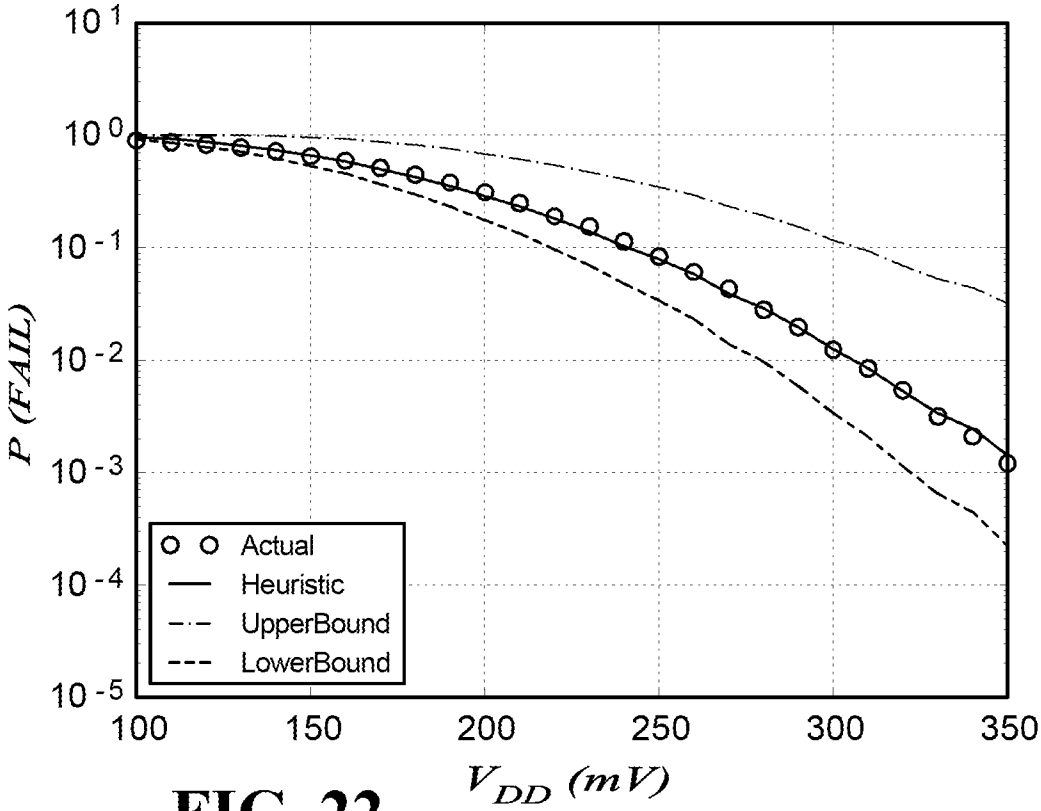
10 1
10 0
10 -1
10 -2
10 -3
10 -4
10 -5
P (FAIL)
Actual
Heuristic
UpperBound
LowerBound
100
150
200
250
300
350
V_{DD} (mV)

FIG. 22

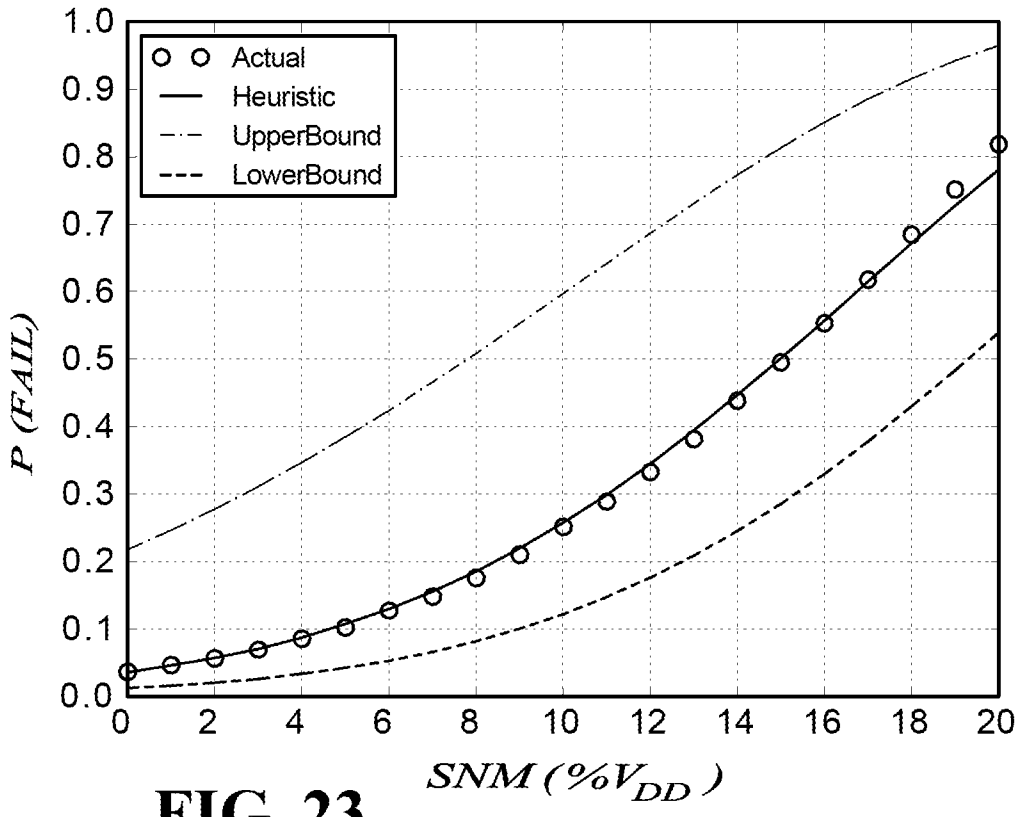
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
P (FAIL)
Actual
Heuristic
UpperBound
LowerBound
0
2
4
6
8
10
12
14
16
18
20
SNM (%V_{DD})

FIG. 23

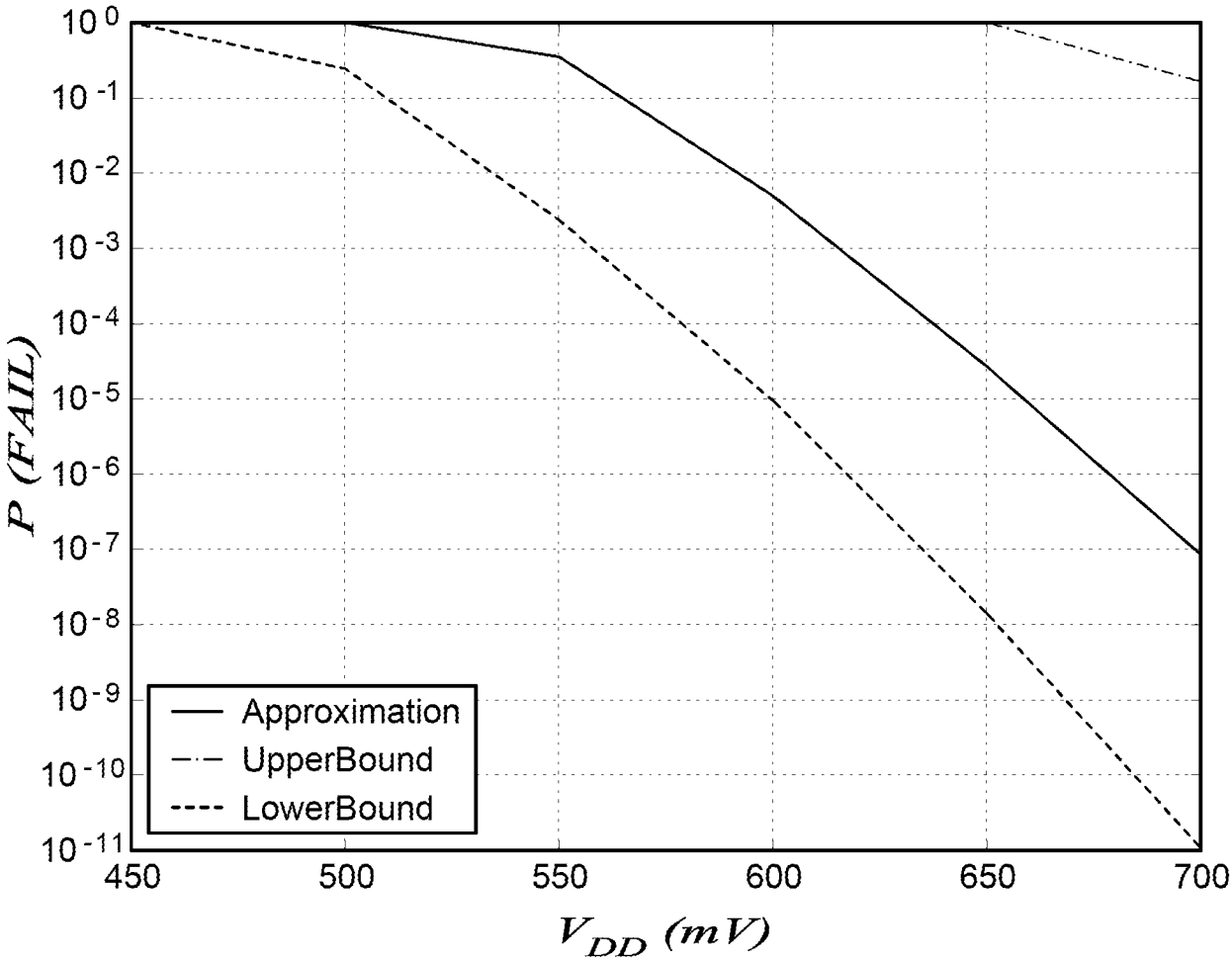
10 0
10 -1
10 -2
10 -3
10 -4
10 -5
10 -6
10 -7
10 -8
10 -9
10 -10
10 -11
P (FAIL)
Approximation
UpperBound
LowerBound
450
500
550
600
650
700
V_{DD} (mV)

FIG. 24

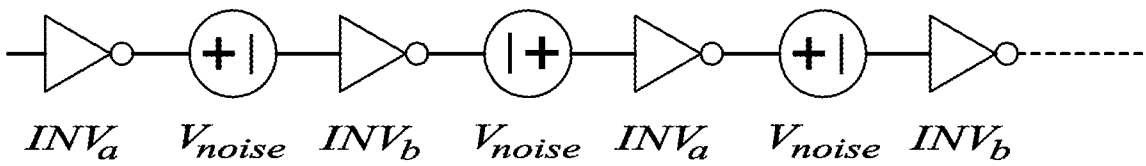
INV_a
V_{noise}
INV_b
V_{noise}
INV_a
V_{noise}
INV_b

FIG. 25

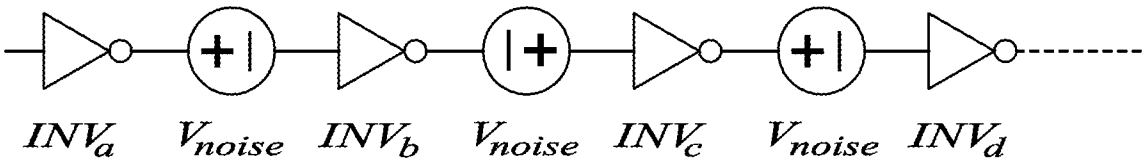
INV_a
V_{noise}
INV_b
V_{noise}
INV_c
V_{noise}
INV_d

FIG. 26

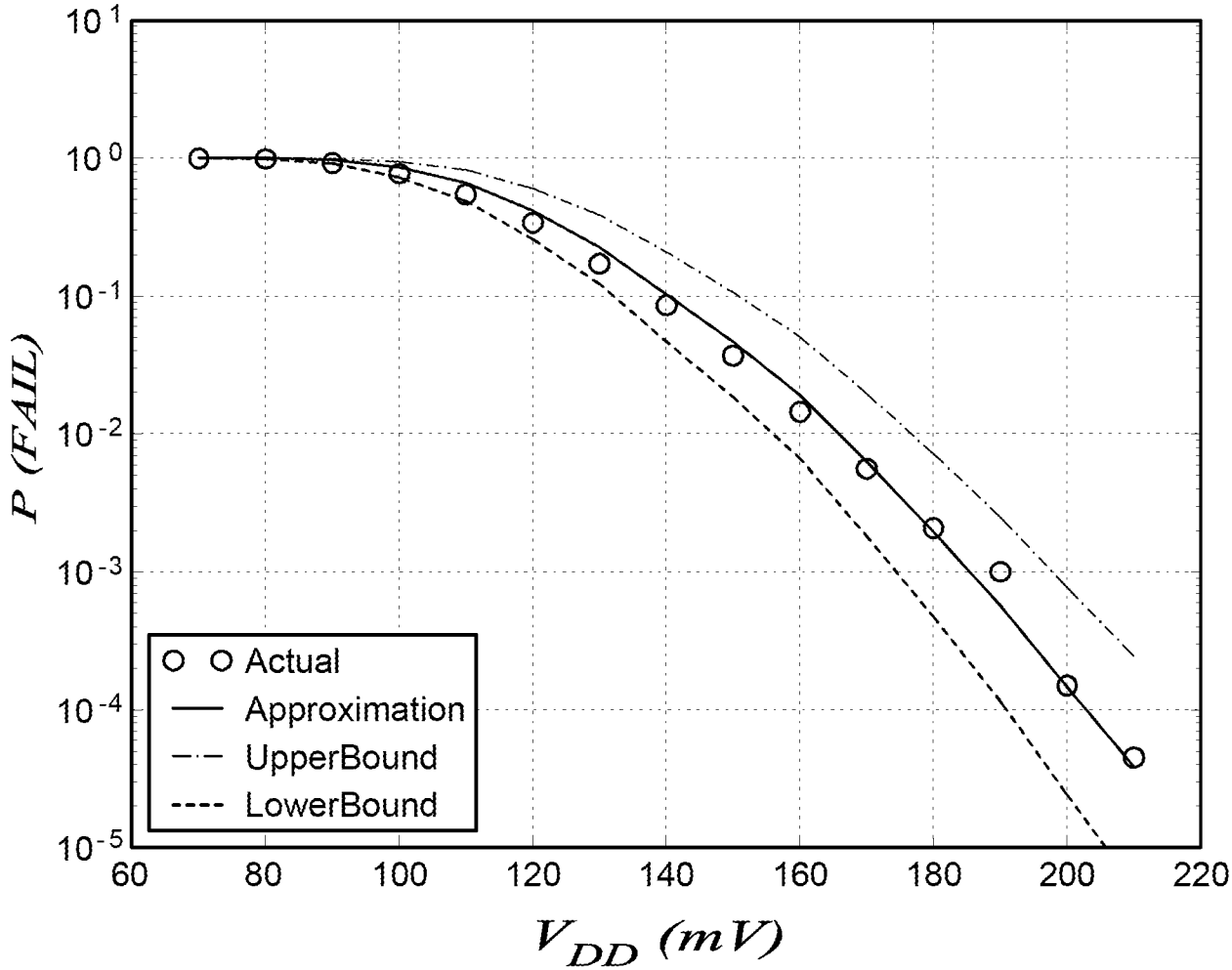
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
P (FAIL)
Actual
Approximation
UpperBound
LowerBound
60
80
100
120
140
160
180
200
220
V_{DD} (mV)

FIG. 27

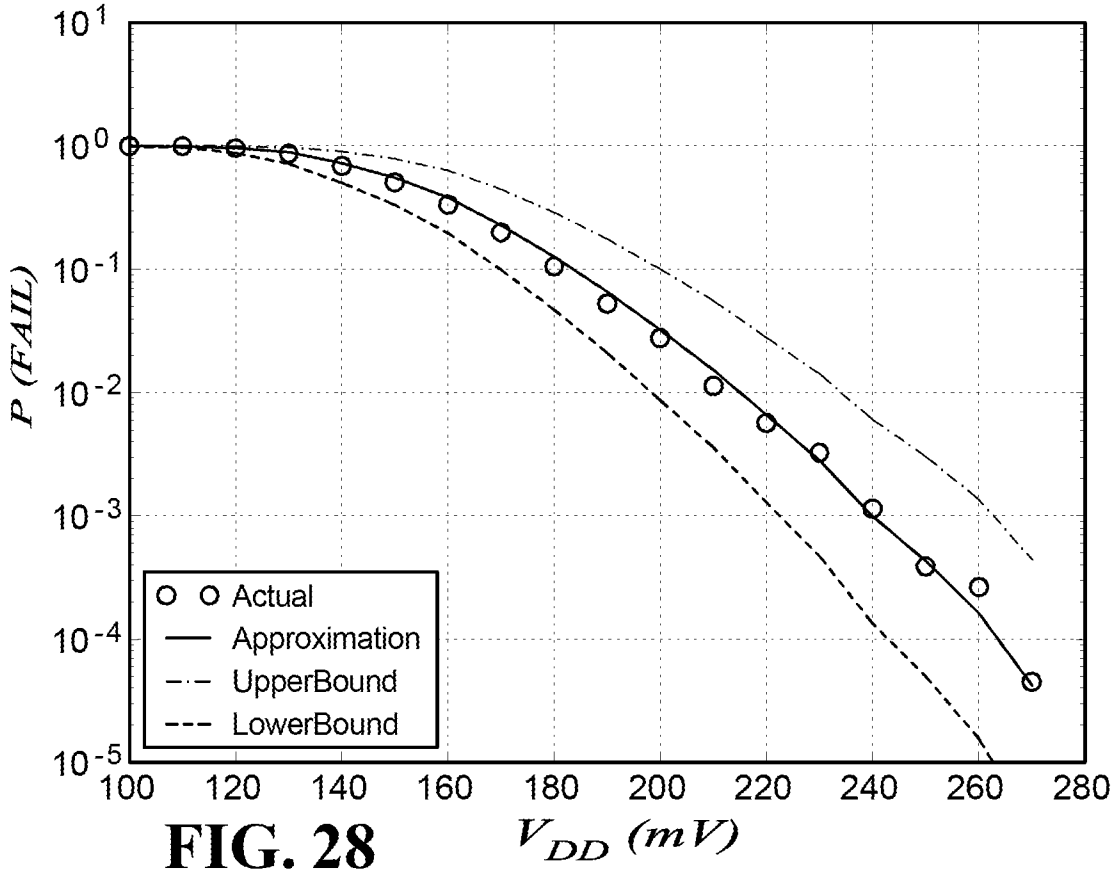
P (FAIL)
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
100 120 140 160 180 200 220 240 260 280
V_{DD} (mV)
Actual
Approximation
UpperBound
LowerBound

FIG. 28

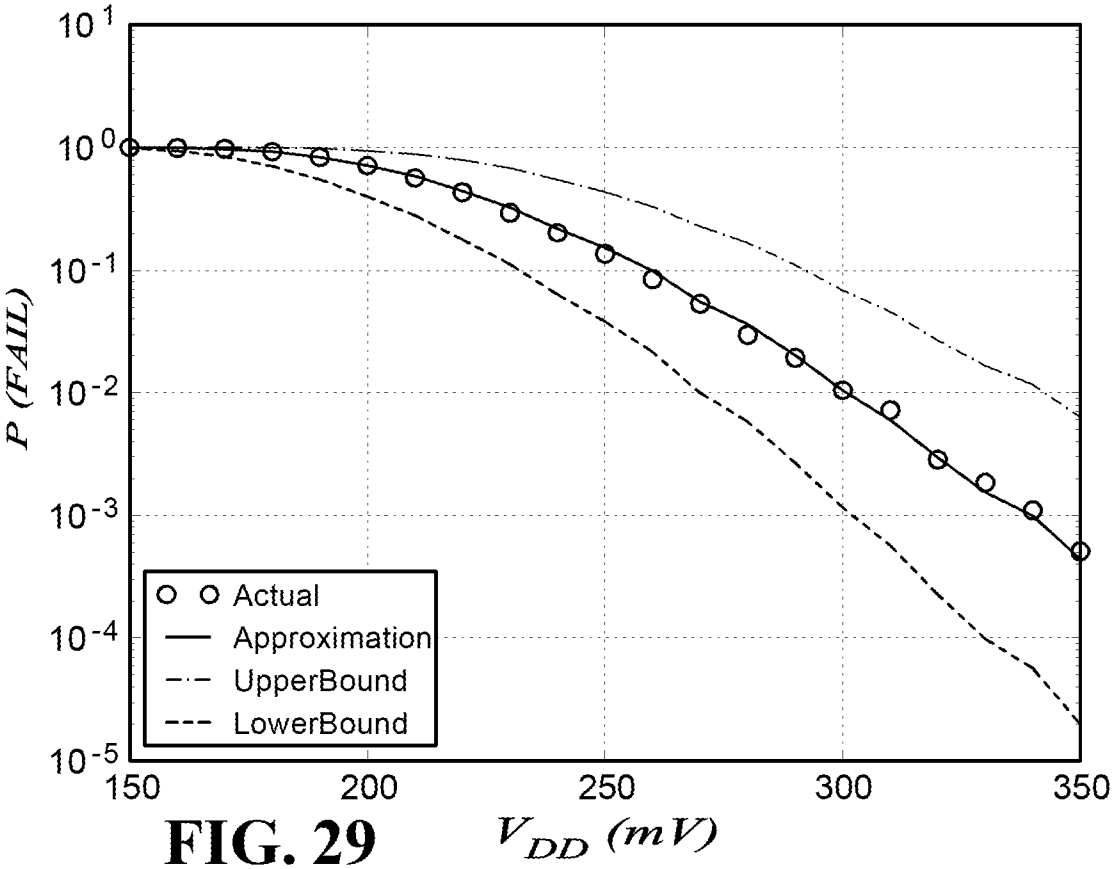
P (FAIL)
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
150 200 250 300 350
V_{DD} (mV)
Actual
Approximation
UpperBound
LowerBound

FIG. 29

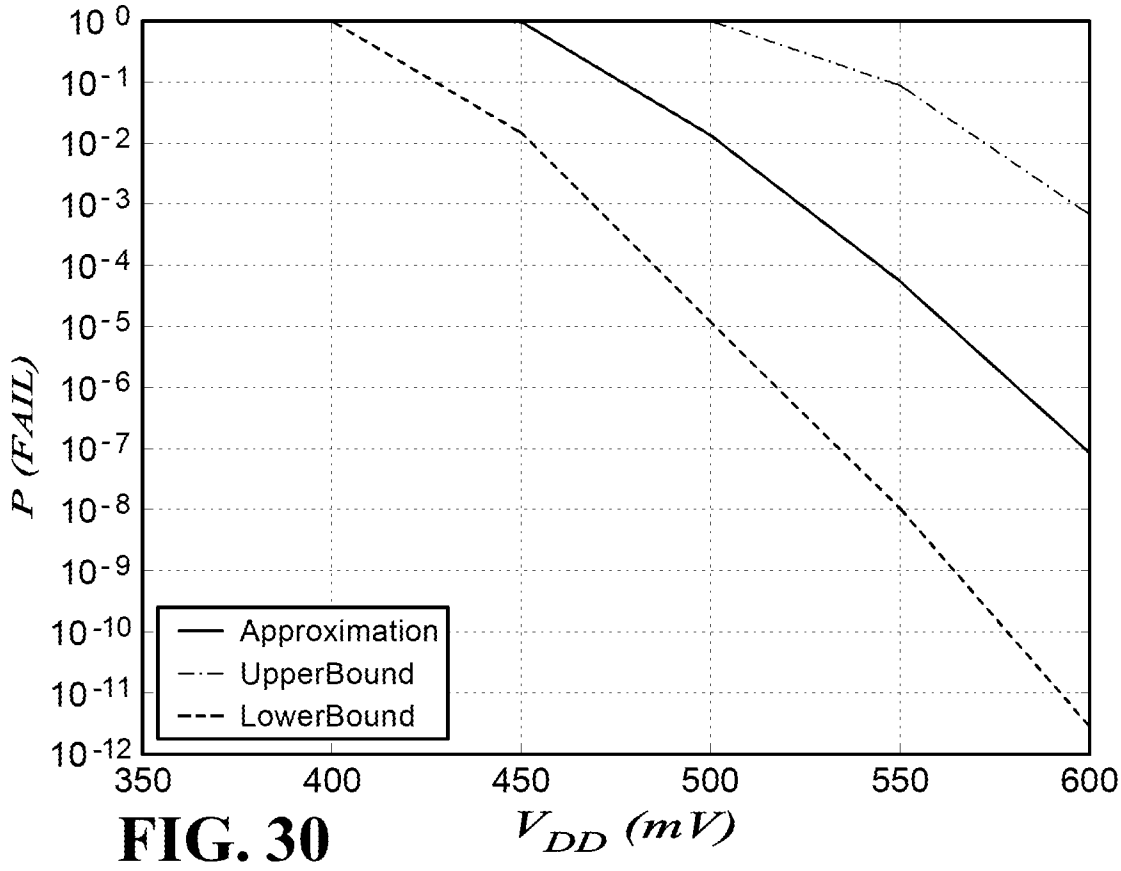
P (FAIL)
10 0
10 -1
10 -2
10 -3
10 -4
10 -5
10 -6
10 -7
10 -8
10 -9
10 -10
10 -11
10 -12
Approximation
UpperBound
LowerBound
350
400
450
500
550
600
V_{DD} (mV)

FIG. 30

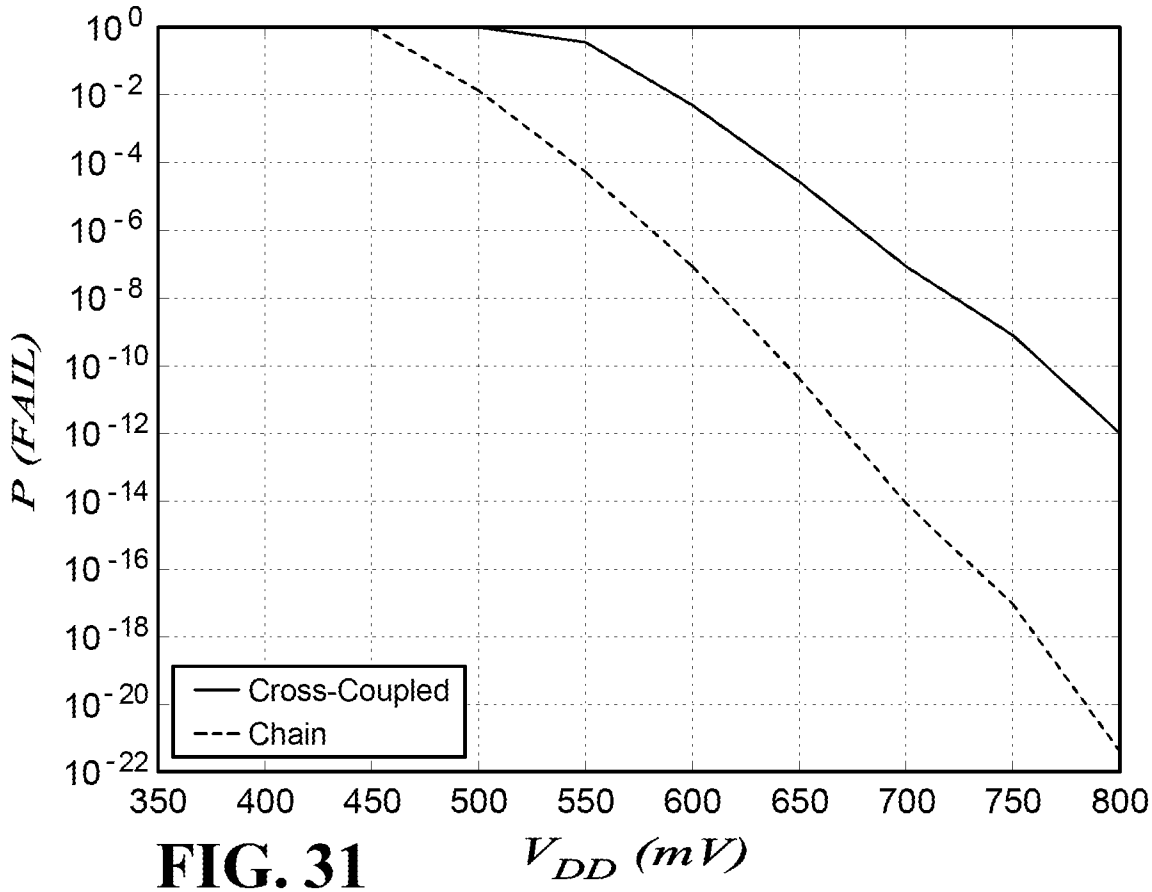
P (FAIL)
10 0
10 -2
10 -4
10 -6
10 -8
10 -10
10 -12
10 -14
10 -16
10 -18
10 -20
10 -22
Cross-Coupled
Chain
350
400
450
500
550
600
650
700
750
800
V_{DD} (mV)

FIG. 31

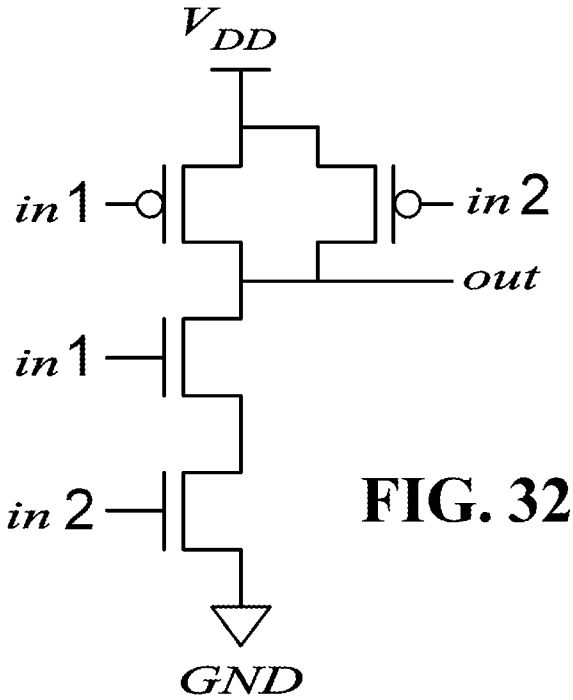
V_{DD}
in 1
in 2
out
in 1
in 2
GND

FIG. 32

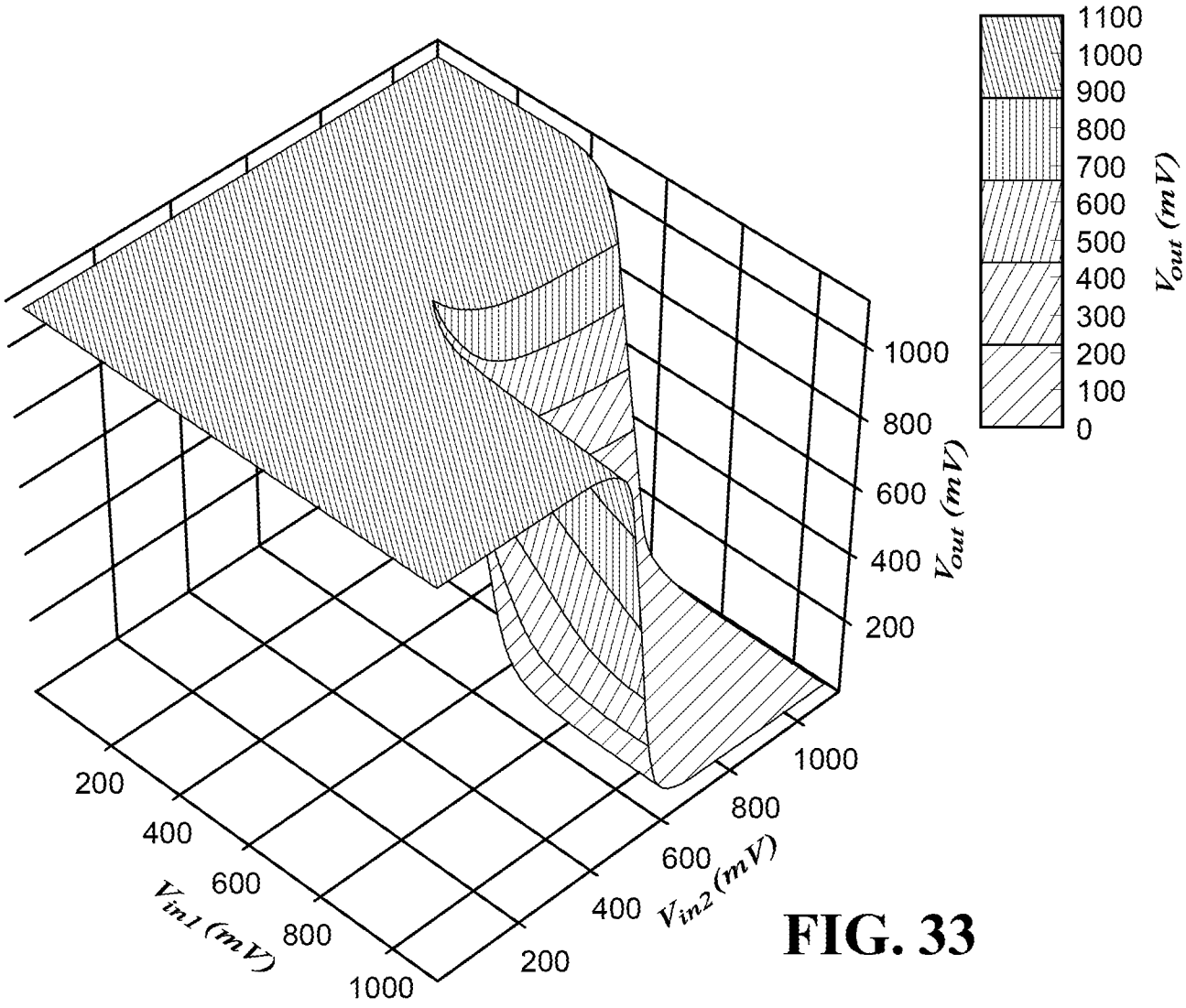
1100
1000
900
800
700
600
500
400
300
200
100
0
V_{out} (mV)
1000
800
600
400
200
V_{out} (mV)
200
400
600
800
1000
V_{in1} (mV)
200
400
600
800
1000
V_{in2} (mV)

FIG. 33

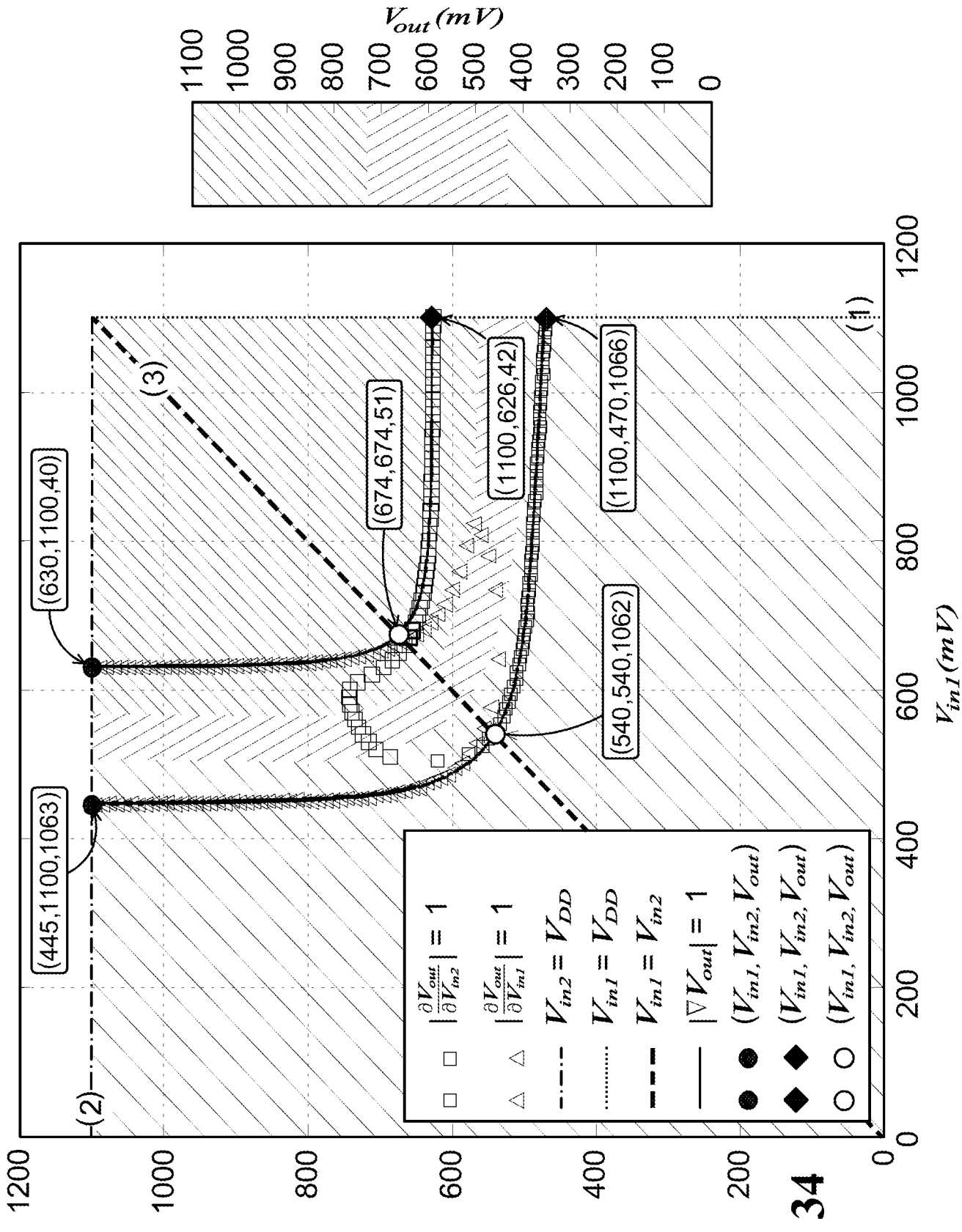
$V_{out}(mV)$
1100
1000
900
800
700
600
500
400
300
200
100
0
(1)
(2)
(3)
(445,1100,1063)
(630,1100,40)
(674,674,51)
(1100,626,42)
(1100,470,1066)
(540,540,1062)
$\left|\frac{\partial V_{out}}{\partial V_{in2}}\right| = 1$
$\left|\frac{\partial V_{out}}{\partial V_{in1}}\right| = 1$
$V_{in2} = V_{DD}$
$V_{in1} = V_{DD}$
$V_{in1} = V_{in2}$
$|\nabla V_{out}| = 1$
$(V_{in1}, V_{in2}, V_{out})$
$(V_{in1}, V_{in2}, V_{out})$
$(V_{in1}, V_{in2}, V_{out})$
0
200
400
600
800
1000
1200
$V_{in2}(mV)$
$V_{in1}(mV)$

FIG. 34

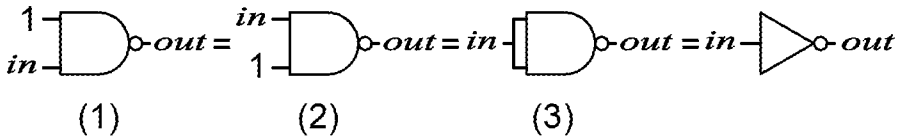

FIG. 35

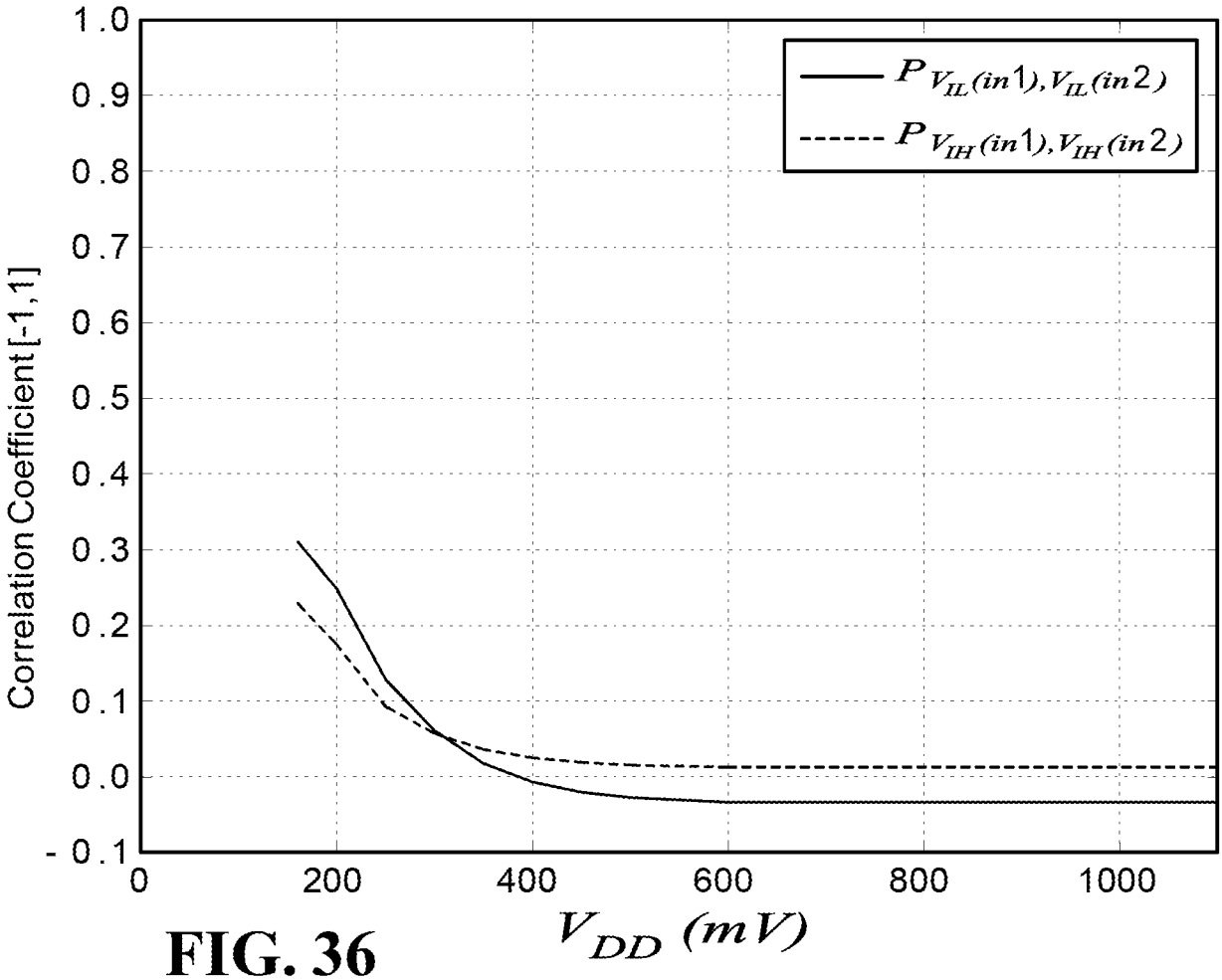

FIG. 36

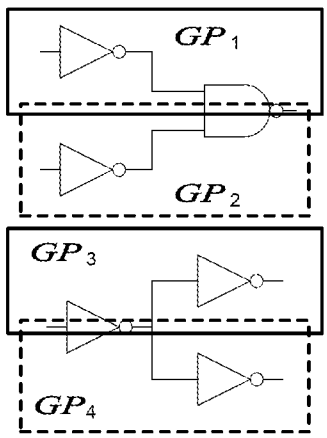

FIG. 37

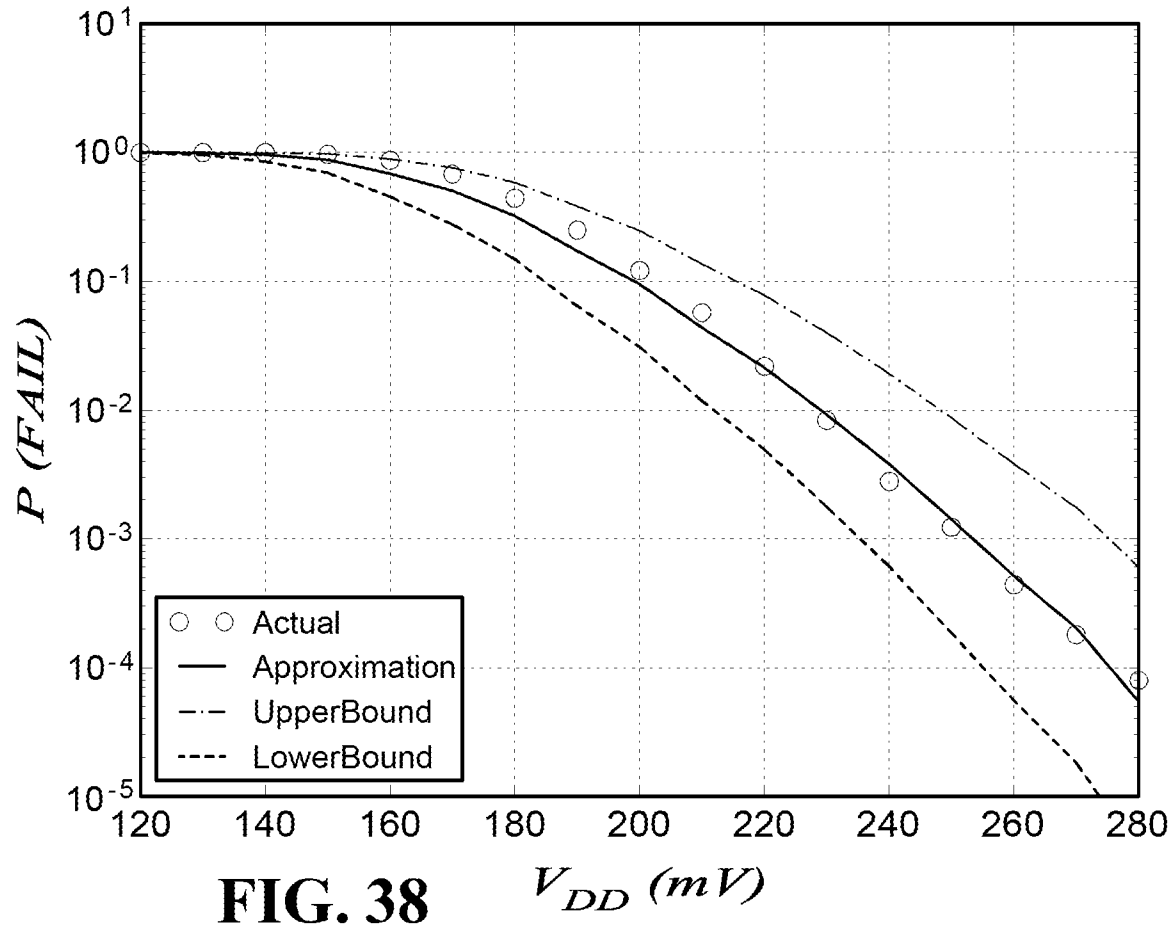
P (FAIL)
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
120
140
160
180
200
220
240
260
280
V_{DD} (mV)
Actual
Approximation
UpperBound
LowerBound

FIG. 38

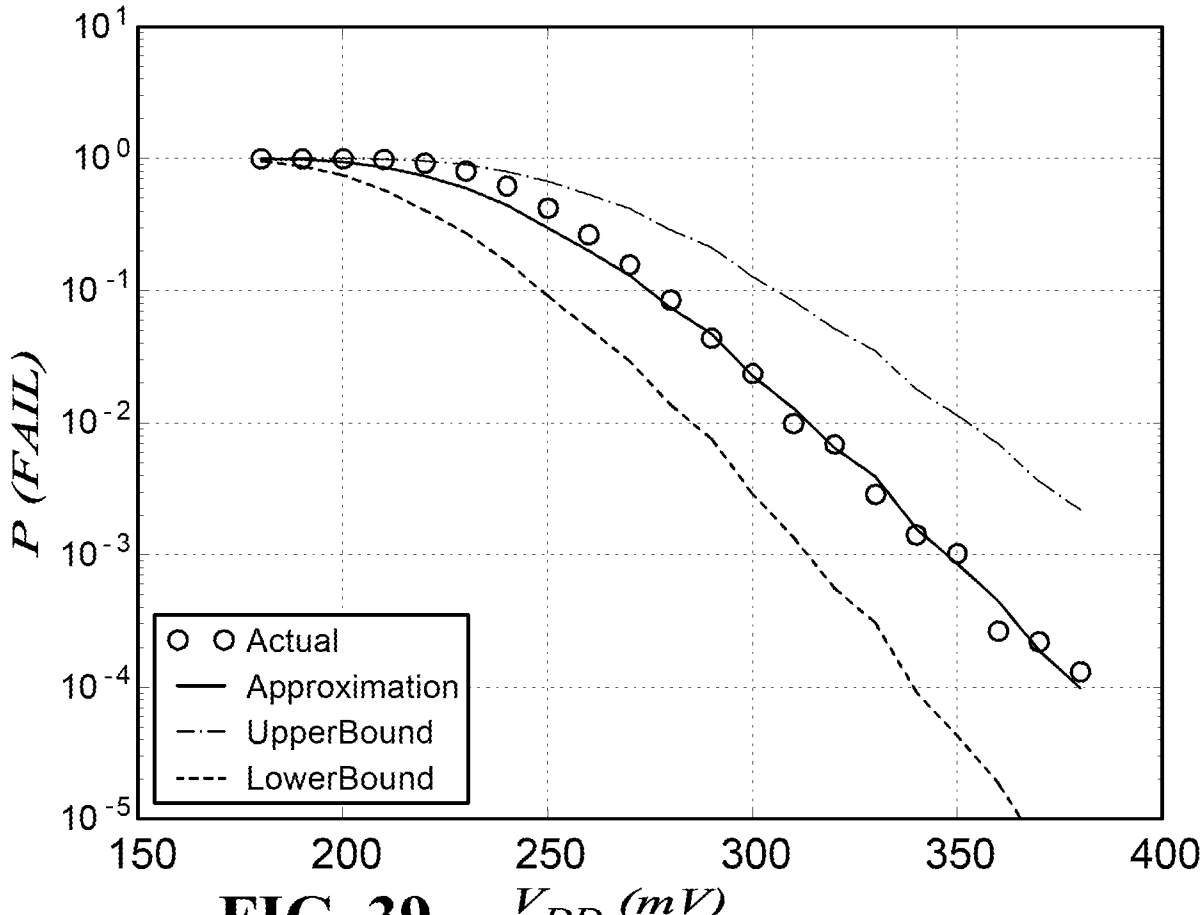
P (FAIL)
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
150
200
250
300
350
400
V_{DD} (mV)
Actual
Approximation
UpperBound
LowerBound

FIG. 39

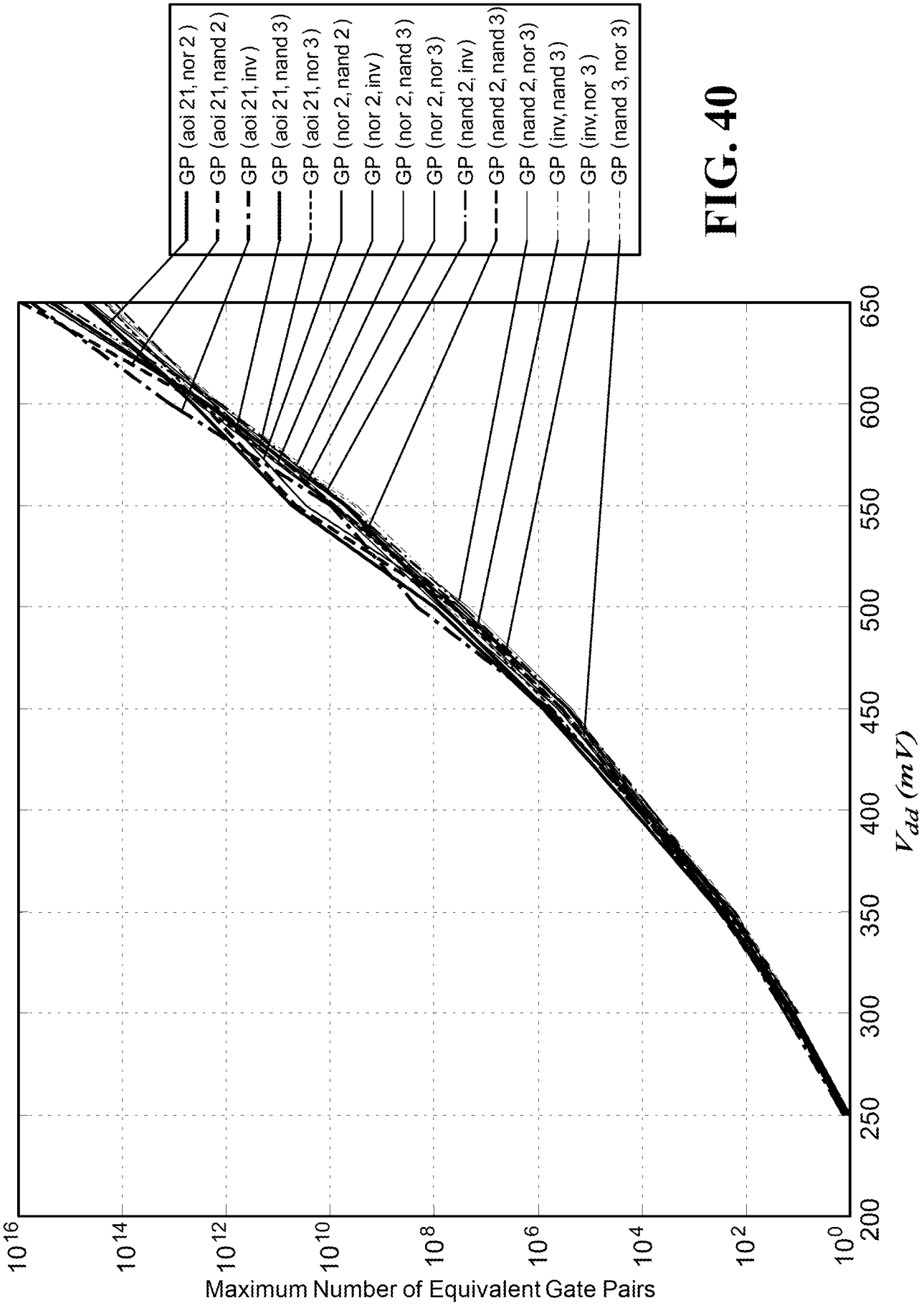
GP (aoi 21, nor 2)
GP (aoi 21, nand 2)
GP (aoi 21, inv)
GP (aoi 21, nand 3)
GP (aoi 21, nor 3)
GP (nor 2, nand 2)
GP (nor 2, inv)
GP (nor 2, nand 3)
GP (nor 2, nor 3)
GP (nand 2, inv)
GP (nand 2, nand 3)
GP (nand 2, nor 3)
GP (inv, nand 3)
GP (inv, nor 3)
GP (nand 3, nor 3)
10^{16}
10^{14}
10^{12}
10^{10}
10^{8}
10^{6}
10^{4}
10^{2}
10^{0}
Maximum Number of Equivalent Gate Pairs
200
250
300
350
400
450
500
550
600
650
V_{dd} (mV)

FIG. 40

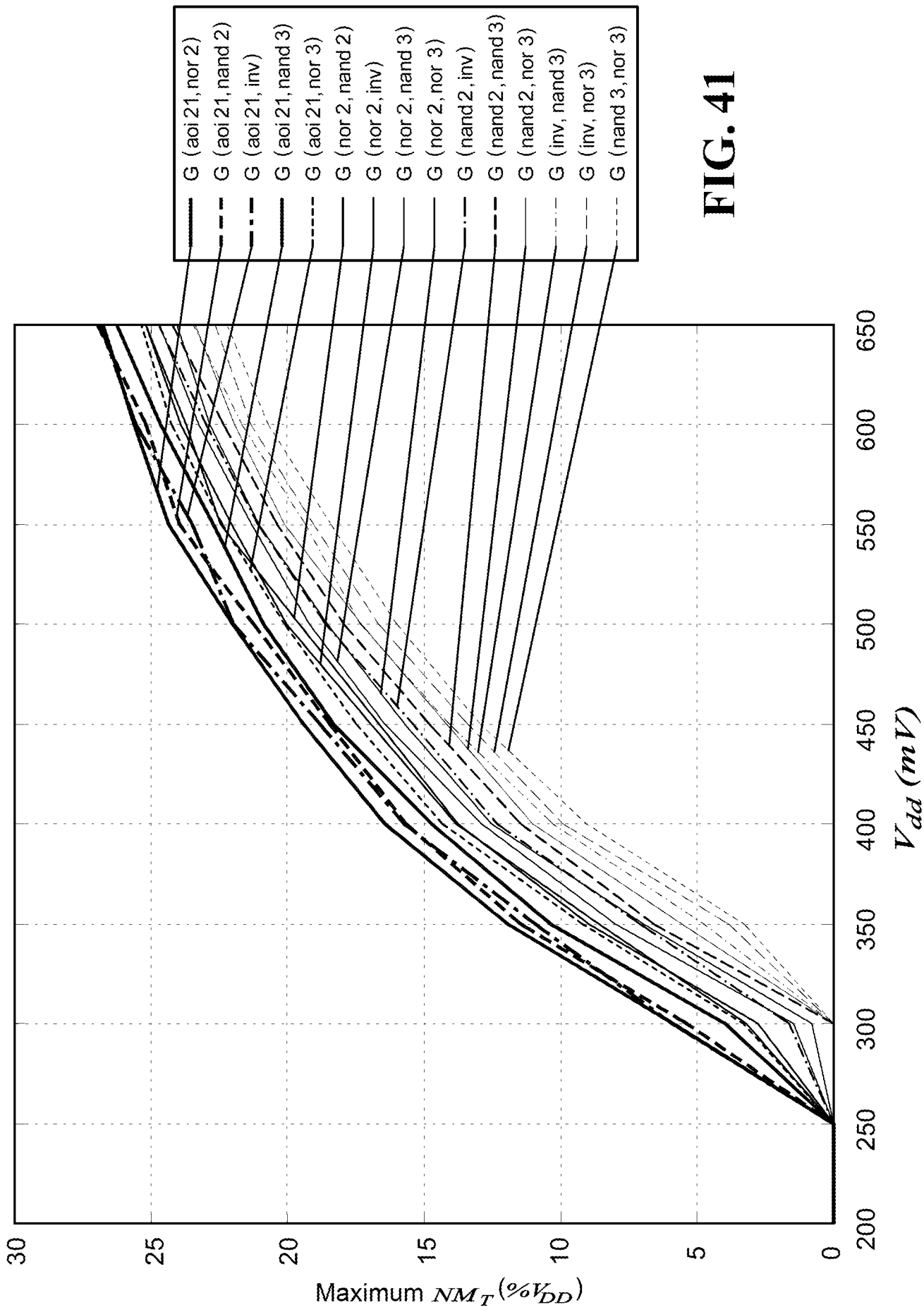
G (aoi 21, nor 2)
G (aoi 21, nand 2)
G (aoi 21, inv)
G (aoi 21, nand 3)
G (aoi 21, nor 3)
G (nor 2, nand 2)
G (nor 2, inv)
G (nor 2, nand 3)
G (nor 2, nor 3)
G (nand 2, inv)
G (nand 2, nand 3)
G (nand 2, nor 3)
G (inv, nand 3)
G (inv, nor 3)
G (nand 3, nor 3)
30
25
20
15
10
5
0
Maximum $NM_T(\%V_{DD})$
200
250
300
350
400
450
500
550
600
650
V_{dd} (mV)

FIG. 41

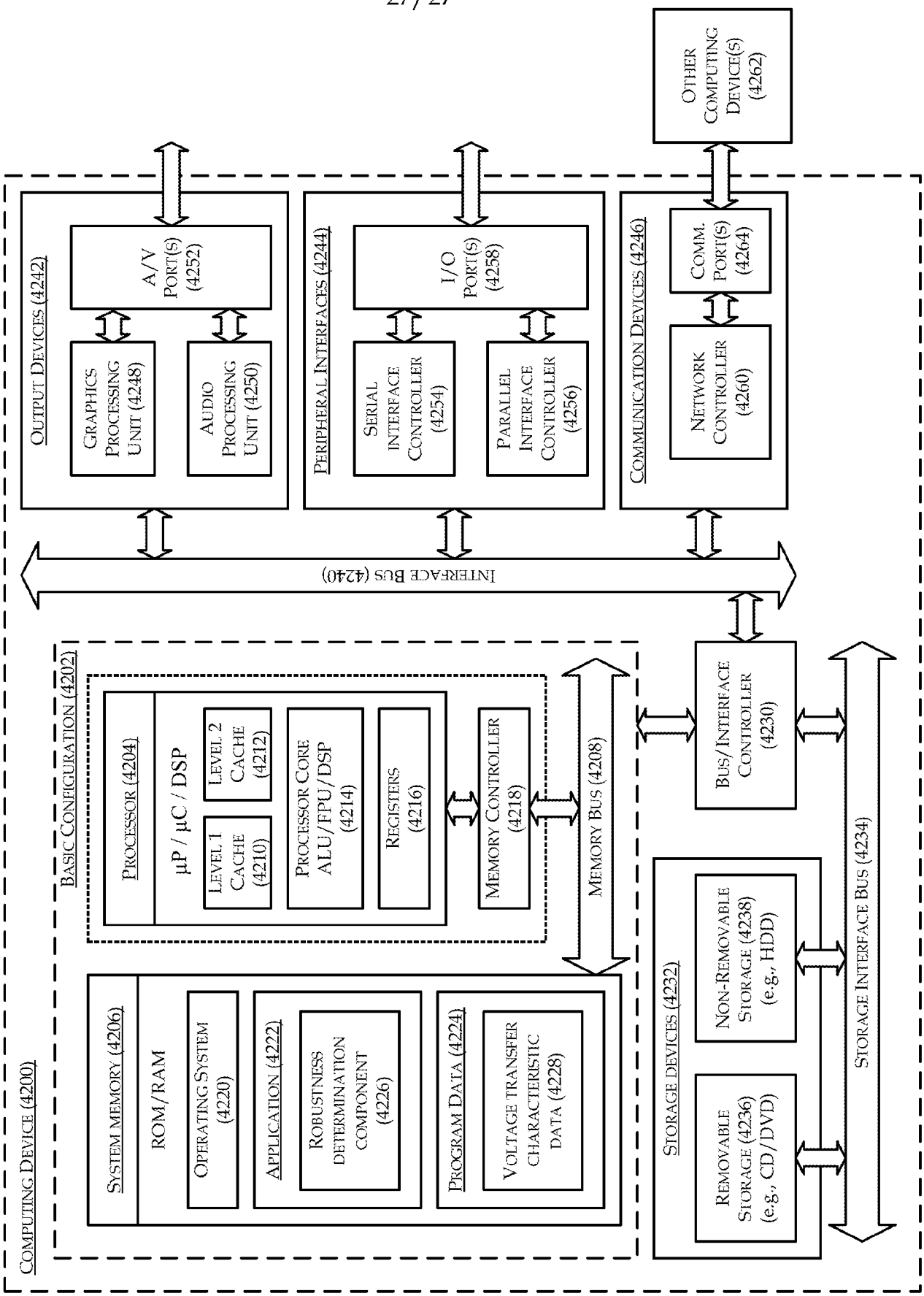
COMPUTING DEVICE (4200)
BASIC CONFIGURATION (4202)
PROCESSOR (4204)
μP / μC / DSP
LEVEL 1 CACHE (4210)
LEVEL 2 CACHE (4212)
PROCESSOR CORE ALU/FPU/DSP (4214)
REGISTERS (4216)
MEMORY CONTROLLER (4218)
SYSTEM MEMORY (4206)
ROM/RAM
OPERATING SYSTEM (4220)
APPLICATION (4222)
ROBUSTNESS DETERMINATION COMPONENT (4226)
PROGRAM DATA (4224)
VOLTAGE TRANSFER CHARACTERISTIC DATA (4228)
MEMORY BUS (4208)
BUS/INTERFACE CONTROLLER (4230)
STORAGE DEVICES (4232)
REMOVABLE STORAGE (4236) (e.g., CD/DVD)
NON-REMOVABLE STORAGE (4238) (e.g., HDD)
STORAGE INTERFACE BUS (4234)
INTERFACE BUS (4240)
OUTPUT DEVICES (4242)
GRAPHICS PROCESSING UNIT (4248)
AUDIO PROCESSING UNIT (4250)
A/V PORT(S) (4252)
PERIPHERAL INTERFACES (4244)
SERIAL INTERFACE CONTROLLER (4254)
PARALLEL INTERFACE CONTROLLER (4256)
I/O PORT(S) (4258)
COMMUNICATION DEVICES (4246)
NETWORK CONTROLLER (4260)
COMM. PORT(S) (4264)
OTHER COMPUTING DEVICE(S) (4262)

FIG. 42

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US14/35020

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G06F 17/00, 17/40, 17/50 (2014.01)
USPC - 703/13; 700/51; 716/115
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8): G06F 17/00, 17/40, 17/50 (2014.01)
USPC: 703/13, 14, 15, 16, 22; 700/28, 51, 52; 716/100, 101, 104, 110, 112, 115, 116, 117

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent (US-G, US-A, EP-A, EP-B, WO, JP-bib, DE-C,B, DE-A, DE-T, DE-U, GB-A, FR-A); Google; Google Scholar; ProQuest; KEYWORDS: integrated circuit design robustness parameters vary variable variance noise margin voltage transfer characteristic statistical analysis channel gate length dopant oxide yield description

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/0273308 A1 (HOUSTON, T.) December 08, 2005; figures 1-5; paragraphs [0022-0033, 0036-0056	1-10, 14-22
X	US 6,490,708 B2 (COHN, J et al.) December 03, 2002; figure 1; column 2, lines 49-63; column 3, lines 10-63; column 6, lines 16-56	11-13
A	US 2012/0046929 A1 (JOSHI, R. et al.) February 23, 2012; entire document	1-22
A	US 2010/0131259 A1 (JOSHI, R. et al.) May 27, 2010; entire document	1-22

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 July 2014 (21.07.2014)	28 AUG 2014
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)