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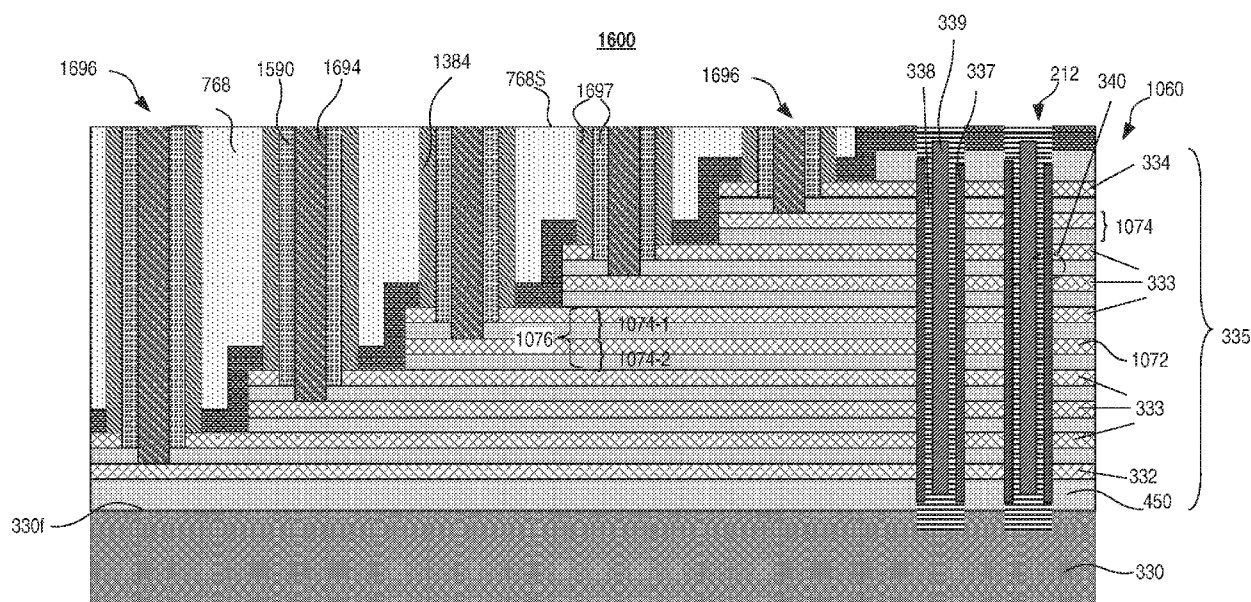


Fig. 16A

(57) Abstract: Embodiments of contact structures of a three-dimensional memory device and fabrication method thereof are disclosed. The three-dimensional memory structure includes a film stack disposed on a substrate, wherein the film stack includes a plurality of conductive and dielectric layer pairs, each conductive and dielectric layer pair having a conductive layer and a first dielectric layer. The three-dimensional memory structure also includes a staircase structure formed in the film stack, wherein the staircase structure includes a plurality of steps, each staircase step having two or more conductive and dielectric layer pairs. The three-dimensional memory structure further includes a plurality of coaxial contact structures formed in a first insulating layer over the staircase structure, wherein each coaxial contact structure includes one or more conductive and insulating ring pairs and a conductive core, each conductive and insulating ring pair having a conductive ring and an insulating ring.

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CONTACT STRUCTURES FOR THREE-DIMENSIONAL MEMORY DEVICE

TECHNICAL FIELD

[0001] The present disclosure generally relates to the field of semiconductor technology, and more particularly, to a method for forming a three-dimensional (3D) memory.

BACKGROUND

[0002] Planar memory cells are scaled to smaller sizes by improving process technology, circuit designs, programming algorithms, and the fabrication process. However, as feature sizes of the memory cells approach a lower limit, planar process and fabrication techniques become challenging and costly. As such, memory density for planar memory cells approaches an upper limit. A three-dimensional (3D) memory architecture can address the density limitation in planar memory cells.

BRIEF SUMMARY

[0003] Embodiments of contact structures for a three-dimensional memory device and methods for forming the same are described in the present disclosure.

[0004] In some embodiments, a three-dimensional memory structure includes a film stack disposed on a substrate, wherein the film stack includes a plurality of conductive and dielectric layer pairs, each conductive and dielectric layer pair having a conductive layer and a first dielectric layer. The three-dimensional memory structure also includes a staircase structure formed in the film stack, wherein the staircase structure includes a plurality of steps, each staircase step having two or more conductive and dielectric layer pairs. The three-dimensional memory structure further includes a plurality of coaxial contact structures formed in a first insulating layer over the staircase structure, wherein each coaxial contact structure includes one or more conductive and insulating ring pairs and a conductive core,

wherein each conductive and insulating ring pair includes a conductive ring and an insulating ring.

[0005] In some embodiments, each conductive ring contacts the conductive layer of a corresponding conductive and dielectric layer pair of the staircase step.

In some embodiments, each coaxial contact structure comprises at least an outer conductive ring and an inner conductive ring, and the outer conductive ring corresponds with an upper conductive and dielectric layer pair of the staircase step, wherein the outer conductive ring includes larger diameter, and the upper conductive and dielectric layer pair is farther away from the substrate.

In some embodiments, each coaxial contact structure comprises at least an outer conductive ring and an inner conductive ring, and the inner conductive ring corresponds with a lower conductive and dielectric layer pair of the staircase step, wherein the inner conductive ring includes smaller diameter, and the lower conductive and dielectric layer pair is closer to the substrate.

[0006] In some embodiments, the conductive core contacts the conductive layer closest to the substrate in the staircase step of two or more conductive and dielectric layer pairs.

[0007] In some embodiments, the insulating ring of the conductive and insulating ring pair is disposed to surround a sidewall of the conductive ring and a sidewall of the conductive layer of the staircase structure, wherein the insulating ring is configured to electrically isolate the conductive ring from another conductive ring or the conductive core.

[0008] In some embodiments, the insulating ring is disposed on a sidewall of the first dielectric layer of the staircase step of two or more conductive and dielectric layer pairs.

[0009] In some embodiments, the three-dimensional memory structure further includes a barrier layer, disposed between the first insulating layer and the staircase structure, and the plurality of coaxial contact structures extending through the barrier layer.

[0010] In some embodiments, the three-dimensional memory structure further includes a gate dielectric layer on the conductive layer, and the conductive rings extending through the gate dielectric layer to contact the conductive layers of the staircase structure.

[0011] Another aspect of the present disclosure provides a method for forming a three-dimensional (3D) memory device. A method for forming a three-dimensional (3D) memory

structure includes disposing a dielectric film stack on a substrate, wherein the dielectric film stack includes a plurality of alternating dielectric layer pairs, each alternating dielectric layer pair having a first dielectric layer and a second dielectric layer different from the first dielectric layer. The method also includes forming a dielectric staircase in the dielectric film stack, wherein the dielectric staircase includes a plurality of steps, each dielectric staircase step having two or more alternating dielectric layer pairs. The method further includes disposing a first insulating layer on the dielectric staircase, forming a plurality of memory strings in the dielectric film stack, and replacing the second dielectric layers with conductive layers to form a staircase structure with a plurality of steps, wherein each staircase step includes two or more conductive and dielectric layer pairs, each conductive and dielectric layer pair having a conductive layer and the first dielectric layer. The method also includes forming a plurality of coaxial contact structures on the staircase structure.

[0012] In some embodiments, forming the coaxial contact structure includes forming a conductive and insulating ring pair for each conductive and dielectric layer pair of the staircase step in the staircase structure.

[0013] In some embodiments, forming the conductive ring includes forming a first contact hole to expose the conductive layer in one of the two or more conductive and dielectric layer pairs of the staircase step in the staircase structure, disposing a conductive film on a sidewall of the contact hole and the exposed conductive layer, and removing the conductive film and a portion of the conductive layer from the bottom of the first contact hole to form a conductive ring, wherein a bottom of the conductive ring is formed to contact the conductive layer in one of the two or more conductive and dielectric layer pairs of the staircase step in the staircase structure.

[0014] In some embodiments, forming the conductive ring further includes etching the dielectric layer of the next conductive and dielectric layer pair.

[0015] In some embodiments, forming the insulating ring includes disposing a second insulating layer in a first contact hole, and removing the second insulating layer from the bottom of the first contact hole. Forming the insulating ring also includes forming the insulating ring surrounding a sidewall of the conductive ring and a sidewall of the conductive layer of one of the two or more conductive and dielectric layer pairs in the staircase step in

the staircase structure, and forming a second contact hole to expose the next conductive layer in the staircase step.

[0016] In some embodiments, forming the coaxial contact structure further includes forming a contact hole to expose the conductive layer closest to the substrate in the staircase step of two or more conductive and dielectric layer pairs, disposing a conductive material to fill the contact hole, and forming a conductive core to contact the conductive layer closest to the substrate in staircase step of two or more conductive and dielectric layer pairs.

[0017] In some embodiments, the method further includes performing a planarization process to remove the conductive material outside the contact hole and form a coplanar surface.

[0018] In some embodiments, the method further includes disposing a barrier layer on the dielectric staircase prior to the first insulating layer.

[0019] In some embodiments, forming the plurality of dielectric staircase steps includes disposing a patterning mask on the dielectric film stack, and etching exposed portions of the dielectric film stack in a direction perpendicular to a main surface of the substrate until portions of the two or more dielectric layer pairs are removed. Forming the plurality of dielectric staircase steps also includes trimming the patterning mask laterally, in a direction parallel to the main surface of the substrate, repeating the etching and the trimming processes until a dielectric staircase step closest to the main surface of the substrate is formed, and removing the patterning mask.

[0020] In some embodiments, replacing the second dielectric layers with the conductive layers to form the staircase structure, includes forming one or more slit structure openings, extending horizontally along the dielectric staircase, wherein the slit structure openings penetrate vertically through the dielectric film stack. Replacing the second dielectric layers also includes removing the second dielectric layers of the dielectric staircase to form a plurality of horizontal tunnels, and disposing the conductive layers inside the plurality of horizontal tunnels.

[0021] In some embodiments, the method further includes disposing a gate dielectric layer on sidewalls of the horizontal tunnels prior to disposing the conductive layer, wherein the

gate dielectric layer includes high-k dielectric material, silicon oxide, silicon nitride or silicon oxynitride.

[0022] Other aspects of the present disclosure can be understood by those skilled in the art in light of the description, the claims, and the drawings of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate embodiments of the present disclosure and, together with the description, further serve to explain the principles of the present disclosure and to enable a person skilled in the pertinent art to make and use the present disclosure.

[0024] Fig. 1 illustrates a schematic top-down view of an exemplary three-dimensional (3D) memory die, according to some embodiments of the present disclosure.

[0025] Fig. 2A-2B illustrate schematic top-down views of some regions of 3D memory die, according to some embodiments of the present disclosure.

[0026] Fig. 3 illustrates a perspective view of a portion of an exemplary 3D memory array structure, in accordance with some embodiments of the present disclosure.

[0027] Fig. 4-15 illustrate schematic cross-sectional views of an exemplary 3D memory structure at certain fabricating stages, according to some embodiments of the present disclosure.

[0028] Fig. 16A illustrates a schematic cross-sectional view of an exemplary 3D memory structure at a certain fabricating stage, according to some embodiments of the present disclosure.

[0029] Fig. 16B illustrates a perspective view of a portion of an exemplary 3D memory structure at a certain fabricating stage, according to some embodiments of the present disclosure.

[0030] Fig. 17A-17D illustrate schematic cross-sectional views of an exemplary 3D memory structure at certain fabricating stages, according to some embodiments of the present disclosure.

[0031] Fig. 18 illustrates a flow diagram of an exemplary method for forming a 3D memory structure, according to some embodiments of the present disclosure.

[0032] The features and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings, in which like reference characters identify corresponding elements throughout. In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally similar elements. The drawing in which an element first appears is indicated by the leftmost digit(s) in the corresponding reference number.

[0033] Embodiments of the present disclosure will be described with reference to the accompanying drawings.

DETAILED DESCRIPTION

[0034] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the pertinent art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the pertinent art that the present disclosure can also be employed in a variety of other applications.

[0035] It is noted that references in the specification to “one embodiment,” “an embodiment,” “an example embodiment,” “some embodiments,” etc., indicate that the embodiment described can include a particular feature, structure, or characteristic, but every embodiment can not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the pertinent art to affect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.

[0036] In general, terminology can be understood at least in part from usage in context. For example, the term “one or more” as used herein, depending at least in part upon context, can be used to describe any feature, structure, or characteristic in a singular sense or can be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as “a,” “an,” or “the,” again, can be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context. In addition, the term “based

on” can be understood as not necessarily intended to convey an exclusive set of factors and may, instead, allow for existence of additional factors not necessarily expressly described, again, depending at least in part on context.

[0037] It should be readily understood that the meaning of “on,” “above,” and “over” in the present disclosure should be interpreted in the broadest manner such that “on” not only means “directly on” something, but also includes the meaning of “on” something with an intermediate feature or a layer therebetween. Moreover, “above” or “over” not only means “above” or “over” something, but can also include the meaning it is “above” or “over” something with no intermediate feature or layer therebetween (i.e., directly on something).

[0038] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper,” and the like, can be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or process step in addition to the orientation depicted in the figures. The apparatus can be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein can likewise be interpreted accordingly.

[0039] As used herein, the term “substrate” refers to a material onto which subsequent material layers are added. The substrate includes a top surface and a bottom surface. The top surface of the substrate is typically where a semiconductor device is formed, and therefore the semiconductor device is formed at a top side of the substrate unless stated otherwise. The bottom surface is opposite to the top surface and therefore a bottom side of the substrate is opposite to the top side of the substrate. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0040] As used herein, the term “layer” refers to a material portion including a region with a thickness. A layer has a top side and a bottom side where the bottom side of the layer is relatively close to the substrate and the top side is relatively away from the substrate. A layer can extend over the entirety of an underlying or overlying structure, or can have an extent

less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any set of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an interconnect layer can include one or more conductive and contact layers (in which contacts, interconnect lines, and/or vertical interconnect accesses (VIAs) are formed) and one or more dielectric layers.

[0041] As used herein, the term “nominal/nominally” refers to a desired, or target, value of a characteristic or parameter for a component or a process step, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term “about” indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term “about” can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., $\pm 10\%$, $\pm 20\%$, or $\pm 30\%$ of the value).

[0042] In the present disclosure, the term “horizontal/horizontally/lateral/laterally” means nominally parallel to a lateral surface of a substrate. In the present disclosure, the term “each” may not only necessarily mean “each of all,” but can also mean “each of a subset.”

[0043] As used herein, the term “3D memory” refers to a three-dimensional (3D) semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as “memory strings,” such as NAND strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term “vertical/vertically” means nominally perpendicular to the lateral surface of a substrate.

[0044] In the present disclosure, for ease of description, “tier” is used to refer to elements of substantially the same height along the vertical direction. For example, a word line and the underlying gate dielectric layer can be referred to as “a tier,” a word line and the underlying

insulating layer can together be referred to as “a tier,” word lines of substantially the same height can be referred to as “a tier of word lines” or similar, and so on.

[0045] In some embodiments, a memory string of a 3D memory device includes a semiconductor pillar (e.g., silicon channel) that extends vertically through a plurality of conductive and dielectric layer pairs. The plurality of conductive and dielectric layer pairs are also referred to herein as an “alternating conductive and dielectric stack.” An intersection of the conductive layer and the semiconductor pillar can form a memory cell. The conductive layer of the alternating conductive and dielectric stack can be connected to a word line at the back-end-of-line, wherein the word line can electrically connect to one or more control gates. For illustrative purposes, word lines and control gates are used interchangeably to describe the present disclosure. The top of the semiconductor pillar (e.g., transistor drain region) can be connected to a bit line (electrically connecting one or more semiconductor pillars). Word lines and bit lines are typically laid perpendicular to each other (e.g., in rows and columns, respectively), forming an “array” of the memory, also called a memory “block” or an “array block”.

[0046] A memory “die” may have one or more memory “planes”, and each memory plane may have a plurality of memory blocks. An array block can also be divided into a plurality of memory “pages”, wherein each memory page may have a plurality of memory strings. In a flash NAND memory device, erase operation can be performed for every memory block and read/write operation can be performed for every memory page. The array blocks are the core area in a memory device, performing storage functions. To achieve higher storage density, the number of vertical 3D memory stacks is increased greatly, adding complexity and cost in manufacturing.

[0047] A memory die has another region, called the periphery, which provides supporting functions to the core. The periphery region includes many digital, analog, and/or mixed-signal circuits, for example, row and column decoders, drivers, page buffers, sense amplifiers, timing and controls, and the like circuitry. Peripheral circuits use active and/or passive semiconductor devices, such as transistors, diodes, capacitors, resistors, etc., as would be apparent to a person of ordinary skill in the art.

[0048] Other parts of the memory devices are not discussed for ease of description. In the present disclosure, a “memory device” is a general term and can be a memory chip (package), a memory die or any portion of a memory die.

[0049] Although using three-dimensional NAND devices as examples, in various applications and designs, the disclosed structures can also be applied in similar or different semiconductor devices to, e.g., to improve metal connections or wiring. The specific application of the disclosed structures should not be limited by the embodiments of the present disclosure.

[0050] Fig. 1 illustrates a top-down view of an exemplary three-dimensional (3D) memory device 100, according to some embodiments of the present disclosure. The 3D memory device 100 can be a memory die and can include one or more memory planes 101, each of which can include a plurality of memory blocks 103. Identical and concurrent operations can take place at each memory plane 101. The memory block 103, which can be megabytes (MB) in size, is the smallest size to carry out erase operations. Shown in Fig. 1, the exemplary 3D memory device 100 includes four memory planes 101 and each memory plane 101 includes six memory blocks 103. Each memory block 103 can include a plurality of memory cells, wherein each memory cell can be addressed through interconnections such as bit lines and word lines. The bit lines and word lines can be laid out perpendicularly, forming an array of metal lines. The direction of bit lines and word lines are labeled as “BL” and “WL” in Fig. 1. In this disclosure, memory blocks 103 is also referred to as “memory arrays”.

[0051] The 3D memory device 100 also includes a periphery regions 105, an area surrounding memory planes 101. The periphery region 105 contains peripheral circuits to support functions of the memory array, for example, page buffers, row and column decoders and sense amplifiers.

[0052] It is noted that, the arrangement of the memory planes 101 in the 3D memory device 100 and the arrangement of the memory blocks 103 in each memory plane 101 illustrated in Fig. 1 are only used as an example, which does not limit the scope of the present disclosure.

[0053] In some embodiments, the memory arrays and the peripheral circuits of the 3D memory device 100 can be formed on different substrates and can be joined together to form the 3D memory device 100 through wafer bonding. In this example, through array contact

structures can provide vertical interconnects between the memory arrays and peripheral circuits, thereby reducing metal levels and shrinking die size. Detailed structure and method of 3D memory with hybrid bonding is described in co-pending U.S. patent application, titled “Hybrid Bonding Contact Structure of Three-Dimensional Memory Device,” (Application No. 16/046,852 and filed on July 26, 2018), which is incorporated herein by reference in its entirety.

[0054] Referring to Fig. 2A, an enlarged top-down view of a region 108 in Fig. 1 is illustrated, according to some embodiments of the present disclosure. The region 108 of the 3D memory device 100 can include a staircase region 210 and a channel structure region 211. The channel structure region 211 can include an array of memory strings 212, each including a plurality of stacked memory cells. The staircase region 210 can include a staircase structure and an array of contact structures 214 formed on the staircase structure. In some embodiments, a plurality of slit structures 216, extending in WL direction across the channel structure region 211 and the staircase region 210, can divide a memory block into multiple memory fingers 218. At least some slit structures 216 can function as the common source contact for an array of memory strings 212 in channel structure regions 211. A top select gate cut 220 can be disposed in the middle of each memory finger 218 to divide a top select gate (TSG) of the memory finger 218 into two portions, and thereby can divide a memory finger into two programmable (read/write) pages. While erase operation of a 3D NAND memory can be carried out at memory block level, read and write operations can be carried out at memory page level. A page can be kilobytes (KB) in size. In some embodiments, region 108 also includes dummy memory strings 222 for process variation control during fabrication and/or for additional mechanical support.

[0055] Referring to Fig. 2B, an enlarged top-down view of a region 109 in Fig. 1 is illustrated, according to some embodiments of the present disclosure. The region 109 of the 3D memory device 100 can include the channel structure region 211, a through array contact region 107, and a top select gate (TSG) staircase region 224.

[0056] The channel structure region 211 in the region 109 can be similar to the channel structure region 211 in region 108. The TSG staircase region 224 can include an array of TSG contacts 226 formed on the staircase structure. The TSG staircase region 224 can be

disposed on the sides of the channel structure region 211 and adjacent to through array contact region 107 in the top-down view. Multiple through array contacts 228 can be formed in the through array contact region 107.

[0057] Fig. 3 illustrates a perspective view of a portion of an exemplary three-dimensional (3D) memory array structure 300, according to some embodiments of the present disclosure. The memory array structure 300 includes a substrate 330, an insulating film 331 over the substrate 330, a tier of lower select gates (LSGs) 332 over the insulating film 331, and a plurality of tiers of control gates 333, also referred to as “word lines (WLs)”, stacking on top of the LSGs 332 to form a film stack 335 of alternating conductive and dielectric layers. The dielectric layers adjacent to the tiers of control gates are not shown in Fig. 3 for clarity.

[0058] The control gates of each tier are separated by slit structures 216-1 and 216-2 through the film stack 335. The memory array structure 300 also includes a tier of top select gates (TSGs) 334 over the stack of control gates 333. The stack of TSG 334, control gates 333 and LSG 332 is also referred to as “gate electrodes.” The memory array structure 300 further includes memory strings 212 and doped source line regions 344 in portions of substrate 330 between adjacent LSGs 332. Each memory strings 212 includes a channel hole 336 extending through the insulating film 331 and the film stack 335 of alternating conductive and dielectric layers. Memory strings 212 also includes a memory film 337 on a sidewall of the channel hole 336, a channel layer 338 over the memory film 337, and a core filling film 339 surrounded by the channel layer 338. A memory cell 340 can be formed at the intersection of the control gate 333 and the memory string 212. The memory array structure 300 further includes a plurality of bit lines (BLs) 341 connected to the memory strings 212 over the TSGs 334. The memory array structure 300 also includes a plurality of metal interconnect lines 343 connected to the gate electrodes through a plurality of contact structures 214. The edge of the film stack 335 is configured in a shape of staircase to allow an electrical connection to each tier of the gate electrodes. The channel structure region 211 and the staircase region 210 correspond to the channel structure region 211 and the staircase region 210 in the top-down view of Fig. 2A, wherein one of the staircase region 210 in Fig. 3 can be used as TSG staircase region 230 for TSG connection.

[0059] In Fig. 3, for illustrative purposes, three tiers of control gates 333-1, 333-2, and 333-3 are shown together with one tier of TSG 334 and one tier of LSG 332. In this example, each memory string 212 can include three memory cells 340-1, 340-2 and 340-3, corresponding to the control gates 333-1, 333-2 and 333-3, respectively. In some embodiments, the number of control gates and the number of memory cells can be more than three to increase storage capacity. The memory array structure 300 can also include other structures, for example, through array contact, TSG cut, common source contact and dummy channel structure. These structures are not shown in Fig. 3 for simplicity.

[0060] With the demand for higher storage capacity in a NAND flash memory, the number of vertical tiers of 3D memory cells 340 or word lines 333 increases accordingly, leading to more process complexity and higher manufacturing cost. When increasing the tiers of memory cells 340 or word lines 333 of the memory array structure 300, it becomes more challenging to etch deeper channel holes 336 for the memory strings 212 and also more challenging to form contact structures 214 on the staircase structures. For example, to form the contact structures 214 on a large number of vertically stacked word lines (gate electrodes), a high aspect ratio etching is needed to form contact holes, followed by a high aspect ratio deposition of conductive materials inside the contact holes. To reduce cost per bit for a 3D memory, dimensions of the memory structures are reduced to allow fabrication of more memory blocks on a wafer. However the increased word line stack also leads to wider staircase structures in a horizontal direction parallel to the substrate surface, resulting in a wider staircase region 210 and less storage density.

[0061] To alleviate etching and deposition difficulties with more and more vertically stacked word lines, portions of a 3D memory device can be formed on two or more wafers and then joined together through wafer bonding or flip-chip bonding. Alternatively, a 3D memory device can be formed by sequentially stacking multi-sessions, wherein each session contains a stack of word lines with less number of tiers. However larger lateral dimensions of staircase structures due to vertically stacked word lines still limits the storage density.

[0062] Various embodiments in the present disclosure describe a structure and method of a 3D memory with coaxial contact structures, each providing electrical contacts to two or more conductive layers of the staircase structure. By sharing contact structures between multiple

conductive layers, the dimension of the staircase region 210 (in Fig. 2) can be reduced. Memory density and cost per bit of the 3D NAND memory can be improved accordingly.

[0063] Fig. 4 illustrates a cross-sectional view of an exemplary structure 400 of a three-dimensional memory device, according to some embodiments, wherein the structure 400 includes a substrate 330 and a dielectric film stack 445. The cross-sectional views of Fig. 4-17D are along WL direction in Fig. 2A.

[0064] Substrate 330 can provide a platform for forming subsequent structures. In some embodiments, the substrate 330 includes any suitable material for forming the three-dimensional memory device. For example, the substrate 330 can include any other suitable material, for example, silicon, silicon germanium, silicon carbide, silicon on insulator (SOI), germanium on insulator (GOI), glass, gallium nitride, gallium arsenide, III-V compound, and/or any combinations thereof.

[0065] A front surface 330f of the substrate 330 is also referred to as a “main surface” of the substrate herein. Layers of materials can be disposed on the front surface 330f of the substrate. A “topmost” or “upper” layer is a layer farthest or farther away from the front surface 330f of the substrate. A “bottommost” or “lower” layer is a layer closest or closer to the front surface 330f of the substrate.

[0066] In some embodiments, peripheral devices can be formed in the periphery region 105 on the front surface 330f of the substrate 330. In some embodiments, active device areas can be formed in the memory blocks 103 on the front surface 330f of the substrate 330. In some embodiments, the substrate 330 can further include an insulating film 331 on the front surface 330f. The insulating film 331 can be made of the same or different material from the dielectric film stack.

[0067] The peripheral devices can include any suitable semiconductor devices, for example, metal oxide semiconductor field effect transistors (MOSFETs), diodes, resistors, capacitor, etc. The peripheral devices can be used in the design of digital, analog and/or mixed signal circuits supporting the storage function of the memory core, for example, row and column decoders, drivers, page buffers, sense amplifiers, timing and controls.

[0068] The active device areas in the memory blocks are surrounded by isolation structures, such as shallow trench isolation. Doped regions, such as p-type doped and/or n-type doped

wells, can be formed in the active device area according to the functionality of the array devices in the memory blocks.

[0069] The dielectric film stack 445 extends in a lateral direction that is parallel to the front surface 330f of the substrate 330. The dielectric film stack 445 includes a dielectric layer 450 (also referred to as “first dielectric layer”) and a sacrificial layer 452 (also referred to as “second dielectric layer”) alternately stacked on each other, wherein the dielectric layer 450 is configured to be the bottommost and the topmost layers of the dielectric film stack 445. In this configuration, each sacrificial layer 452 is sandwiched between two dielectric layers 450, and each dielectric layer 450 is sandwiched between two sacrificial layers 452 (except the bottommost and the topmost layer).

The dielectric layer 450 and the underlying sacrificial layer 452 are also referred to as an alternating dielectric layer pair 454. The formation of the dielectric film stack 445 can include disposing the dielectric layers 450 to each have the same thickness or to have different thicknesses. Example thicknesses of the dielectric layers 450 can range from 10 nm to 500 nm. Similarly, the sacrificial layer 452 can each have the same thickness or have different thicknesses. Example thicknesses of the sacrificial layer 452 can range from 10 nm to 500 nm.

[0070] Although only 21 total layers are illustrated in the dielectric film stack 445 in Fig. 4, it should be understood that this is for illustrative purposes only and that any number of layers may be included in the dielectric film stack 445.

[0071] In some embodiments, the dielectric film stack 445 can include layers in addition to the dielectric layer 450 and the sacrificial layer 452, and can be made of different materials and with different thicknesses.

[0072] In some embodiments, the dielectric layer 450 includes any suitable insulating materials, for example, silicon oxide, silicon oxynitride, silicon nitride, TEOS or silicon oxide with F-, C-, N-, and/or H- incorporation. The dielectric layer 450 can also include high-k dielectric materials, for example, hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, or lanthanum oxide films.

[0073] The formation of the dielectric layer 450 on the substrate 330 can include any suitable deposition methods such as, chemical vapor deposition (CVD), physical vapor deposition

(PVD), plasma-enhanced CVD (PECVD), rapid thermal chemical vapor deposition (RTCVD), low pressure chemical vapor deposition (LPCVD), sputtering, metal-organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), high-density-plasma CVD (HDP-CVD), thermal oxidation, nitridation, any other suitable deposition method, and/or combinations thereof.

[0074] In some embodiments, the sacrificial layer 452 includes any suitable material that is different from the dielectric layer 450 and can be removed selectively. For example, the sacrificial layer 452 can include silicon oxide, silicon oxynitride, silicon nitride, TEOS, poly-crystalline silicon, poly-crystalline germanium, poly-crystalline germanium-silicon, and any combinations thereof. In some embodiments, the sacrificial layer 452 also includes amorphous semiconductor materials, such as amorphous silicon or amorphous germanium. The sacrificial layer 452 can be disposed using a similar technique as the dielectric layer 450, such as CVD, PVD, ALD, thermal oxidation or nitridation, or any combination thereof.

[0075] In some embodiments, the dielectric layer 450 can be silicon oxide and the sacrificial layer 452 can be silicon nitride.

[0076] Fig. 5 illustrates a cross-sectional view of an exemplary structure 500 of a three dimensional memory device, according to some embodiments, wherein the structure 500 includes a dielectric staircase 560 formed in the dielectric film stack 445. In the dielectric staircase 560, a dielectric staircase step 562, or a “staircase layer”, refers to a layer stack with the same lateral dimension in a surface parallel to the substrate surface 330f. Each dielectric staircase step 562 terminates at a shorter length than the staircase step underneath, with a lateral dimension “a” shown in Fig. 5.

[0077] In some embodiments, each dielectric staircase step 562 includes two or more alternating dielectric layer pairs 454. Each dielectric staircase step 562 can have a same number of alternating dielectric layer pairs or a different number of alternating dielectric layer pairs. As an example, Fig. 5 depicts the dielectric staircase 560 with two alternating dielectric layer pairs 454.

[0078] The plural steps of the dielectric staircase 560 can be formed by applying a repetitive etch-trim process on the dielectric film stack 445 using a patterning mask (not shown). In

some embodiments, the patterning mask can include a photoresist or carbon-based polymer material. The patterning mask can be removed after forming the dielectric staircase 560.

[0079] The etch-trim process includes an etching process and a trimming process. During the etching process, a portion of each dielectric staircase step 562 with exposed surface can be removed. The remaining portion of each dielectric staircase step 562, either covered by upper levels of staircase steps or covered by the patterning mask, is not etched. The etch depth is a thickness of the dielectric staircase step 562. In some embodiments, the thickness of the dielectric staircase step 562 is the total thickness of two or more alternating dielectric layer pairs 454. In the example shown in Fig. 5, the thickness of a dielectric staircase step 562 is the thickness of two alternating dielectric layer pairs 454. The etching process for the dielectric layer 450 can have a high selectivity over the sacrificial layer 452, and/or vice versa. Accordingly, an underlying alternating dielectric layer pair 454 can function as an etch-stop layer. By switching etching process for each layer, the dielectric staircase step 562 with multiple alternating dielectric layer pairs 454 can be etched during one etching cycle. And as a result, one staircase step is formed during each etch-trim cycle.

[0080] In some embodiments, the dielectric staircase step 562 can be etched using an anisotropic etching such as a reactive ion etch (RIE) or other dry etch processes. In some embodiments, the dielectric layer 450 is silicon oxide. In this example, the etching of silicon oxide can include RIE using fluorine based gases, for example, carbon-fluorine (CF_4), hexafluoroethane (C_2F_6), CHF_3 , or C_3F_8 and/or any other suitable gases. In some embodiments, the silicon oxide layer can be removed by wet chemistry, such as hydrofluoric acid or a mixture of hydrofluoric acid and ethylene glycol. In some embodiments, a timed etching approach can be used. In some embodiments, the sacrificial layer 452 is silicon nitride. In this example, the etching of silicon nitride can include RIE using O_2 , N_2 , CF_4 , NF_3 , Cl_2 , HBr , BCl_3 , and/or combinations thereof. The methods and etchants to remove a single layer stack should not be limited by the embodiments of the present disclosure.

[0081] The trimming process includes applying a suitable etching process (e.g., an isotropic dry etch or a wet etch) on the patterning mask such that the patterning mask can be pulled back laterally. The lateral pull-back dimension determines the lateral dimension “a” of each step of the dielectric staircase 560. After patterning mask trimming, one portion of the

topmost dielectric staircase step 562 is exposed and the other portion of the topmost dielectric staircase step 562 remains covered by the patterning mask. The next cycle of etch-trim process resumes with the etching process.

[0082] In some embodiments, the patterning mask trimming process can include dry etching, such as RIE using O₂, Ar, N₂, etc.

[0083] In some embodiments, the topmost dielectric staircase step 562 can be covered by the dielectric layer 450. In some embodiments, the topmost dielectric staircase step 562 can further be covered by other dielectric materials. A process step of removing the dielectric layer 450 and/or the other dielectric materials can be added to the etching process of each etch-trim cycle to form the dielectric staircase 560.

[0084] Fig. 6 illustrates a cross-sectional view of an exemplary structure 600 of a three dimensional memory device, according to some embodiments, wherein the structure 600 includes a barrier layer 664 disposed over the structure 500.

[0085] The barrier layer 664 covers the dielectric staircase 560 on both the top surfaces and sidewalls. In some embodiments, the barrier layer 664 can be an optional etch-stop layer. For example, the barrier layer 664 can be used as an etch-stop layer for protecting the underlying structure during contact hole etching processes. In some embodiments, a thickness of the barrier layer 664 on sidewalls can be the same as a thickness of the barrier layer 664 on the top surfaces. In some embodiments, the thickness of the barrier layer 664 on sidewalls can be different from the thickness of the barrier layer 664 on the top surfaces. In some embodiments, the barrier layer 664 can be made of similar material as the dielectric layer 450 using a similar technique.

[0086] Fig. 7 illustrates a cross-sectional view of an exemplary structure 700 of a three dimensional memory device, according to some embodiments, wherein the structure 700 includes a first insulating layer 768 disposed over the structure 600.

[0087] The first insulating layer 768 can be disposed on dielectric staircase 560 after forming the barrier layer 664. The first insulating layer 768 can be made of any a suitable insulator and can be made of a similar material as the dielectric layer 450 using a similar technique. In some embodiments, the first insulating layer 768 can also include spin-on-glass, a mixture of silicon oxide and dopants (either boron or phosphorous) that is suspended in a solvent

solution, and can be disposed using processes, for example, spin-coating. In some embodiments, the first insulating layer 768 can include a low-k dielectric material, such as carbon-doped oxide (CDO or SiOC or SiOC:H), or fluorine doped oxide (SiOF), etc. The low-k dielectric material can be disposed by CVD, PVD, sputtering, etc.

[0088] In some embodiments, a planarization process, for example RIE etch-back or chemical mechanical polishing (CMP), can be performed to form a coplanar surface, parallel to the surface 330f of the substrate 330. In some embodiments, the top surface 768S of the first insulating layer 768 can be coplanar with the top surface 664S of the uppermost portion of the barrier layer 664. In this example, the barrier layer 664 can be used as a polish-stop.

[0089] Fig. 8 illustrates a cross-sectional view of an exemplary structure 800 of a three dimensional memory device, according to some embodiments, wherein the structure 800 includes a plurality of memory strings 212 through the dielectric film stack 445. The memory strings 212 correspond to the memory strings 212 in Fig. 2A-2B and Fig. 3. For illustrative purpose, two memory strings are shown in Fig. 8. Each memory string 212 extends through the dielectric film stack 445 of alternating dielectric layer pairs, and includes a memory film 337 over the inner surface of memory strings 212, a channel layer 338 over the memory film 337, and a core filling film 339 surrounded by the channel layer 338. Detailed structure and method of the NAND memory string is described in the co-pending U.S. patent application, titled "Method for Forming Gate Structure of Three-Dimensional Memory Device," (Application No. 16/047,158 and filed on July 27, 2018), which is incorporated herein by reference in its entirety.

[0090] Fig. 9 illustrates a cross-sectional view of an exemplary structure 900 of a three dimensional memory device (along WL direction), according to some embodiments, wherein the sacrificial layers 452 are removed and a plurality of horizontal tunnels 970 are formed.

[0091] After forming the memory strings 212, a plurality of slit structure openings can be formed along WL directions (see Fig. 2A-2B and Fig. 3). These slit structure openings extend through the dielectric film stack 445. The sacrificial layers 452 can then be removed from the openings of the slit structures 216 along BL direction (perpendicular to WL direction, e.g., perpendicular to the cross-section shown in Fig. 9).

- [0092] The sacrificial layers 452 can be removed by any suitable etching process, e.g., an isotropic dry etch or wet etch, that is selective over the dielectric layers 450, such that the etching process can have minimal impact on the dielectric layer 450. In some embodiments, the sacrificial layer 452 can be silicon nitride. In this example, the sacrificial layer 452 can be removed by RIE using one or more etchants of CF₄, CHF₃, C₄F₈, C₄F₆, and CH₂F₂. In some embodiments, the sacrificial layer 452 can be removed using wet etch, such as phosphoric acid.
- [0093] After removing the sacrificial layers 452, sidewalls of the memory film 337 are exposed in the horizontal tunnels 970.
- [0094] Fig. 10 illustrates a cross-sectional view of an exemplary structure 1000 of a three dimensional memory device, according to some embodiments, wherein the structure 1000 includes the film stack 335 of alternating conductive and dielectric layers (e.g., corresponding to the film stack 335 in Fig. 3). The film stack 335 of alternating conductive and dielectric layers includes conductive layers 1072 sandwiched between the dielectric layers 450. In structure 1000, each staircase step 1076 includes two or more conductive and dielectric layer pairs 1074, each conductive and dielectric layer pair 1074 having one conductive layer 1072 and one dielectric layer 450. In Fig. 10, as an example, each staircase step 1076 includes two conductive and dielectric layer pairs 1074-1 and 1074-2, referred to as an “upper layer pair” and a “lower layer pair”, respectively. After disposing the conductive layers 1072 inside the plurality of horizontal tunnels, the dielectric staircase 560 with alternating dielectric and sacrificial layers is now changed into a staircase structure 1060 with alternating conductive and dielectric layers.
- [0095] The conductive layer 1072 can include any suitable conductive material that is suitable for a gate electrode, e.g., tungsten (W), aluminum (Al), copper (Cu), cobalt (Co), titanium (Ti), tantalum (Ta), titanium nitride (TiN), tantalum nitride (TaN), and/or any combination thereof. The conductive material can fill the horizontal tunnel 970 using a suitable deposition method such as CVD, physical vapor deposition (PVD), plasma-enhanced CVD (PECVD), sputtering, thermal evaporation, e-beam evaporation, metal-organic chemical vapor deposition (MOCVD), and/or ALD. In some embodiments, the conductive layers 1072 include tungsten (W) deposited by CVD.

[0096] In some embodiments, the conductive layer 1072 can also be poly-crystalline semiconductors, such as poly-crystalline silicon, poly-crystalline germanium, poly-crystalline germanium-silicon and any other suitable material, and/or combinations thereof. In some embodiments, the poly-crystalline material can be incorporated with any suitable types of dopant, such as boron, phosphorous, or arsenic. In some embodiments, the conductive layer 1072 can also be amorphous semiconductors.

[0097] In some embodiments, the conductive layer 1072 can be made from a metal silicide, including WSi_x , CoSi_x , NiSi_x , or AlSi_x , etc. The forming of the metal silicide material can include forming a metal layer and a poly-crystalline semiconductor using similar techniques described above. The forming of metal silicide can further include applying a thermal annealing process on the deposited metal layer and the poly-crystalline semiconductor layer, followed by removal of unreacted metal.

[0098] In some embodiments, a gate dielectric layer can be disposed in the horizontal tunnels 970 prior to the conductive layer 1072 (not shown in Fig. 10) to reduce leakage current between adjacent word lines (gate electrodes) and/or to reduce leakage current between gate and channel. The gate dielectric layer can include silicon oxide, silicon nitride, silicon oxynitride, and/or any suitable combinations thereof. The gate dielectric layer can also include high-k dielectric materials, such as hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, and/or any combination thereof. The gate dielectric layer can be disposed by one or more suitable deposition processes, such as CVD, PVD, and/or ALD.

[0099] The conductive layers 1072 function as gate electrodes at the intersection with memory strings 212. In Fig. 10, the ten conductive layers 1072 can form ten gate electrodes for each memory string 212, e.g., TSG 334, LSG 332 and eight control gates 333. Corresponding to eight control gates 333, each memory string 212 can have eight memory cells 340. It is noted that the number of memory strings and memory cells are shown for illustrative purposes in Fig. 10, and can be increased for higher storage capacity.

[0100] After forming gate electrodes, conductive materials can be removed and insulating materials can be deposited in the openings to form slit structures 216, separating a memory block into multiple programmable and readable memory fingers (see Fig. 2A-2B).

- [0101] In some embodiments, the doped source line regions 344 in portions of substrate 330 can be formed using techniques such as ion implantation (see Fig. 3). In this example, a conductive core can be inserted in the slit structure 216 to form common source contact to the doped source line region 344.
- [0102] Structure 1000 can include other structures, for example, through array contact (TAC), TSG cut, common source contact and dummy channel structure, which are not shown in Fig. 10 for simplicity.
- [0103] Fig. 11 illustrates a cross-sectional view of an exemplary structure 1100 of a three dimensional memory device, according to some embodiments, wherein the structure 1100 includes a plurality of first contact holes 1180 in the first insulating layer 768 with a diameter of " d_1 ". In Fig. 11, one first contact hole 1180 is shown for each staircase step 1076, which is only for illustrative purpose. Multiple first contact holes 1180 can be formed on each staircase step 1076. In some embodiments, there are no first contact holes 1180 on dummy staircase levels.
- [0104] In some embodiments, photoresist or polymer material can be used as a mask layer to etch the first contact holes 1180. Due to the topology of the staircase structure, depth "H" of the first contact hole 1180 from the top surface to staircase step depends on the location of each step. For a 3D NAND memory with many tiers of word lines, the first contact holes 1180 for the lower staircase steps can be much deeper than the first contact holes 1180 for the upper staircase steps. Therefore, the first contact hole 1180 for the staircase step 1076 closer to the surface 330f of the substrate 330 requires longer etch time than the first contact hole 1180 for the staircase step 1076 away from the surface 330f of the substrate 330. A selective etching process can be used such that the etching rate of the first insulating layer 768 is higher than the conductive layer 1072 and/or the barrier layer 664.
- [0105] In some embodiments, during the etching process for first contact holes 1180, the barrier layer 664 can function as an etch-stop layer and can protect the underlying structure until all the first contact holes 1180 are formed on top of the barrier layer 664 for all levels of the staircase structure 1060. And then the portions of the barrier layer 664 inside the first contact holes 1180 can be removed using the same mask layer. In some embodiments, when

a gate dielectric layer is disposed on the conductive layer 1072, the etching also includes removing the gate dielectric layer inside the first contact holes 1180.

[0106] The first contact holes 1180 extend through the first insulating layer 768, the barrier layer 664, and the optional gate dielectric layer, exposing a portion of the conductive layer 1072 of the upper layer pair 1074-1 in each staircase step 1076. In some embodiments, the first insulating layer 768 is silicon oxide and the barrier layer is a combination of silicon nitride and silicon oxide. In this example, etching silicon oxide can use anisotropic RIE with chemical etchant, for example, CF_4 , CHF_3 , C_2F_6 , C_3F_6 , and/or any combination thereof. Etching silicon nitride can use RIE with chemical etchant, for example, O_2 , N_2 , CF_4 , NF_3 , Cl_2 , HBr , BCl_3 , and/or combinations thereof.

[0107] The diameter “ d_1 ” of the first contact holes 1180 is preferably smaller than the lateral dimension “ a ” of the staircase structure 1060, and will be discussed in detail in the subsequent processes.

[0108] Fig. 12 illustrates a cross-sectional view of an exemplary structure 1200 of a three dimensional memory device, according to some embodiments, wherein the structure 1200 includes a conductive film 1282, disposed over the structure 1100.

[0109] In some embodiments, the conductive film 1282 inside the first contact hole 1180 is in direct contact with the conductive layer 1072 of the upper layer pair 1074-1. The conductive film 1282 also covers a sidewall of the first contact hole 1180. The thickness “ t_1 ” of the conductive film 1282 at the bottom of the first contact hole 1180 can be the same or different from the thickness “ t_2 ” on the sidewall. The height of the conductive film 1282 inside the first contact hole 1180 is determined by the depth “ H ” of the first contact hole 1180.

[0110] The conductive film 1282 can include any suitable conductive material, for example, a metal or metallic compound such as tungsten (W), aluminum (Al), copper (Cu), cobalt (Co), titanium (Ti), tantalum (Ta), titanium nitride (TiN), tantalum nitride (TaN), and/or any combination thereof. The metal or metallic compound can be disposed using a suitable deposition method such as CVD, PVD, PECVD, sputtering, thermal evaporation, e-beam evaporation, MOCVD, and/or ALD.

- [0111] The conductive film 1282 can also be a metal silicide, including WSi_x , CoSi_x , NiSi_x , or AlSi_x , etc. Metal silicide material can be formed by disposing a metal layer directly on a polycrystalline silicon layer inside the first contact hole 1180 and then applying a thermal annealing process followed by removal of unreacted metal.
- [0112] In some embodiments, the conductive film 1282 includes a combination of TiN/W/TiN deposited by CVD.
- [0113] Fig. 13 illustrates a cross-sectional view of an exemplary structure 1300 of a three dimensional memory device, according to some embodiments, wherein the structure 1300 includes a plurality of conductive rings 1384 and a plurality of ring openings 1386. The conductive ring 1384 covers a sidewall of the first insulating layer 768. Bottom of the conductive ring 1384 contacts the conductive layer 1072 of the upper layer pair 1074-1.
- [0114] The conductive ring 1384 can be formed by removing the conductive film 1282 and the conductive layer 1072 from the bottom of the ring openings 1386 using anisotropic etching, such as anisotropic RIE. In some embodiments, the conductive film 1282 and the conductive layer 1072 of the staircase structure 1060 can be tungsten. In this example, the anisotropic etching to form the conductive ring 1384 can include dry etching, for example RIE with a mixture of O_2 and CF_4 , CClF_3 , or CBrF_3 .
- [0115] Anisotropic RIE can include low-pressure plasma system to increase mean-free path of the ions and reduce random scattering. During anisotropic etching, the ions strike the structure 1300 in a vertical direction, perpendicular to the top surface 330f of the substrate 330. In some embodiment, the height “H” (shown in Fig. 12) of the conductive film 1282 can be greater than the total thickness of “ t_1 ” at the bottom of the first contact holes 1180 and the thickness of the conductive layer 1072. Therefore, the conductive film 1282 and the conductive layer 1072 at the bottom of the first contact holes 1180 can be removed, while there is remaining conductive film on the sidewall of the first contact hole 1180, forming the conductive ring 1384.
- [0116] The thickness “ t_3 ” of the conductive ring 1384 depends on the initial sidewall thickness “ t_2 ” of the conductive film 1282, as well as the sidewall profile of the first contact holes 1180. The thickness “ t_3 ” can further depend on the RIE process conditions, for example, total etch time, ion direction angle, pressure, DC bias voltage and RF power, etc. To reduce

parasitic resistance and metal line loading, the conductive ring 1384 with a greater thickness “ t_3 ” is preferred. However trade-off between memory performance and area is needed for a limited diameter “ d_1 ” of the first contact holes 1180.

[0117] For each staircase step 1076, the ring openings 1386 extend through the conductive layer 1072 of the upper layer stack 1074-1, with a smaller diameter “ d_2 ” than the diameter “ d_1 ” of the first contact holes 1180, as shown in Fig. 13.

[0118] Fig. 14 illustrates a cross-sectional view of an exemplary structure 1400 of a three dimensional memory device, according to some embodiments, wherein the structure 1400 includes a second insulating layer 1488 disposed over the structure 1300.

[0119] The second insulating layer 1488 covers the exposed conductive materials inside the ring openings 1386, e.g., the conductive ring 1384 and sidewalls of the conductive layer 1072 of the upper layer pair 1074-1 for each staircase step 1076. The second insulating layer 1488 can be made of a similar material as the first insulating layer 768 and used a similar deposition technique.

[0120] Fig. 15 illustrates a cross-sectional view of an exemplary structure 1500 of a three dimensional memory device, according to some embodiments, wherein the structure 1500 includes a plurality of insulating rings 1590 and a plurality of second contact holes 1592. The insulating rings 1590 can be formed by etching portions of the second insulating layer 1488 and the dielectric layer 450 from the bottom of the ring openings 1386 on structure 1400 (in Fig. 14), wherein the layer 1488 and 450 can be etched using an anisotropic etching, similar to the technique used for forming the conductive ring 1384 except using a different etchant for the dielectric material. In some embodiments, the second insulating layer 1488 can be silicon oxide. In this example, the etching of silicon oxide can include RIE using fluorine based gases, for example, carbon-fluorine (CF_4), hexafluoroethane (C_2F_6), CHF_3 , or C_3F_8 and/or any other suitable gases.

[0121] The second contact hole 1592 extends through the second insulating layer 1488 and the dielectric layer 450 of the upper layer pair 1074-1 for each staircase step 1076, exposing the conductive layer 1072 of the lower layer pair 1074-2.

[0122] Fig. 16A illustrates a cross-sectional view of an exemplary structure 1600 of a three dimensional memory device, according to some embodiments, wherein the structure 1600 includes a plurality of conductive cores 1694.

[0123] The conductive core 1694 can be made of any suitable conductive materials and can be similar to the conductive film 1282, forming by a similar technique. The conductive material for the conductive core 1694 can be disposed over the structure 1500, filling the second contact hole 1592. The conductive core 1694 directly contacts with the conductive layer 1072 of the lower layer pair 1074-2 of each staircase step 1076.

[0124] In some embodiments, a planarization process, such as CMP, can be used to remove any conductive materials on the top surface 768S of the first insulating layer 768.

[0125] Fig. 16B illustrates a perspective view of the structures 1600, wherein the insulating and dielectric layers are omitted for clarity. The conductive ring 1384 and the conductive core 1694 form a coaxial contact structure 1696 on the staircase structure 1060. In some embodiments, the staircase step 1076 of the staircase structure 1060 includes two conductive and dielectric layer pairs, the upper layer pair 1074-1 and the lower layer pair 1074-2. The conductive ring 1384 can be electrically connected to the conductive layer 1072 of the upper layer pair 1074-1 of the staircase step 1076. The conductive core 1694 can be electrically connected to the conductive layer 1072 of the lower layer pair 1074-2 of the staircase step 1076. The conductive ring 1384 and the insulating ring 1590 form a conductive and insulating ring pair 1697, corresponding to one of the conductive and dielectric layer pairs of the staircase step 1076.

[0126] Fig. 17A-17D shows another embodiment of the contact structures for the gate electrodes of a three dimensional memory device. In Fig. 17A-17D a portion of the contact structure and staircase structure are illustrated as an example. Similar elements are labeled with the same reference numbers to compare with the corresponding elements in Fig. 13-16A.

[0127] In this example, during the formation of the conductive ring 1384, using similar processes as described in Fig. 13, the etching process can be performed longer to form a first contact hole 1786, wherein the first contact hole 1786 can extend further through the dielectric layer 450 of the upper layer pair 1074-1 in the staircase step 1076, exposing the conductive layer 1072 of the lower layer pair 1074-2 (see structure 1710 in Fig. 17A).

- [0128] Fig. 17B shows a cross-sectional view of an exemplary structure 1720 of a three dimensional memory device, according to some embodiments, wherein the structure 1720 includes the second insulating layer 1488 disposed over the structure 1710 on the conductive ring 1384, a sidewall of the dielectric layer 450 and the exposed portion of the conductive layer 1072 of the lower layer pair 1074-2 of the staircase step 1076.
- [0129] Fig. 17C shows a cross-sectional view of an exemplary structure 1730 of a three dimensional memory device, according to some embodiments, wherein the structure 1730 includes an insulating spacer 1790 and a contact hole 1792, wherein the contact hole 1792 extends through the second insulating layer 1488 at the bottom, exposing the conductive layer 1072 of the lower layer pair 1074-2 of the staircase step 1076.
- [0130] Fig. 17D shows a cross-sectional view of an exemplary structure 1740 of a three dimensional memory device, according to some embodiments, wherein the structure 1740 includes a conductive core 1794, wherein the conductive core 1794 can be made from a similar material as the conductive core 1694 and formed by a similar technique. In this example, a coaxial contact structure 1796, similar to the coaxial contact structures 1696 is formed.
- [0131] Through the coaxial contact structures 1696/1796, the electrical conductive path for the gate electrode of each memory cell can be wired up to the surface of the wafer, enabling various configurations of word lines and select gates for the 3D memory in the back-of-line process.
- [0132] After forming structure 1600/1740, fabrication of 3D memory device can be resumed with back-end-of-line (BEOL) metal interconnects, and are known to a person with ordinary skill in the art. In some embodiments, a second session of word line stack can be added to the structure 1600/1740 to further increase the vertical number of memory cells.
- [0133] In some embodiments, the staircase structure 1060 can include a plurality of staircase steps 1076, each staircase step 1076 having N number of conductive and dielectric layer pairs 1697, wherein N is a whole number no less than two. In this example, there can be N-1 number of conductive and insulating ring pairs 1697 in addition to a conductive core 1694. Each conductive and insulating ring pair 1697 includes one conductive ring 1384 and one insulating ring 1590, wherein the insulating ring 1590 is disposed to surround a sidewall of

the conductive ring 1384 and is configured to electrically isolate the conductive ring 1384 from another conductive ring 1384 or the conductive core 1694. The conductive core 1694 is located in the center of the coaxial contact structure 1696. In some embodiments, the conductive core 1694 can also include an insulating core that fills possible seams or holes in the conductive core 1694.

[0134] The conductive core 1694 and the conductive rings 1384 can be arranged so that the conductive rings 1384 make electrical contact with the conductive layer 1072 of a corresponding conductive and dielectric layer pair 1697 of the staircase step 1076. An outer conductive ring with a larger diameter can connect to the conductive layer 1072 of an upper conductive and dielectric layer pair of the staircase step 1076. An inner conductive ring with a smaller diameter can connect to the conductive layer 1072 of a lower conductive and dielectric layer pair of the staircase step 1076. The upper conductive and dielectric layer pair is farther away from the substrate, whereas the lower conductive and dielectric layer pair is closer to the substrate. The conductive core 1694 can connect to the bottommost conductive layer, e.g., the pair closest to the substrate, within the staircase step 1076 of N number of conductive and dielectric layer pairs.

[0135] In some embodiments, the conductive rings 1384 extend through the first insulating layer 768 to contact the conductive layer 1072 of the staircase structure 1060. In some embodiments, the conductive rings 1384 also extend through the barrier layer 664 to contact the conductive layer 1072 of the staircase structure 1060. In some embodiments, a gate dielectric layer can be disposed on the conductive layer 1072. In this example, the conductive rings 1384 extend further through the gate dielectric layer to contact the conductive layer of the staircase structure 1060.

[0136] In some embodiments, the insulating ring 1590 of the conductive and insulating ring pair 1697 can be disposed to surround a sidewall of the conductive layer of the staircase structure in addition to the sidewall of the conductive ring. In some embodiments, the insulating ring can be disposed on a sidewall of the dielectric layer of the staircase step of N number of conductive and dielectric layer pairs (similar to the structure shown in Fig. 17D).

[0137] By using the coaxial contact structure to connect two or more conductive layers of the staircase structure, the number of staircase steps can be reduced and thereby the overall

lateral dimension of the staircase structure can be reduced. Accordingly the area of staircase region 210 (shown in Fig. 2A) can be greatly reduced, and higher density memory storage can be achieved.

[0138] Fig. 18 illustrates an exemplary method 1800 for forming staircase and contact structures for a three-dimensional memory array, according to some embodiments. The process steps of the method 1800 can be used to form memory device structures illustrated in Figs. 4-16A. The process steps shown in method 1800 are not exhaustive and other process steps can be performed as well before, after, or between any of the illustrated process steps. In some embodiments, some process steps of exemplary method 1800 can be omitted or include other process steps that are not described here for simplicity. In some embodiments, process steps of method 1800 can be performed in a different order and/or vary.

[0139] At process step 1810, a dielectric film stack is disposed on a substrate. The dielectric film stack can be the dielectric film stack 445 in Fig. 4, with alternating dielectric (first dielectric) and sacrificial (second dielectric) layers. The dielectric and sacrificial layers are similar to the dielectric layer 450 and the sacrificial layer 452 in Fig. 4 and can be disposed using a similar technique. The dielectric layer and the sacrificial layer below are called an alternating dielectric layer pair.

[0140] At process step 1815, a dielectric staircase is formed in the dielectric film stack. An example of the dielectric staircase is shown as the dielectric staircase 560 in Fig. 5, wherein the dielectric staircase includes a plurality of staircase layers, e.g., staircase steps. Each staircase step includes two or more alternating dielectric layer pairs. As an example, Fig. 5 depicts a dielectric staircase with two alternating dielectric layer pairs. The plural steps of the dielectric staircase can be formed by applying a repetitive etch-trim process on the dielectric film stack. First, a patterning mask is disposed and patterned on the dielectric film stack. Then, portions of the dielectric film stack can be exposed and etched in a direction perpendicular to a main surface of the substrate until portions of the two dielectric layer pairs are removed. Afterwards, the patterning mask is trimmed laterally, in a direction parallel to the main surface of the substrate. The etching and trimming processes can be repeated until a dielectric staircase step closest to the main surface of the substrate is formed. Finally, the patterning mask can be removed.

- [0141] At process step 1820, a barrier layer is disposed over the dielectric staircase, wherein the barrier layer can be the barrier layer 664 in Fig. 6 and can be made of a similar material and formed using a similar technique.
- [0142] At process step 1825, a first insulating layer is disposed over the dielectric staircase. In some embodiments, the first insulating layer is disposed on the barrier layer. The first insulating layer can be the first insulating layer 768 in Fig. 7. Next, a planarization process, such as chemical mechanical polishing (CMP) or reaction-ion-etching, can be performed to form a coplanar surface. An example of the structure is shown in Fig. 7.
- [0143] At process step 1830, a plurality of memory strings are formed in the dielectric film stack with alternating dielectric layer pairs. The memory string is similar to the memory string 212 in Fig. 8, and includes a memory film, a channel layer and a core filling film.
- [0144] At process step 1835, the dielectric film stack of alternating dielectric layer pairs is patterned to form a plurality of slit openings. The slit openings extend horizontally along the dielectric staircase and extend vertically through the dielectric film stack. Next, the sacrificial layers of the dielectric staircase are removed horizontally from the slit openings to form a plurality of horizontal tunnels in the staircase structure. After removing the sacrificial layers, the memory film of the memory strings are exposed inside the plurality of tunnels. Fig. 9 shows an example of the structure after removing the sacrificial layers.
- [0145] At process step 1840, conductive materials are disposed inside the horizontal tunnels, forming a staircase structure with alternating conductive and dielectric layers, which is similar to the staircase structure 1060 in Fig. 10. The conductive layer can be made of a similar material as the conductive layer 1072 and can be disposed using a similar technique. In some embodiments, a gate dielectric layer can be disposed on sidewalls of the horizontal tunnels prior to the conductive layer deposition, wherein the gate dielectric layer includes high-k dielectric material, silicon oxide, silicon nitride or silicon oxynitride. After replacing the sacrificial layer with the conductive layer, the staircase structure include a plurality of staircase steps, each having two conductive and dielectric layer pairs, e.g., upper layer pair and lower layer pair.
- [0146] At process step 1845, the first insulating layer is patterned, forming a plurality of first contact holes. The first contact holes extend through the first insulating layer and the optional

barrier layer and expose the conductive layer of upper layer pair of the staircase step. The first contact holes 1180 in Fig. 11 is an example of the plurality of first contact holes.

[0147] At process step 1850, a conductive film is disposed over the staircase structure. The conductive film is disposed on the exposed portion of the conductive layer of the staircase structure and also on a sidewall of the first contact hole. The conductive film can be the conductive film 1282 in Fig. 12, and can be disposed using a similar technique.

[0148] At process step 1855, the conductive film at the bottom of the first contact holes is removed through anisotropic etching, forming conductive rings along a sidewall of the first insulating layer. Examples of the conductive rings are shown in Fig. 13 as the conductive rings 1384. The conductive rings can be made of a similar material as the conductive rings 1384 and be formed using a similar technique.

[0149] At process step 1860, a second insulating layer is disposed over the staircase structure on the conductive rings. The second insulating layer is similar to the second insulating layer 1488 in Fig. 14 and can be made of a similar material using a similar technique.

[0150] At process step 1865, a plurality of insulating rings are formed by anisotropic etching of the second insulating layer. The insulating ring surrounds a sidewall of the conductive ring as well as an exposed portion of the conductive layer of the upper layer pair in the staircase step. During the etching process, the dielectric layer of the upper layer pair can also be removed and the conductive layer of the lower layer pair can be exposed. A plurality of second contact holes are formed accordingly. An example of the insulating rings and second contact holes is shown in Fig. 15, as the insulating rings 1590 and the second contact hole 1592.

[0151] At process step 1870, a plurality of conductive cores are formed inside the second contact holes. The conductive core contact the conductive layer of the lower layer pair in the staircase step. The conductive core can be the conductive core 1694 in Fig. 16, and can be formed using a similar technique. A planarization process, for example CMP, can be used to form a coplanar surface. From top down, the conductive ring, insulating ring and the conductive core form a coaxial contact structure. The coaxial contact structures can provide electrical connections to each of the conductive layer of the staircase structure. With two conductive and dielectric layer pairs per staircase step, the number of contact structures can

be reduced to half, saving the area of staircase region. From these coaxial contact structures, back-end-of-line processes can be resumed with metal interconnect lines to form a functional 3D NAND memory.

[0152] In some embodiments, the staircase structure 1060 can include a plurality of staircase steps 1076, each staircase step 1076 having N number of conductive and dielectric layer pairs 1697, wherein N is a whole number no less than two. In this example, there can be N-1 number of conductive and insulating ring pairs 1697 in addition to a conductive core 1694. N-1 number of conductive and insulating ring pairs and the conductive core can be formed using similar processes as described in process steps 1845-1870.

[0153] In some embodiments, to form the N-1 number of conductive and insulating ring pairs, a first contact hole can be formed to expose a conductive layer in one of the N number of conductive and dielectric layer pairs of the staircase step in the staircase structure. Then a conductive film can be disposed on a sidewall of the contact hole and the exposed conductive layer. Next, the conductive film and a portion of the conductive layer from the bottom of the first contact hole can be removed to form a conductive ring, wherein a bottom of the conductive ring is formed to contact the conductive layer in one of the N number of conductive and dielectric layer pairs of the staircase step in the staircase structure. In some embodiments, the dielectric layer of the next conductive and dielectric layer pair can also be removed during the etching process for the conductive ring.

[0154] In some embodiments, a second insulating layer can be disposed in the first contact hole and the second insulating layer can then be removed from the bottom of the first contact hole to form an insulating ring, thereby surrounding a sidewall of the conductive ring and a sidewall of the conductive layer is exposed in the first contact hole. The cyclic processes for the next conductive and insulating ring pairs resume, starting by forming a second contact hole to expose the next conductive layer in the staircase step, etc..

[0155] In some embodiments, the conductive core of the coaxial contact structure can be formed last. After forming a contact hole to expose the bottommost conductive layer, e.g., closest to the substrate, in the staircase step of N number of conductive and dielectric layer pairs, a conductive material can be disposed to fill the contact hole, and a conductive core can be formed to contact the bottommost conductive layer using a planarization process, such

as chemical mechanical polishing. The conductive material outside the contact hole can be removed and the structure can be formed with a coplanar surface.

[0156] Accordingly, a staircase structure is formed with a plurality of staircase steps, each step having N number of conductive layers. A plurality of coaxial contact structures are formed on the staircase structure. Each coaxial contact structure can provide N number of conductive paths to connect to the N number of the conductive layers, and to the word lines for the vertically stacked memory strings. By sharing contact structures, the lateral dimension of the staircase structure can be greatly reduced, the storage density of the 3D memory devices can be increased.

[0157] Various embodiments in accordance with the present disclosure provide a 3D memory device with smaller die size, higher device density, and improved performance compared with other 3D memory devices.

[0158] Accordingly, various embodiments of three-dimensional memory device and methods of making the same are described in the present disclosure.

[0159] In some embodiments, the three-dimensional memory structure includes a film stack disposed on a substrate, wherein the film stack includes a plurality of conductive and dielectric layer pairs, each conductive and dielectric layer pair having a conductive layer and a first dielectric layer. The three-dimensional memory structure also includes a staircase structure formed in the film stack, wherein the staircase structure includes a plurality of steps, each staircase step having two or more conductive and dielectric layer pairs. The three-dimensional memory structure further includes a plurality of coaxial contact structures formed in a first insulating layer over the staircase structure, wherein each coaxial contact structure includes one or more conductive and insulating ring pairs and a conductive core, wherein each conductive and insulating ring pair includes a conductive ring and an insulating ring.

[0160] In some embodiments, a method for forming a three-dimensional memory structure includes disposing a dielectric film stack on a substrate, wherein the dielectric film stack includes a plurality of alternating dielectric layer pairs, each alternating dielectric layer pair having a first dielectric layer and a second dielectric layer different from the first dielectric layer. The method also includes forming a dielectric staircase in the dielectric film stack,

wherein the dielectric staircase includes a plurality of steps, each dielectric staircase step having two or more alternating dielectric layer pairs. The method further includes disposing a first insulating layer on the dielectric staircase, forming a plurality of memory strings in the dielectric film stack, and replacing the second dielectric layers with conductive layers to form a staircase structure with a plurality of steps, wherein each staircase step includes two or more conductive and dielectric layer pairs, each conductive and dielectric layer pair having a conductive layer and the first dielectric layer. The method also includes forming a plurality of coaxial contact structures on the staircase structure.

[0161] The foregoing description of the specific embodiments will so fully reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt, for various applications, such specific embodiments, without undue experimentation, and without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the disclosure and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the disclosure and guidance.

[0162] Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0163] The Summary and Abstract sections can set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s), and thus, are not intended to limit the present disclosure and the appended claims in any way.

[0164] The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

WHAT IS CLAIMED IS:

1. A three-dimensional memory structure, comprising:

a film stack disposed on a substrate, wherein the film stack comprises a plurality of conductive and dielectric layer pairs, each conductive and dielectric layer pair comprising a conductive layer and a first dielectric layer;

a staircase structure formed in the film stack, wherein the staircase structure comprises a plurality of steps, each staircase step comprising two or more conductive and dielectric layer pairs; and

a plurality of coaxial contact structures formed in a first insulating layer over the staircase structure,

wherein each coaxial contact structure comprises one or more conductive and insulating ring pairs and a conductive core,

wherein each conductive and insulating ring pair comprises a conductive ring and an insulating ring.

2. The three-dimensional memory structure of claim 1, wherein each conductive ring contacts the conductive layer of a corresponding conductive and dielectric layer pair of the staircase step.

3. The three-dimensional memory structure of claim 2, wherein

each coaxial contact structure comprises at least an outer conductive ring and an inner conductive ring; and

the outer conductive ring corresponds with an upper conductive and dielectric layer pair of the staircase step, wherein

the outer conductive ring comprises larger diameter, and

the upper conductive and dielectric layer pair is farther away from the substrate.

4. The three-dimensional memory structure of claim 2, wherein
each coaxial contact structure comprises at least an outer conductive ring and an inner conductive ring; and
the inner conductive ring corresponds with a lower conductive and dielectric layer pair of the staircase step, wherein
the inner conductive ring comprises smaller diameter, and
the lower conductive and dielectric layer pair is closer to the substrate.
5. The three-dimensional memory structure of claim 1, wherein the conductive core contacts the conductive layer closest to the substrate in the staircase step of two or more conductive and dielectric layer pairs.
6. The three-dimensional memory structure of claim 1, wherein
the insulating ring of the conductive and insulating ring pair is disposed to surround a sidewall of the conductive ring and a sidewall of the conductive layer of the staircase structure, wherein the insulating ring is configured to electrically isolate the conductive ring from another conductive ring or the conductive core.
7. The three-dimensional memory structure of claim 6, wherein the insulating ring is disposed on a sidewall of the first dielectric layer of the staircase step of two or more conductive and dielectric layer pairs.
8. The three-dimensional memory structure of claim 1, further comprising a barrier layer, disposed between the first insulating layer and the staircase structure, and the plurality of coaxial contact structures extending through the barrier layer.
9. The three-dimensional memory structure of claim 1, further comprising:
a gate dielectric layer on the conductive layer, and

the conductive rings extending through the gate dielectric layer to contact the conductive layers of the staircase structure.

10. A method for forming a three-dimensional memory structure, comprising:

disposing a dielectric film stack on a substrate, wherein the dielectric film stack comprises a plurality of alternating dielectric layer pairs, each alternating dielectric layer pair comprising a first dielectric layer and a second dielectric layer different from the first dielectric layer;

forming a dielectric staircase in the dielectric film stack, wherein the dielectric staircase comprises a plurality of steps, each dielectric staircase step comprising two or more alternating dielectric layer pairs;

disposing a first insulating layer on the dielectric staircase;

forming a plurality of memory strings in the dielectric film stack;

replacing the second dielectric layers with conductive layers to form a staircase structure with a plurality of steps, wherein each staircase step comprises two or more conductive and dielectric layer pairs, each conductive and dielectric layer pair comprising a conductive layer and the first dielectric layer; and

forming a plurality of coaxial contact structures on the staircase structure.

11. The method of claim 10, wherein forming the coaxial contact structure comprises:

forming a conductive and insulating ring pair for each conductive and dielectric layer pair of the staircase step in the staircase structure, wherein the conductive and insulating ring pair comprises a conductive ring and an insulating ring.

12. The method of claim 11, wherein forming the conductive ring comprises:

forming a first contact hole to expose the conductive layer in one of the two or more conductive and dielectric layer pairs of the staircase step in the staircase structure;

disposing a conductive film on a sidewall of the contact hole and the exposed conductive layer; and

removing the conductive film and a portion of the conductive layer from a bottom of the first contact hole to form a conductive ring, wherein a bottom of the conductive ring is formed to contact the conductive layer in one of the two or more conductive and dielectric layer pairs of the staircase step in the staircase structure.

13. The method of claim 12, wherein forming the conductive ring further comprises etching the first dielectric layer of the next conductive and dielectric layer pair.

14. The method of claim 11, wherein forming the insulating ring comprises:
disposing a second insulating layer in a first contact hole;
removing the second insulating layer from the bottom of the first contact hole; and
forming the insulating ring surrounding a sidewall of the conductive ring and a sidewall of the conductive layer of one of the two or more conductive and dielectric layer pairs in the staircase step in the staircase structure; and
forming a second contact hole to expose the next conductive layer in the staircase step.

15. The method of claim 10, wherein forming the coaxial contact structure further comprises:
forming a contact hole to expose the conductive layer closest to the substrate in the staircase step of two or more conductive and dielectric layer pairs;
disposing a conductive material to fill the contact hole; and
forming a conductive core to contact the conductive layer closest to the substrate in staircase step of two or more conductive and dielectric layer pairs.

16. The method of claim 15, further comprising performing a planarization process to remove the conductive material outside the contact hole and form a coplanar surface.

17. The method of claim 10, further comprising disposing a barrier layer on the dielectric staircase prior to the first insulating layer.

18. The method of claim 10, wherein forming the plurality of dielectric staircase steps, each having two or more dielectric layer pairs, comprises:

disposing a patterning mask on the dielectric film stack;

etching exposed portions of the dielectric film stack in a direction perpendicular to a main surface of the substrate until portions of the two or more dielectric layer pairs are removed;

trimming the patterning mask laterally, in a direction parallel to the main surface of the substrate;

repeating the etching and the trimming until a dielectric staircase step closest to the main surface of the substrate is formed; and

removing the patterning mask.

19. The method of claim 10, wherein replacing the second dielectric layers with the conductive layers to form the staircase structure, comprises:

forming one or more slit structure openings, extending horizontally along the dielectric staircase, wherein the slit structure openings penetrate vertically through the dielectric film stack;

removing the second dielectric layers of the dielectric staircase to form a plurality of horizontal tunnels; and

disposing the conductive layers inside the plurality of horizontal tunnels.

20. The method of claim 19, further comprising:

disposing a gate dielectric layer on sidewalls of the horizontal tunnels prior to disposing the conductive layer, wherein the gate dielectric layer comprises high-k dielectric material, silicon oxide, silicon nitride or silicon oxynitride.

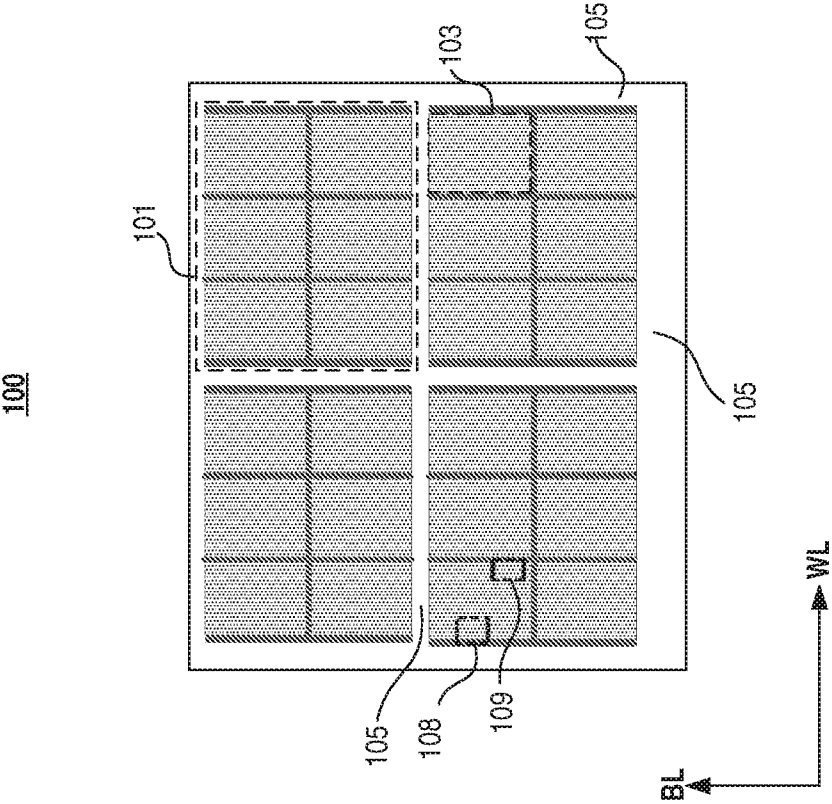
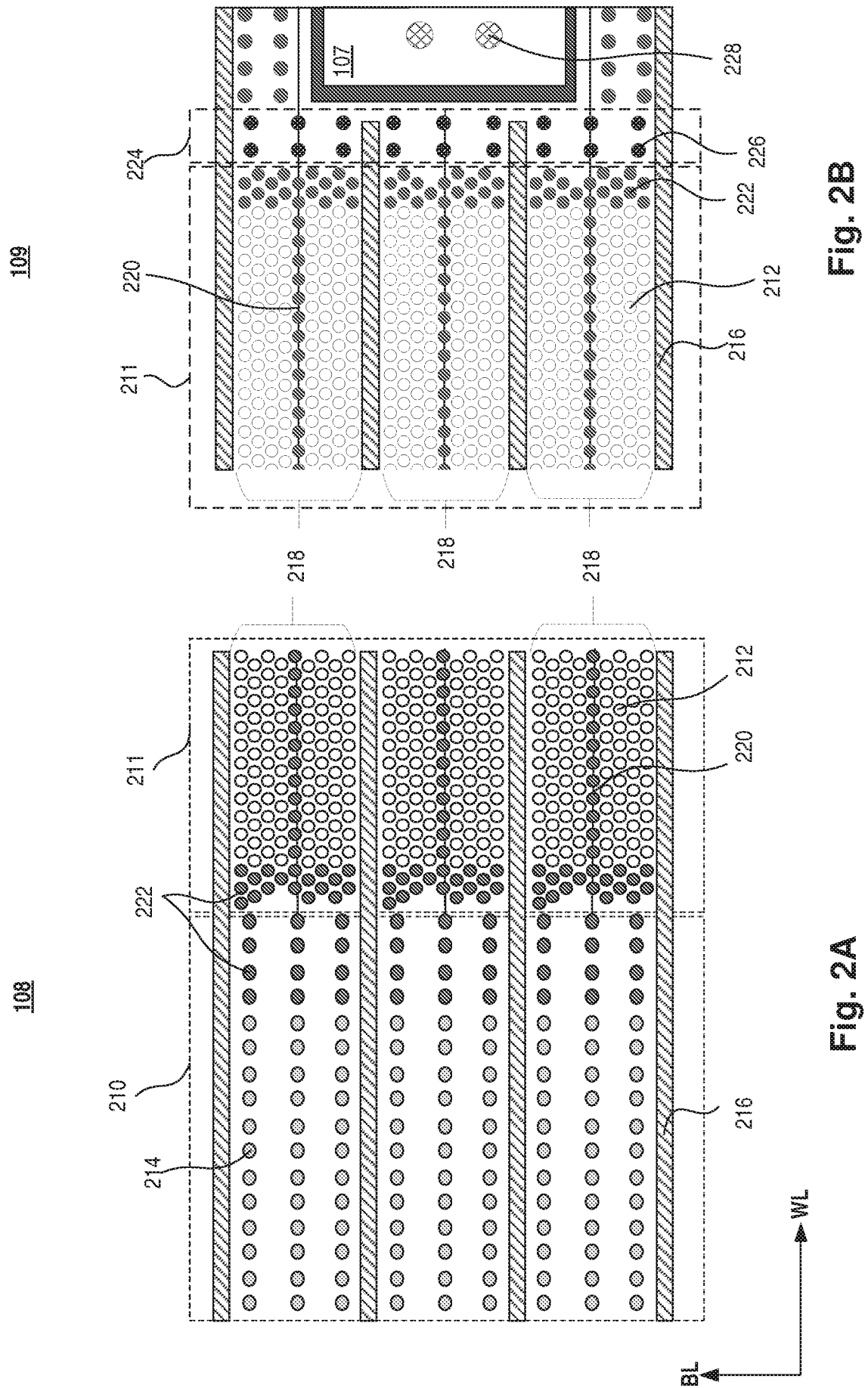
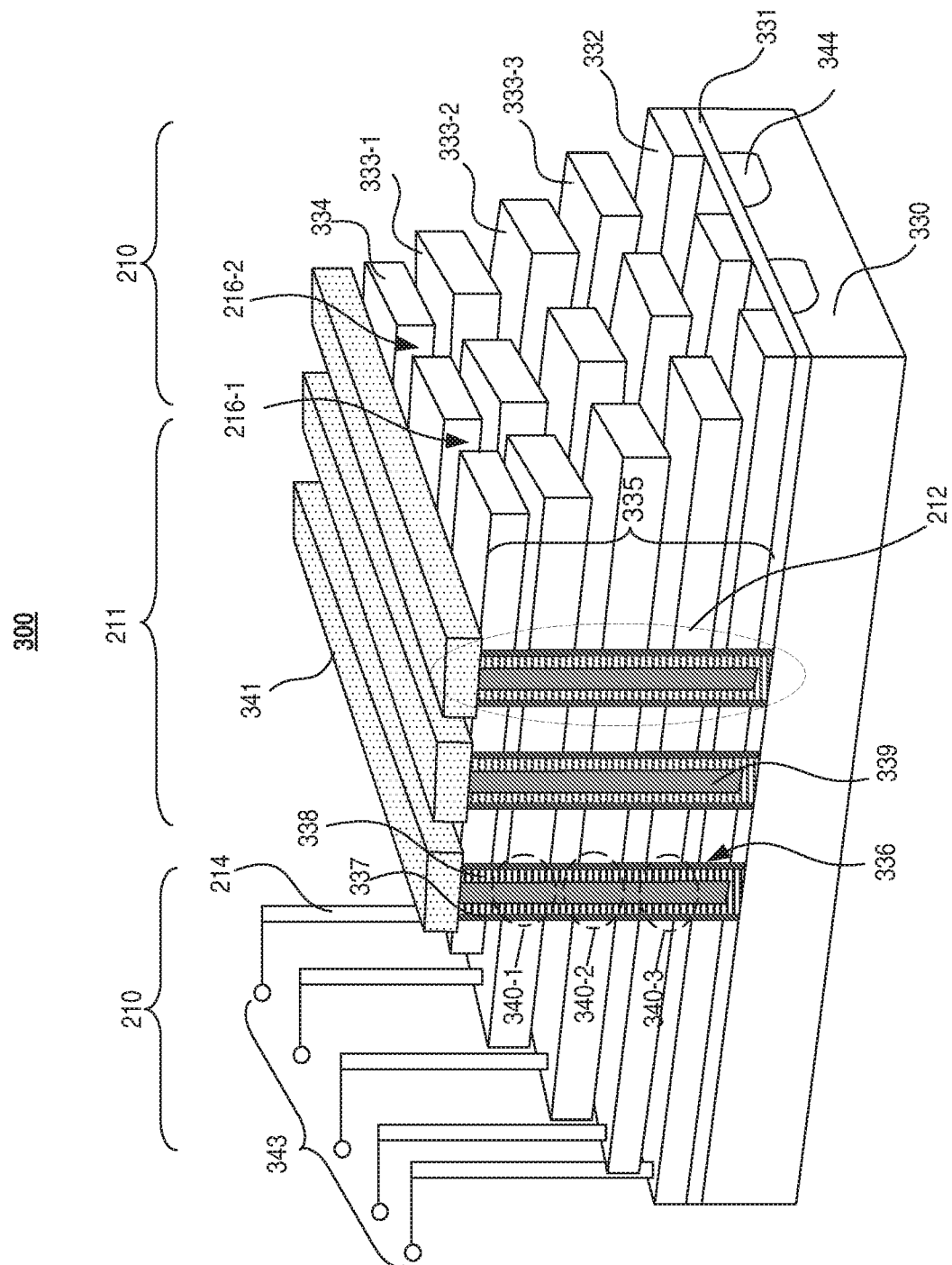


Fig. 1





400

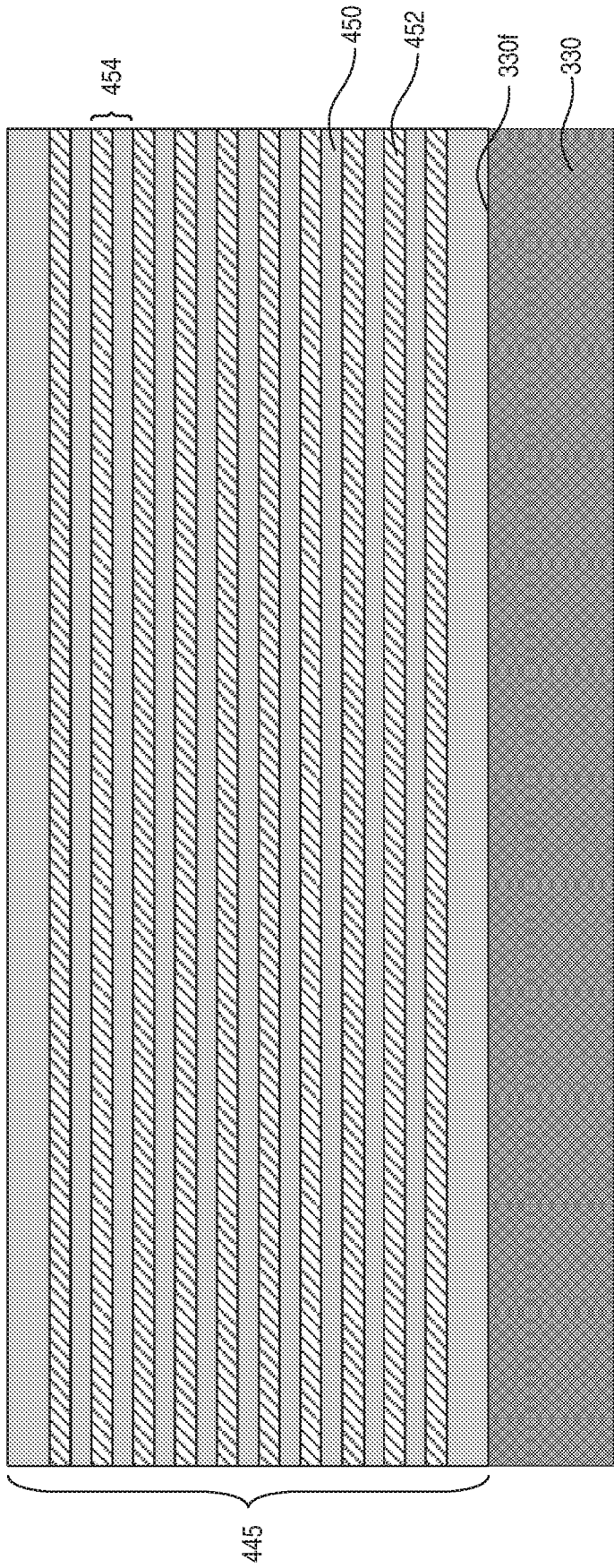


Fig. 4

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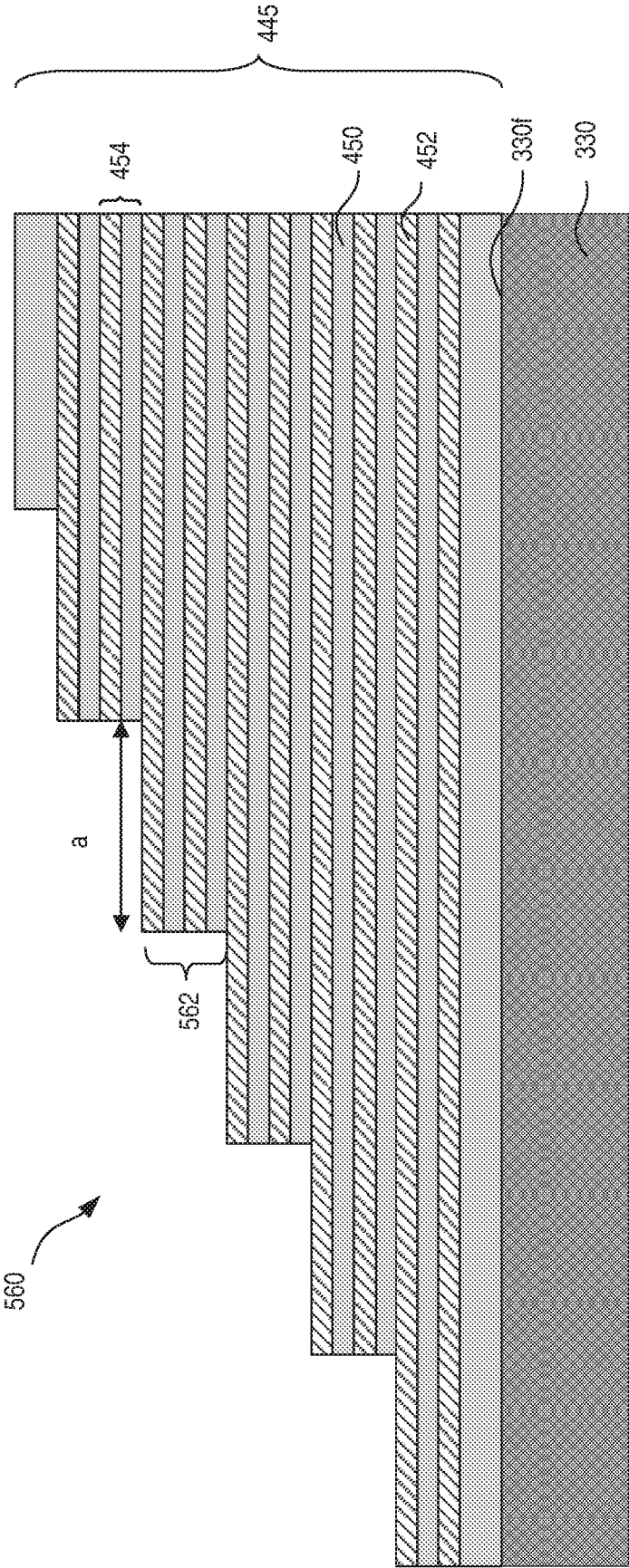


Fig. 5

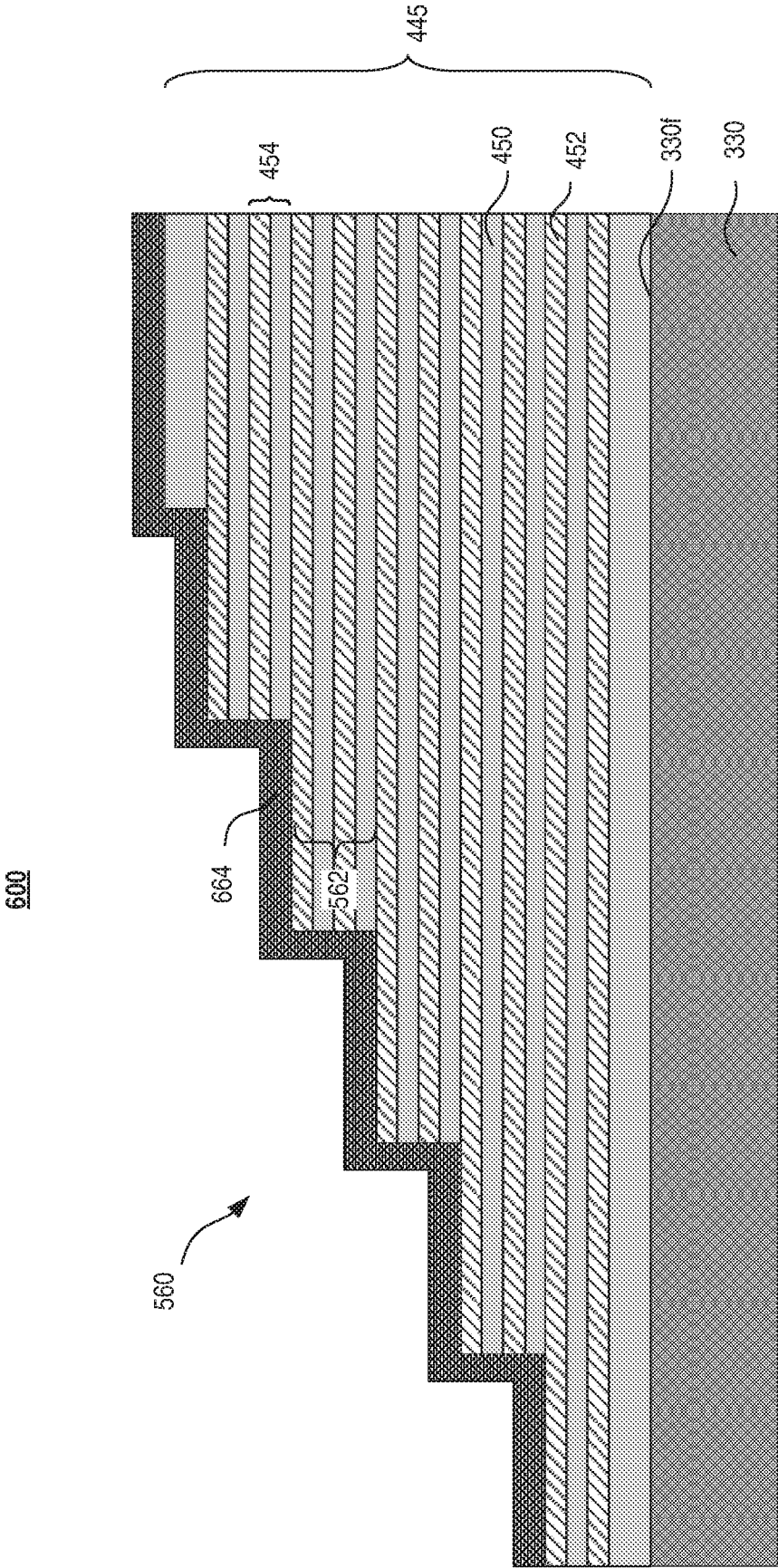


Fig. 6

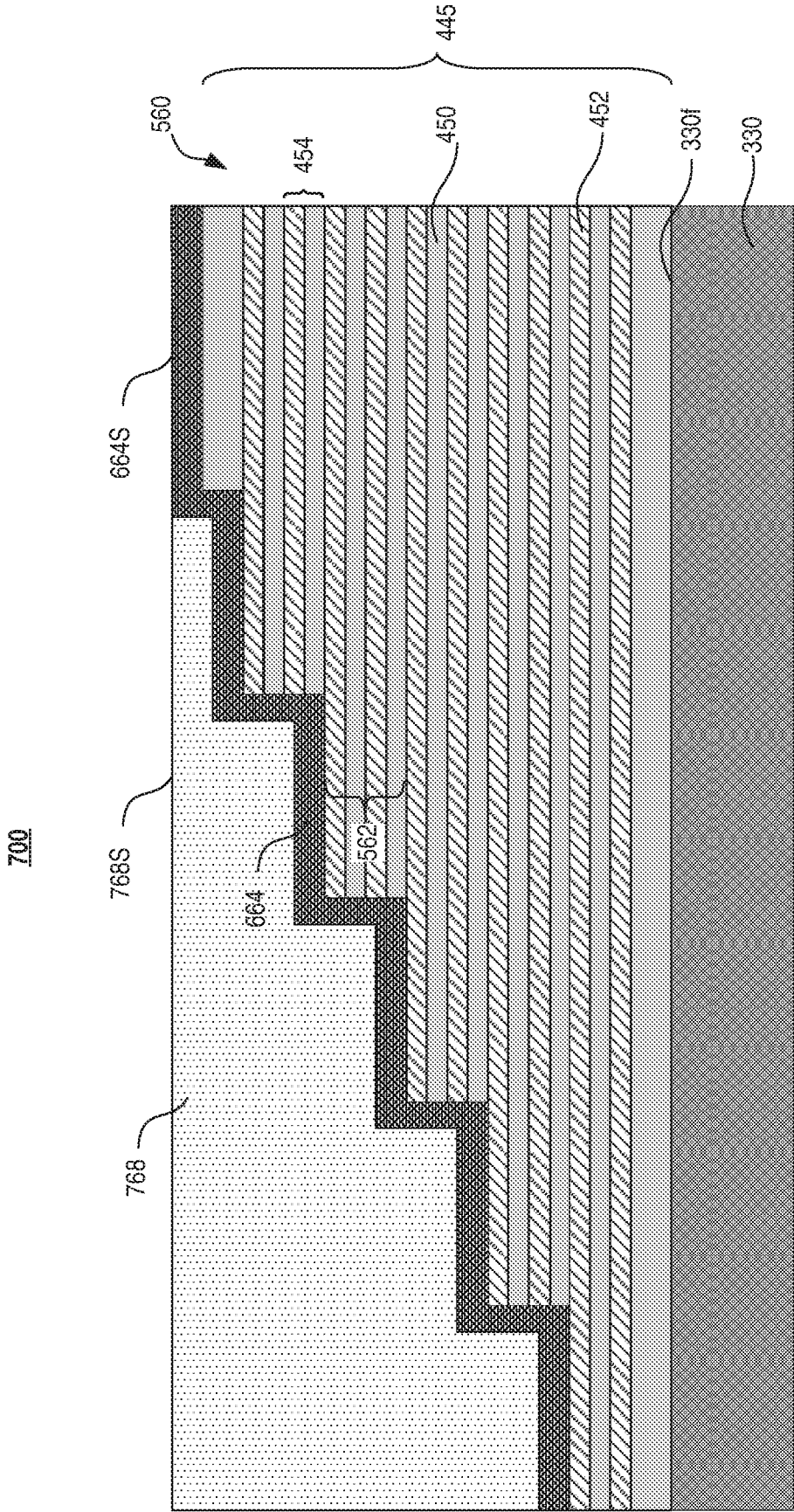
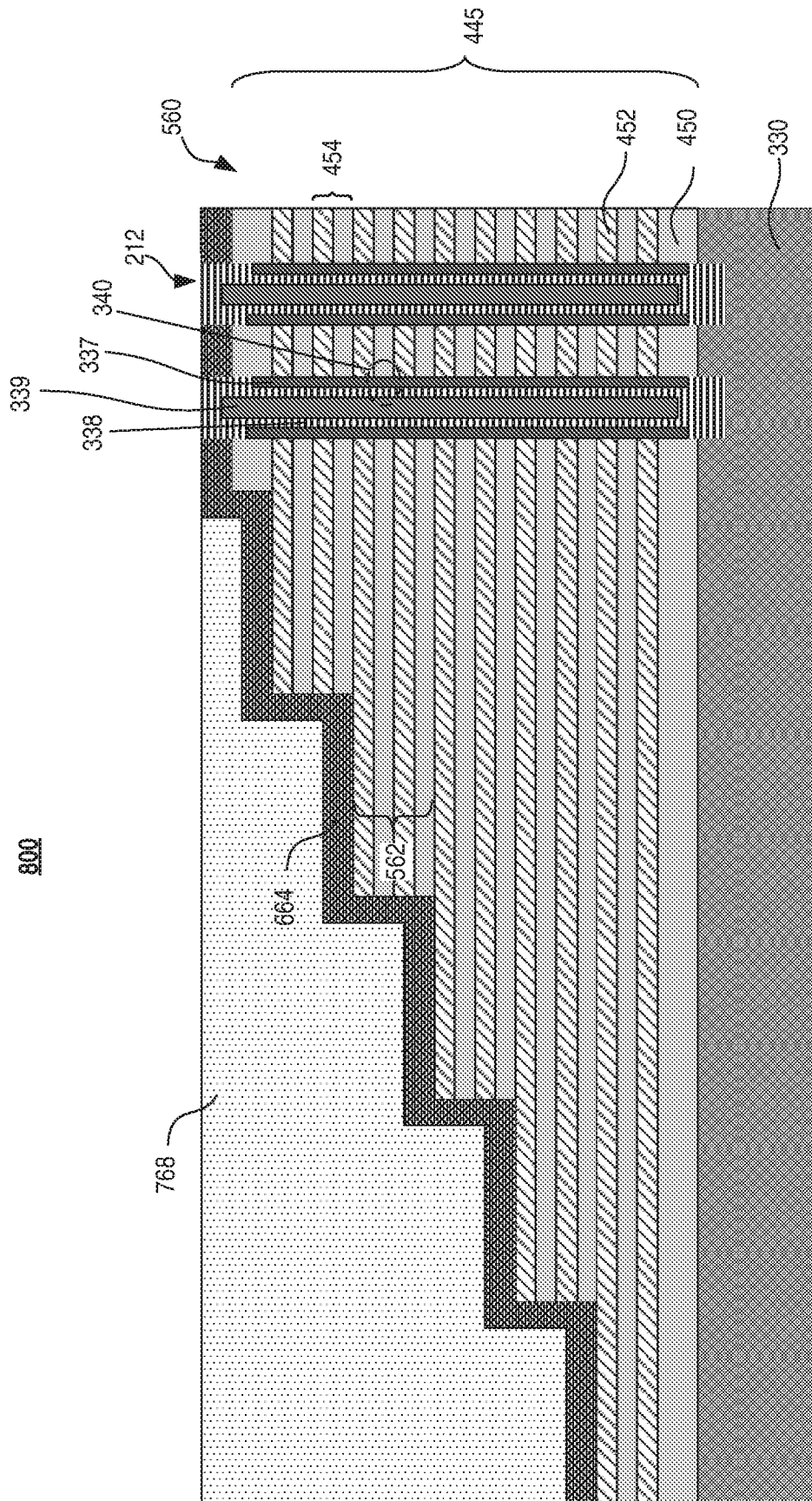


Fig. 7



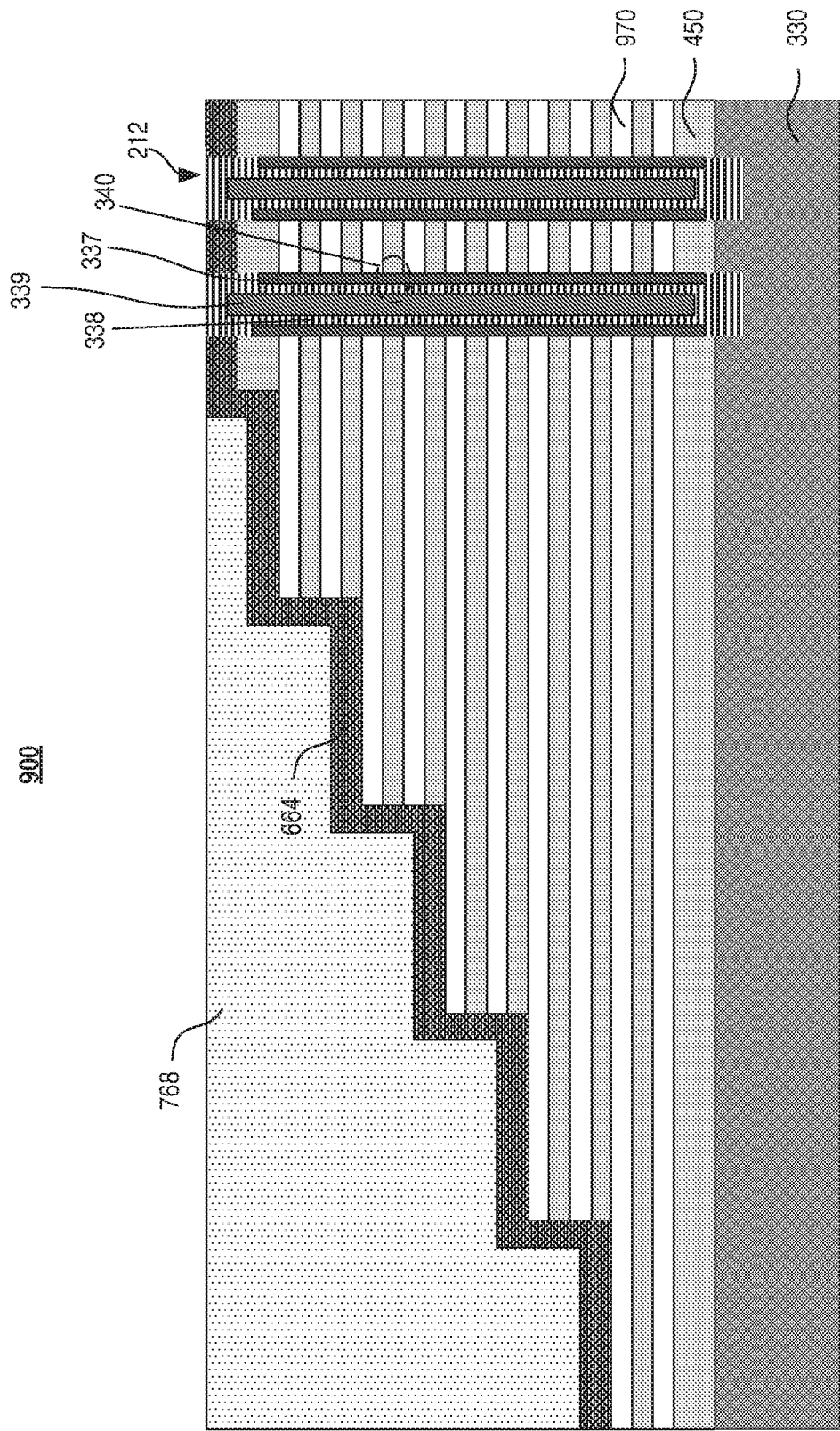
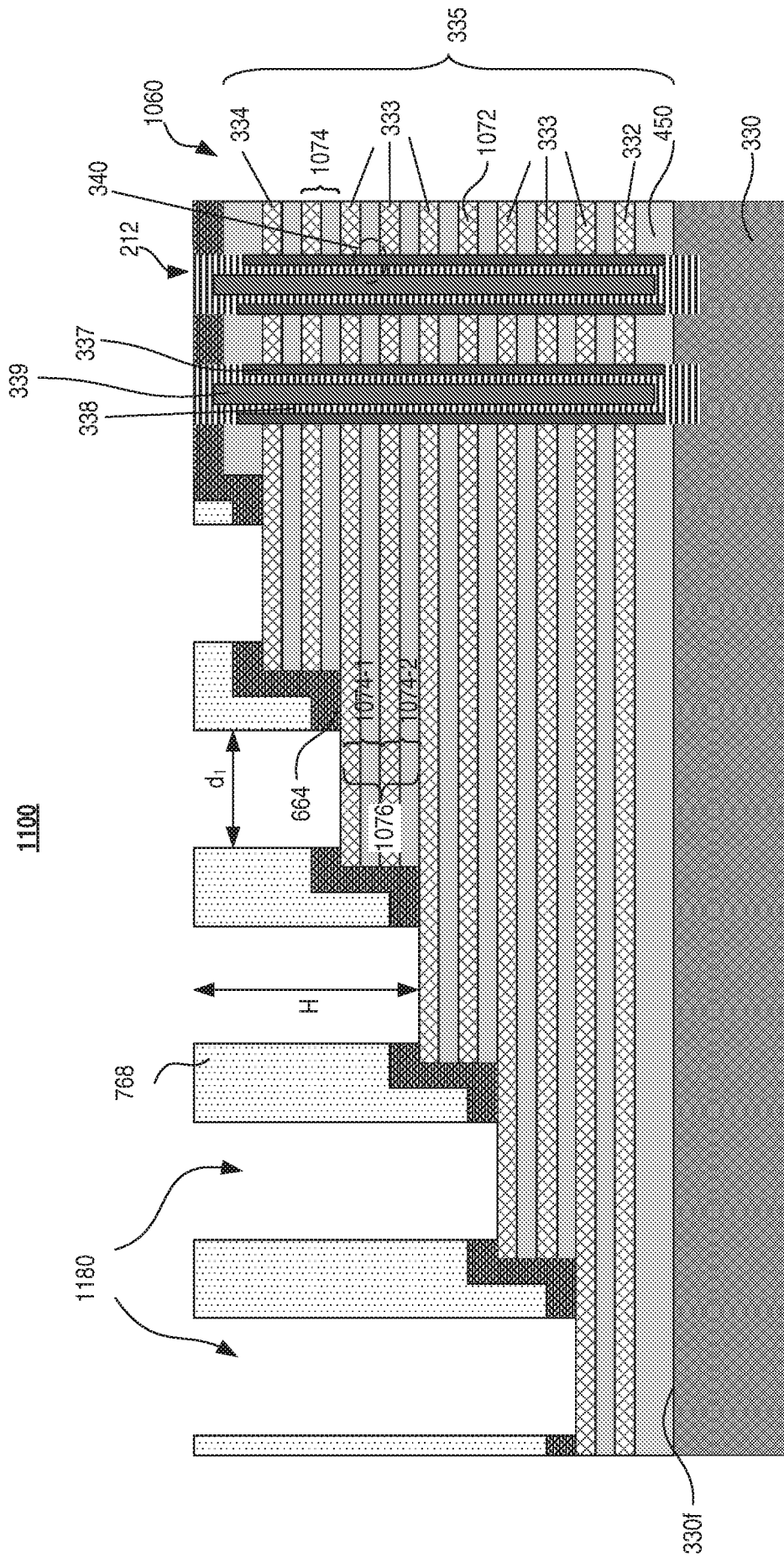


Fig. 9



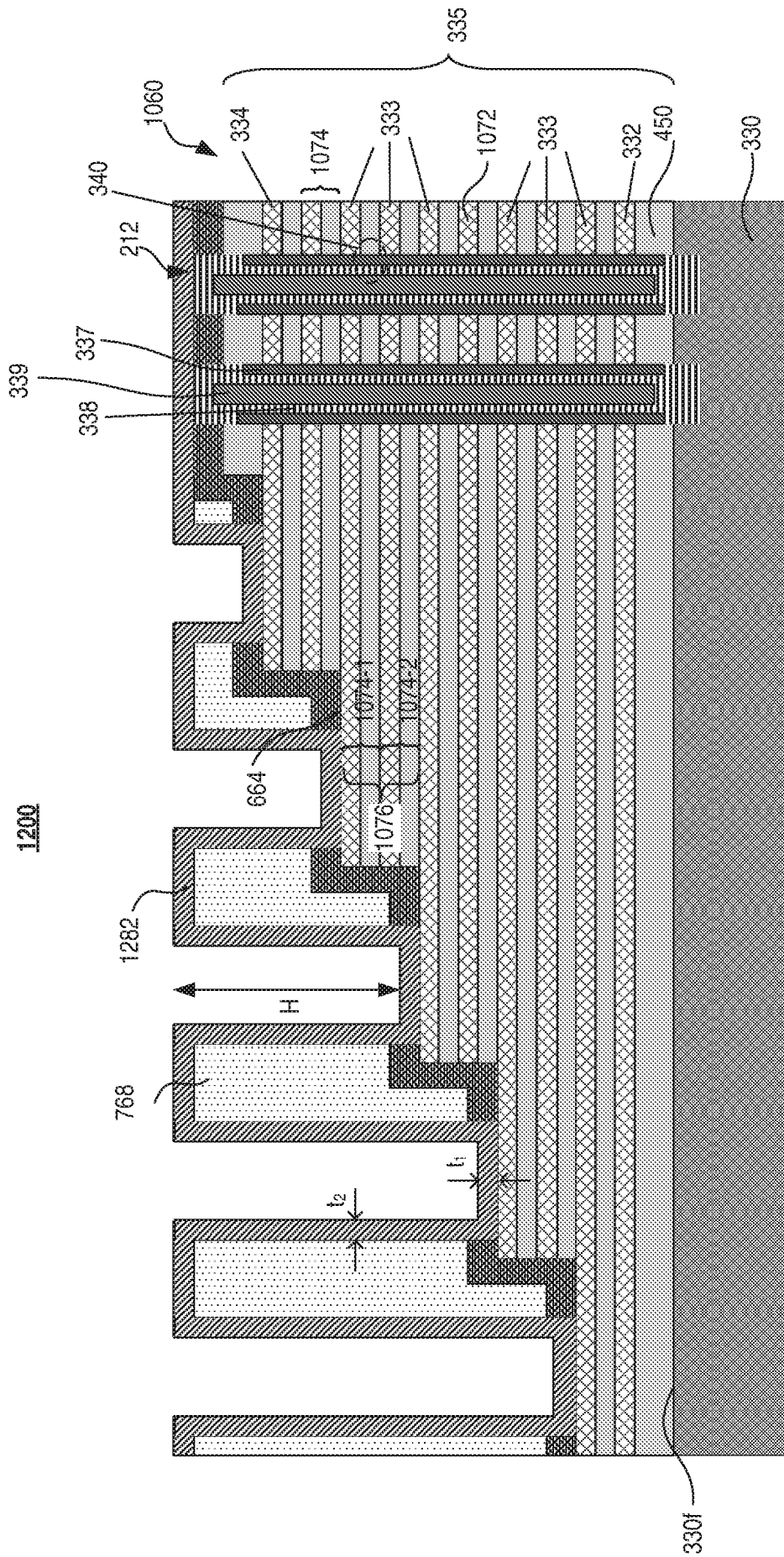


Fig. 12

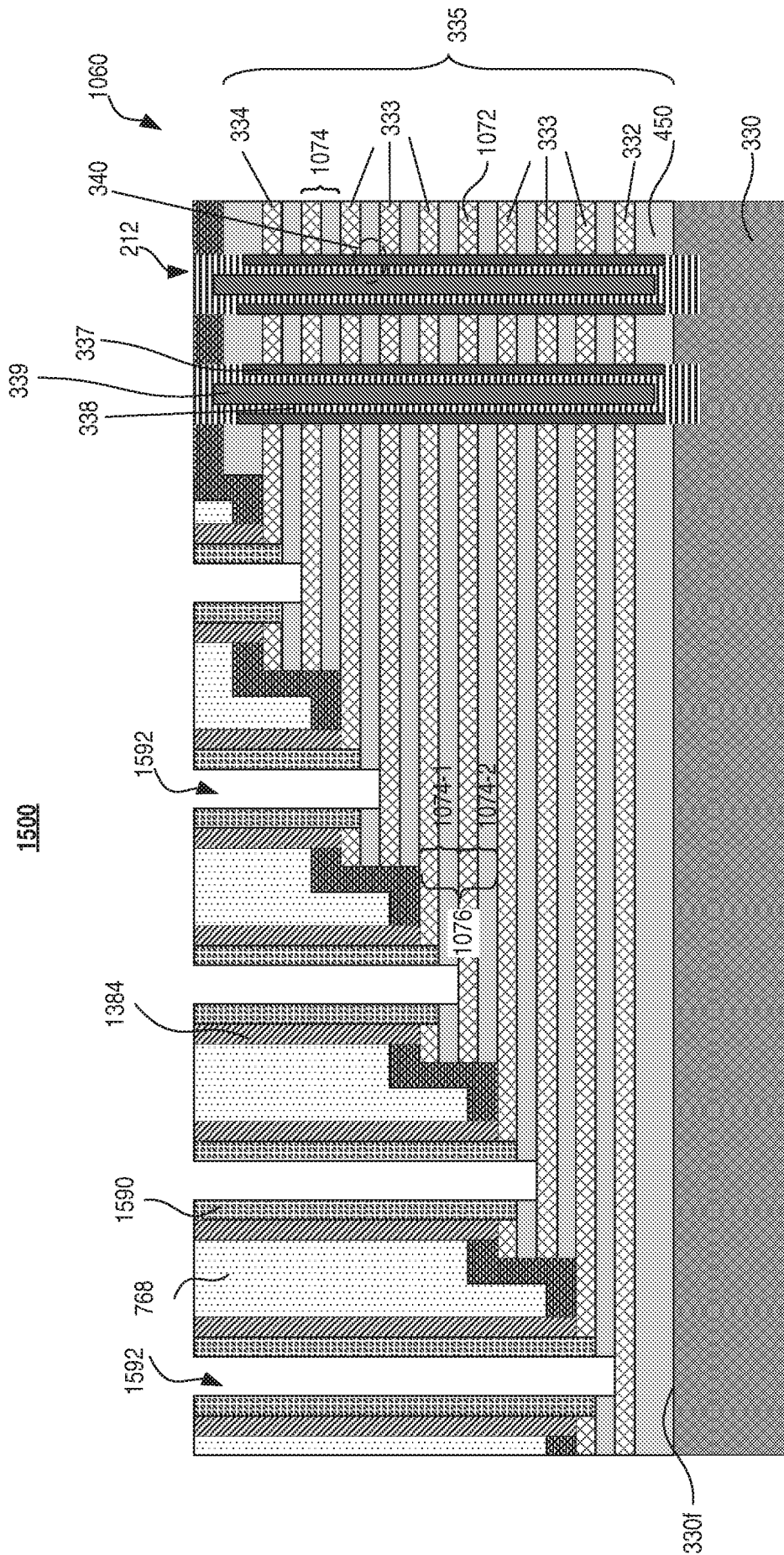


Fig. 15

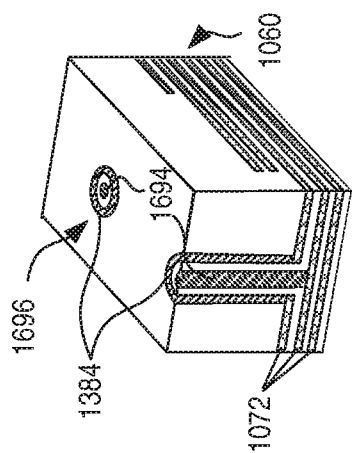


Fig. 16B

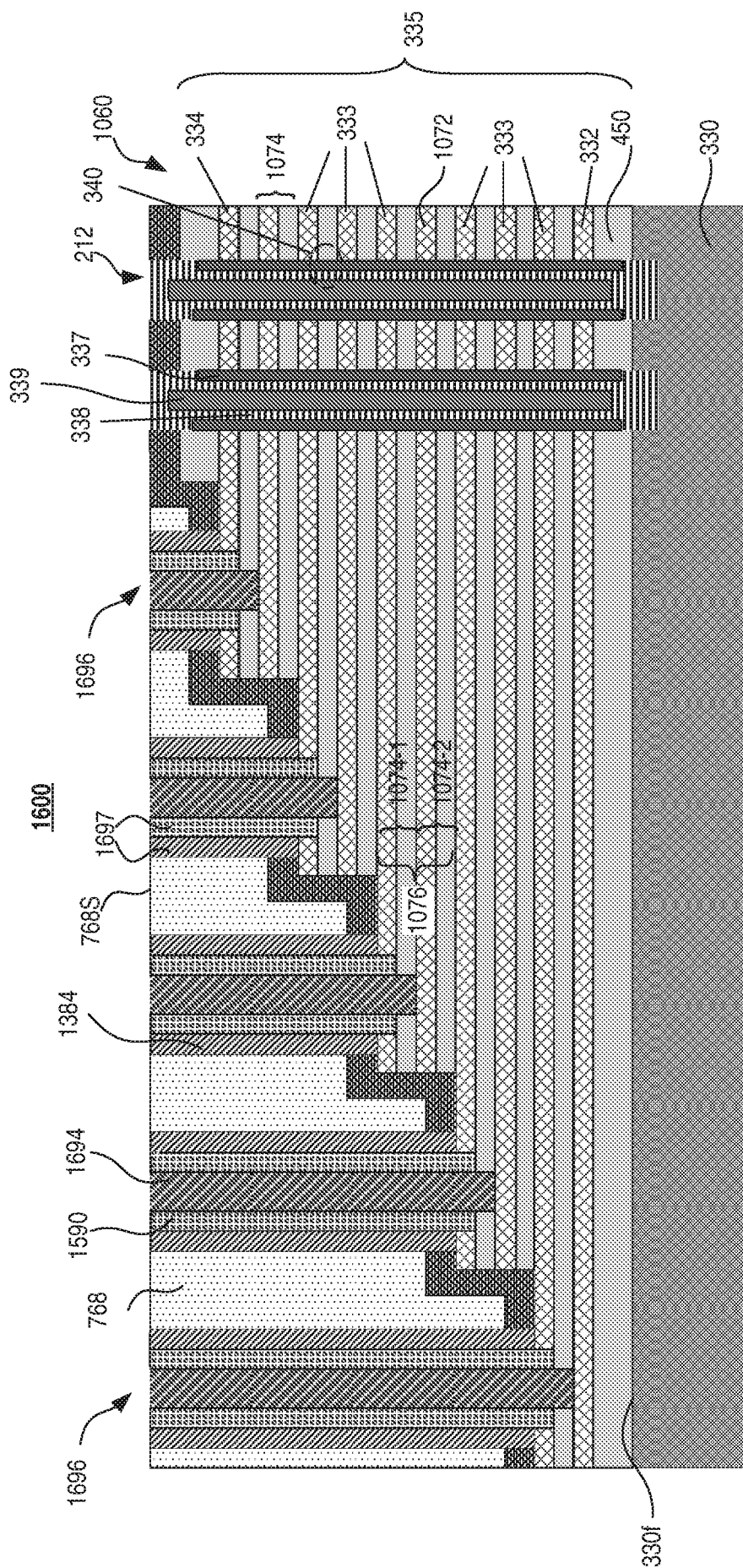


Fig. 16A

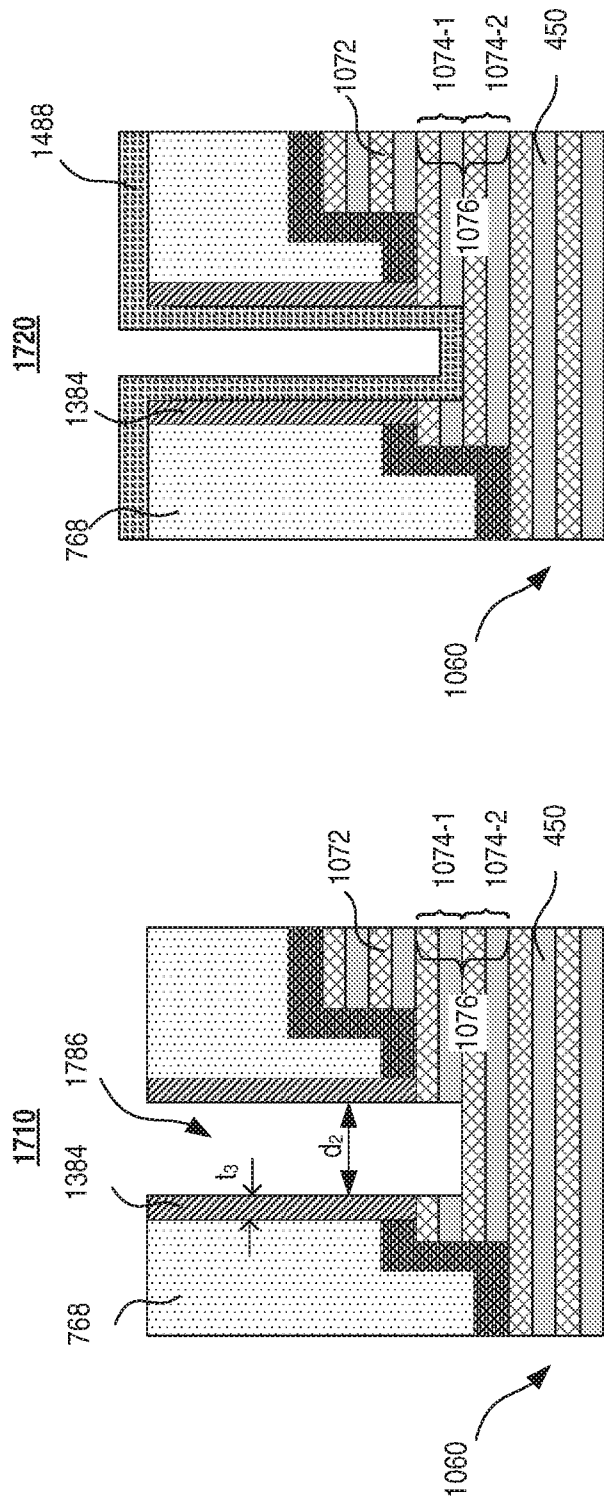
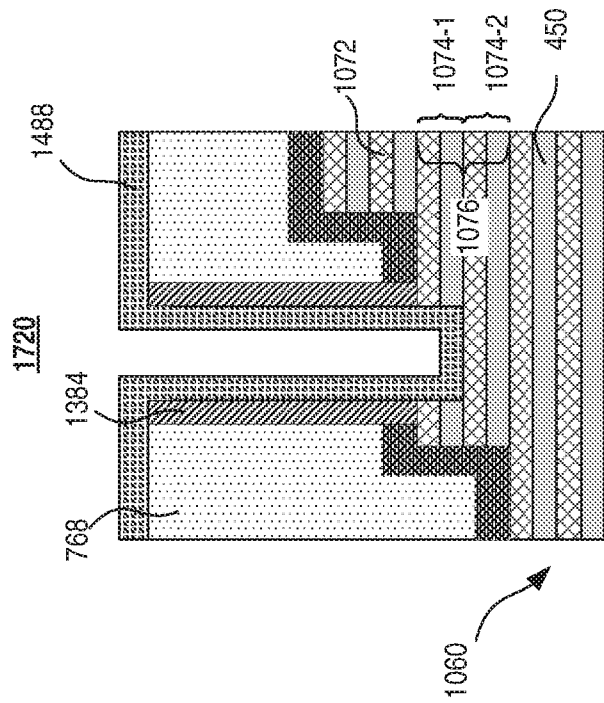


Fig. 17A



1979

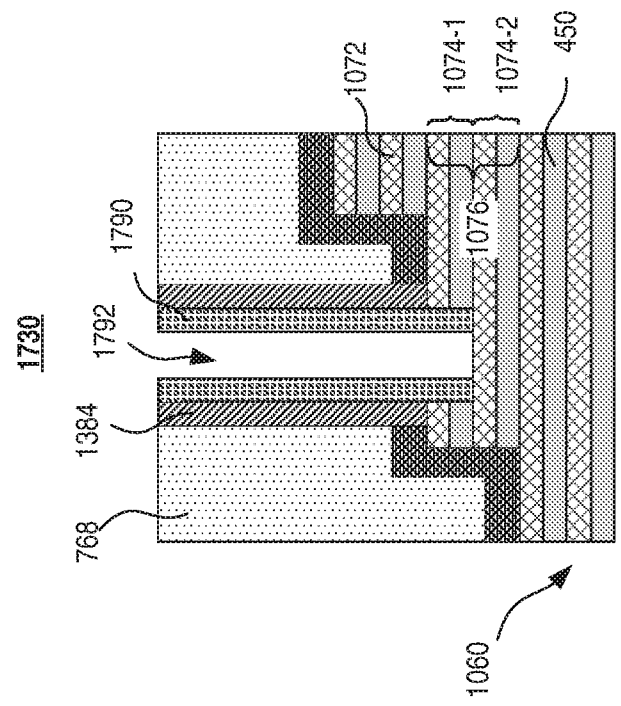


Fig. 17C

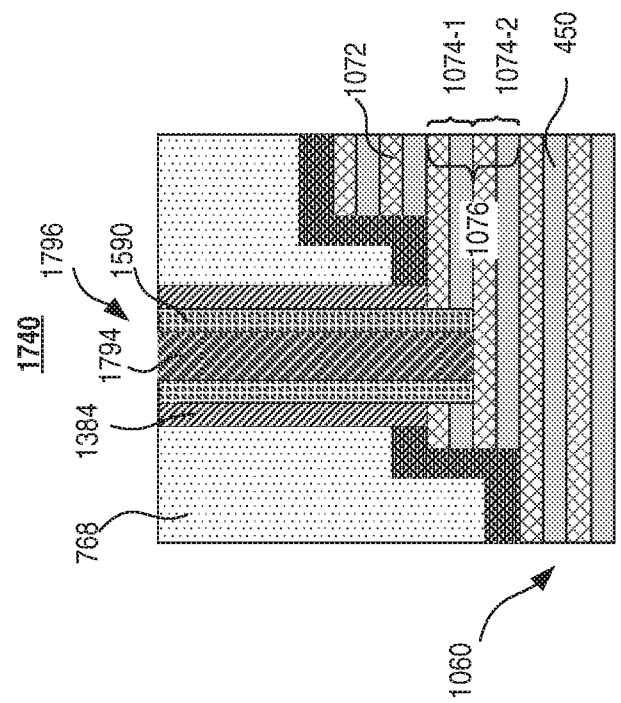
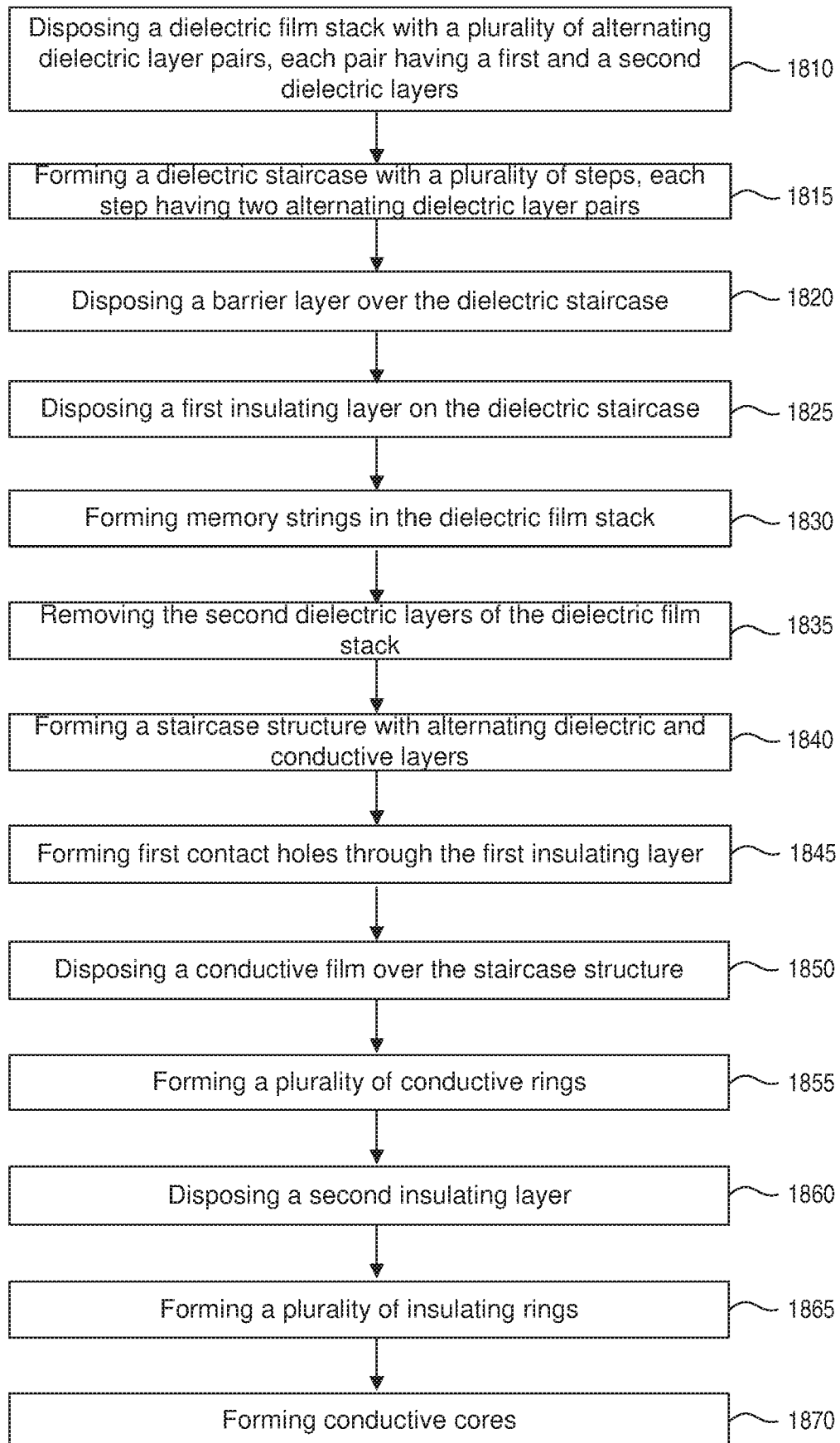


Fig. 21

**Fig. 18**

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2018/120715

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/115(2017.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L; G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,CNKI,WPI,EPODOC,IEEE: three, dimensional, memory, film, stack, conductive, dielectric, layer, pair, stair, step, coaxial, insulating, ring, core, inner, outer, surround, barrier, mask, etching, trimming, slit, horizontal, tunnel

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2012306090 A1 (MICRON TECHNOLOGY, INC.) 06 December 2012 (2012-12-06) description, paragraphs [0015]-[0033], figures 1-16	1-20
Y	US 2015137216 A1 (LEE, SEOK-WON ET AL.) 21 May 2015 (2015-05-21) description, paragraphs [0108]-[0137], [0200]-[0277], figures 9A-17D, 39-58	1-20
A	US 2017179025 A1 (YUN, SEOK-JUNG ET AL.) 22 June 2017 (2017-06-22) the whole document	1-20
A	CN 108493192 A (YANGTZE MEMORY TECHNOLOGIES CO., LTD.) 04 September 2018 (2018-09-04) the whole document	1-20
A	CN 108899322 A (YANGTZE MEMORY TECHNOLOGIES CO., LTD.) 27 November 2018 (2018-11-27) the whole document	1-20

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

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“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

02 September 2019

Date of mailing of the international search report

11 September 2019

Name and mailing address of the ISA/CN

National Intellectual Property Administration, PRC
6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing
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WANG,Jing

Facsimile No. (86-10)62019451

Telephone No. 86-(10)-53961317

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2018/120715

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CN	108899322	A	27 November 2018	None			