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(71) Applicant *(for all designated States except US)*: **ACORN TECHNOLOGIES, INC.** [US/US]; 881 Alma Real Drive, Suite 305, Pacific Palisades, California 90272 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **GRUPP, Daniel, E.** [US/US]; 334 Leland Ave., Palo Alto, California 94306 (US). **CONNELLY, Daniel, J.** [US/US]; 924 Potrero Avenue, San Francisco, California 94110 (US). **CLIFTON, Paul, A.** [GB/US]; 675 Sharon Park Drive, #321, Menlo Park, California 94025 (US). **FAULKNER, Carl, A.** [US/US]; 2847 Alhambra Drive, Belmont, California 94002 (US).

(74) Agent: FAHMI, Tarek; Blakely, Sokoloff, Taylor & Zafman LLP, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 (US).

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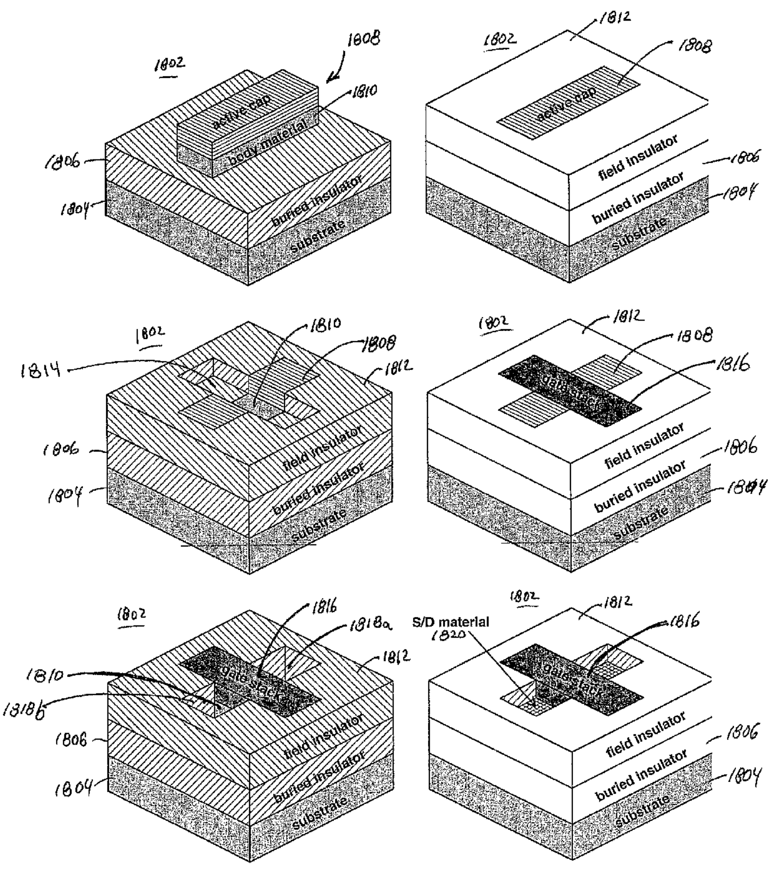
(54) Title: PROCESS FOR FABRICATING A SELF-ALIGNED DEPOSITED SOURCE/DRAIN INSULATED GATE FIELD-EFFECT TRANSISTOR



(57) Abstract: Processes for forming self-aligned, deposited source/drain, insulated gate, transistors and, in particular, FETs. By depositing a source/drain in a recess such that it remains only in the recess, the source/drain can be formed self-aligned to a gate and/or a channel of such a device. For example, in one such process a gate structure of a transistor may be formed and, in a material surrounding the gate structure, a recess created so as to be aligned to an edge of the gate structure. Subsequently, a source/drain conducting material may be deposited in the recess. Such a source/drain conducting material may be deposited, in some cases, as layers, with one or more such layers being planarized following its deposition. In this way, the conducting material is kept within the boundaries of the recess.

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2004/142524 A1 (GRUPP DANIEL E ET AL) 22 July 2004 (2004-07-22) figures 4,5 -----	1-6, 10-46 7-9
X	US 5 943 575 A (CHUNG ET AL) 24 August 1999 (1999-08-24) figure 3 -----	1-3
X	US 6 091 076 A (DELEONIBUS ET AL) 18 July 2000 (2000-07-18) paragraph ‘0061!; figures 9,14 -----	1-3

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Information on patent family members

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