SEMICONDUCTOR DEVICE PROVIDED WITH FEEDBACK CIRCUIT INCLUDING RESISTIVE ELEMENT AND CAPACITIVE ELEMENT

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ABSTRACT
The present invention provides a switching power supply circuit capable of stabilizing an output voltage as well as increasing a response speed of the output voltage by improving a phase margin of an open loop as a whole of the switching power supply circuit. The switching power supply circuit according to the present invention includes a resistor and a capacitor in addition to a configuration of a conventional switching power supply circuit. The resistor is connected between a node and the capacitor. The capacitor is connected between the resistor and another node. The resistor and the capacitor configure a phase compensation circuit. The phase compensation circuit has a cut-off frequency in accordance with a resonance frequency of an inductor and a capacitor by adjusting a resistance value of the resistor and a capacitance of the capacitor.
FIG. 3

Diagram showing a control circuit output voltage detection circuit with labels for VIN, N1a, LOW-PASS FILTER, LOAD, OUTPUT VOLTAGE DETECTION CIRCUIT, 30, 31, 34, 36, 4a, 20, 21, 19, 32, 33, N2.
FIG. 11 PRIOR ART

FIG. 12

TRIANGULAR WAVE OSCILLATOR

TRIANGULAR WAVE OSCILLATOR
FIG. 13 PRIOR ART

TRIANGULAR WAVE OSCILLATOR

FIG. 14

TRIANGULAR WAVE OSCILLATOR
FIG. 15 PRIOR ART
Fig. 16
SEMICONDUCTOR DEVICE PROVIDED WITH FEEDBACK CIRCUIT INCLUDING RESISTIVE ELEMENT AND CAPACITIVE ELEMENT

RELATED APPLICATIONS


BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention
[0003] The present invention relates to a semiconductor device. In particular, the present invention relates to a switching power supply circuit.
[0004] 2. Description of the Background Art
[0005] In a switching power supply circuit as one of semiconductor devices, an error between a voltage obtained by division of an output voltage by a serial resistive element and a predetermined reference voltage is amplified with an error amplifier. On the basis of the error, On-Duty of a switching element is controlled with a PWM (Pulse Width Modulator) comparator to keep an output voltage value constant. Thus, it is possible to obtain a desired direct current voltage from an input direct current voltage.

[0006] It is to be noted that conventional techniques regarding the switching power supply circuit are disclosed in, for example, Japanese Patent Application Laid-Open Nos. 2001-86740, 2003-52170 and 2004-80985.

[0007] As described in the switching power supply circuit, an output voltage is fed back to the error amplifier to control the output voltage. Incidentally, in the switching power supply circuit, a low-pass filter circuit including an inductor and a capacitor is connected between an input terminal and an output terminal. Therefore, according to the configuration where the output voltage is fed back to the error amplifier, the aforementioned inductor and capacitor are included in the feedback loop. For this reason, there is a problem in that a phase of an open loop as a whole of the power supply circuit in a resonance frequency of the inductor and the capacitor changes by about 180°, which causes a phase margin to be lost, leading to oscillation of the circuit.

SUMMARY OF THE INVENTION

[0008] It is an object of the present invention to provide a semiconductor device capable of stabilizing an output voltage as well increasing a response speed of the output voltage by addition of a new feedback loop for improving a phase margin of an open loop as a whole of a switching power supply circuit.
[0009] According to a first aspect of the present invention, a semiconductor device includes an input terminal, an output terminal, a switching element, an output voltage detection circuit, a control circuit and a feedback circuit. The switching element is connected between the input terminal and the output terminal. The output voltage detection circuit detects an output voltage as a voltage of the output terminal. The control circuit is connected between a control electrode of the switching element and the output voltage detection circuit, and controls driving of the switching element on the basis of the output voltage detected by the output voltage detection circuit. The feedback circuit is connected between a first node as an output electrode of the switching element and a second node located between the output voltage detection circuit and the control circuit, and includes a resistive element and a capacitive element.

[0010] Thus, it is possible to improve a phase margin of the open loop as a whole of the switching power supply circuit.

[0011] A semiconductor device according to a second aspect of the present invention includes an input terminal, an output terminal, a switching element, an output voltage detection circuit, a control circuit and a feedback circuit. The switching element is connected between a first node located between the input terminal and the output terminal and a ground potential. The output voltage detection circuit detects an output voltage as a voltage of the output terminal. The control circuit is connected between a control electrode of the switching element and the output voltage detection circuit, and controls driving of the switching element on the basis of the output voltage detected by the output voltage detection circuit. The feedback circuit is connected between the control electrode and a second node located between the output voltage detection circuit and the control circuit, and includes a resistive element and a capacitive element.

[0012] Thus, it is possible to improve a phase margin of the open loop as a whole of the switching power supply circuit.

[0013] A semiconductor device according to a third aspect of the present invention includes an input terminal, an output terminal, a transformer, a switching element, an output voltage detection circuit, a control circuit and a feedback circuit. The transformer is connected between the input terminal and the output terminal. The switching element is connected to the transformer. The output voltage detection circuit detects an output voltage as a voltage of the output terminal. The control circuit is connected between a control electrode of the switching element and the output voltage detection circuit, and controls driving of the switching element on the basis of the output voltage detected by the output voltage detection circuit. The feedback circuit is connected between a first node located between the control electrode and the output voltage detection circuit and a second node located between the output voltage detection circuit and the control circuit, and includes a resistive element and a capacitive element.

[0014] Thus, it is possible to improve a phase margin of the open loop as a whole of the switching power supply circuit.

[0015] A semiconductor device according to a fourth aspect of the present invention includes an input terminal, an output terminal, a switching element, an output voltage detection circuit, a control circuit and a feedback circuit. The switching element is connected between the input terminal and the output terminal. The output voltage detection circuit detects an output voltage as a voltage of the output terminal. The control circuit is connected between a control electrode of the switching element and the output voltage detection circuit, and controls driving of the switching element on the basis of the output voltage detected by the output voltage detection circuit. The feedback circuit is connected between the control electrode and a node located between the output voltage detection circuit and the control circuit, and includes a resistive element and a capacitive element.

[0016] Thus, it is possible to improve a phase margin of the open loop as a whole of the switching power supply circuit.

[0017] A semiconductor device according to a fifth aspect of the present invention includes a first input terminal, a first output terminal, a first switching element, a first output voltage detection circuit, a control circuit and a feedback circuit. The switching element is connected between a first node located between the input terminal and the output terminal and a ground potential. The output voltage detection circuit detects an output voltage as a voltage of the output terminal. The control circuit is connected between a control electrode of the switching element and the output voltage detection circuit, and controls driving of the switching element on the basis of the output voltage detected by the output voltage detection circuit. The feedback circuit is connected between the control electrode and a second node located between the output voltage detection circuit and the control circuit, and includes a resistive element and a capacitive element.
age detection circuit, a first control circuit, a first feedback circuit, a second input terminal, a second output terminal, a second switching element, a second output voltage detection circuit, a second control circuit and a second feedback circuit. The first switching element is connected between the first input terminal and the first output terminal. The first output voltage detection circuit detects a first output voltage as a voltage of the first output terminal. The first control circuit is connected between a control electrode of the first switching element and the first output voltage detection circuit, and controls driving of the first switching element on the basis of the first output voltage detected by the first output voltage detection circuit. The first feedback circuit is connected between a first node as an output electrode of the first switching element and a second node located between the first output voltage detection circuit and the first control circuit, and includes a first resistive element and a first capacitive element. The second switching element is connected between a third node located between the second input terminal and the second output terminal and a ground potential. The second output voltage detection circuit detects a second output voltage as a voltage of the second output terminal. The second control circuit is connected between a control electrode of the second switching element and the second output voltage detection circuit, and controls driving of the second switching element on the basis of the second output voltage detected by the second output voltage detection circuit. The second feedback circuit is connected between the control electrode of the second switching element and a fourth node located between the second output voltage detection circuit and the second control circuit, and includes a second resistive element and a second capacitive element.

Thus, it is possible to improve a phase margin of the open loop as a whole of the switching power supply circuit.

These and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram showing a configuration of a conventional switching power supply circuit;
FIG. 2 is a circuit diagram showing a configuration of a switching power supply circuit according to an embodiment of the present invention, which corresponds to FIG. 1;
FIG. 3 is a block diagram functionally representing the switching power supply circuit shown in FIG. 2;
FIG. 4 is an open loop Bode diagram regarding the switching power supply circuit shown in FIG. 1 and the switching power supply circuit shown in FIG. 2;
FIG. 5 is a circuit diagram showing a configuration of a conventional switching power supply circuit;
FIG. 6 is a circuit diagram showing a configuration of a switching power supply circuit according to a first modification of the present invention, which corresponds to FIG. 5;
FIG. 7 is a circuit diagram showing a configuration of a conventional switching power supply circuit;
FIG. 8 is a circuit diagram showing a configuration of a switching power supply circuit according to a second modification of the present invention, which corresponds to FIG. 7;
FIG. 9 is a circuit diagram showing a configuration of a conventional switching power supply circuit;
FIG. 10 is a circuit diagram showing a configuration of a switching power supply circuit according to a third modification of the present invention, which corresponds to FIG. 9;
FIG. 11 is a circuit diagram showing a configuration of a conventional switching power supply circuit;
FIG. 12 is a circuit diagram showing a configuration of a switching power supply circuit according to a fourth modification of the present invention, which corresponds to FIG. 11;
FIG. 13 is a circuit diagram showing a configuration of a conventional switching power supply circuit;
FIG. 14 is a circuit diagram showing a configuration of a switching power supply circuit according to a fifth modification of the present invention, which corresponds to FIG. 13;
FIG. 15 is a circuit diagram showing a configuration of a conventional switching power supply circuit;
FIG. 16 is a circuit diagram showing a configuration of a switching power supply circuit according to a sixth modification of the present invention, which corresponds to FIG. 15;
FIG. 17 is a circuit diagram showing a configuration of a conventional switching power supply circuit;
FIG. 18 is a circuit diagram showing a configuration of a switching power supply circuit according to a seventh modification of the present invention, which corresponds to FIG. 17;
FIG. 19 is a circuit diagram showing a configuration of a switching power supply circuit according to an eighth modification of the present invention;
FIG. 20 is a circuit diagram showing a first configuration of a switching power supply circuit according to a ninth modification of the present invention;
FIG. 21 is a circuit diagram showing a second configuration of the switching power supply circuit according to the ninth modification of the present invention;
FIG. 22 is a top view schematically showing part of a layout pattern of an IC chip on which the switching power supply circuit according to the present invention is mounted; and
FIG. 23 is a sectional view showing a cross-sectional structure of a portion of the IC chip shown in FIG. 22, where a resistor and a capacitor are formed.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The semiconductor device according to the present invention is applicable to various electronic devices, in particular, portable devices such as a digital still camera (DSC) and a digital video camera (DVC), although not limited thereto, as a switching power supply with an input direct current voltage of the order of 1.5 to 4.2 V and an output direct current voltage of the order of -8 to +16 V.

In the following, embodiments of the semiconductor device according to the present invention will be specifically described by means of drawings, taking a switching power supply circuit as an example. It is to be noted that elements provided with the same one symbol in different drawings are equivalent or correspond to one another.

FIG. 1 is a circuit diagram showing a configuration of a conventional switching power supply circuit. FIG. 2 is a circuit diagram showing a configuration of a switching power supply circuit according to an embodiment of the present
invention, corresponding to FIG. 1. FIGS. 1 and 2 each show a step-down diode rectification switching power supply circuit.

[0046] Referring to FIG. 1, the conventional step-down diode rectification switching power supply circuit includes an input terminal 1, an output terminal 2, a terminal 34, a PMOS transistor 3a, a diode 4a, an inductor 5a (inductance L1), capacitors 6, 16, 17 (capacitances C1, C2, C3), resistors 7, 8, 18 (resistance values R1, R2, R3), an error amplifier 9, a power supply 10, a PWM comparator 11, a triangular wave oscillator 12, and a gate driver 13a.

[0047] An input voltage VIN as a direct current voltage is inputted into the input terminal 1. An output voltage VOUT as a direct current voltage is outputted from the output terminal 2. A gate electrode of the PMOS transistor 3a is connected to an output terminal of the gate driver 13a, a source electrode thereof is connected to the input terminal 1, and a drain electrode thereof is connected to a node N1a. An anode electrode of the diode 4a is connected to a ground potential (reference potential of the circuit), and a cathode electrode thereof is connected to the node N1a.

[0048] The inductor 5a is connected between the node N1a (the terminal 34) and the output terminal 2. The capacitor 6 is connected between the output terminal 2 and a ground potential. The resistor 7 is connected between the output terminal 2 and a node N2. The resistor 8 is connected between the node N2 and a ground potential. The capacitor C2 is connected between the output terminal 2 and the node N2, to constitute a phase compensation circuit 14.

[0049] A first input terminal (minus side) of the error amplifier 9 is connected to the node N2, a second input terminal (plus side) thereof is connected to the power supply 10, and an output terminal thereof is connected to a node N3. The power supply 10 is connected between the second input terminal of the error amplifier 9 and a ground potential, and outputs a predetermined reference voltage. The capacitor 17 is connected between the node N3 and the resistor 18. The resistor 18 is connected between the capacitor 17 and the node N2. The capacitor 17 and the resistor 18 constitute a phase compensation circuit 15.

[0050] A first input terminal (plus side) of the PWM comparator 11 is connected to the node N3, a second input terminal (minus side) thereof is connected to the triangular wave oscillator 12, and an output terminal thereof is connected to an input terminal of the gate driver 13a. An output terminal of the gate driver 13a is connected to the gate electrode of the PMOS transistor 3a.

[0051] Referring to FIG. 2, similar to the conventional switching power supply circuit shown in FIG. 1, the switching power supply circuit according to this embodiment also includes an input terminal 1, an output terminal 2, a terminal 34, a PMOS transistor 3a, a diode 4a, an inductor 5a, capacitors 6, 16, 17, resistors 7, 8, 18, an error amplifier 9, a power supply 10, a PWM comparator 11, a triangular wave oscillator 12, and a gate driver 13a. In addition to the configuration of the conventional switching power supply circuit, the switching power supply circuit according to this embodiment further includes a resistor 20 (resistance value R4) and a capacitor 21 (capacitance C4).

[0052] The resistor 20 is connected between the node N1a and the capacitor 21. The capacitor 21 is connected between the resistor 20 and the node N2. The resistor 20 and the capacitor 21 constitute a phase compensation circuit 19. The phase compensation circuit 19 improves a cut-off frequency of the open loop as a whole of the switching power circuit over a resonance frequency of the inductor 5a and the capacitor 6 by adjusting the resistance value R4 of the resistor 20 and the capacitance C4 of the capacitor 21. A feedback circuit, not including the inductor 5a and the capacitor 6 but including a serial connection of the resistor 20 and the capacitor 21 is connected between a drain electrode of the PMOS transistor 3a and a first input terminal of the error amplifier 9, to increase a phase margin of an open loop as a whole of the switching power supply circuit. Namely, addition of the phase compensation circuit 19 leads to phase progression, thereby to alleviate a phase change made due to the inductor 5a and the capacitor 6.

[0053] In the node N2, a partial voltage appears, which is obtained by division of the output voltage VOUT by the resistance values R1, R2 of the resistors 7, 8. Namely, the resistors 7, 8 function as an output voltage detection circuit for detecting the output voltage VOUT.

[0054] The error amplifier 9 amplifies an error between the partial voltage of the node N2 and the predetermined reference voltage inputted from the power supply 10, to output an error signal. The PWM comparator 11 generates a pulse signal a pulse width of which is modulated according to the error signal inputted from the error amplifier 9 and a triangular wave signal inputted from the triangular wave oscillator 12. The gate driver 13a controls drive of the PMOS transistor 3a, which is a switching element, based upon the pulse signal inputted from the PWM comparator 11. Thereby, the value of the output voltage VOUT is kept constant, to obtain a desired direct current voltage (VOUT) from the inputted direct current voltage (VIN). That is, the error amplifier 9, the PWM comparator 11, the power supply 10, the triangular wave oscillator 12 and the gate driver 13a function as a control circuit for controlling switching of the PMOS transistor 3a based upon the output voltage VOUT (strictly speaking, the partial voltage of the node N2) detected by the output voltage detection circuit including the resistors 7, 8.

[0055] FIG. 3 is a block diagram functionally representing the switching power supply circuit shown in FIG. 2. In FIG. 3, the PMOS transistor 3a shown in FIG. 2 is represented as a switching element 30. Further, the inductor 5a and the capacitor 6 which are shown in FIG. 2 are represented as a low-pass filter 31. The resistors 7, 8 which are shown in FIG. 2 are represented as an output voltage detection circuit 32. The error amplifier 9, the PWM comparator 11, the power supply 10, the triangular wave oscillator 12 and the gate driver 13a which are shown in FIG. 2 are represented as a control circuit 33. It is to be noted that, in FIG. 3, the phase compensation circuits 14, which are shown in FIG. 2 are not shown. In FIG. 3, a portion surrounded with a thick line 35 is a portion capable of integration as an IC. The input terminal 1 is connected to a direct current power supply 36. The output terminal 2 is connected to a load 37. The low-pass filter 31 is connected to a terminal 34.

[0056] FIG. 4 is an open loop Bode diagram regarding the conventional switching power supply circuit (conventional circuit) shown in FIG. 1 and the switching power supply circuit of this embodiment (circuit in the present invention) shown in FIG. 2. In the conventional circuit, a phase margin in the resonance frequency of the inductor 5a and the capacitor 6 is 0° or less. Namely, since the phase margin is small in the conventional circuit, it is likely that the output voltage VOUT oscillates due to an external parasitic LCR, and the output voltage VOUT is unstable. On the other hand, in the circuit in
the present invention, the phase margin in the resonance frequency of the inductor 5a and the capacitor 6 is about 52°, indicating significant improvement in phase margin as compared with the conventional circuit (see a region P in FIG. 4).

[0057] As shown in FIG. 2, according to the switching power supply circuit of this embodiment, the phase compensation circuit 19 including the serial connection of the resistor 20 and the capacitor 21 is connected between the drain electrode of the PMOS transistor 3a and the first input terminal of the error amplifier 9. Thereby, as apparent from the Bode diagram shown in FIG. 4, the phase margin of the open loop as a whole of the switching power supply circuit increases. This results in significant improvement in phase margin as compared with the conventional switching power supply circuit shown in FIG. 1, to allow stabilization of the output voltage VOUT as well as increase a response speed of the output voltage VOUT.

[0058] In the following, modifications of the present invention will be described. Also in all modifications described below, it is possible to obtain a similar effect to the switching power supply circuit according to the above-mentioned embodiment.

First Modification

[0059] FIG. 5 is a circuit diagram showing a configuration of a conventional switching power supply circuit. FIG. 6 is a circuit diagram showing a configuration of a switching power supply circuit according to a first modification of the present invention, corresponding to FIG. 5. FIGS. 5 and 6 each show a step-down synchronous rectification switching power supply circuit.

[0060] In the conventional switching power supply circuit shown in FIG. 5, an NMOS transistor 40a and a gate driver 41a are provided in place of the diode 4a in the conventional switching power supply circuit shown in FIG. 1. A gate electrode of the NMOS transistor 40a is connected to an output terminal of the gate driver 41a, a source electrode thereof is connected to a ground potential, and a drain electrode thereof is connected to a node 11a. An input terminal of the gate driver 41a is connected to an output terminal of the PWM comparator 11.

[0061] The switching power supply circuit according to the first modification of the present invention shown in FIG. 6 includes a phase compensation circuit 19 including a resistance 20 and a capacitor 21, in addition to the conventional switching power supply circuit shown in FIG. 5. As in the switching power supply circuit according to the embodiment of the present invention shown in FIG. 2, the resistor 20 is connected between the node 11a and the capacitor 21, and the capacitor 21 is connected between the resistor 20 and a node 12.

Second Modification

[0062] FIG. 7 is a circuit diagram showing a configuration of a conventional switching power supply circuit. FIG. 8 is a circuit diagram showing a configuration of a switching power supply circuit according to a second modification of the present invention, corresponding to FIG. 7. FIGS. 7 and 8 each show a step-up diode rectification switching power supply circuit.

[0063] Referring to FIG. 7, the conventional step-up diode rectification switching power supply circuit includes an NMOS transistor 36, a diode 46, an inductor 56, and a gate driver 13b. Similar to the conventional switching power supply circuit shown in FIG. 1, this conventional switching power supply circuit also includes an input terminal 1, an output terminal 2, capacitors 6, 16, 17, resistors 7, 8, 18, an error amplifier 9, a power supply 10, a PWM comparator 11, and a triangular wave oscillator 12.

[0064] The inductor 5b is connected between the input terminal 1 and a node 11b. A gate electrode of the NMOS transistor 5b is connected to an output terminal of the gate driver 13b, a source electrode thereof is connected to a ground potential, and a drain electrode thereof is connected to the node 11b. An input terminal of the gate driver 13b is connected to an output terminal of the PWM comparator 11. An anode electrode of the diode 4b is connected to the node 11b, and a cathode electrode thereof is connected to the output terminal 2.

[0065] The switching power supply circuit according to the second modification of the present invention shown in FIG. 8 includes a phase compensation circuit 19 including a resistor 20 and a capacitor 21, in addition to the conventional switching power supply circuit shown in FIG. 7. The resistor 20 is connected between the gate electrode of the NMOS transistor 3b and the capacitor 21, and the capacitor 21 is connected between the resistor 20 and a node 22.

Third Modification

[0066] FIG. 9 is a circuit diagram showing a configuration of a conventional switching power supply circuit. FIG. 10 is a circuit diagram showing a configuration of a switching power supply circuit according to a third modification of the present invention, corresponding to FIG. 9. FIGS. 9 and 10 each show a step-up synchronous rectification switching power supply circuit.

[0067] In the conventional switching power supply circuit shown in FIG. 9, a PMOS transistor 40b and a gate driver 41b are provided in place of the diode 4b in the conventional switching power supply circuit shown in FIG. 7. A gate electrode of the PMOS transistor 40b is connected to an output terminal of the gate driver 41b, a source electrode thereof is connected to a node 11b, and a drain electrode thereof is connected to the output terminal 2. An input terminal of the gate driver 41b is connected to an output terminal of the PWM comparator 11.

[0068] The switching power supply circuit according to the third modification of the present invention shown in FIG. 10 includes a phase compensation circuit 19 including a resistor 20 and a capacitor 21, in addition to the conventional switching power supply circuit shown in FIG. 9. As in the switching power supply circuit according to the second modification of the present invention shown in FIG. 8, the resistor 20 is connected between the gate electrode of the NMOS transistor 3b and the capacitor 21, and the capacitor 21 is connected between the resistor 20 and a node 22.

Fourth Modification

[0069] FIG. 11 is a circuit diagram showing a configuration of a conventional switching power supply circuit. FIG. 12 is a circuit diagram showing a configuration of a switching power supply circuit according to a fourth modification of the present invention, corresponding to FIG. 11. FIGS. 11 and 12 each show a step-up/down diode rectification switching power supply circuit.
Referring to FIG. 11, similar to the conventional switching power supply circuit shown in FIG. 1, the conventional step-up/down diode rectification switching power supply circuit includes an input terminal 1, an output terminal 2, a PMOS transistor 3a, a diode 4a, an inductor 5a, capacitors 6, 16, 17, resistors 7, 8, 18, an error amplifier 9, a power supply 10, a PWM comparator 11, a triangular wave oscillator 12, and a gate driver 13a. Similar to the conventional switching power supply circuit shown in FIG. 7, this conventional switching power supply circuit in the fourth modification also includes an NMOS transistor 3b, a diode 4b, and a gate driver 13b.

The switching power supply circuit according to the fourth modification of the present invention shown in FIG. 12 includes a phase compensation circuit 19 including a resistor 20 and a capacitor 21, in addition to the conventional switching power supply circuit shown in FIG. 11. As in the switching power supply circuit according to the embodiment of the present invention shown in FIG. 2, the resistor 20 is connected between a node N1a and the capacitor 21, and the capacitor 21 is connected between the resistor 20 and a node N2.

Fifth Modification

FIG. 13 is a circuit diagram showing a configuration of a conventional switching power supply circuit. FIG. 14 is a circuit diagram showing a configuration of a switching power supply circuit according to a fifth modification of the present invention, corresponding to FIG. 13. FIGS. 13 and 14 each show a step-up/down synchronous rectification switching power supply circuit.

In the conventional switching power supply circuit shown in FIG. 13, an NMOS transistor 40a and a gate driver 41a are provided in place of the diode 4a in the conventional switching power supply circuit shown in FIG. 11. Further, a PMOS transistor 40b and a gate driver 41b are provided in place of the diode 4b in the conventional switching power supply circuit shown in FIG. 11.

As in the conventional switching power supply circuit shown in FIG. 5, a gate electrode of the NMOS transistor 40a is connected to an output terminal of the gate driver 41a, a source electrode thereof is connected to a ground potential, and a drain electrode thereof is connected to a node N1a. An input terminal of the gate driver 41a is connected to an output terminal of the PWM comparator 11. Further, as in the conventional switching power supply circuit shown in FIG. 9, a gate electrode of the PMOS transistor 40b is connected to an output terminal of the gate driver 41b, a source electrode thereof is connected to a node N1b, and a drain electrode thereof is connected to the output terminal 2. An input terminal of the gate driver 41b is connected to the output terminal of the PWM comparator 11.

The switching power supply circuit according to the fifth modification of the present invention shown in FIG. 14 includes a phase compensation circuit 19 including a resistor 20 and a capacitor 21, in addition to the conventional switching power supply circuit shown in FIG. 13. As in the switching power supply circuit according to the fourth modification of the present invention shown in FIG. 12, the resistor 20 is connected between the node N1a and the capacitor 21, and the capacitor 21 is connected between the resistor 20 and a node N2.

Sixth Modification

FIG. 15 is a circuit diagram showing a configuration of a conventional switching power supply circuit. FIG. 16 is a circuit diagram showing a configuration of a switching power supply circuit according to a sixth modification of the present invention, corresponding to FIG. 15. FIGS. 15 and 16 each show a flyback-type switching power supply circuit.

Referring to FIG. 15, the conventional flyback-type switching power supply circuit includes a transformer 5c and, similar to the conventional switching power supply circuit shown in FIG. 7, an input terminal 1, an output terminal 2, an NMOS transistor 36, a diode 4b, a gate driver 13b, capacitors 6, 16, 17, resistors 7, 8, 18, an error amplifier 9, a power supply 10, a PWM comparator 11, and a triangular wave oscillator 12. Namely, in the example of the conventional switching power supply circuit shown in FIG. 15, a transformer 5c is provided in place of the inductor 5b shown in FIG. 7.

The switching power supply circuit according to the sixth modification of the present invention shown in FIG. 16 includes a phase compensation circuit 19 including a resistor 20 and a capacitor 21, in addition to the conventional switching power supply circuit shown in FIG. 15. The resistor 20 is connected between a node N1b located between the gate electrode of the NMOS transistor 36 and the gate driver 13b and the capacitor 21. The capacitor 21 is connected between the resistor 20 and a node N2.

Seventh Modification

FIG. 17 is a circuit diagram showing a configuration of a conventional switching power supply circuit. FIG. 18 is a circuit diagram showing a configuration of a switching power supply circuit according to a seventh modification of the present invention, corresponding to FIG. 17. FIGS. 17 and 18 each show an inverter-type switching power supply circuit.

Referring to FIG. 17, the conventional inverter-type switching power supply circuit includes a PMOS transistor 3c, an inductor 5c, a diode 4c, and a gate driver 13c. Similar to the conventional switching power supply circuit shown in FIG. 1, this switching power supply circuit also includes an input terminal 1, an output terminal 2, capacitors 6, 16, 17, resistors 7, 8, 18, an error amplifier 9, a power supply 10, a PWM comparator 11, and a triangular wave oscillator 12.

A gate electrode of the PMOS transistor 3c is connected to an output terminal of the gate driver 13c, a drain electrode thereof is connected to the input terminal 1, and a source electrode thereof is connected to a node N1c. An input terminal of the gate driver 13c is connected to an output terminal of the PWM comparator 11. An anode electrode of the diode 4c is connected to the output terminal 2, and a cathode electrode thereof is connected to the node N1c. The inductor 5c is connected between the node N1c and a ground potential.

FIG. 19 is a circuit diagram showing a configuration of a switching power supply circuit according to an eighth modification of the present invention. The switching power
supply circuit according to the eighth modification of the present invention is constituted such that the step-down synchronous rectification switching power supply circuit shown in FIG. 6 and the step-up synchronous rectification switching power supply circuit shown in FIG. 10 are mounted within the same one IC chip.

**[0084]** The step-down synchronous rectification switching power supply circuit includes an input terminal I₁, an output terminal 2, a PMOS transistor 3a, an NMOS transistor 40a, an inductor 5a, capacitors 6, 16, 17, 21, resistors 7, 8, 18, 20, an error amplifier 9, a power supply 10, a PWM comparator 11, a triangular wave oscillator 12, gate drivers 13a, 41a, a DTC (Dead Time Controller) 50, an AND circuit 51, and a control circuit 52. The resistor 20, and the capacitor 21, constitute a phase compensation circuit 19.

**[0085]** The step-up synchronous rectification switching power supply circuit includes an input terminal I₁, an output terminal 2, an NMOS transistor 3b, a PMOS transistor 40b, an inductor 5b, capacitors 6, 16, 17, 21, resistors 7, 8, 18, 20, an error amplifier 9, a power supply 10, a PWM comparator 11, a triangular wave oscillator 12, gate drivers 13b, 41b, a DTC 50, an AND circuit 51, and a control circuit 52. The resistor 20, and the capacitor 21, constitute a phase compensation circuit 19.

**[0086]** It is to be noted that the gate drivers 13a, 13b, 41a, 41b may be switching elements such as MOS transistors or bipolar transistors.

**[0087]** Since connection relationships among each element in the circuit shown in FIG. 19 are basically similar to those among each element in the circuits shown in FIGS. 6 and 10, specific descriptions thereof are omitted here. It is to be noted that the DTC 50 and the AND circuit 51, 52, perform a control for periodically turning off the PMOS transistors 3a, 40b and the NMOS transistors 3b, 40a. Further, the control circuit 52, performs a control for making the timing for switching on/off of the NMOS transistor 3b disagree with the timing for switching on/off of the PMOS transistor 40b. Similarly, the control circuit 52 performs a control for making the timing for switching on/off of the PMOS transistor 3a disagree with the timing for switching on/off of the NMOS transistor 40a.

**[0088]** It is to be noted that, although the combination of the circuit shown in FIG. 6 and the circuit shown in FIG. 10 is described above, the combination is not limited thereto. It is possible to arbitrarily combine the circuits respectively shown in FIGS. 2, 6, 8, 10, 12, 14, 16 and 18.

**Ninth Modification**

**[0089]** FIG. 20 is a circuit diagram showing a first configuration of a switching power supply circuit according to a ninth modification of the present invention, corresponding to FIG. 2. In the circuit shown in FIG. 20, the connection order of a resistor 20 and a capacitor 21 is opposite to that in the circuit shown in FIG. 2. Namely, in a phase compensation circuit 19a shown in FIG. 20, the capacitor 21 is connected to a node N2 through the resistor 20. On the other hand, in the phase compensation circuit 19 shown in FIG. 2, the resistor 20 is connected to the node N2 through the capacitor 21.

**[0090]** FIG. 21 is a circuit diagram showing a second configuration of a switching power supply circuit according to the ninth modification of the present invention, corresponding to FIG. 2. In the circuit shown in FIG. 21, resistors 20a, 20b are respectively connected to each side of a capacitor 21. Namely, in a phase compensation circuit 19b shown in FIG. 21, a resistor 20a is connected to a node N2 through the capacitor 21 and the resistor 20b.

**[0091]** As thus described, the phase compensation circuit 19a shown in FIG. 20 or the phase compensation circuit 19b shown in FIG. 21 may be used in place of the phase compensation circuit 19 shown in FIG. 2. This applies to the phase compensation circuits 19 respectively shown in FIGS. 6, 8, 10, 12, 14, 16 and 18, and the phase compensation circuits 19, 19, shown in FIG. 19.

**[0092]** However, in cases including a case where a gate capacitor of a transistor constitutes a capacitor C4, a desirable configuration from the viewpoint of enhancing surge withstand capability to protect the circuit is made by arrangement of a resistor R4 and the capacitor 21 in this order seen from the input terminal 1. Namely, the phase compensation circuits 19 shown in FIG. 2 and the like and the phase compensation circuit 19b shown in FIG. 21 are preferred for the phase compensation circuit 19a shown in FIG. 20.

**First Embodiment**

**[0093]** In the following, the step-down synchronous rectification switching power supply circuit shown in FIG. 6 is taken as an example, and respective specific numerical values of the resistance values R3, R4 of the resistors 18, 20, capacitances C1, C3, C4 of the capacitances 6, 17, 21, and the inductance L1 of the inductor 5a will be described.

**[0094]** Respective desirable ranges of the resistance value R4, the capacitances C1, C4 and the inductance L1 change according to an oscillation frequency of the triangular wave oscillator 12. The oscillation frequency of the triangular wave oscillator 12 is in the range of 500 Hz to several MHz. In this case, the desirable range of the resistance value R4 is from 10 to 1000 kΩ, the desirable range of the capacitance C1 is from 1 to 100 μF, the desirable range of the capacitance C4 is from 1 to 1000 pF, and the desirable range of the inductance L1 is from 0.1 to 100 μH.

**[0095]** Specifically, when the oscillation frequency of the triangular wave oscillator 12 is 1 MHz, the desirable range of the resistance value R4 is from 10 to several hundreds kΩ, and the desirable range of the capacitance C1 is from 1 to several tens μF, the desirable range of the capacitance C4 is from 1 to several hundreds pF, and the desirable range of the inductance L1 is from 0.1 to several μH.

**[0096]** Further, the desirable range of the resistance value R3 is from several to several tens kΩ, and the desirable range of the capacitance C3 is from several to several tens pF. Therefore, a difference between the order (10⁵ to 10⁶) of the resistance value R3 and the order (10⁴ to 10⁵) of the resistance value R4 is within two digits, and a difference between the order (10⁻¹² to 10⁻¹¹) of the capacitance C3 and the order (10⁻⁹ to 10⁻⁸) of the capacitance C4 is within two digits.

**[0097]** When the resistance value R3 and the capacitance C3 become extremely small as compared with the resistance value R4 and the capacitance C4, the effect due to the phase compensation circuit 15 cannot be obtained. Such a problem can be avoided by setting the resistance values R3, R4 and the capacitances C3, C4 such that the above-mentioned order differences are within two digits.

**[0098]** It is to be noted that, although specific numerical values of the resistance values R3, R4, the capacitances C1, C3, C4, and the inductances L1 are described above taking the circuit shown in FIG. 6 as an example, similar numerical
values can be applied to the respective circuits shown in FIGS. 2, 8, 10, 12, 14, 16, 18 and 19.

Second Embodiment

[0099] FIG. 22 is a top view schematically showing part of a layout pattern of an IC chip on which the switching power supply circuit according to the present invention is mounted. In a predetermined region of a silicon substrate 100, an error amplifier 9, resistors 18, 20, and capacitors 17, 21 are formed. [0100] Further, FIG. 23 is a sectional view showing a cross-sectional structure of a portion of an IC chip shown in FIG. 22, where the resistor 20 and the capacitor 21 are formed. N-type wells 101, 102 are partially formed within the top face of a P-type silicon substrate 100. A P*-type impurity diffusion layer 103 which functions as the resistor 20 is partially formed within the top face of the well 101. A gate insulating film 104, made of silicon oxide or the like, is partially formed on the top face of the well 102. A gate electrode 105, made of polysilicon or the like, is formed on the gate insulating film 104. The gate electrode 105, the gate insulating film 104, and the well 102 function as the capacitor 21.

[0101] While the invention has been shown and described in detail, the foregoing description is in all aspects illustrative and not restrictive. It is therefore understood that numerous modifications and variations can be devised without departing from the scope of the invention.

1-16. (canceled)
17. A switching power supply circuit comprising:
an input terminal;
an output terminal;
a NMOS transistor whose source electrode is connected to a ground potential, drain electrode is connected to a first node, and gate electrode is connected to an output terminal of a gate driver, wherein said first node is located between said drain electrode and said output terminal; an output voltage detection circuit which detects an output voltage as a voltage of said output terminal; a control circuit which is connected between said gate electrode of said NMOS transistor and said output voltage detection circuit, and controls driving of said NMOS transistor on the basis of said output voltage detected by said output voltage detection circuit; and a feedback circuit which is connected between said gate electrode of said NMOS transistor and a second node located between said output voltage detection circuit and said control circuit, and includes a resistive element and a capacitive element, wherein said control circuit comprises:
an error amplifier whose first input node is connected to said second node and whose output is connected to a third node;
a power supply connected between a second input node of the error amplifier and a ground potential;
a pulse width modulator comparator with a first input connected to said third node, a second input node connected to a triangular wave oscillator, and whose output is connected to the input of said gate driver, wherein said resistive element is connected between said gate electrode of said NMOS transistor and said capacitive element, and said capacitive element is connected between said resistive element and said first input node of said error amplifier, and wherein said control circuit includes a phase compensation circuit being connected between said input node of the error amplifier and an output node of the error amplifier via said third node.

18. The switching power supply circuit according to claim 17, wherein said resistive element is connected to said second node through said capacitive element.
19. The switching power supply circuit according to claim 17, wherein said phase compensation circuit includes a resistive element and a capacitive element, a difference between the order of a resistance value of said resistive element in said feedback circuit and the order of a capacitance value of said capacitive element in said phase compensation circuit is within two digits, and a difference between the order of a capacitance of said capacitive element in said feedback circuit and the order of a capacitance of said capacitive element in said phase compensation circuit is within two digits.

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