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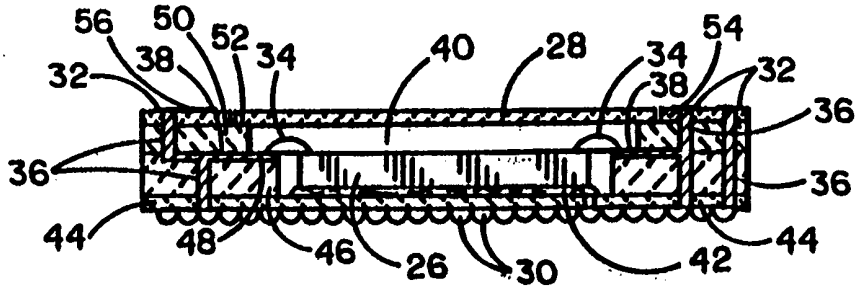

(57) Abstract

A structure and process are disclosed in which IC chip–containing layers are stacked to create electronic density. Each layer is formed with a cavity (42) in which at least one IC chip (26) is placed, electrically connected, and then covered to enclose the chip. Full tests to establish known good quality are performed on individual layers containing enclosed chips. Within each layer horizontal conducting traces connect with conductor–containing vias (36), in order to carry electrical signals vertically from layer to layer, and also to connect to a ball grid array on the bottom of the stack, the entire surface of which is available for I/O ports.

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Stacking Layers Containing Enclosed IC Chips

This application claims the benefit of U.S. Provisional Application No. 60/049,025, filed June 9, 1997; and U.S. Provisional Application No. 60/049,026, filed June 9, 1997.

Background of the Invention

This invention relates to the stacking of layers containing IC chips, thereby obtaining high density electronic circuitry. In general, the goal of the present invention is to combine high circuit density with reasonable cost. Cost reduction involves (a) relatively low cost initial forming of layers, (b) ability to use simple layer-testing techniques, and (c) effective ways of guaranteeing that defective layers will not be included in the stacks.

Another aspect of successful stacking of chip-containing layers is the availability of large numbers of input/output (I/O) terminals (or pads) for connecting the stack to external circuitry.

In most of the extensive prior art disclosures, the leads from the chip-embedded IC circuitry are brought out at one or more sides of the stack, i.e., at the periphery of the stacked layers. Some packages bring conductors from the IC circuitry through vertical vias extending to the bottom of the package, permitting the use of I/O pads on the bottom of the package, i.e., ball grid arrays of terminals on a single flat surface.

Hayden et al Patent No. 5,579,207 shows a structure in which stacked chip-enclosing layers have vertically-extending vias serving as conductors between the IC chips and a plurality of pads on the top and bottom of the stack. Each layer substrate (chip carrier) in the Hayden et al patent has an IC chip mounted on its upper surface, and a cavity formed in its lower surface, which provides space for the IC chip on the layer below. The layers are separately formed and then stacked, using flat sealing strips around the peripheral edge between adjacent layers to provide sealing of the cavities, i.e., sealing occurs as a result of stacking. Because the Hayden et al patent extends the IC chip mounted on one carrier into the cavity of the next carrier, it is not possible to pretest the individual carriers as sealed, or covered, units.

What is not available in the prior art is a stack of IC-chip-containing layers which can

be fully tested individually prior to stacking, and can connect the chip circuitry through vias to a ball grid array at the bottom of the stack, which array may if desired have terminals located at points throughout the full planar surface.

Summary of the Invention

This application discloses two versions of fully pre-testable chip-containing layers, which can be stacked and have the chips electrically connected to a ball grid array on the bottom of the stack. One version, which is hermetically sealed, uses ceramic as the dielectric body material which provides the chip-containing cavity in each layer. The other version uses polyimide as the dielectric body material which provides the chip-containing cavity in each layer. In each version the individual layers are proved to be "known good" parts before stacking.

In each version, the dielectric layer material is laminated, so that electrical conductors (traces) can extend horizontally inside the dielectric material and be connected by wire bonding to I/O terminals on the chip die. Vias containing vertical conductors are formed in each stacked layer, which vias extend from top to bottom of the layer and intersect the appropriate horizontal traces. The vias also provide electrical conduction to an array of terminals located on the bottom of one layer, which terminals engage aligned terminals located on the top of the next layer.

Each layer is completed and enclosed before stacking, with the IC chip or chips inside the cavity, and covered on top either by a lid in a ceramic layer, or by epoxy which fills the cavity of a polyimide layer. Therefore, in order to provide good stack test yields and stack integrity, each enclosed chip may be conventionally tested and prepared prior to stacking of the layers, including:

(a) Tested at extreme temperatures (e.g., minus 55°C, plus 125°C);

(b) Burned in (both temperature and bias); and

(c) Environmentally screened (i.e., temperature cycle, thermal shock, humidity, bias).

If necessary, because the stack consists of completed IC packages, the stack can be

conventionally reworked to remove defective layers, without compromising the integrity of the IC chips themselves.

The availability of the full bottom surface of the stack for terminals, and the virtually unlimited vertical interconnections, allow for a very high input/output (I/O) count to accommodate the needs of the stacked ICs.

Brief Description of the Drawings

Figures 1-3 show, respectively, top, side, and bottom views of a stack of ceramic IC chip-enclosing layers;

Figures 4-7 show, respectively, top, side, bottom, and vertical cross-section views of a single ceramic chip-enclosing layer.

Figures 8-10 show, respectively, top, side, and bottom views of a stack of polyimide IC chip-enclosing layers;

Figures 11-14 show, respectively, top, side, bottom, and vertical cross-section views of a single polyimide chip-enclosing layer;

Figures 15-17 show, respectively, vertical-cross-section, top, and bottom views of the lower layer of a two-layer stack; and

Figures 18-19 show, respectively, vertical cross-section, and top views of the two-layer stack.

Detailed Description of Specific Embodiments

Figures 1-7 relate to the ceramic version of the invention; and Figures 8-14 relate to the polyimide version of the invention.

Figures 1-3 show a stack 20 of ceramic packages (or layers) 22, each of which encloses one or more IC chips. Four ceramic layers 22 are seen in Figure 2; the number of layers can be varied as desired. The layer-enclosed semiconductor integrated circuits (ICs) are electrically and mechanically interconnected in the vertical direction. The end user of this stack will connect it to a substrate, such as a printed circuit board (PCB). The vertical placement of ICs will save considerable substrate area as opposed to conventional horizontal

placement of an equivalent number of ICs on the substrate. Electrical and mechanical interconnection between adjacent layers is accomplished by solder connections 24.

Figures 4-7 show views of a single layer. It is desirable from an economic standpoint to use identical layer structures, whenever feasible. The use of ceramic material to enclose the IC chips permits each layer and the stack of layers to be hermetically sealed. Each layer in the ceramic stack comprises a hermetically sealed co-fired multi-lamination ceramic layer 22 containing an IC chip die 26 attached and wire bonded within the package cavity. A lid 28 attached over this cavity provides a hermetic seal. The bottom surface of each ceramic package has an array 30 of metal bumps or balls called a ball grid array (BGA). The top surface of each ceramic package has a mechanically corresponding array of metal pads or lands 32 called a land grid array (LGA). Wire bonding 34 (see Fig. 7) accomplishes electrical connection from IC chip bond pads to the package bond pads. Buried conductors within the ceramic package route the electrical connections from the package bond pads to either the balls 30 on the bottom surface of the package, or the lands 32 on the top surface of the package, or to both balls 30 and lands 32, by virtue of vias 36 connecting the buried conductors to the balls and/or lands. In the case of a dual ball and land connection, the ball and land need not be vertically aligned, thus allowing for electrical routing flexibility in the vertical direction within the stack when assembled.

The ceramic body of each layer is formed by lamination of horizontal layers on top of one another, as seen in Figures 5 and 7. The laminating process permits various metal conductors, or traces, 38 to be formed which lead from the wire bonds 34 to the vertical vias 36. The traces 38 are formed during the co-firing process. The vias 36 are formed by creating holes, and conductive material is inserted into the vias usually in the form of cylindrical conductors, but the conductors may fill the vias. The laminated ceramic package is formed with a cavity 40, in which the IC chip 26 is placed and bonded to the bottom of the cavity by die attach material 42. The wire bonds 34 are then formed leading from terminals on the chip to aligned traces 38, which in turn lead to the appropriate via conductors 36.

As seen in Figure 7, there are at least four flat ceramic laminations in the ceramic layer. The lower lamination 44 extends across the entire layer. Successive laminations above

the bottom of the layer are open-centered, and are designed to provide exposed shelves for the wire bond terminals, and for the outer edge of lid 28. The layer 46 above layer 44 provides a shelf 48 for the traces 38 to which the wire bonds 34 are connected. The layer 50 above layer 46 provides a shelf 52 against which lid 28 engages. The top layer 54 provides a surface 56 on which are located the terminals (or lands) which constitute the land grid array (LGA).

The use of a ball grid array on the bottom of each layer and a land grid array on the top of each layer permits adjacent layers to be bonded together, because the balls protrude far enough to engage the much thinner lands, compensating for any surface unevenness. An example of relative ball and land thickness would be a 5 mil vertical thickness of the balls and a 1 mil vertical thickness of the lands. The arrangement could be reversed, with the lands on the bottom and the balls on the top. However, the relatively thick terminals are preferably on the bottom for convenience in testing.

The stack of layers shown in Figures 1-3 shows the solder connections 24 between layers, in which the aligned ball and land terminals are soldered together. Figure 3 shows a bottom array of terminals 30, (I/O ports) which do not extend into the center area of the bottom layer. The entire area is available for terminals 30, if desired (see Figure 17). In a stack of identical layers, e.g., all memory chips, it is easier to manufacture a bottom layer which is identical with the other layers.

However, if the bottom layer encloses a chip, or chips, having higher density I/O requirements, such as an ASIC or microprocessor, the entire bottom surface, including center portion 58, is available for terminals connecting to external circuitry, e.g., terminals on a PC board. In that case, the bottom layer would differ from the other layers, and would have a trace-supporting lamination below the chip-supporting lamination.

The following is a process flow list of steps in manufacturing the layers and stack using ceramic enclosures:

- Die attach die to package
- Wire bond die pads to package bond pads
- Seal metal or ceramic lid to package

- Environmentally screen to verify package integrity and hermeticity
- Electrically test package
- Apply a high melting point solder to BGA pads on one or both sides of each package
- Stack packages and reflow solder
- Electrically test stack

Figures 8-14 relate to the polyimide version of the invention, which is generally similar to the ceramic version shown in Figures 1-7. The polyimide version does not permit hermetic sealing because of the porous nature of the material. Figures 8-10 show a stack 60 of polyimide packages (or layers) 62, each of which encloses one or more IC chips 64 (see Figure 14). The layer-enclosed semiconductor integrated circuits (ICs) are electrically and mechanically interconnected in the vertical direction.

Figures 11-14 show views of a single layer enclosed by polyimide. A difference from the ceramic enclosed layer is that epoxy 66 is used to cover the encapsulated IC chip 64. No lid is needed to enclose the chip.

As in the ceramic version, four polyimide layers 62 are seen in Figure 9; the number of layers can be varied as desired. The layer-enclosed semiconductor integrated circuits (ICs) are electrically and mechanically interconnected in the vertical direction. The end user of this stack will connect it to a substrate, such as a printed circuit board (PCB). Electrical and mechanical interconnection between adjacent layers is accomplished by solder connections 68.

Each layer 62 is formed of at least two laminations of polyimide material. The bottom lamination 70 extends across the entire layer. The upper lamination 72 is open-centered (i.e., provides a cavity) so that the IC chip can be secured by die attach material 74 to the surface 76 of layer 70 and can have its terminals attached by wire bonds 78 to conductors (traces) 80 formed on the surface 76. Vias 82 having conductive material 84 are used to provide vertical conduction, some via conductors functioning as up/down connect vias, some as through vias, and some as re-route connection vias.

After the IC chip has been installed in the cavity and the conductors have been

connected, liquid epoxy is dispensed into the cavity to provide environmental protection for the IC chip. As in the ceramic version, terminals 86 are provided on the bottom of each layer, and terminals 88 are provided on the top of each layer.

The individual chip carrier packages 62 having the IC chip electrical functions are brought out to the top surface and/or the bottom surface of the package and prepared for stacking by printing or dispensing a high melting temperature solder paste on each ball and/or land. The melting point of solder should be high enough such that it will not reflow when the end user solders and stack to the substrate. The individual chip carrier packages can then be stacked such that each land on the top surface of each package is aligned with a corresponding ball on the bottom surface of the next higher package. All of the ball-to-land solder connections can be made simultaneously by reflowing the solder in a convection, or vapor phase reflow furnace. The stack so assembled may be soldered to a substrate by the end user. Leads or pins will not be required for stress relief between the stack and the substrate since the coefficient of thermal expansion (CTE) of the polyimide chip carrier is very close to the CTE of most all PCB substrates.

The following is a process flow list of steps in manufacturing the layers and stack using polyimide enclosures:

- Die attach die to package
- Wire bond die pads to package bond pads
- Fill die cavity with epoxy
- Electrically test package
- Apply a high melting point solder to BGA pads on one or both sides of each package
- Stack packages and reflow solder
- Electrically test stack

Figures 15-19 show a two-layer stack comprising a lower layer enclosing a non-memory IC chip, and an upper layer enclosing a memory chip in a thin small outline package (TSOP), which is an off-the-shelf commercially available enclosed IC chip. Figures 15 and 16 are, respectively, a vertical cross-section and a plan view of the lower layer. Figure 17 is

a view of the bottom of the lower layer.

As seen in Figures 15 and 16, the lower layer 100 has a container 102 formed of a suitable material, e.g., polyimide. It has a cavity 104 formed by its lower wall 106 and its side walls 108. Inside cavity 104 a non-memory (e.g., ASIC, microprocessor) IC chip 110 is secured to the surface 112 of lower lamination 114. A second lamination 116 provides a wire bond shelf 118 having conductors on the shelf connected by wire bonds 120 to the terminals on IC chip 110. A top lamination 122 supports a multiplicity of terminals 124 to which conductors from the TSOP are connected (soldered).

Epoxy 126 is used to fill cavity 104 and to cover the chip 110 and its electrical connections. Horizontal conductors (traces) and vertical via conductors are used in the same manner as in the other embodiments. The internal conductors lead to terminals 128 on the bottom of layer 100. In order to accommodate a large number of I/O ports, the bottom layer 100, which is shown in Figure 17, has an array of terminals 128 located throughout the area of the bottom surface. The horizontal conductors leading to the terminals 128 may be formed on the surface 112 of lower lamination 114.

Figure 16 shows terminals 130 formed on the IC chip 110, which terminals are connected by wire bonds to terminals 132 formed on wire bond shelf 118. Figure 16 also shows the terminals 124 which are connected to terminals on the TSOP layer.

Figures 18 and 19 are, respectively, a vertical cross-section and a plan view of the two-layer stack. A standard off-the-shelf memory TSOP 140, which contains an IC memory chip, is mounted above the non-memory layer 100, and is both supported by, and electrically connected by, a multiplicity of leads 142, each of which is connected to a separate one of the terminals 124 formed on the upper surface of lower layer 100.

The TSOP has been fully tested by its supplier. The lower layer 100 is fully tested before the two layers are interconnected. The reason for leaving a space between the top of lower layer 100 and the TSOP (about a 10 mil gap) is to permit cleaning out of any flux which remains after processing the two-layer stack.

From the foregoing description, it will be apparent that the device and method disclosed in this application will provide the significant functional benefits summarized in the

introductory portion of the specification.

The following claims are intended not only to cover the specific embodiments disclosed, but also to cover the inventive concepts explained herein with the maximum breadth and comprehensiveness permitted by the prior art.

What Is Claimed Is:

1. A stack of IC chip-enclosing layers, comprising:

a lower layer having a dielectric body providing a cavity and having via conductors in its wall which electrically connect the top and bottom surfaces of the lower layer;

an IC chip inside the cavity having I/O terminals thereon;

means for sealing the cavity to permit testing to establish known good quality of the layer prior to stacking;

terminals located on the bottom surface of the layer adapted to be connected to external circuitry;

electrical connections between the chip terminals and the terminals on the bottom surface of the layer;

a second pre-tested layer supported on the top of the lower layer;

an IC chip enclosed in the second layer; and

electrical connections from the IC chip in the second layer to the via conductors in the wall of the lower layer.

2. The structure of claim 1 in which:

the IC chip enclosed in the lower layer is a non-memory chip; and

the IC chip enclosed in the second layer is a memory chip.

3. The structure of claim 2 which also includes:

terminals on the top of the lower layer which are located along its periphery;

terminals along the periphery of the second layer; and

conducting wires connected between the terminals on the second layer and the terminals on the lower layer, which wires support the second layer with space between it and the upper surface of the lower layer.

4. The structure of claim 1 in which the terminals on the bottom surface of the

lower layer provide an array of terminals located throughout substantially the full area of said surface.

5. A stack of IC chip-enclosing layers, each comprising:

a dielectric body providing a cavity and having via conductors in its cavity-enclosing wall which are electrical connections between the top and bottom surfaces of the layer;

an IC chip inside the cavity having I/O terminals thereon;

means above the chip for closing the cavity in order to permit layer testing to establish known good quality of the layer prior to stacking;

terminals located on the top surface of the layer;

terminals located on the bottom surface of the layer;

electrical connections between the I/O terminals on the IC chip and the terminals on the bottom of the layer; and

means for electrically connecting terminals on each layer to terminals on the next layer in the stack.

6. The structure of claim 5 in which:

the dielectric body of each layer is ceramic; and

a cover is mounted over the cavity to hermetically seal the IC chip enclosure.

7. The structure of claim 5 in which:

the dielectric body of each layer is polyimide; and

epoxy material is located above the IC chip to close the cavity.

8. The structure of claim 5 in which:

the electrical connections in each layer include horizontal conductor traces connecting the I/O terminals on the enclosed IC chip to the via conductors.

9. The structure of claim 5 in which:

the dielectric body of each layer includes a plurality of laminations; and

horizontally-extending conductors are located between adjacent laminations.

10. The structure of claim 5 in which the bottom surface of the bottom layer in the stack of layers has an array of I/O terminals located throughout substantially the full area of said surface.

11. A method for manufacturing a layer ready for stacking with other layers in order to provide a dense electronic package, comprising the steps of:

forming a layer having a dielectric body providing a cavity, said body having a plurality of vertically-extending vias in which conductors are formed, and further having a plurality of horizontally-extending conductors embedded therein;

placing inside the cavity an IC-chip having I/O terminals;

connecting the I/O terminals of the IC chip with the horizontally-extending conductors;

forming a plurality of electrically conducting connections between individual horizontally-extending conductors and individual vertically-extending conductors;

closing the cavity to cover the IC chip and the conductors formed in the dielectric body; and

providing I/O terminals on the bottom of the layer to connect the IC circuitry to external circuitry.

12. The method of claim 11 which also comprises:

stacking a plurality of the layers; and

electrically interconnecting conductors in each layer with conductors in the adjacent layer.

13. The method of claim 12 in which the bottom surface of the bottom layer of the stack is provided with an array of I/O terminals located substantially throughout its area.

14. The method of claim 12 which also comprises:

testing , prior to stacking, for performance of the circuitry in each layer to establish the layer as a known good element.

15. The method of claim 14 in which the performance testing includes testing at extreme temperatures, burning-in at elevated temperatures, testing through thermal cycles and thermal shock, and testing for performance under humidity conditions.

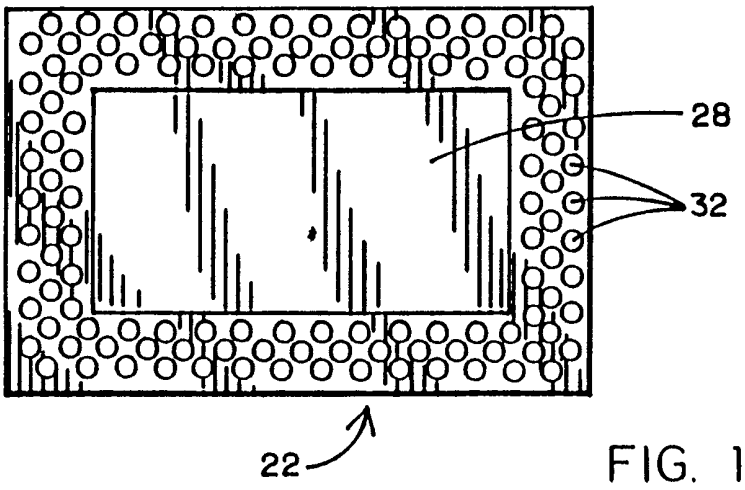


FIG. 1

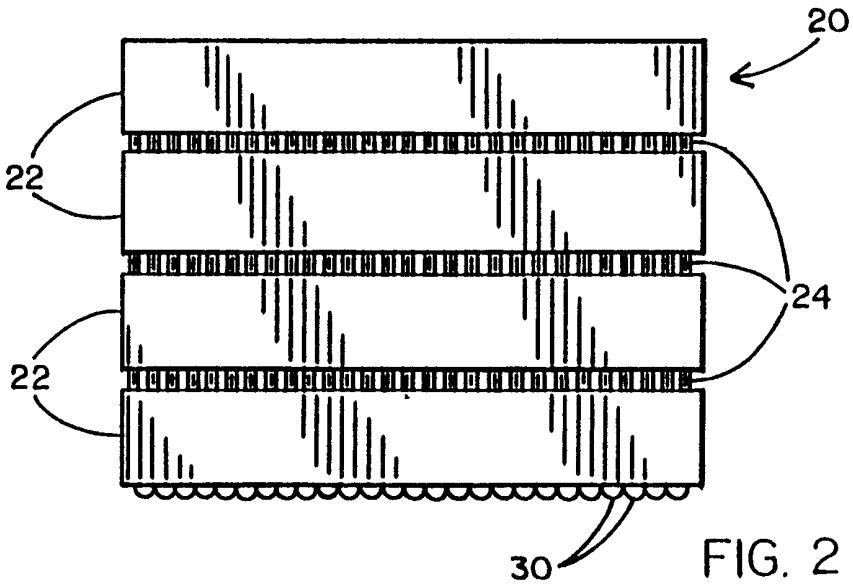


FIG. 2

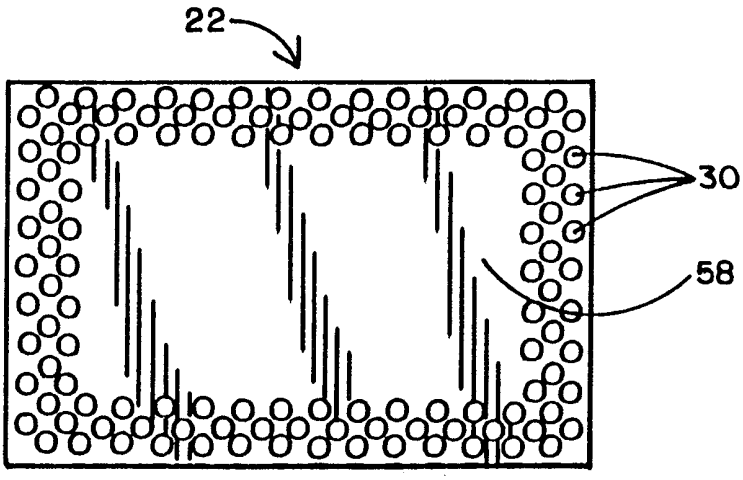


FIG. 3

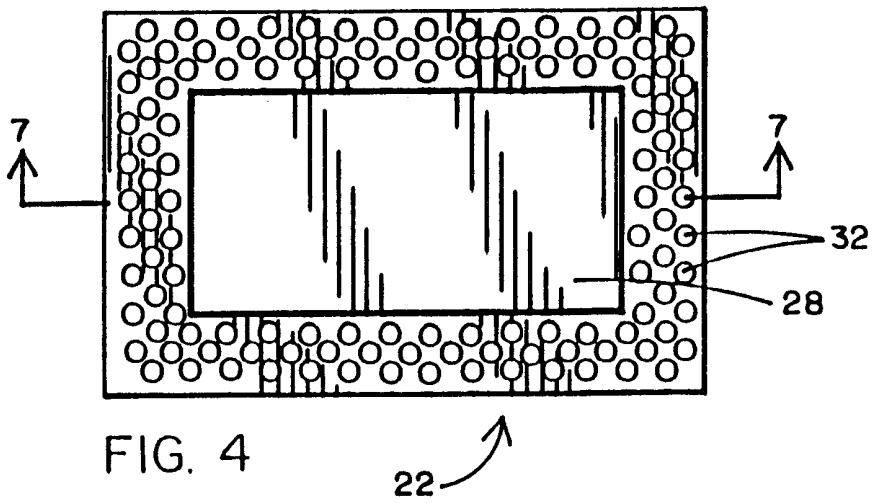


FIG. 4

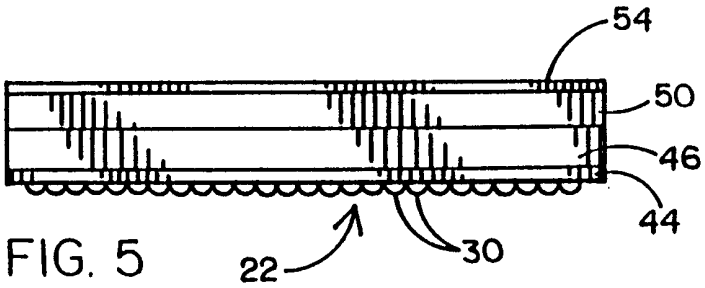


FIG. 5

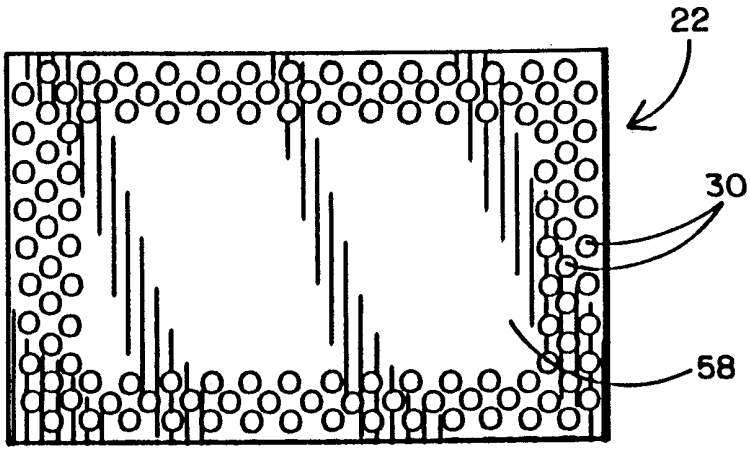


FIG. 6

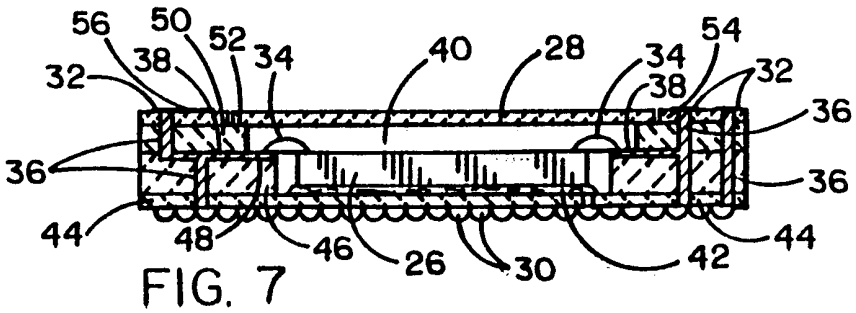


FIG. 7

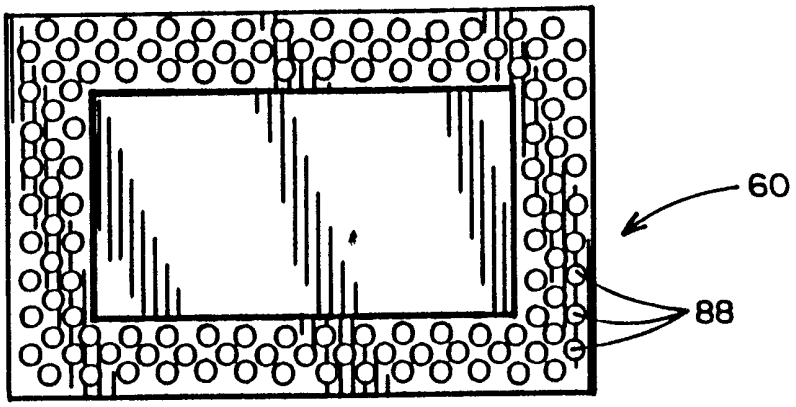


FIG. 8

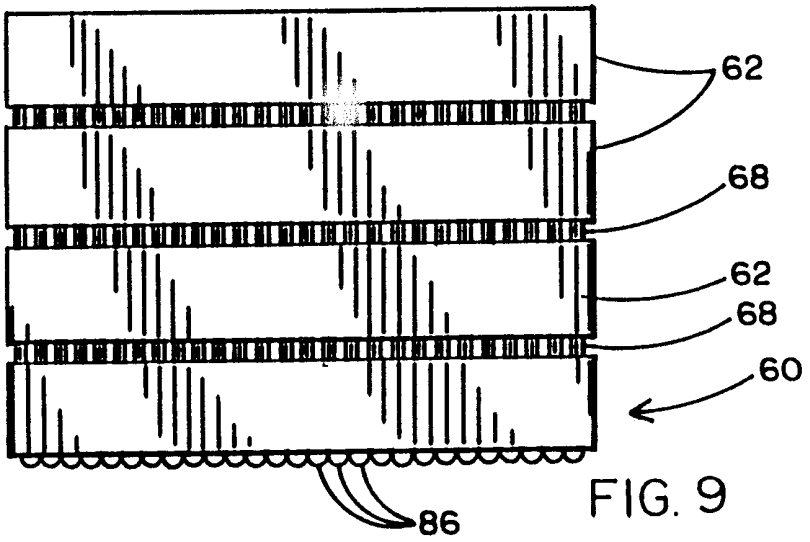


FIG. 9

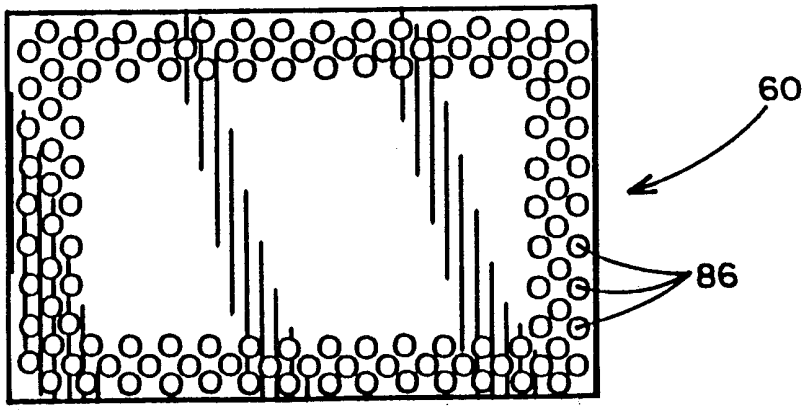


FIG. 10

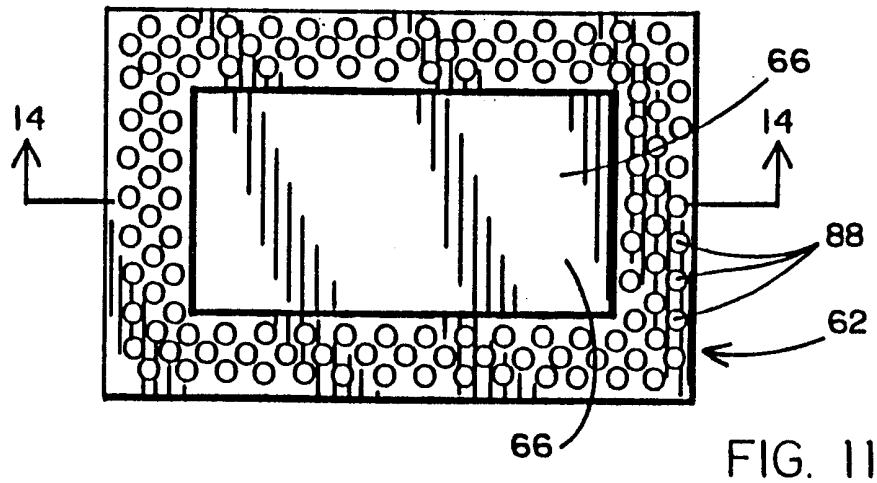


FIG. 11

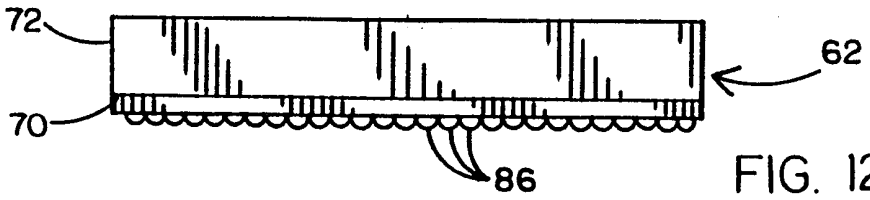


FIG. 12

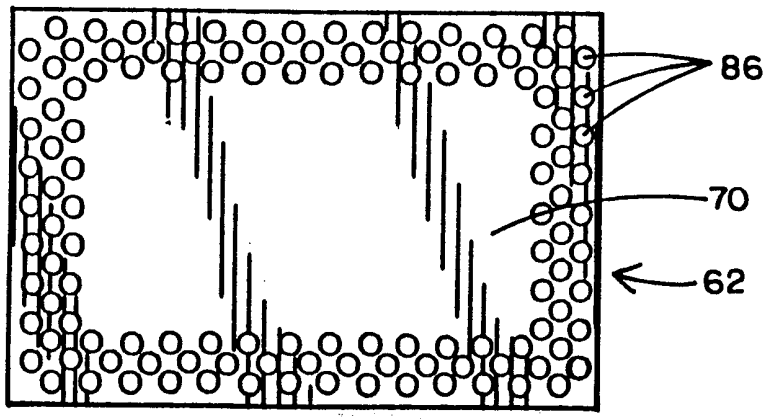


FIG. 13

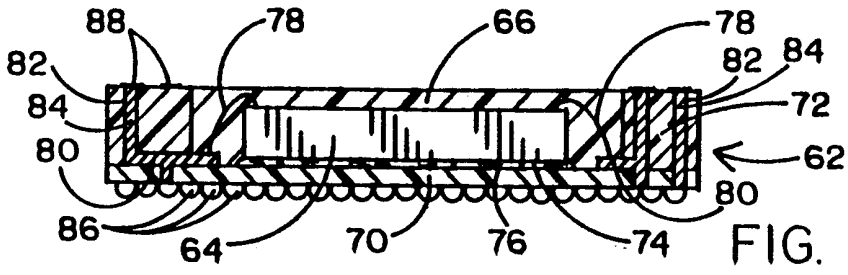
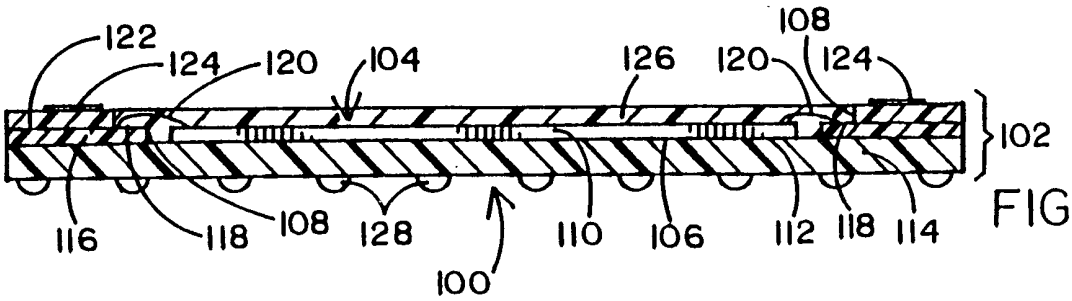


FIG. 14


122
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120
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126
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102
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118
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114
100

FIG. 15

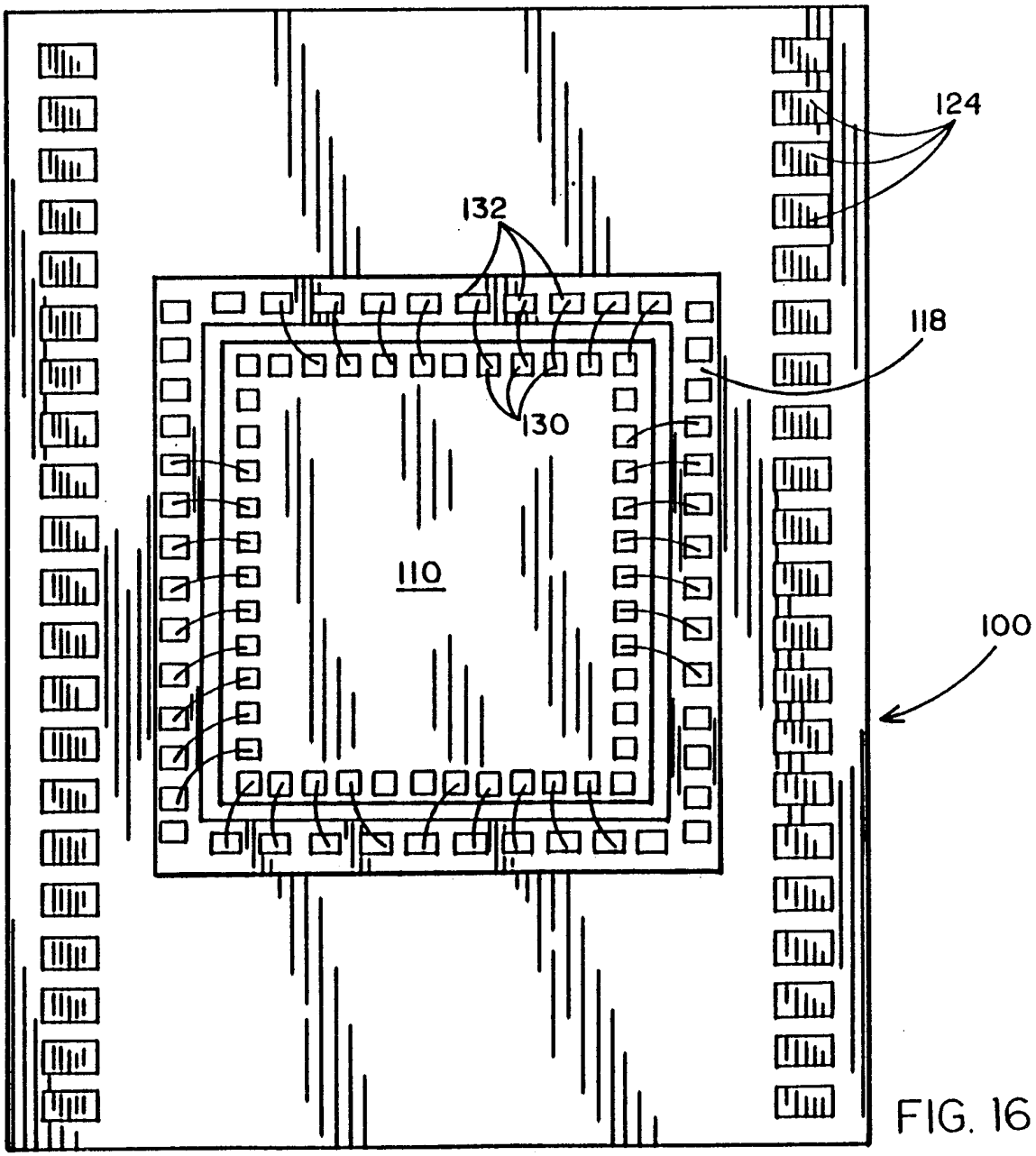
124
132
118
130
110
100

FIG. 16

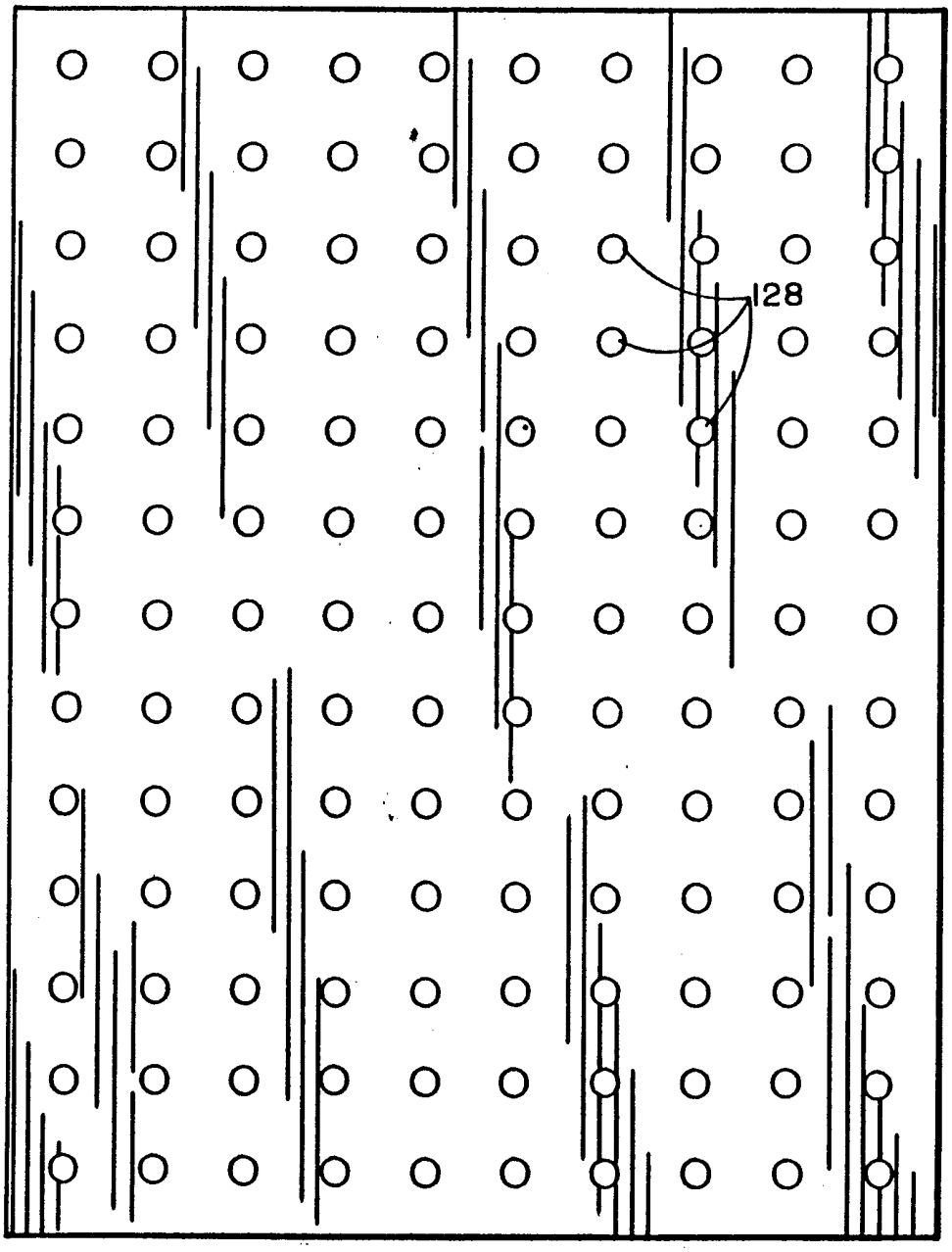

FIG. 17

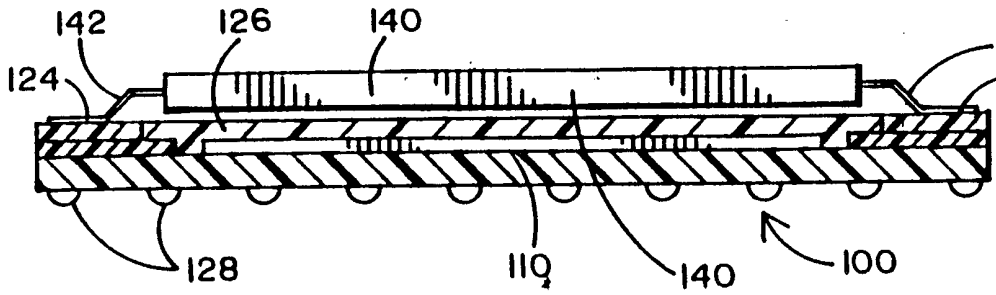

FIG. 18

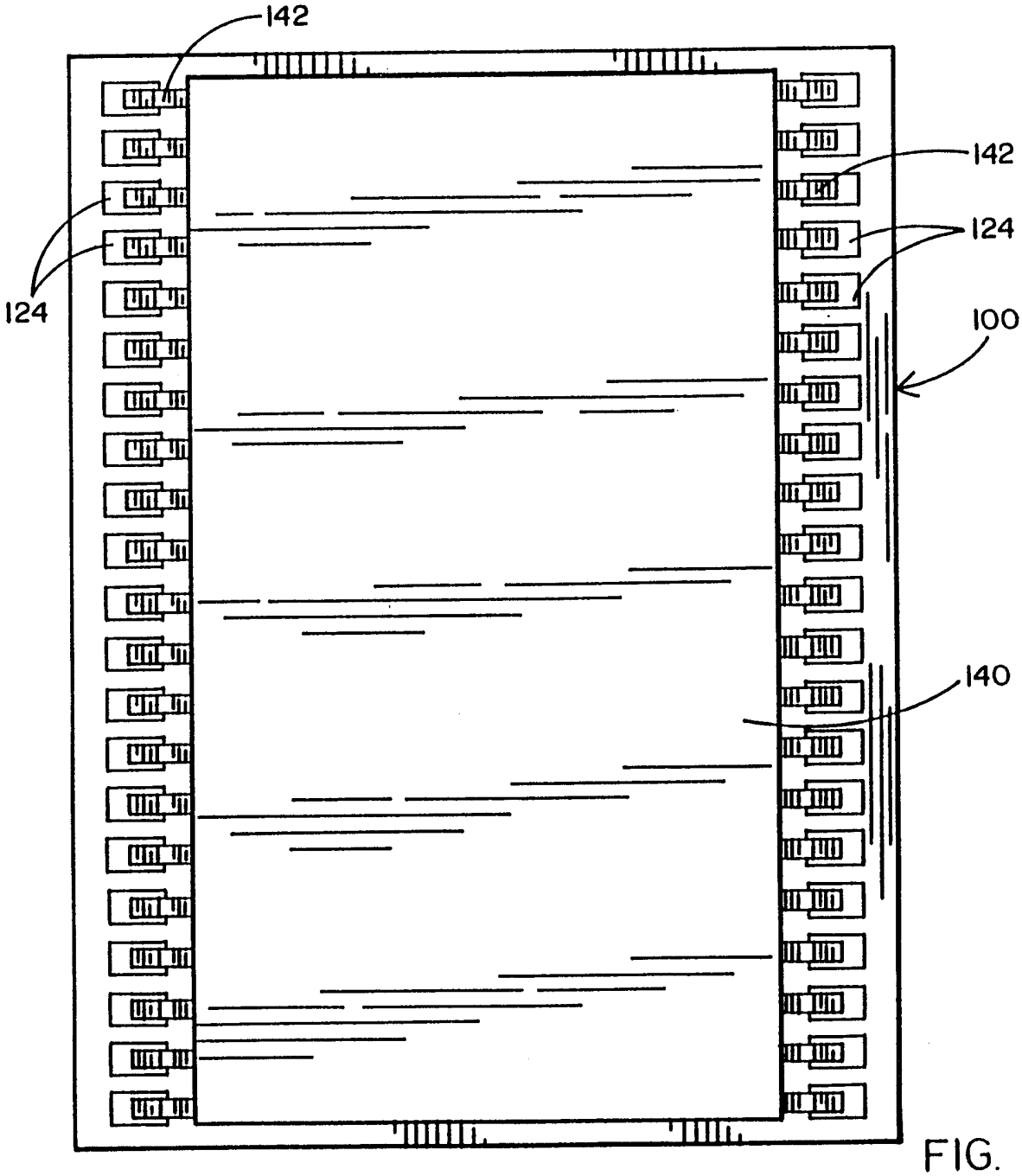

FIG. 19

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/04211

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :Please See Extra Sheet.
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : Please See Extra Sheet.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

STN, GPIC, WEST, DERWENT

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,376,825 A (TUKAMOTO ET AL.) 27 December 1994 (27/12/94), see entire document, especially figures 7 and 8.	1-15

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 28 JUNE 1999	Date of mailing of the international search report 06 JUL 1999
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer DONALD A. SPARKS Telephone No. (703) 308-1756

Form PCT/ISA/210 (second sheet)(July 1992)★

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/04211

A. CLASSIFICATION OF SUBJECT MATTER:
IPC (6):

H05K 1/14, 1/16, 1/18, 7/02; H01L 23/02, 23/12, 23/28, 23/48, 23/488, 23/538; H01R 4/02, 9/09

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

29/830,, 832, 840, 841; 174/52.1-52.4, 255, 260, 261; 257/686, 687, 692, 693, 723, 724, 737, 738, 777, 778; 361/735, 744, 784, 790, 803, 807, 809; 438/108, 109, 125, 126, 127, 612; 439/68, 69, 70, 71

B. FIELDS SEARCHED
Minimum documentation searched
Classification System: U.S.

29/830,, 832, 840, 841; 174/52.1-52.4, 255, 260, 261; 257/686, 687, 692, 693, 723, 724, 737, 738, 777, 778; 361/735, 744, 784, 790, 803, 807, 809; 438/108, 109, 125, 126, 127, 612; 439/68, 69, 70, 71