(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
9 December 2010 (09.12.2010)

PCT

(10) International Publication Number
WO 2010/141295 A1

(51) International Patent Classification:
H01L 23/04 (2006.01)

(21) International Application Number:
PCT/US2010/036282

(22) International Filing Date:
27 May 2010 (27.05.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/183,340 2 June 2009 (02.06.2009) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

WO 2010/141295 A1

(54) **Title**: COMPLIANT PRINTED FLEXIBLE CIRCUIT

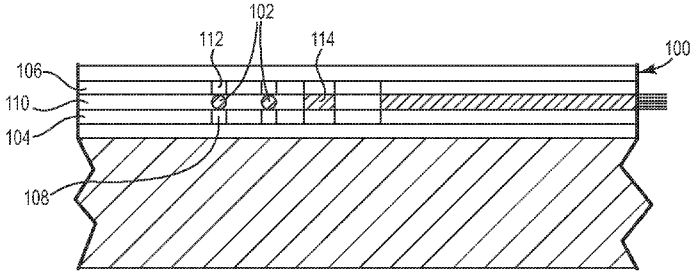

Fig. 5

(57) **Abstract**: A compliant printed flexible circuit including a flexible polymeric film and at least one dielectric layer bonded to the polymeric film with recesses corresponding to a target circuit geometry. A conductive material is printed in at least a portion of the recesses to form a circuit geometry. At least one dielectric covering layer is printed over at least the circuit geometry. Openings can be printed in the dielectric covering layer to provide access to at least a portion of the circuit geometry.

COMPLIANT PRINTED FLEXIBLE CIRCUIT

Technical Field

[0001] The present application relates to a high performance compliant printed flexible circuit that merges the long-term performance advantages of flexible circuits, with the flexibility of additive printing technology.

Background of the Invention

[0002] Traditional printed circuits are often constructed in what is commonly called rigid or flexible formats. The rigid versions are used in nearly every electronic system, where the printed circuit board (PCB) is essentially a laminate of materials and circuits that when built is relatively stiff or rigid and cannot be bent significantly without damage.

[0003] Flexible circuits have become very popular in many applications where the ability to bend the circuit to connect one member of a system to another has some benefit. These flexible circuits are made in a very similar fashion as rigid PCB's, where layers of circuitry and dielectric materials are laminated. The main difference is the material set used for construction. Typical flexible circuits start with a polymer film that is clad, laminated, or deposited with copper. A photolithography image with the desired circuitry geometry is printed onto the copper, and the polymer film is etched to remove the unwanted copper. Flexible circuits are very commonly used in many electronic systems such as notebook computers, medical devices, displays, handheld devices, autos, aircraft and many others.

[0004] Flexible circuits are processed similar to that of rigid PCB's with a series of imaging, masking, drilling, via creation, plating, and trimming steps. The resulting circuit can be bent, without damaging the copper circuitry. Flexible circuits are solderable, and can have devices attached to provide some desired function. The materials used to make flexible circuits can be used in high frequency applications where the material set and design features can often provide better electrical performance than a comparable rigid circuit.

[0005] Flexible circuits are connected to electrical system in a variety of ways. In most cases, a portion of the circuitry is exposed to create a connection point. Once exposed, the circuitry can be connected to another circuit or component by

soldering, conductive adhesive, thermosonic welding, pressure or a mechanical connector. In general, the terminals are located on an end of the flexible circuit, where edge traces are exposed or in some cases an area array of terminals are exposed. Often there is some sort of mechanical enhancement at or near the connection to prevent the joints from being disconnected during use or flexure.

[0006] In general, flexible circuits are expensive compared to some rigid PCB products. Flexible circuits also have some limitations regarding layer count or feature registration, and are therefore generally only used for small or elongated applications.

Brief Summary of the Invention

[0007] The present disclosure is directed to a high performance compliant printed flexible circuit ("CFPC") that will enable next generation electrical performance. The present disclosure merges the long-term performance advantages of flexible circuits, with the flexibility of additive printing technology.

[0008] This present compliant printed flexible circuit enables internal and/or external compliance to enhance the mechanical performance of the circuit. Electrical devices can be printed on the CFPC, such as for example, ground planes, power planes, transistors, capacitors, resistors, RF antennae, shielding, filters, signal or power altering and enhancing devices, memory devices, embedded IC, and the like.

[0009] The present CFPC can be produced digitally, without tooling or costly artwork. The CFPC can be produced as a "Green" product, with dramatic reductions in environmental issues related to the production of conventional flexible circuits.

[0010] Contact members can be printed in a variety of shapes and sizes, depending on the terminal structure on the circuit members. The contact members can be positioned at a variety of locations, heights, or spacing to match the parameters of existing connections, allowing replacement of existing interconnect connectors, without changing hardware or the PCB. In some embodiments, the tips of the contact members are treated with specialty materials to increase long term reliability, such as for a test socket application.

[0011] The use of additive printing processes permits the material set in a given layer to vary. Traditional PCB and flex circuit fabrication methods take sheets of material and stack them up, laminate, and/or drill. The materials in each layer are limited to the materials in a particular sheet. Additive printing technologies permit a wide variety of materials to be applied on a layer with a registration relative to the

features of the previous layer. Selective addition of conductive, non-conductive, or semi-conductive materials at precise locations to create a desired effect has the major advantages in tuning impedance or adding electrical function on a given layer. Tuning performance on a layer by layer basis relative to the previous layer greatly enhances electrical performance.

[0012] Since the individual contact members are preferably printed, the present CFPC can be removed and replaced without having to handle or assemble individual contact members. The circuit members on the CFPC can be configured to mate with existing or custom connectors in a LIF, ZIF, or plugged connector configuration, while maintaining or improving signal integrity.

[0013] One embodiment is directed to a compliant printed flexible circuit including a flexible polymeric film and at least one dielectric layer bonded to the polymeric film with recesses corresponding to a target circuit geometry. A conductive material is printed in at least a portion of the recesses to form a circuit geometry. At least one dielectric covering layer is printed over at least the circuit geometry. At least one opening in the dielectric covering layer provides access to at least a portion of the circuit geometry.

[0014] A conductive plating layer is optionally applied on at least a portion of the circuit geometry. The conductive material can be sintered conductive particles or a conductive ink. In one embodiment, a compliant material is located between the polymeric film and at least a portion of the circuit geometry. The compliant material is preferably aligned with the opening in the dielectric layer.

[0015] The resulting circuit geometry preferably has conductive traces that have substantially rectangular cross-sectional shapes, corresponding to the recesses. The use of additive printing processes permit conductive material, non-conductive material, and semi-conductive material to be located on a single layer.

[0016] In one embodiment, pre-formed conductive trace materials are located in the recesses. The recesses are than plated to form conductive traces with substantially rectangular cross-sectional shapes. In another embodiment, a conductive foil is pressed into at least a portion of the recesses. The conductive foil is sheared along edges of the recesses. The excess conductive foil not located in the recesses is removed and the recesses are plated to form conductive traces with substantially rectangular cross-sectional shapes.

[0017] At least one electrical device is optionally printed on a dielectric layer or the polymeric film and electrically coupled to at least a portion of the circuit geometry. Optical quality materials can be printed or deposited in at least a portion of the recesses to form optical circuit geometries. Alternatively, optical fibers can be located in the recesses.

[0018] Vias can be printed on the compliant printed flexible circuit to electrically couple adjacent layers of the circuit geometry. One or more contact members electrically coupled to at least a portion of the circuit geometry are printed to extend above the dielectric covering layer. The compliant printed flexible circuit is optionally singulated adjacent at least one of the contact members.

[0019] In one embodiment, at least one contact member extends along a first surface of the compliant printed flexible circuit and at least one printed compliant member is located on a second surface of the compliant printed flexible circuit opposite at least one of the contact members.

[0020] The present disclosure is also directed to an edge connector on the compliant printed flexible circuit. A first portion of the circuit geometry extends beyond the dielectric covering layer. A compliant material is located along a surface of the first portion of the circuit geometry. A second portion of the circuit geometry is located on top of the compliant material.

[0021] The present disclosure is also directed to an electrical interconnect assembly. A housing retains the compliant printed flexible circuit. Electrical contacts on a first circuit member are compressively engaged with contact members located along a first surface of the compliant printed flexible circuit. Electrical contacts on a second circuit member are compressively engaged with contact members located along a second surface of the compliant printed flexible circuit. The first and second circuit members are selected from one of a dielectric layer, a printed circuit board, a flexible circuit, a bare die device, an integrated circuit device, organic or inorganic substrates, or a rigid circuit.

[0022] The present disclosure is also directed to a method of making a compliant printed flexible circuit. At least one dielectric layer is bonded to a flexible polymeric film to create recesses corresponding to a target circuit geometry. A conductive material is printed in at least a portion of the recesses to form a circuit geometry. At least one dielectric covering layer is printed over at least the circuit geometry.

[0023] The dielectric covering layer can be printed with at least one opening that provides access to at least a portion of the circuit geometry. The conductive material is preferably plated. The conductive material, compliant materials, electrical devices, optical quality material, and the contact members are all preferably printed.

[0024] The present disclosure is also directed to a method of making an edge connector for a compliant printed flexible circuit. A first portion of the circuit geometry is printed beyond the dielectric covering layer. A compliant material is printed along a surface of the first portion of the circuit geometry. A second portion of the circuit geometry is printed on top of the compliant material.

[0025] The present disclosure is also directed to a method of making an electrical interconnect assembly. A compliant printed flexible circuit is retained in a housing. Electrical contacts on a first circuit member are compressively coupled with contact members located along a first surface of the compliant printed flexible circuit, and electrical contacts on a second circuit member are compressively coupled with contact members located along a second surface of the compliant printed flexible circuit.

[0026] The present disclosure is also directed to several additive processes that combine the mechanical or structural properties of a polymer material, while adding metal materials in an unconventional fashion, to create electrical paths that are refined to provide electrical performance improvements. By adding or arranging metallic particles, conductive inks, plating, or portions of traditional alloys, the the compliant printed flexible circuit reduces parasitic electrical effects and impedance mismatch, potentially increasing the current carrying capacity.

[0027] The present compliant printed flexible circuit can serve as a platform to add passive and active circuit features to improve electrical performance or internal function and intelligence. For example, electrical features and devices are printed onto the interconnect assembly using, for example, inkjet printing technology or other printing technologies. The ability to enhance the compliant printed flexible circuit, such that it mimics aspects of an IC package and a PCB, allows for reductions in complexity for the IC package and the PCB, while improving the overall performance of the interconnect assembly.

[0028] The printing process permits the fabrication of functional structures, such as conductive paths and electrical devices, without the use of masks or resists. Features down to about 10 microns can be directly written in a wide variety of

functional inks, including metals, ceramics, polymers and adhesives, on virtually any substrate - silicon, glass, polymers, metals and ceramics. The substrates can be planar and non-planar surfaces. The printing process is typically followed by a thermal treatment, such as in a furnace or with a laser, to achieve dense functionalized structures.

[0029] The compliant printed flexible circuit can be configured with conductive traces that reduce or redistribute the terminal pitch, without the addition of an interposer or daughter substrate. Grounding schemes, shielding, electrical devices, and power planes can be added to the interconnect assembly, reducing the number of connections to the PCB and relieving routing constraints while increasing performance.

Brief Description of the Several Views of the Drawing

[0030] Figure 1 is a cross-sectional view of a method of making a compliant printed flexible circuit in accordance with an embodiment of the present disclosure.

[0031] Figure 2 illustrates a printed circuit geometry on the compliant printed flexible circuit of Figure 1.

[0032] Figure 3 illustrates the compliant printed flexible circuit of Figure 1.

[0033] Figure 4 illustrates a compliant printed flexible circuit with printed compliant features in accordance with an embodiment of the present disclosure.

[0034] Figure 5 illustrates a compliant printed flexible circuit with optical features in accordance with an embodiment of the present disclosure.

[0035] Figure 6 illustrates an alternate compliant printed flexible circuit with optical features in accordance with an embodiment of the present disclosure.

[0036] Figure 7 illustrates an alternate compliant printed flexible circuit with printed vias in accordance with an embodiment of the present disclosure.

[0037] Figure 8 illustrates an alternate compliant printed flexible circuit with printed electrical devices in accordance with an embodiment of the present disclosure.

[0038] Figure 9 illustrates an alternate compliant printed flexible circuit with printed compliant electrical pads to plug into another connector in accordance with an embodiment of the present disclosure.

[0039] Figure 10 illustrates a method of making a compliant printed flexible circuit in accordance with an embodiment of the present disclosure.

[0040] Figures 11 and 12 illustrate other aspects of the method of Figure 10.

[0041] Figure 13 illustrates a compliant printed flexible circuit made in accordance with the method of Figures 10, 11 and 12.

[0042] Figure 14 illustrates a compliant printed flexible circuit incorporated into a socket assembly in accordance with an embodiment of the present disclosure.

[0043] Figure 15 illustrates an alternate compliant printed flexible circuit in accordance with an embodiment of the present disclosure.

[0044] Figure 16 illustrates an alternate compliant printed flexible circuit in accordance with an embodiment of the present disclosure.

[0045] Figure 17 illustrates an alternate compliant printed flexible circuit in accordance with an embodiment of the present disclosure.

[0046] Figure 18 illustrates an alternate compliant printed flexible circuit in accordance with an embodiment of the present disclosure.

Detailed Description of the Invention

[0047] A complaint printed flexible circuit according to the present disclosure may permit fine contact-to-contact spacing (pitch) on the order of less than 1.0 mm pitch, and more preferably a pitch of less than about 0.7 millimeter, and most preferably a pitch of less than about 0.4 millimeter. Such fine pitch compliant printed flexible circuits are especially useful for communications, wireless, and memory devices.

[0048] The present compliant printed flexible circuit can be configured as a low cost, high signal performance interconnect assembly, which has a low profile that is particularly useful for desktop and mobile PC applications. IC devices to be installed and uninstalled without the need to reflow solder. The solder-free electrical connection of the IC devices is environmentally friendly.

[0049] Figure 1 is a side cross-sectional view of a method for replicating a flexible circuit member using additive processes in accordance with an embodiment of the present disclosure. Flexible polymeric film 50 includes one or more dielectric layers 52, 54 configured to include recesses 56 corresponding to a desired circuit geometry. In one embodiment, the dielectric layers 52, 54 are printed or placed on surface 58 of the flexible polymeric film 50. The recesses 56 can be defined by printing, embossing, imprinting, chemical etching with a printed mask, or a variety of other techniques. A number of different materials are used as the flexible polymeric film 50 including: polyester (PET), polyimide (PI), polyethylene napthalate (PEN), Polyetherimide (PEI), along with various fluropolymers (FEP) and copolymers.

Polyimide films are the most prevalent due to their advantageous electrical, mechanical, chemical, and thermal properties.

[0050] As illustrated in Figure 2, a metalizing layer is deposited in the recesses 56 to create circuit geometry 62. Metalizing can be performed by printing conductive particles followed by a sintering step, by printing conductive inks, or a variety of other techniques. The resulting metalized layer is preferably plated to improve conductive properties. The circuit geometry 62 is preferably of copper or similar metallic materials such as phosphor bronze or beryllium-copper. The plating is preferably a corrosion resistant metallic material such as nickel, gold, silver, palladium, or multiple layers thereof.

[0051] As illustrated in Figure 3, another dielectric or insulating layer 64 is applied to the circuit geometry 62 and the dielectric layer 54. The nature of the printing process allows for selective application of dielectric layer 64 to leave selected portions 66 of the circuit geometry 62 expose if desired. The resulting compliant printed flexible circuit 68 can potentially be considered entirely "green" with limited or no chemistry used to produce beyond the direct write materials.

[0052] The recesses 56 in the layers 52, 54, 64 permit control of the location, cross section, material content, and aspect ratio of the conductive traces in the circuit geometry 62. Maintaining the conductive traces with a cross-section of 1:1 or greater provides greater signal integrity than traditional subtractive trace forming technologies. For example, traditional methods take a sheet of a given thickness and etches the material between the traces away to have a resultant trace that is usually wider than it is thick. The etching process also removes more material at the top surface of the trace than at the bottom, leaving a trace with a trapezoidal cross-sectional shape, degrading signal integrity in some applications. Using the recesses 56 to control the aspect ratio of the conductive traces results in a more rectangular or square cross-section of the conductive traces in the circuit geometry 62, with the corresponding improvement in signal integrity.

[0053] In another embodiment, pre-patterned or pre-etched thin conductive foil circuit traces are transferred to the recesses 56. For example, a pressure sensitive adhesive can be used to retain the copper foil circuit traces in the recesses 56. The trapezoidal cross-sections of the pre-formed conductive foil traces are then post-plated. The plating material fills the open spaces in the recesses 56 not occupied by

the foil circuit geometry, resulting in a substantially rectangular or square cross-sectional shape corresponding to the shape of the recesses 56.

[0054] In another embodiment, a thin conductive foil is pressed into the recesses 56, and the edges of the recesses 56 acts to cut or shear the conductive foil. The process locates a portion of the conductive foil in the trenches 56, but leaves the negative pattern of the conductive foil not wanted outside and above the trenches 56 for easy removal. Again, the foil in the trenches 56 is preferably post plated to add material to increase the thickness of the conductive traces in the circuit geometry 62 and to fill any voids left between the conductive foil and the recesses 56.

[0055] The dielectric layers 52, 54, 64 may be constructed of any of a number of dielectric materials that are currently used to make sockets, semiconductor packaging, and printed circuit boards. Examples may include UV stabilized tetrafunctional epoxy resin systems referred to as Flame Retardant 4 (FR-4); bismaleimide-triazine thermoset epoxy resins referred to as BT-Epoxy or BT Resin; and liquid crystal polymers (LCPs), which are polyester polymers that are extremely unreactive, inert and resistant to fire. Other suitable plastics include phenolics, polyesters, and Ryton® available from Phillips Petroleum Company.

[0056] In one embodiment, one or more of the layer 52, 54, 64 are designed to provide electrostatic dissipation or to reduce cross-talk between the traces of the circuit geometry 62. An efficient way to prevent electrostatic discharge ("ESD") is to construct one of the layers from materials that are not too conductive but that will slowly conduct static charges away. These materials preferably have resistivity values in the range of 10^5 to 10^{11} Ohm-meters.

[0057] Figure 4 illustrates an alternate compliant printed flexible circuit 80 in accordance with an embodiment of the present disclosure. Dielectric layer 82 includes openings 84 into which compliant material 86 is printed before formation of circuit geometry 88. The compliant printed material 86 improves reliability during flexure of exposed portion 90 the circuit geometry 88.

[0058] Figure 5 illustrates an alternate compliant printed flexible circuit 100 in accordance with an embodiment of the present disclosure. Optical fibers 102 are located between layers 104, 106 of dielectric material. In one embodiment, optical fibers 102 is positioned over printed compliant layer 108, and dielectric layer 110 is printed over and around the optical fibers 102. A compliant layer 112 is preferably printed above the optical fiber 102 as well. The compliant layers 108, 112 support

the optical fibers 102 during flexure. In another embodiment, the dielectric layer 110 is formed or printed with recesses into which the optical fibers 102 are deposited.

[0059] In another embodiment, optical quality materials 114 are printed during printing of the compliant printed flexible circuit 100. The optical quality material 114 and/or the optical fibers 102 comprise optical circuit geometries. The printing process allows for deposition of coatings in-situ that enhance the optical transmission or reduce loss. The precision of the printing process reduces misalignment issues when the optical materials 114 are optically coupled with another optical structure.

[0060] Figure 6 illustrates another embodiment of a present compliant printed flexible circuit 140 in accordance with an embodiment of the present disclosure. Embedded coaxial RF circuits 142 or printed micro strip RF circuits 144 are located with dielectric/metal layers 146. These RF circuits 142, 144 are preferably created by printing dielectrics and metallization geometry.

[0061] As illustrated in Figure 7, use of additive processes allows the creation of a compliant printed flexible circuit 160 with inter-circuit, 3D lattice structures 162 having intricate routing schemes. Vias 164 can be printed with each layer, without drilling.

[0062] Figure 8 illustrates a compliant printed flexible circuit 180 with printed electrical devices 182. The electrical devices 182 can include passive or active functional elements. Passive structure refers to a structure having a desired electrical, magnetic, or other property, including but not limited to a conductor, resistor, capacitor, inductor, insulator, dielectric, suppressor, filter, varistor, ferromagnet, and the like. In the illustrated embodiment, electrical devices 182 include printed LED indicator 184 and display electronics 186. Geometries can also be printed to provide capacitive coupling 188.

[0063] The electrical devices 182 are preferably printed during construction of the interconnect assembly 100. The electrical devices 182 can be ground planes, power planes, electrical connections to other circuit members, dielectric layers, conductive traces, transistors, capacitors, resistors, RF antennae, shielding, filters, signal or power altering and enhancing devices, memory devices, embedded IC, and the like. For example, the electrical devices 182 can be formed using printing technology, adding intelligence to the compliant printed flexible circuit 180. Features that are

typically located on other circuit members can be incorporated into the flexible circuit 180 in accordance with an embodiment of the present disclosure.

[0064] The availability of printable silicon inks provides the ability to print electrical devices 90, 92, such as disclosed in U.S. Pat. No. 7,485,345 (Renn et al.); 7,382,363 (Albert et al.); 7,148,128 (Jacobson); 6,967,640 (Albert et al.); 6,825,829 (Albert et al.); 6,750,473 (Amundson et al.); 6,652,075 (Jacobson); 6,639,578 (Comiskey et al.); 6,545,291 (Amundson et al.); 6,521,489 (Duthaler et al.); 6,459,418 (Comiskey et al.); 6,422,687 (Jacobson); 6,413,790 (Duthaler et al.); 6,312,971 (Amundson et al.); 6,252,564 (Albert et al.); 6,177,921 (Comiskey et al.); 6,120,588 (Jacobson); 6,118,426 (Albert et al.); and U.S. Pat. Publication No. 2008/0008822 (Kowalski et al.), which are hereby incorporated by reference. In particular, U.S. Patent Nos. 6,506,438 (Duthaler et al.) and 6,750,473 (Amundson et al.), which are incorporated by reference, teach using ink-jet printing to make various electrical devices, such as, resistors, capacitors, diodes, inductors (or elements which may be used in radio applications or magnetic or electric field transmission of power or data), semiconductor logic elements, electro-optical elements, transistor (including, light emitting, light sensing or solar cell elements, field effect transistor, top gate structures), and the like.

[0065] The electrical devices 202 can also be created by aerosol printing, such as disclosed in U.S. Patent Nos. 7,674,671 (Renn et al.); 7,658,163 (Renn et al.); 7,485,345 (Renn et al.); 7,045,015 (Renn et al.); and 6,823,124 (Renn et al.), which are hereby incorporated by reference.

[0066] Printing processes are preferably used to fabricate various functional structures, such as conductive paths and electrical devices, without the use of masks or resists. Features down to about 10 microns can be directly written in a wide variety of functional inks, including metals, ceramics, polymers and adhesives, on virtually any substrate - silicon, glass, polymers, metals and ceramics. The substrates can be planar and non-planar surfaces. The printing process is typically followed by a thermal treatment, such as in a furnace or with a laser, to achieve dense functionalized structures.

[0067] Ink jet printing of electronically active inks can be done on a large class of substrates, without the requirements of standard vacuum processing or etching. The inks may incorporate mechanical, electrical or other properties, such as, conducting,

insulating, resistive, magnetic, semi conductive, light modulating, piezoelectric, spin, optoelectronic, thermoelectric or radio frequency.

[0068] A plurality of ink drops are dispensed from the print head directly to a substrate or on an intermediate transfer member. The transfer member can be a planar or non-planar structure, such as a drum. The surface of the transfer member can be coated with a non-sticking layer, such as silicone, silicone rubber, or Teflon.

[0069] The ink (also referred to as function inks) can include conductive materials, semi-conductive materials (e.g., p-type and n-type semiconducting materials), metallic material, insulating materials, and/or release materials. The ink pattern can be deposited in precise locations on a substrate to create fine lines having a width smaller than 10 microns, with precisely controlled spaces between the lines. For example, the ink drops form an ink pattern corresponding to portions of a transistor, such as a source electrode, a drain electrode, a dielectric layer, a semiconductor layer, or a gate electrode.

[0070] The substrate can be an insulating polymer, such as polyethylene terephthalate (PET), polyester, polyethersulphone (PES), polyimide film (e.g. Kapton, available from DuPont located in Wilmington, DE; Upilex available from Ube Corporation located in Japan), or polycarbonate. Alternatively, the substrate can be made of an insulator such as undoped silicon, glass, or a plastic material. The substrate can also be patterned to serve as an electrode. The substrate can further be a metal foil insulated from the gate electrode by a non-conducting material. The substrate can also be a woven material or paper, planarized or otherwise modified on at least one surface by a polymeric or other coating to accept the other structures.

[0071] Electrodes can be printed with metals, such as aluminum or gold, or conductive polymers, such as polythiophene or polyaniline. The electrodes may also include a printed conductor, such as a polymer film comprising metal particles, such as silver or nickel, a printed conductor comprising a polymer film containing graphite or some other conductive carbon material, or a conductive oxide such as tin oxide or indium tin oxide.

[0072] Dielectric layers can be printed with a silicon dioxide layer, an insulating polymer, such as polyimide and its derivatives, poly-vinyl phenol, polymethylmethacrylate, polyvinyldenedifluoride, an inorganic oxide, such as metal oxide, an inorganic nitride such as silicon nitride, or an inorganic/organic composite material such as an organic-substituted silicon oxide, or a sol-gel organosilicon

glass. Dielectric layers can also include a bicylcobutene derivative (BCB) available from Dow Chemical (Midland, Mich.), spin-on glass, or dispersions of dielectric colloid materials in a binder or solvent.

[0073] Semiconductor layers can be printed with polymeric semiconductors, such as, polythiophene, poly(3-alkyl)thiophenes, alkyl-substituted oligothiophene, polythienylenevinylene, poly(para-phenylenevinylene) and doped versions of these polymers. An example of suitable oligomeric semiconductor is alpha-hexathienylene. Horowitz, Organic Field-Effect Transistors, Adv. Mater., 10, No. 5, p. 365 (1998) describes the use of unsubstituted and alkyl-substituted oligothiophenes in transistors. A field effect transistor made with regioregular poly(3-hexylthiophene) as the semiconductor layer is described in Bao et al., Soluble and Processable Regioregular Poly(3-hexylthiophene) for Thin Film Field-Effect Transistor Applications with High Mobility, Appl. Phys. Lett. 69 (26), p. 4108 (December 1996). A field effect transistor made with a-hexathienylene is described in U.S. Pat. No. 5,659,181, which is incorporated herein by reference.

[0074] A protective layer can optionally be printed onto the electrical devices. The protective layer can be an aluminum film, a metal oxide coating, a polymeric film, or a combination thereof.

[0075] Organic semiconductors can be printed using suitable carbon-based compounds, such as, pentacene, phthalocyanine, benzodithiophene, buckminsterfullerene or other fullerene derivatives, tetracyanonaphthoquinone, and tetrakisimethylanimoethylene. The materials provided above for forming the substrate, the dielectric layer, the electrodes, or the semiconductor layer are exemplary only. Other suitable materials known to those skilled in the art having properties similar to those described above can be used in accordance with the present disclosure.

[0076] The ink-jet print head preferably includes a plurality of orifices for dispensing one or more fluids onto a desired media, such as for example, a conducting fluid solution, a semiconducting fluid solution, an insulating fluid solution, and a precursor material to facilitate subsequent deposition. The precursor material can be surface active agents, such as octadecyltrichlorosilane (OTS).

[0077] Alternatively, a separate print head is used for each fluid solution. The print head nozzles can be held at different potentials to aid in atomization and imparting a charge to the droplets, such as disclosed in U.S. Pat. No. 7,148,128

(Jacobson), which is hereby incorporated by reference. Alternate print heads are disclosed in U.S. Pat. No. 6,626,526 (Ueki et al.), and U.S. Pat. Publication Nos. 2006/0044357 (Andersen et al.) and 2009/0061089 (King et al.), which are hereby incorporated by reference.

[0078] The print head preferably uses a pulse-on-demand method, and can employ one of the following methods to dispense the ink drops: piezoelectric, magnetostrictive, electromechanical, electro pneumatic, electrostatic, rapid ink heating, magneto hydrodynamic, or any other technique well known to those skilled in the art. The deposited ink patterns typically undergo a curing step or another processing step before subsequent layers are applied.

[0079] While ink jet printing is preferred, the term "printing" is intended to include all forms of printing and coating, including: pre-metered coating such as patch die coating, slot or extrusion coating, slide or cascade coating, and curtain coating; roll coating such as knife over roll coating, forward and reverse roll coating; gravure coating; dip coating; spray coating; meniscus coating; spin coating; brush coating; air knife coating; screen printing processes; electrostatic printing processes; thermal printing processes; and other similar techniques.

[0080] Figure 9 illustrates an alternate compliant printed flexible circuit 200 with printed compliant material 202 added between circuit geometries 204, 206 to facilitate insertion of exposed circuit geometries 208, 210 into a receptacle or socket. The compliant material 202 can supplement or replace the compliance in the receptacle or socket. In one embodiment, the compliance is provided by a combination of the compliant material 202 and the exposed circuit geometriess 208, 210.

[0081] Figure 10 is a side sectional view of a method of making a compliant printed flexible circuit 250 in accordance with an embodiment of the present disclosure. Polymeric film 252 includes a plurality of cavities 254 extending through dielectric layer 256. The cavities 254 can be formed using a variety of techniques, such as molding, machining, printing, imprinting, embossing, etching, coining, and the like. Although the cavities 254 are illustrated as truncated cones or pyramids, a variety of other shapes can be used, such as for example, cones, hemispherical shapes, and the like.

[0082] As illustrated in Figure 11, metalizing layer is printed in the cavities 254 to create contact member 258, as discussed above. As illustrated in Figure 12, a

compliant layer 260 is printed on the dielectric layer 256, followed by dielectric layer 262 establishing circuit geometry.

[0083] Figure 13 illustrates circuit geometries 264 printed as discussed above. In one embodiment, the circuit geometries 264 are formed by depositing a conductive material in a first state in the recesses, and then processed to create a second more permanent state. For example, the metallic powder is printed according to the circuit geometry and subsequently sintered, or the curable conductive material flows into the circuit geometry and is subsequently cured. As used herein "cure" and inflections thereof refers to a chemical-physical transformation that allows a material to progress from a first form (e.g., flowable form) to a more permanent second form. "Curable" refers to an uncured material having the potential to be cured, such as for example by the application of a suitable energy source.

[0084] Second compliant layer 270 is printed on exposed surfaces 272 of the dielectric layers 262 and circuit geometries 264. The second compliant layer 270 and second dielectric layer 274 are selectively printed to permit printing of contact member 276. Alternatively, pre-fabricated contact members 276 can be bonded to the circuit geometries 264. As used herein, "bond" or "bonding" refers to, for example, adhesive bonding, solvent bonding, ultrasonic welding, thermal bonding, or any other techniques suitable for attaching adjacent layers to a substrate.

[0085] The dielectric layer 274 adjacent contact members 276 is optionally singulated to permit greater compliance. As used herein, “singulated” refers to slits, cuts, depressions, perforations, and/or points of weakness. In another embodiment, the compliant printed flexible circuit 250 is made in two portions and then bonded together.

[0086] Figure 14 illustrates a socket assembly 300 incorporating the compliant printed flexible circuit 250 of Figure 13, in accordance with an embodiment of the present disclosure. The dielectric layer 256 is separated from the polymeric film 252 to expose contact member 258. In the illustrated embodiment, the dielectric layer 274 is bonded to surface 302 of socket housing 304 so that contact members 276 are positioned in recess 306. First circuit member 308, such as an IC device, is positioned in the recess 306 so that the terminals 310 align with the contact members 276.

[0087] The contact members 258, 276 are optionally plated, either before or after the compliant printed flexible circuit 250 is installed in the socket housing 304. In

another embodiment, the contact members 258, 276 are deformed, such as for example by coining or etching, to facilitate engagement with terminals 310 on the first circuit member 308 and/or terminal 312 on second circuit member 314.

[0088] In operation, the first circuit member 308, socket assembly 300 and the second circuit member 314 are compressively coupled so that contact member 276 electrically couples with terminal 310 and contact member 258 electrically couples with contact pad 312. Compliant layer 260 biases the contact member 276 into engagement with the terminal 310, while the compliant layer 270 biases the contact member 258 into engagement with the pad 312. The compliant layers 260, 270 also permit the contact members 276, 258 to deflect and compensate for non-planarity of the terminals 310 or the pads 312. As used herein, the term "circuit members" refers to, for example, a packaged integrated circuit device, an unpackaged integrated circuit device, a printed circuit board, a flexible circuit, a bare-die device, an organic or inorganic substrate, a rigid circuit, or any other device capable of carrying electrical current.

[0089] Figure 15 illustrates a compliant printed flexible circuit 330 with compliant structure 332 printed to add compliance and normal force 334 external to the circuit geometry 336. For example, the compliant structure 332 can be a printed/sintering metallic spring. In another embodiment, the compliant structure 332 is a stamped or etched metallic, plastic, or overmolded leadframe that is added to the compliant printed flexible circuit 330. The compliant members 332 can optionally be singulated in tandem with the circuit geometry 336 to allow for individual contact compliance.

[0090] Figure 16 illustrates a compliant printed flexible circuit 350 with male contact member 352 in accordance with an embodiment of the present disclosure. Contact member 352 is preferably inserted through opening 354 printed in dielectric layers 356, 358 and circuit geometry 360. The resiliency of the dielectric layers 356, 358 permits plastic deformation to permit enlarged end 362 to penetrate the opening 354 in the compliant printed flexible circuit 350. The resilience of the dielectric layers 356, 358 also permit the contact member 360 to move in all six degrees of freedom (X-Y-Z-Pitch-Roll-Yaw) to facilitate electrical coupling with first and second circuit members 364, 366.

[0091] Figure 17 illustrates a compliant printed flexible circuit 370 with printed compliant member 372 located above contact member 374 in accordance with an embodiment of the present disclosure. The printed compliant member 372 and

associated contact member 374 is preferably singulated to promote flexure and compliance.

[0092] Figure 18 illustrates an alternate embodiment of a compliant printed flexible circuit 380 where printed compliant member 382 is located on circuit member 384. In the illustrated embodiment, secondary printed compliant member 386 is located on the compliant printed flexible circuit 380 above contact member 388.

[0093] Where a range of values is provided, it is understood that each intervening value, to the tenth of the unit of the lower limit unless the context clearly dictates otherwise, between the upper and lower limit of that range and any other stated or intervening value in that stated range is encompassed within the embodiments of the disclosure. The upper and lower limits of these smaller ranges which may independently be included in the smaller ranges is also encompassed within the embodiments of the disclosure, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either both of those included limits are also included in the embodiments of the present disclosure.

[0094] Unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skill in the art to which the embodiments of the present disclosure belong. Although any methods and materials similar or equivalent to those described herein can also be used in the practice or testing of the embodiments of the present disclosure, the preferred methods and materials are now described. All patents and publications mentioned herein, including those cited in the Background of the application, are hereby incorporated by reference to disclose and described the methods and/or materials in connection with which the publications are cited.

[0095] The publications discussed herein are provided solely for their disclosure prior to the filing date of the present application. Nothing herein is to be construed as an admission that the present disclosure is not entitled to antedate such publication by virtue of prior invention. Further, the dates of publication provided may be different from the actual publication dates which may need to be independently confirmed.

[0096] Other embodiments of the disclosure are possible. Although the description above contains much specificity, these should not be construed as limiting the scope of the disclosure, but as merely providing illustrations of some of

the presently preferred embodiments of this disclosure. It is also contemplated that various combinations or sub-combinations of the specific features and aspects of the embodiments may be made and still fall within the scope of the present disclosure. It should be understood that various features and aspects of the disclosed embodiments can be combined with or substituted for one another in order to form varying modes of the disclosed embodiments of the disclosure. Thus, it is intended that the scope of the present disclosure herein disclosed should not be limited by the particular disclosed embodiments described above.

[0097] Thus the scope of this disclosure should be determined by the appended claims and their legal equivalents. Therefore, it will be appreciated that the scope of the present disclosure fully encompasses other embodiments which may become obvious to those skilled in the art, and that the scope of the present disclosure is accordingly to be limited by nothing other than the appended claims, in which reference to an element in the singular is not intended to mean “one and only one” unless explicitly so stated, but rather “one or more.” All structural, chemical, and functional equivalents to the elements of the above-described preferred embodiment(s) that are known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the present claims. Moreover, it is not necessary for a device or method to address each and every problem sought to be solved by the present disclosure, for it to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims.

What is claimed is:

1. A compliant printed flexible circuit comprising:

a flexible polymeric film;

at least one dielectric layer bonded to the polymeric film with recesses corresponding to a target circuit geometry;

a conductive material deposited in at least a portion of the recesses comprising a circuit geometry;

at least one dielectric covering layer; and

at least one opening in the dielectric covering layer providing access to at least a portion of the circuit geometry.

2. The compliant printed flexible circuit of claim 1 comprising a conductive plating layer on at least a portion of the circuit geometry.

3. The compliant printed flexible circuit of claim 1 wherein the conductive material comprises one of sintered conductive particles or a conductive ink.

4. The compliant printed flexible circuit of claim 1 comprising a compliant material located between the polymeric film and at least a portion of the circuit geometry.

5. The compliant printed flexible circuit of claim 1 comprising a compliant material generally aligned with the opening in the dielectric layer and positioned between the polymeric film and at least a portion of the circuit geometry.

6. The compliant printed flexible circuit of claim 1 comprising at least one printed electrical device on one of a dielectric layer or the polymeric film and electrically coupled to at least a portion of the circuit geometry.

7. The compliant printed flexible circuit of claim 1 comprising an optical quality material deposited in at least a portion of the recesses comprising one or more optical circuit geometries.

8. The compliant printed flexible circuit of claim 1 comprising one or more optical fibers located in at least a portion of the recesses comprising one or more optical circuit geometries.

9. The compliant printed flexible circuit of claim 1 wherein at least a portion of the circuit geometry comprises a via electrically coupling adjacent layers of the circuit geometry.

10. The compliant printed flexible circuit of claim 1 comprising one or more contact members electrically coupled to at least a portion of the circuit geometry and extending above the dielectric covering layer.

11. The compliant printed flexible circuit of claim 10 wherein the compliant printed flexible circuit is singulated adjacent at least one of the contact members.

12. The compliant printed flexible circuit of claim 1 comprising:

at least one contact member extending along a first surface of the compliant printed flexible circuit; and

at least one printed compliant member located on a second surface of the compliant printed flexible circuit opposite at least one of the contact members.

13. The compliant printed flexible circuit of claim 1 wherein conductive traces in the circuit geometry comprise substantially rectangular cross-sectional shapes.

14. The compliant printed flexible circuit of claim 1 wherein a conductive material, a non-conductive material, and a semi-conductive material are printed on a single layer.

15. An edge connector on the compliant printed flexible circuit of claim 1 comprising:

a first portion of the circuit geometry extending beyond the dielectric covering layer;

a compliant material located along a surface of the first portion of the circuit geometry; and

a second portion of the circuit geometry located on top of the compliant material.

16. An electrical interconnect assembly comprising:

a housing retaining the compliant printed flexible circuit of claim 1;

a first circuit member comprising electrical contacts compressively engaged with contact members located along a first surface of the compliant printed flexible circuit; and

a second circuit member comprising electrical contacts compressively engaged with contact members located along a second surface of the compliant printed flexible circuit.

17. The electrical interconnect assembly of claim 16 wherein the first and second circuit members are selected from one of a dielectric layer, a printed circuit board, a flexible circuit, a bare die device, an integrated circuit device, organic or inorganic substrates, or a rigid circuit.

18. The compliant printed flexible circuit of claim 1 comprising:

at least one opening extending through the compliant printed flexible circuit; and

at least one contact member inserted in the opening and electrically coupled to at least a portion of the circuit geometry.

19. A method of making a compliant printed flexible circuit comprising:

bonding at least one dielectric layer to a flexible polymeric film to create recesses corresponding to a target circuit geometry;

printing a conductive material in at least a portion of the recesses comprising a circuit geometry; and

printing at least one dielectric covering layer over at least the circuit geometry.

20. The method of claim 19 comprising printing the dielectric covering layer with at least one opening that provides access to at least a portion of the circuit geometry.

21. The method of claim 19 comprising plating a conductive material on at least a portion of the circuit geometry.

22. The method of claim 19 wherein printing the conductive material comprises:

printing a conductive material in the recesses; and

sintering the conductive material.

23. The method of claim 19 wherein printing the conductive material comprises printing a conductive ink in the recesses.

24. The method of claim 19 comprising printing a compliant material in a location between the polymeric film and at least a portion of the circuit geometry.

25. The method of claim 24 comprising aligning the printed compliant material with an opening in the dielectric covering layer.

26. The method of claim 19 comprising:

printing at least one electrical device on one of a dielectric layer or the polymeric film; and

electrically coupled the electrical device to at least a portion of the circuit geometry.

27. The method of claim 19 comprising printing an optical quality material in at least a portion of the recesses comprising one or more optical circuit geometries.

28. The method of claim 19 comprising locating one or more optical fibers in at least a portion of the recesses comprising one or more optical circuit geometries.

29. The method of claim 19 comprising printing at least one via in a dielectric layer to electrically couple adjacent layers of the circuit geometry.

30. The method of claim 19 comprising printing one or more contact members that extends above the dielectric covering layer and electrically couple to at least a portion of the circuit geometry.

31. The method of claim 30 comprising singulating at least a portion of the compliant printed flexible circuit adjacent at least one of the contact members.

32. The method of claim 19 comprising:

printing one or more contact members that extend above a first surface of the compliant printed flexible circuit and electrically couple to at least a portion of the circuit geometry; and

printing at least one compliant member on a second surface of the compliant printed flexible circuit opposite at least one of the contact members.

33. The method of claim 19 wherein conductive traces in the circuit geometry comprise substantially rectangular cross-sectional shapes.

34. The method of claim 19 comprising printing a conductive material, a non-conductive material, and a semi-conductive material is printed on a single layer.

35. The method of claim 19 comprising the steps of:

locating pre-formed conductive trace materials in the recesses; and

plating the recesses to form conductive traces with substantially rectangular cross-sectional shapes.

36. The method of claim 19 comprising the steps of:

pressing a conductive foil into at least a portion of the recesses;

shearing the conductive foil along edges of the recesses;

removing excess conductive foil not located in the recesses; and

plating the recesses to form conductive traces with substantially rectangular cross-sectional shapes.

37. A method of making an edge connector for a compliant printed flexible circuit made according to claim 19 comprising the steps of:

printing a first portion of the circuit geometry beyond the dielectric covering layer;

printing a compliant material along a surface of the first portion of the circuit geometry; and

printing a second portion of the circuit geometry on top of the compliant material.

38. A method of making an electrical interconnect assembly comprising the steps of:

retaining a compliant printed flexible circuit made according to the method of claim 19 in a housing;

compressively coupling electrical contacts on a first circuit member with contact members located along a first surface of the compliant printed flexible circuit; and

compressively coupling electrical contacts on a second circuit member with contact members located along a second surface of the compliant printed flexible circuit.

39. The method of claim 38 wherein the first and second circuit members are selected from one of a dielectric layer, a printed circuit board, a flexible circuit, a bare die device, an integrated circuit device, organic or inorganic substrates, or a rigid circuit.

40. The method of claim 19 comprising the steps of:

printing at least one opening extending through the compliant printed flexible circuit; and

inserting at least one contact member into the opening and electrically coupling the contact member with at least a portion of the circuit geometry.

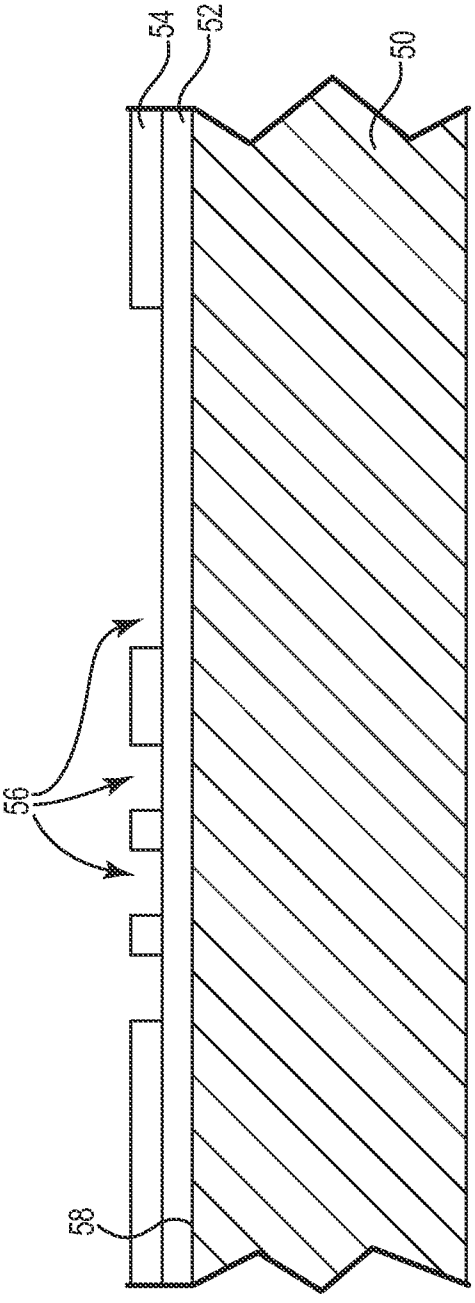

Fig. 1

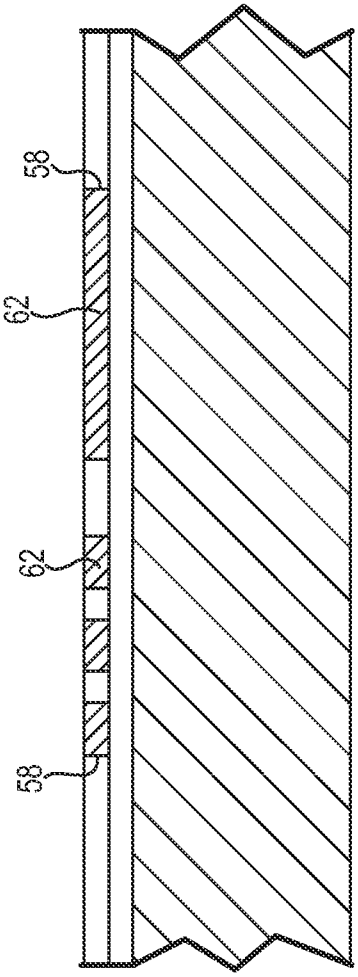

Fig. 2

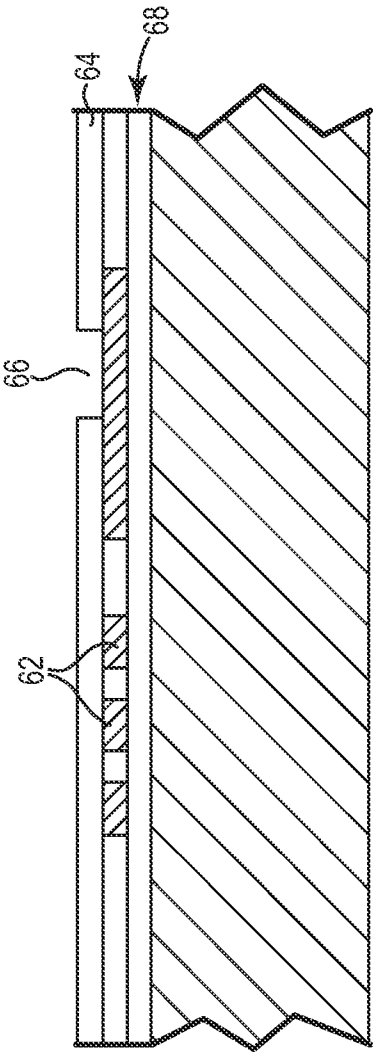

Fig. 3

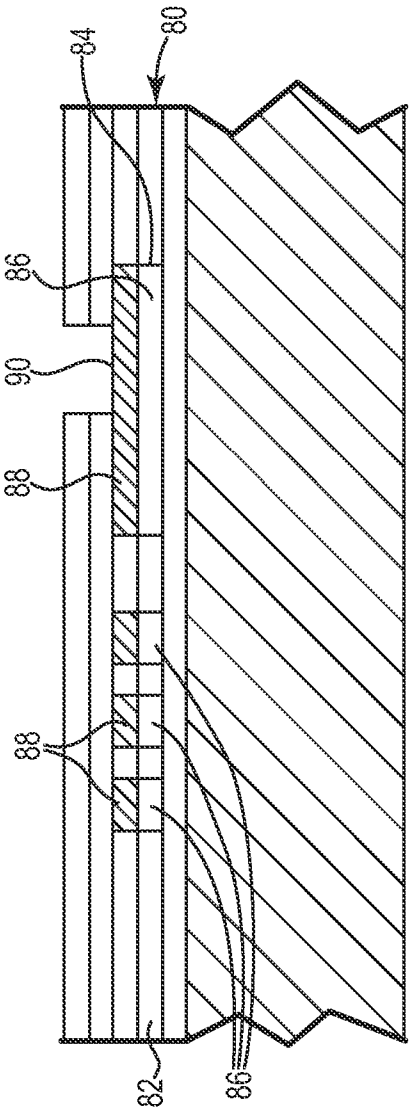

Fig. 4

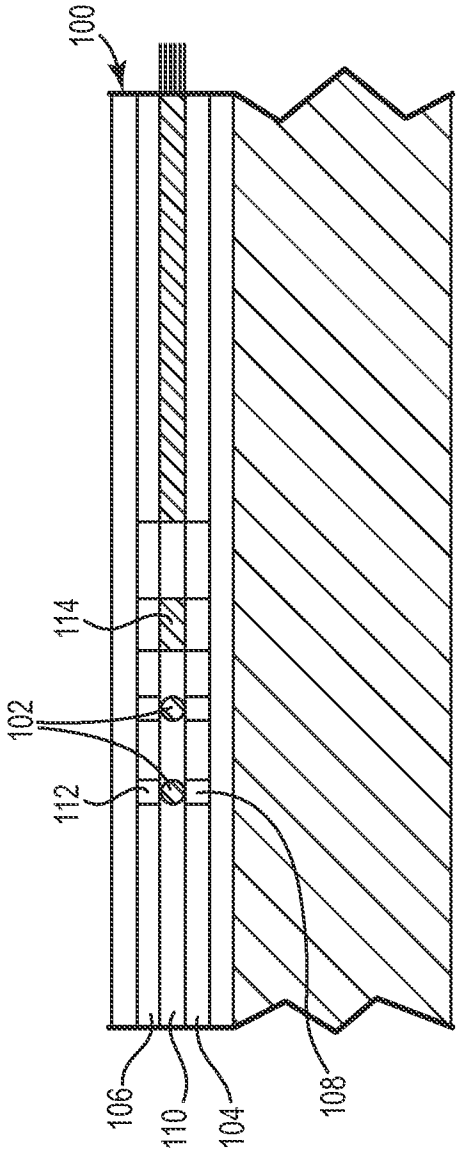

Fig. 5

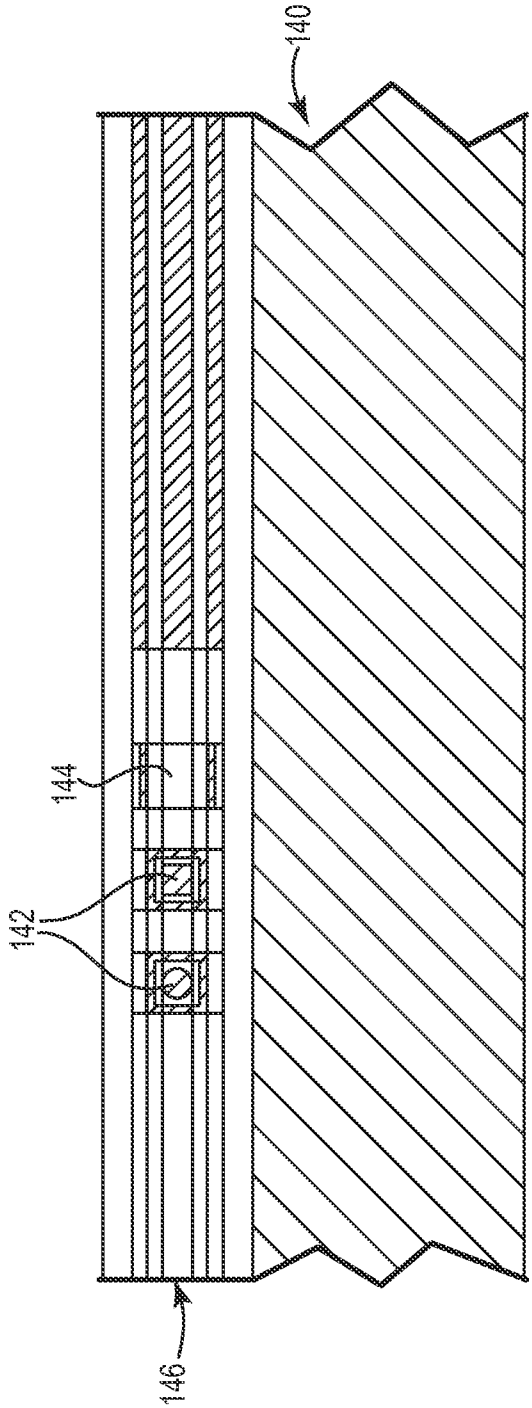

Fig. 6

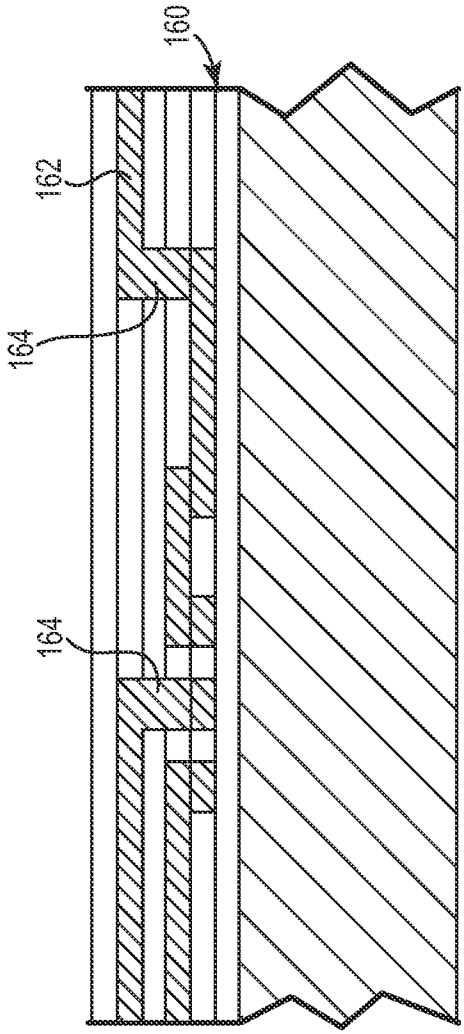

Fig. 7

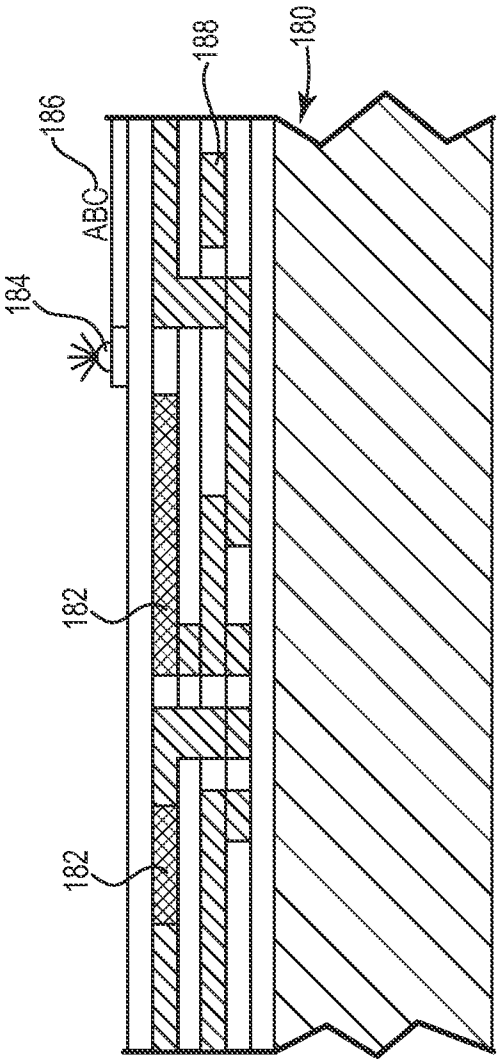

Fig. 8

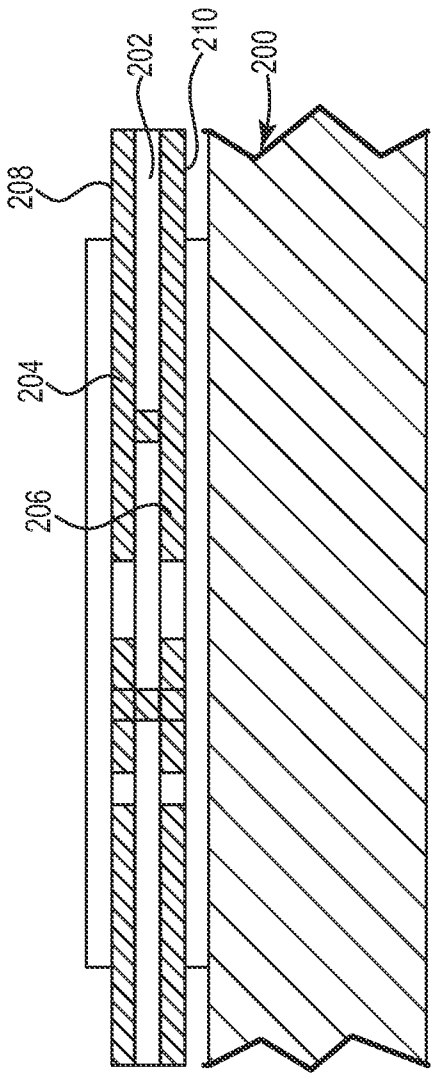

Fig. 9

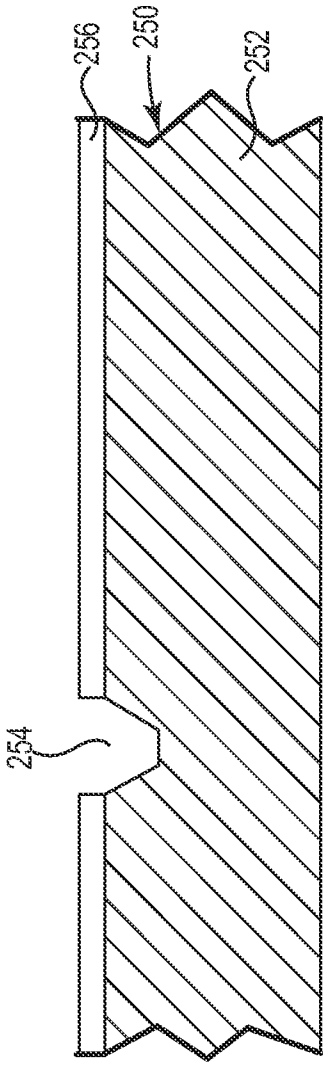

Fig. 10

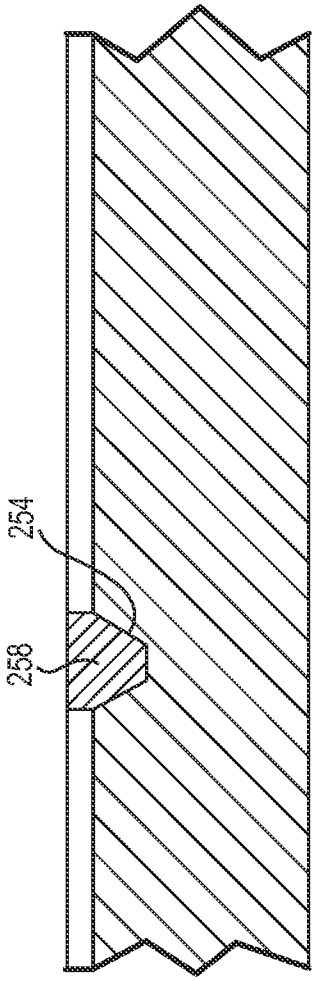

Fig. 11

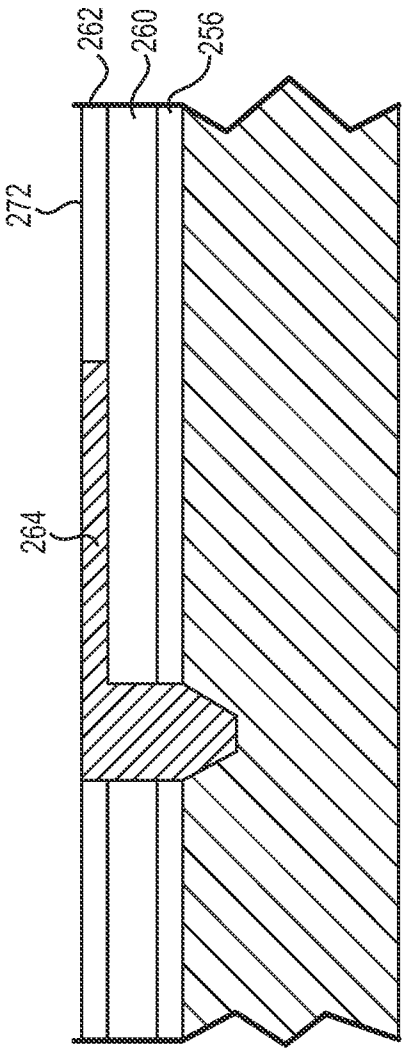

Fig. 12

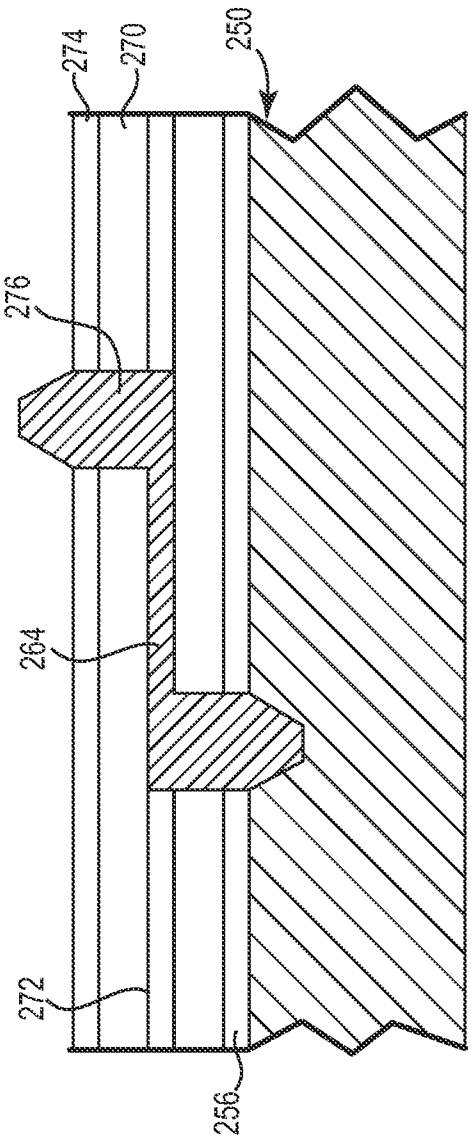

Fig. 13

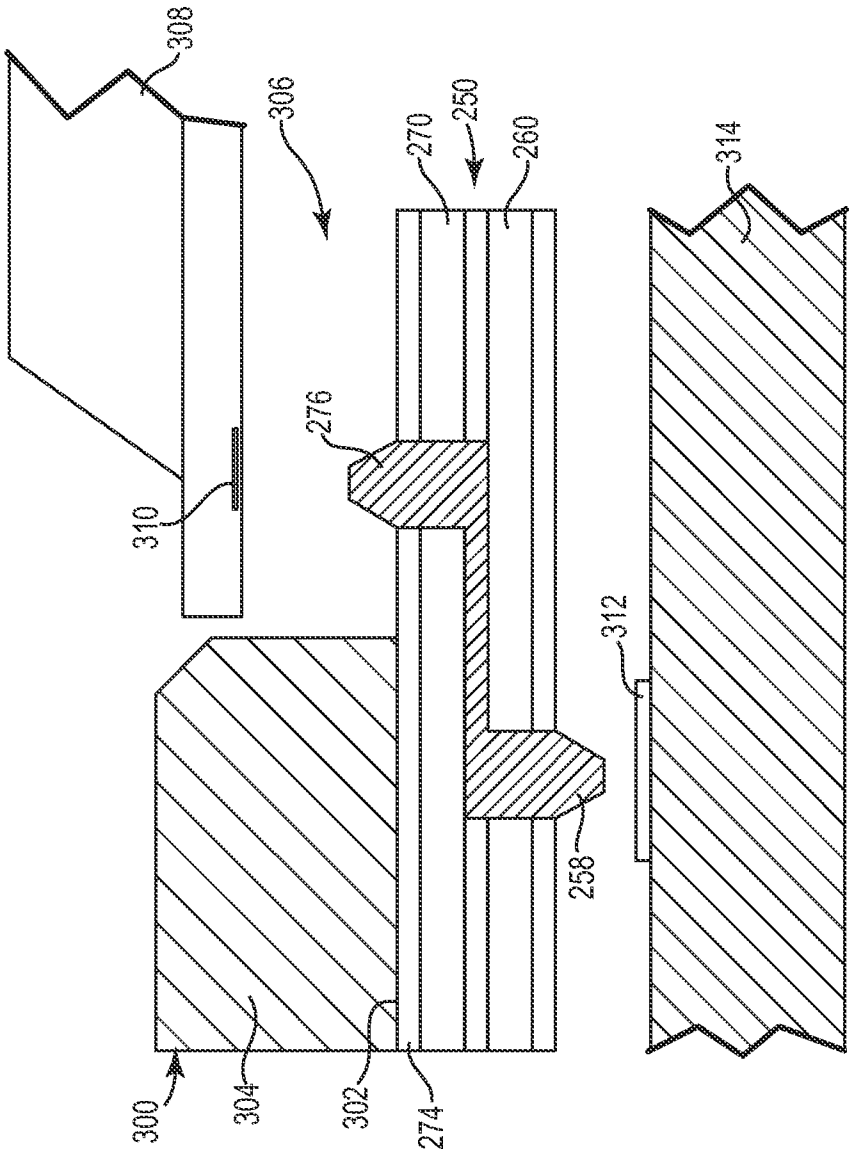

Fig. 14

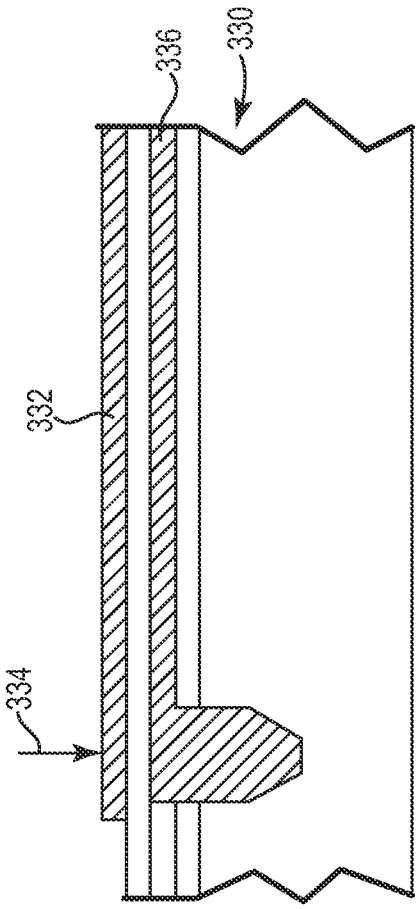

Fig. 15

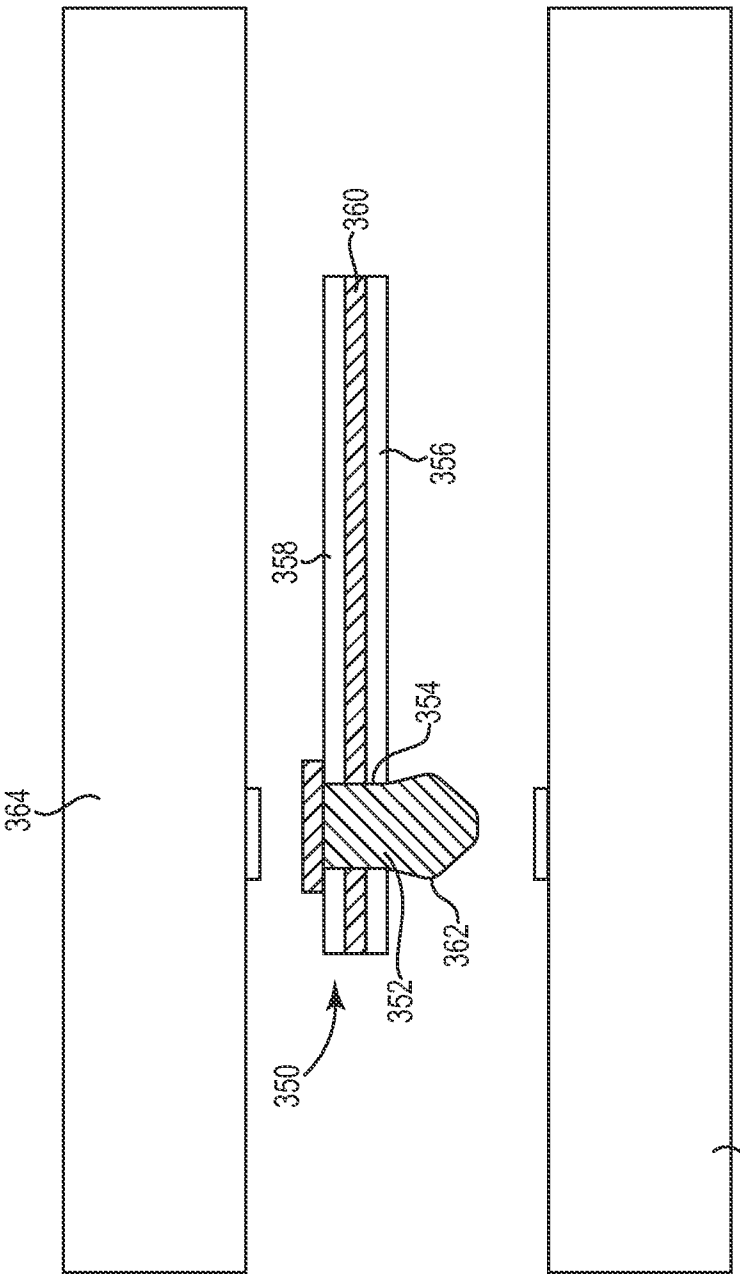

Fig. 16

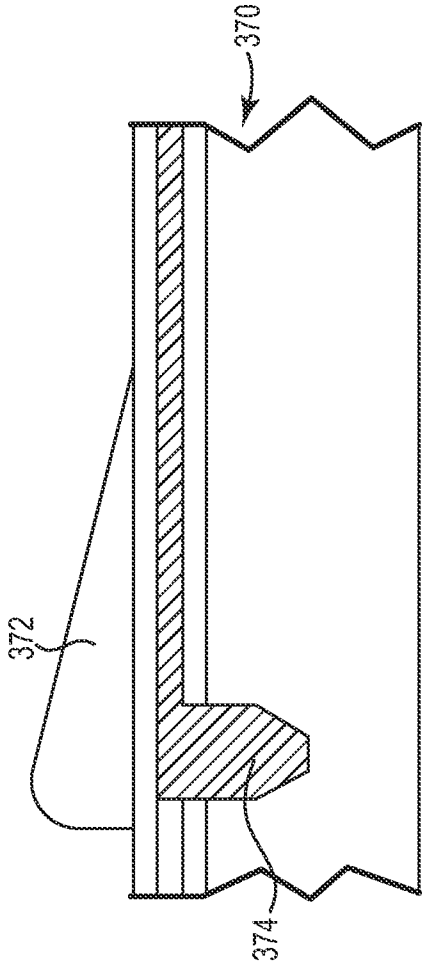

Fig. 17

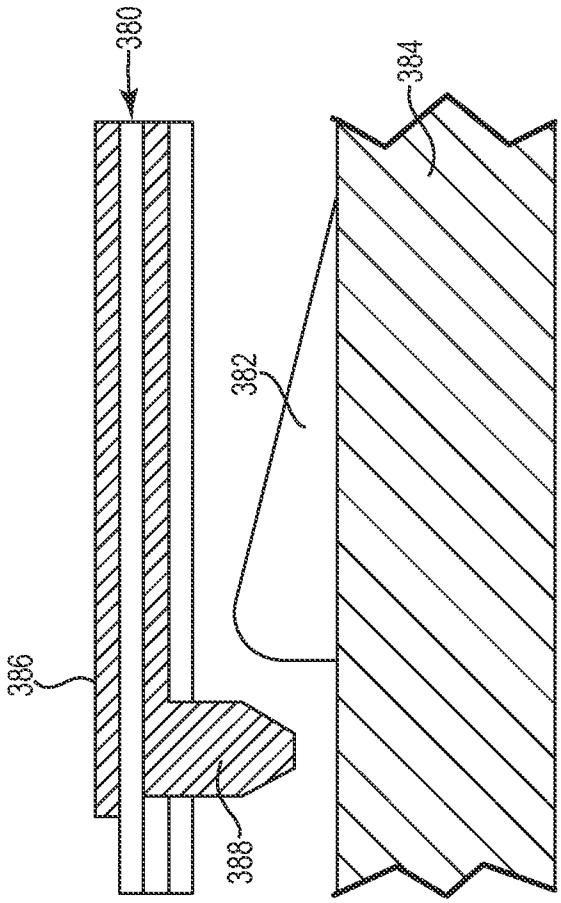

Fig. 18

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/036282

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 23/04 (2010.01)
USPC - 257/698
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 23/04, 23/12 (2010.01)
USPC - 257/698, 730, E23.023, E23.151

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/0127698 A1 (RATHBURN) 21 May 2009 (21.05.2009) entire document	1-2, 4, 6, 9-10, 12, 14, 16-21, 26, 29-30, 34 and 40
Y		3, 5, 7-8, 11, 13, 15, 22-25, 27-28, 31-33 and 35-39
Y	US 2008/0143358 A1 (BREINLINGER) 19 June 2008 (19.06.2008) entire document	3, 7-8, 11, 13, 23, 27-28, 31, 33 and 35
Y	US 5,913,109 A (DISTEFANO et al) 15 June 1999 (15.06.1999) entire document	5, 15, 24-25, 32, 37-39
Y	US 6,661,084 B1 (PETERSON et al) 09 December 2003 (09.12.2003) entire document	22 and 36
A	US 2006/0258912 A1 (BELSON et al) 16 November 2006 (16.11.2006) entire document	1-40

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 July 2010	30 JUL 2010
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774