A sample and hold circuit architecture samples using two capacitors that are cyclically switched between charge and discharge modes. The sample and hold circuit includes a buffer to receive an input signal to be sampled, a first sampling capacitor, a second sampling capacitor, and an amplifier. The first sampling capacitor is connected to the output of the buffer during the positive phase of a clock and across the feedback path of the amplifier during the zero phase of the clock. The second sampling capacitor is connected to the output of the buffer during the zero phase of the clock and across the feedback path of the amplifier during the positive phase of the clock. Neither the first sampling capacitor nor the second sampling capacitor is simultaneously connected to the buffer, the amplifier, or to each other.
**INTERNATIONAL SEARCH REPORT**

**International application No**
PCT/US2007/063470

**A. CLASSIFICATION OF SUBJECT MATTER**

| INV. | 611C27/02 |

**FIELD OF CLASSIFICATION**

- A 340, T 2280, Θ 2040, Θ 651

**TERMINATION**

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**Category**

- A
- B
- C
- D

**DOCUMENTS CONSIDERED TO BE RELEVANT**

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<td>Y</td>
<td>paragraph [0021] - paragraph [0028]; figures 1-3; paragraph [0031]; figures 5A,5B</td>
<td>13-20</td>
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<td>paragraph [0006] - paragraph [0049]; figures 3-12</td>
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**D**

Further documents are listed in the continuation of Box C

**X** See patent family annex

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**Date of the actual completion of the international search**

10 July 2007

**Date of mailing of the international search report**

06. 09. 2007

**Name and mailing address of the ISA/**

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Colling, Pierre

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<td>US 2005073351 A1</td>
<td>07-04-2005</td>
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