



(51) International Patent Classification:

H01L 33/12 (2010.01) H01L 33/22 (2010.01)
H01L 33/20 (2010.01)

(21) International Application Number:

PCT/KR2014/006091

(22) International Filing Date:

8 July 2014 (08.07.2014)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

10-2013-0088170 25 July 2013 (25.07.2013) KR

(71) Applicant: SEOUL VIOSYS CO., LTD. [KR/KR]; 1B-36, 65-16, Sandan-ro 163beon-gil, Danwon-gu, Ansan-si, Gyeonggi-do 425-851 (KR).

(72) Inventors: KIM, Chang Yeon; 1B-36, 65-16, Sandan-ro 163beon-gil, Danwon-gu, Ansan-si, Gyeonggi-do 425-851 (KR). CHOI, Joo Won; 1B-36, 65-16, Sandan-ro 163beon-gil, Danwon-gu, Ansan-si, Gyeonggi-do 425-851 (KR).

(74) Agent: AIP PATENT & LAW FIRM; 30-1, Teheran-ro 14-gil, Gangnam-gu, Seoul 135-933 (KR).

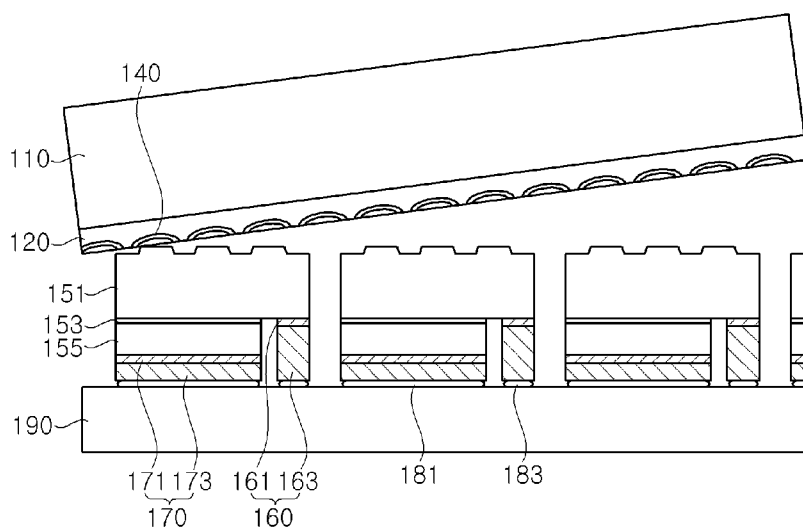
(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: METHOD OF FABRICATING LIGHT EMITTING DEVICE



(57) Abstract: Disclosed herein is a method of fabricating a light emitting device. The method includes forming a sacrificial layer on a growth substrate; forming a mask pattern on the sacrificial layer; partially removing the sacrificial layer to form fine voids within the sacrificial layer; forming a plurality of light emitting structures on the sacrificial layer while forming voids within the sacrificial layer, the plurality of light emitting structures covering at least a portion of the mask pattern and being separated from each other; bonding a sub-mount onto the plurality of light emitting structures; and separating the growth substrate from the plurality of light emitting structures via chemical lift-off or stress lift-off, wherein the growth substrate is monolithically separated from the plurality of light emitting structures. Thus, the method of fabricating a light emitting device has improved processability and productivity.

Description

Title of Invention: METHOD OF FABRICATING LIGHT EMITTING DEVICE

Technical Field

- [1] The present invention relates to a method of fabricating a light emitting device, and more particularly, to a method of fabricating a light emitting device, which is formed by separating a growth substrate from a plurality of light emitting structures.

Background Art

- [2] Light emitting devices refer to inorganic semiconductor devices configured to emit light through recombination of electrons and holes, and have been recently applied to various fields including displays, automobile lamps, general luminaires, and the like.
- [3] The light emitting devices can be classified into horizontal type, vertical type, and flip-chip type light emitting devices according to structures thereof.
- [4] A horizontal type light emitting device includes a growth substrate disposed beneath semiconductor layers and can be relatively easily fabricated. However, in the horizontal type light emitting device, since the growth substrate is disposed below an active layer, it is difficult to achieve efficient dissipation of heat generated during light emission. Particularly, a sapphire substrate generally used as the growth substrate of the horizontal type light emitting device has very low thermal conductivity, so that a bonding temperature of the light emitting device increases, thereby causing efficiency droop of the light emitting device. In addition, the horizontal type light emitting device necessarily includes wires connected to the semiconductor layers, whereby an encapsulation material encapsulating the light emitting device is deteriorated by heat generated from the wires, thereby causing deterioration in efficiency and reliability of the light emitting device. Accordingly, the horizontal type light emitting device is not suitable for a high output light emitting device to which high density current is applied.
- [5] To overcome such drawbacks of the horizontal type light emitting device, a flip-chip type light emitting device directly bonded onto a sub-mount via bumps and the like instead of the wires can be used. The flip-chip type light emitting device includes electrodes directly bonded onto the sub-mount and does not employ wires, thereby providing much higher heat dissipation efficiency than the horizontal type light emitting device. Accordingly, the flip-chip type light emitting device allows effective conduction of heat towards the sub-mount upon application of high density current, and thus can be suitably applied to high output light emitting devices.
- [6] However, since the flip-chip type light emitting device has the growth substrate disposed on a light exit face, the flip-chip type light emitting device suffers from dete-

rioration in light extraction efficiency due to the growth substrate. To solve such problems of the flip-chip type light emitting device, the growth substrate is removed from the semiconductor layers. For example, US Patent No. 8,329,482 B2 and the like disclose a flip-chip type light emitting device fabricated by removing the growth substrate from the semiconductor layers.

[7] In the flip-chip type light emitting device disclosed in US Patent No. 8,329,482 B2, the growth substrate is removed from the semiconductor layers by a physical method, such as grinding or etching, or laser lift-off. However, when the growth substrate is simultaneously separated from a plurality of light emitting device units by such a conventional separation method, there are problems such as breakage of the growth substrate or damage to the semiconductor layers. Accordingly, as disclosed in US Patent No. 8,329,482 B2 and the like, a method of separating the growth substrate from the semiconductor layers after dividing into a plurality of light emitting device units is used in the art.

[8] As a result, in the conventional method of fabricating a flip-chip type light emitting device, the growth substrate has to be separated from individual light emitting device units, thereby providing a very complicated process and making it difficult to reuse the growth substrate. Moreover, use of an expensive substrate such as a GaN substrate as the growth substrate causes increase in manufacturing costs because the growth substrate cannot be reused. Therefore, there is a need for a method of fabricating a light emitting device that provides improved processability and productivity.

Disclosure of Invention

Technical Problem

[9] Aspects of the present invention provide a method of fabricating a light emitting device, which enables easy separation of a growth substrate from a plurality of light emitting structures.

[10] Other aspects of the present invention provide a method of fabricating a light emitting device, which enables efficient fabrication of a plurality of light emitting devices.

[11] Further, other aspects of the present invention provide a method of fabricating a light emitting device, which enables reuse of a growth substrate separated from light emitting light emitting structures.

Solution to Problem

[12] In accordance with one aspect of the present invention, a method of fabricating a light emitting device comprises: forming a sacrificial layer on a growth substrate; forming a mask pattern on the sacrificial layer; forming fine voids within the sacrificial layer by partially removing the sacrificial layer; forming a plurality of light emitting

structures on the sacrificial layer while forming voids within the sacrificial layer, the plurality of light emitting structures at least partially covering the mask pattern and being separated from each other; bonding a sub-mount onto the plurality of light emitting structures; and separating the growth substrate from the plurality of light emitting structures using chemical lift-off or stress lift-off, wherein the growth substrate is monolithically separated from the plurality of light emitting structures, and each of the light emitting structures comprises a first conductive type semiconductor layer, a second conductive type semiconductor layer disposed on the first conductive type semiconductor layer, and an active layer interposed between the first and second conductive type semiconductor layers, and the second conductive type semiconductor layer and the active layer are partially removed to expose a portion of the first conductive type semiconductor layer.

- [13] In this way, the method according to the present invention enables monolithic separation of the growth substrate from the plurality of light emitting structures, thereby providing improved processability and productivity.
- [14] The method may further comprise dividing the sub-mount into a plurality of individual light emitting device units so as to correspond to the respective light emitting structures, after separating the growth substrate from the plurality of light emitting structures.
- [15] The method may further comprise forming a first electrode on an exposed region of the first conductive type semiconductor layer and a second electrode on the second conductive type semiconductor layer, before bonding the sub-mount, wherein the sub-mount may be bonded onto the first and second electrodes.
- [16] The first electrode may comprise a first electrode pad and a first bump, and the second electrode may comprise a second electrode pad and a second bump. An upper surface of the first electrode is flush with an upper surface of the second electrode.
- [17] The sub-mount may comprise a first lead and a second lead electrically connected to the first electrode and second electrode, respectively.
- [18] The using of chemical lift-off may comprise at least partially removing the mask pattern by chemical etching.
- [19] Partial removal of the sacrificial layer to form the fine voids may comprise etching the sacrificial layer via electrochemical etching (ECE), chemical etching (CE), or photo enhanced chemical etching (PEC).
- [20] The voids may be formed by combination or expansion of the fine voids.
- [21] In some embodiments, one surface of the first conductive type semiconductor layer exposed by separation of the growth substrate may comprise a roughness structure.
- [22] The method may further comprise forming a fine roughness structure on the one surface of the first conductive type semiconductor layer exposed by separation of the

growth substrate.

[23] The formation of the fine roughness structure may comprise performing at least one of wet etching and dry etching on the one exposed surface of the first conductive type semiconductor layer to form the fine roughness structure.

[24] In other embodiments, the method may further comprise removing the one exposed surface of the first conductive type semiconductor layer to a predetermined thickness, before forming the fine roughness structure.

[25] The growth substrate may be a nitride substrate.

[26] The method may further comprise forming an insulation layer filling a space between the first electrode and side surfaces of the second conductive type semiconductor layer and the active layer.

Advantageous Effects of Invention

[27] According to the present invention, the method enables monolithic separation of a growth substrate from a plurality of light emitting structures, thereby providing a simple process, reducing process costs, and enabling easy manufacture of plural light emitting devices through a single process. As a result, the method of fabricating a light emitting device has improved processability and productivity.

Brief Description of Drawings

[28] Figures 1 to 12 are sectional views illustrating a method of fabricating a light emitting device in accordance with one embodiment of the present invention.

Mode for the Invention

[29] Hereinafter, embodiments of the present invention will be described in more detail with reference to the accompanying drawings. It should be understood that the following embodiments are given by way of illustration only to provide a thorough understanding of the invention to those skilled in the art. Therefore, the present invention is not limited to the following embodiments and may be embodied in different ways. Further, the widths, lengths, and thicknesses of certain elements, layers or features may be exaggerated for clarity.

[30] It will be understood that when an element or layer is referred to as being "on" or "connected to" another element or layer, it can be directly on or directly connected to the other element or layer, or intervening elements or layers may be present. In contrast, when an element is referred to as being "directly on" or "directly connected to" another element or layer, there are no intervening elements or layers present. It will be understood that for the purposes of this disclosure, "at least one of X, Y, and Z" can be construed as X only, Y only, Z only, or any combination of two or more items X, Y, and Z (e.g., XYZ, XYY, YZ, ZZ).

[31] Like components will be denoted by like reference numerals throughout the speci-

fication

- [32] Figures 1 to 12 are sectional views illustrating a method of fabricating a light emitting device in accordance with one embodiment of the present invention.
- [33] Referring to Figure 1, a sacrificial layer 120 is formed on a growth substrate 110.
- [34] The growth substrate 110 may be any substrate on which epitaxial layers 150 can be grown. For example, the growth substrate 110 may be a sapphire substrate, a SiC substrate, a silicon substrate, a GaN substrate, an AlN substrate, and the like. In this embodiment, the growth substrate 110 may be a nitride substrate.
- [35] The sacrificial layer 120 may comprise a nitride semiconductor such as (Al, Ga, In)N, and may be grown on the growth substrate 110 by metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), hydride vapor phase epitaxy (HVPE), or the like. In addition, the sacrificial layer 120 may comprise an N-type or P-type nitride semiconductor layer, which has a high concentration of impurities. For example, the sacrificial layer 120 may be an N-type GaN layer, which is doped with Si in a concentration of $3 \times 10^{18}/\text{cm}^3$ or more, preferably in a concentration of $3 \times 10^{18}/\text{cm}^3$ to $3 \times 10^{19}/\text{cm}^3$. As the sacrificial layer 120 has N-type or P-type conductivity, it is possible to form fine voids 141 in the sacrificial layer 120 through electrochemical etching (ECE) described below.
- [36] Next, referring to Figure 2, a mask pattern 130 is formed on the sacrificial layer 120.
- [37] The mask pattern 130 comprises a plurality of openings 131, through which the sacrificial layer 120 is partially exposed. The mask pattern 130 may comprise an insulation material, for example, SiO_2 .
- [38] The mask pattern 130 may be formed on the sacrificial layer 120 by a deposition process. For example, the mask pattern 130 may be formed on the sacrificial layer 120 by depositing a SiO_2 layer on the sacrificial layer 120 by e-beam evaporation, followed by patterning the SiO_2 layer to form the openings 131. Alternatively, the mask pattern 130 comprising the openings 131 may be formed on the sacrificial layer 120 by deposition using a photoresist pattern and lift-off.
- [39] In addition, the mask pattern 130 comprising the openings 131 may have various pattern shapes. For example, with respect to an upper surface of the growth substrate 110, the mask pattern 130 may have a stripe shape, an island shape, a mesh shape, and the like. Here, the present invention is not limited thereto, and the mask pattern 130 may be formed in various shapes as needed. According to the pattern shape of the mask pattern 130, a region of the sacrificial layer 120 to be partially removed by the following process will be defined. This will be described in more detail below.
- [40] Referring to Figure 3, the sacrificial layer 120 is partially removed to form the fine voids within the sacrificial layer 120. Partial removal of the sacrificial layer 120 may comprise partially etching the sacrificial layer 120 using, for example, electrochemical

etching (ECE). As a result, the fine voids 141 can be formed within the sacrificial layer 120 in regions under the openings 131 and regions adjacent thereto.

[41] For electrochemical etching, first, etching electrodes (not shown) are formed on the sacrificial layer 120. For example, three In (indium) electrodes separated from each other are formed thereon to be electrically connected to the sacrificial layer 120. Then, the growth substrate 110 having the sacrificial layer 120 formed thereon and a negative electrode (for example, a Pt electrode) are dipped in a solution. The solution may be an electrolyte solution, which comprises, for example, oxalic acid, HF or NaOH. In addition, when a predetermined voltage is applied to the etching electrodes and the negative electrode, the sacrificial layer 120 is partially etched, thereby forming the fine voids 141, as shown in Figure 3. In the electrochemical etching process, the mask pattern may act as an etching mask, whereby the fine voids 141 can be mainly formed within the sacrificial layer 120 in the regions under the openings 131 and the regions adjacent thereto.

[42] In the electrochemical etching process, the size and shape of the fine voids 141 can be adjusted by selectively controlling the composition and concentration of the solution, voltage application time, and applied voltage. For example, the fine voids 141 may be formed by partially etching the sacrificial layer 120 through continuous application of a voltage in the range of 10~60V, or through sequential application of different voltages in two stages. For example, a voltage of 9V may be applied for 180 seconds in a first stage electrochemical etching process and a voltage of 16.5V may be applied for 180 seconds in a second stage electrochemical etching process. As a result, relatively small fine voids can be initially formed and then relatively large fine voids can be formed, as shown in Figure 3.

[43] With the two-stage electrochemical etching process, the surface of the sacrificial layer 120 can maintain good crystallinity, and relatively large fine voids can be formed within the sacrificial layer 120, thereby providing advantages to the subsequent process.

[44] On the other hand, the etching electrodes (not shown) may be separately removed after completion of electrochemical etching. In addition, regions of the sacrificial layer 120 under the etching electrodes may be removed by etching. The fine voids 141 formed in the regions of the sacrificial layer 120 under the etching electrodes may have a lower density than those of other regions, or few fine voids may be formed in the regions of the sacrificial layer 120 under the etching electrodes. The regions of the sacrificial layer 120 having a low density of the fine voids 141 can obstruct separation of the growth substrate 110 in a process of separating the growth substrate 110 described below. Accordingly, after completion of electrochemical etching, the etching electrodes and the regions of the sacrificial layer 120 under the etching electrodes may

be removed to facilitate separation of the growth substrate 110.

[45] In this embodiment, the fine voids 141 are formed by electrochemical etching.

However, the present invention is not limited thereto. For example, the fine voids 141 may be also formed by chemical etching (CE), photo enhanced chemical etching (PEC), and the like.

[46] Referring to Figures 4 to 6, a plurality of light emitting structures 100 separated from each other is formed on the sacrificial layer 120 to cover at least a portion of the mask pattern 130. In addition, voids 140 may be formed in the sacrificial layer 120.

[47] Specifically, referring to Figure 4, a first conductive type semiconductor layer 151 covering the mask pattern 130 is formed on the sacrificial layer 120.

[48] The first conductive type semiconductor layer 151 may comprise a nitride semiconductor layer such as (Al, Ga, In)N, and may be grown on the sacrificial layer 120 by MOCVD, MBE, HVPE, or the like. The first conductive type semiconductor layer 151 may be grown using exposed regions of the sacrificial layer 120 under the openings 131 as seeds. Thus, lateral overgrowth also occurs in formation of the first conductive type semiconductor layer 151. Such growth of the first conductive type semiconductor layer 151 including lateral overgrowth provides good crystallinity.

[49] In addition, during growth of the first conductive type semiconductor layer 151, the fine voids 141 may combine with each other or expand to form the voids 140. The voids 140 have a larger scale than the fine voids 141. The voids 140 are mainly formed in regions in which the fine voids 141 have been formed, and may be formed to have an enlarged area over the regions in which the fine voids 141 have been formed. The voids 140 may be mainly formed in the regions of the sacrificial layer 120 under the openings 131.

[50] Then, referring to Figure 5, an active layer 153 and a second conductive type semiconductor layer 155 are formed on the first conductive type semiconductor layer 151.

[51] The active layer 153 and the second conductive type semiconductor layer 155 may comprise nitride semiconductor layers such as (Al, Ga, In)N, and may be grown on the first conductive type semiconductor layer 151 by MOCVD, MBE, HVPE, or the like.

[52] The active layer 153 may have a multi-quantum well (MQW) structure, and the elements and composition of semiconductor layers forming the multi-quantum well structure may be adjusted such that light having a desired peak wavelength can be emitted from the semiconductor layers. The first conductive type semiconductor layer 151 may be an N-type semiconductor layer, which is doped with N-type impurities (for example, Si), and the second conductive type semiconductor layer 155 may be a P-type semiconductor layer, which is doped with P-type impurities (for example, Mg), or vice versa. In addition, the first conductive type semiconductor layer 151 may comprise an undoped layer and a doped layer. When the first conductive type semiconductor layer

151 is formed, the undoped layer is first formed and then the doped layer is formed, whereby the first conductive type semiconductor layer 151 comprises multiple layers. In this way, the undoped layer is first formed in formation of the first conductive type semiconductor layer 151, thereby improving crystallinity of the first conductive type semiconductor layer 151.

[53] In this way, the first conductive type semiconductor layer 151, the active layer 153 and the second conductive type semiconductor layer 155 are grown, thereby forming the epitaxial layers 150 on the growth substrate 110.

[54] Hereinafter, with regard to the semiconductor layers 151, 153, 155 including nitride semiconductor materials, descriptions of details apparent to a person having ordinary knowledge in the art (hereinafter, "those skilled in the art") will be omitted.

[55] The method according to this embodiment may further comprise forming a transparent electrode layer (not shown) on the second conductive type semiconductor layer 155. The transparent electrode layer may comprise an ITO layer. The transparent electrode layer can improve current spreading of the light emitting device fabricated by the method according to the present invention.

[56] Referring to Figure 6, the epitaxial layers 150 are partially removed to form isolation trenches 210. The isolation trenches 210 partially expose the upper surface of the sacrificial layer 120 and the mask pattern 130, and isolate the plurality of light emitting structures 100 from each other. In addition, for each of the light emitting structures 100, the second conductive type semiconductor layer 155 and the active layer 153 are partially removed to expose a portion of the upper surface of the first conductive type semiconductor layer 151. As a result, each of the plural light emitting structures 100 comprises a mesa structure including the second conductive type semiconductor layer 155 and the active layer 153.

[57] The isolation trenches 210 may be formed by dry etching, such that the first conductive type semiconductor layer 151 on the growth substrate is divided into a plurality of first conductive type semiconductor layers 151 thereby.

[58] For each of the light emitting structures 100, partial removal of the second conductive type semiconductor layer 155 and the active layer 153 may be carried out by dry etching, which may be performed until the first conductive type semiconductor layer 151 is partially exposed. Thus, the mesa structure formed by this process comprises the second conductive type semiconductor layer 155 and the active layer 153, and may further comprise a portion of the first conductive type semiconductor layer 151. In Figure 6, the mesa structure has a side surface perpendicular to a horizontal plane. Alternatively, the mesa structure may have an inclined side surface.

[59] Referring to Figure 7, a first electrode 160 and a second electrode 170 may be formed on the first conductive type semiconductor layer 151 and the second

conductive type semiconductor layer 155 of each of the light emitting structures 100, respectively. The first electrode 160 and the second electrode 170 are electrically connected to the first conductive type semiconductor layer 151 and the second conductive type semiconductor layer 155, respectively.

- [60] The first and second electrodes 160, 170 may be formed by deposition and lift-off. For example, the first electrode 160 and the second electrode 170 may be formed by forming a photoresist pattern covering other regions excluding regions allocated to the first electrode 160 and the second electrode 170, followed by e-beam evaporation and removal of the photoresist pattern. However, it should be understood that the present invention is not limited thereto and various other methods known to those skilled in the art may be used.
- [61] The first electrode 160 comprises a first electrode pad 161 and a first bump 163. The first electrode pad 161 may be formed on the first conductive type semiconductor layer 151 to contact an upper surface thereof, and the first bump 163 is formed on the first electrode pad 161 such that the first electrode 160 can extend upwards from the surface of the first conductive type semiconductor layer 151. Further, the first electrode 160 may be separated from the side surface of the mesa structure, thereby preventing electrical short circuit.
- [62] The first electrode pad 161 and the first bump 163 may comprise metal, for example, at least one of Ni, Pt, Pd, Rh, W, Ti, Cr, Al, Ag and Au.
- [63] The second electrode 170 may comprise a second electrode pad 171 and a second bump 173. The second electrode pad 171 may be formed on the second conductive type semiconductor layer 155 to contact an upper surface of the second conductive type semiconductor layer 155 while partially covering the upper surface thereof, and the second bump 173 is formed on the second electrode pad 171 such that the second electrode 170 can extend upwards from the surface of the second conductive type semiconductor layer 155.
- [64] The second electrode pad 171 and the second bump 173 may comprise a metal, for example, at least one of Ni, Pt, Pd, Rh, W, Ti, Cr, Al, Ag and Au.
- [65] The first electrode 160 may be formed to have an upper surface coplanar with an upper surface of the second electrode 170. That is, the upper surface of the first electrode 160 is flush with the upper surface of the second electrode 170, thereby facilitating a sub-mount bonding process.
- [66] On the other hand, an insulation layer (not shown) may be further formed to fill a space between the first electrode 160 and the side surface of the mesa structure. The insulation layer can more effectively prevent short circuit of the light emitting device due to electrical contact between the first electrode 160 and the second conductive type semiconductor layer 155 or the active layer 153.

- [67] In addition, the insulation layer can support the first conductive type semiconductor layer 151 by filling the space between the first electrode 160 and the mesa structure. Accordingly, when the growth substrate 110 is separated from the light emitting structure 100, the insulation layer can prevent damage such as cracking of a region of the first conductive type semiconductor layer 151 on the space between the first electrode 160 and the mesa structure. Specifically, the region of the first conductive type semiconductor layer 151 on the space between the first electrode 160 and the mesa structure is relatively weakly supported and thus can be easily damaged due to concentration of stress during separation of the growth substrate 110. Thus, the insulation layer is formed to support this region of the first conductive type semiconductor layer, thereby preventing damage due to concentration of stress.
- [68] In addition, the method of fabricating a light emitting device according to the present invention may further comprise forming a reflective layer (not shown) on the second conductive type semiconductor layer 155 before forming the second electrode 170. The reflective layer can improve luminous efficacy by reflecting light emitted from the active layer 153.
- [69] The reflective layer may comprise a reflective metal layer (not shown) and a barrier metal layer (not shown). Here, the barrier metal layer may be formed to cover the reflective metal layer.
- [70] The reflective metal layer may serve to reflect light and may also act as an electrode electrically connected to the second conductive type semiconductor layer 155. Accordingly, the reflective metal layer preferably comprises a material having high reflectivity and capable of forming ohmic contact. The reflective metal layer may comprise a metal, for example, at least one of Ni, Pt, Pd, Rh, W, Ti, Al, Ag and Au. Further, the barrier metal layer prevents inter-diffusion between the reflective metal layer and other materials. Accordingly, the barrier metal can prevent increase in contact resistance and deterioration in reflectivity due to damage to the reflective metal layer. The barrier metal layer may comprise Ni, Cr and Ti, and may be formed as multiple layers. The reflective metal layer and the barrier metal layer including such metal may be formed by deposition such as e-beam evaporation and lift-off.
- [71] Referring to Figure 8, a sub-mount 190 is formed on a plurality of light emitting structures 100. The sub-mount 190 may be bonded onto the first electrode 160 and the second electrode 170 to be bonded onto the plurality of light emitting structures 100.
- [72] The plurality of light emitting structures 100 and the sub-mount 190 may be bonded onto each other via first and second bonding layers 181, 183. The first and second bonding layers 181 may be formed by solder bonding or eutectic bonding, and may comprise, for example, Ag, Au, Sn, Cu, and the like.
- [73] As for the sub-mount 190, any substrate capable of supporting the light emitting

structures 100 may be used. For example, the sub-mount 190 may comprise an insulation substrate, a conductive substrate, or a circuit substrate. Particularly, the sub-mount 190 may be an AlN substrate having high thermal conductivity, or a Si substrate having high processability.

- [74] The sub-mount 190 may comprise leads (for example, a first lead and a second lead) electrically connected to the first electrode 160 and the second electrode 170. For example, the sub-mount 190 may be a Si substrate including leads. As the sub-mount 190 comprises the leads, it is possible to fabricate a light emitting device package by dividing the sub-mount 190 into individual light emitting device units in the following process described below. Accordingly, it is also possible to fabricate a wafer-level package using the fabrication method according to the present invention.
- [75] Next, referring to Figure 9, the growth substrate 110 is separated from the plurality of light emitting structures 100.
- [76] Separation of the growth substrate 110 may be achieved by chemical lift-off or stress lift-off. It should be understood that the present invention is not limited thereto. Further, the growth substrate 110 is monolithically separated from the plurality of light emitting structures 100.
- [77] Thus, as compared with a conventional method by which the growth substrate is separated from each of individual light emitting device units, the present invention enables separation of the entirety of the growth substrate 110, that is, at the wafer level, thereby providing a simplified manufacturing process. Accordingly, the overall manufacturing process has improved productivity.
- [78] In addition, unlike the conventional technique in which the growth substrate 110 is divided into the individual light emitting device units and then separated from the semiconductor layers, the method according to the present invention allows monolithic separation of the growth substrate 110 from the plurality of light emitting structures 100, thereby enabling reuse of the separated growth substrate 110. Reuse of the growth substrate 110 can provide reduction of the overall process cost and, particularly, significant reduction in process cost in the case of using an expensive growth substrate such as a GaN substrate.
- [79] Separation of the growth substrate 110 by chemical lift-off may comprise at least partial removal of the mask pattern 130 by chemical etching. When the mask pattern 130 comprises SiO₂, the mask pattern 130 may be removed by etching with a buffered oxide etchant (BOE) or an etching solution containing HF. The etching solution can etch the mask pattern 130 while diffusing on the overall surface of growth substrate 110 through the voids 140 as etching channels. As at least a portion of the mask pattern 130 is removed, separation occurs at an interface between the sacrificial layer 120 and the first conductive type semiconductor layer 151. Furthermore, after removal of the

mask pattern 130, stress is further applied to the interface between the sacrificial layer 120 and the first conductive type semiconductor layer 151, whereby the growth substrate 110 can be more easily separated from the first conductive type semiconductor layer 151.

- [80] Separation of the growth substrate 110 by stress lift-off may comprise applying stress to the interface between the sacrificial layer 120 and the first conductive type semiconductor layer 151. Since formation of the voids 140 can cause weakened bonding between the sacrificial layer 120 and the first conductive type semiconductor layer 151, applied stress can be concentrated on the weakened portion. Accordingly, upon application of stress, cracks can be generated in the mask pattern 130 between the sacrificial layer 120 and the first conductive type semiconductor layer 151, and the mask pattern 130 can be separated and break by propagation of the cracks. As a result, the growth substrate 110 can be separated from the first conductive type semiconductor layer 151.
- [81] It should be understood that these methods of separating the growth substrate 110 are provided for illustration and separation of the growth substrate 110 using other methods known to those skilled in the art is also within the scope of the present invention.
- [82] Then, referring to Figure 10, roughness R1 is formed on the upper surface of the first conductive type semiconductor layer 151 exposed by separation of the growth substrate 110.
- [83] The roughness R1 is formed on the upper surface of the first conductive type semiconductor layer 151 corresponding to the shape of the mask pattern 130. In this way, since the roughness R1 can be naturally formed on the upper surface of the first conductive type semiconductor layer 151 simply by separation of the growth substrate 110, it is possible to enhance light extraction efficiency of the light emitting device without a separate process for forming roughness.
- [84] Referring to Figure 11, fine roughness R2 is additionally formed on the exposed surface of the first conductive type semiconductor layer 151.
- [85] The fine roughness R2 may have an uneven roughness pattern and may be formed by wet etching and the like. For example, the fine roughness R2 may be formed by photochemical etching, photo enhanced chemical etching, etching using a sulfuric-phosphoric acid solution, and the like. The size of the fine roughness R2 is determined in various ways according to etching conditions, and may have an average height of $0.5\ \mu\text{m}$ or less. Formation of the fine roughness R2 results in further improved light extraction efficiency of the semiconductor device fabricated by the method according to the present invention. Furthermore, the fine roughness R2 can be formed by at least one of wet etching and dry etching. For example, the fine roughness R2 may be formed

by forming a predetermined roughness pattern through dry etching, followed by wet etching, or otherwise, by dry etching the overall surface of the first conductive type semiconductor layer 151 without using the mask pattern after wet etching.

[86] On the other hand, before forming the fine roughness R2, the method may further comprise physically or chemically removing residues from the surface of the first conductive type semiconductor layer 151 and removing the surface of the first conductive type semiconductor layer 151 to a predetermined thickness.

[87] The surface of the first conductive type semiconductor layer 151 may be removed to a thickness of, for example, about 7 μm to about 9 μm by dry etching and the like. As a result, the roughness on the surface of the first conductive type semiconductor layer 151 may have a gentler slope than the roughness R1 before removal of the surface of the first conductive type semiconductor layer 151.

[88] Then, as shown in Figure 11, the sub-mount 190 is divided into a plurality of individual light emitting device 200 units along separation lines S in spaces between the plurality of light emitting structures 100 so as to correspond to the respective light emitting structures 100. As a result, a light emitting device 200 as shown in Figure 12 can be provided.

[89] Although some embodiments have been described above, the present invention is not limited to the aforementioned embodiments and features, and various modifications, changes, and alterations can be made without departing from the spirit and scope of the invention.

[90]

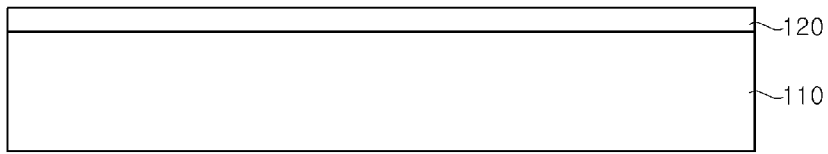
[91]

Claims

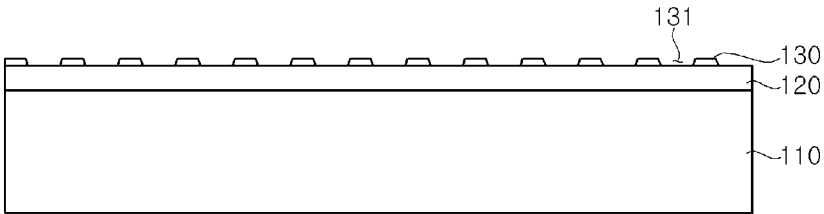
- [Claim 1] A method of fabricating a light emitting device, comprising:
forming a sacrificial layer on a growth substrate;
forming a mask pattern on the sacrificial layer;
forming fine voids within the sacrificial layer by partially removing the sacrificial layer;
forming a plurality of light emitting structures on the sacrificial layer while forming voids within the sacrificial layer, the plurality of light emitting structures at least partially covering the mask pattern and being separated from each other;
bonding a sub-mount onto the plurality of light emitting structures; and
separating the growth substrate from the plurality of light emitting structures using chemical lift-off or stress lift-off,
wherein the growth substrate is monolithically separated from the plurality of light emitting structures,
wherein each of the light emitting structures comprises a first conductive type semiconductor layer, a second conductive type semiconductor layer disposed on the first conductive type semiconductor layer, and an active layer interposed between the first and second conductive type semiconductor layers, and
the second conductive type semiconductor layer and the active layer are partially removed to expose a portion of the first conductive type semiconductor layer.
- [Claim 2] The method of claim 1, further comprising:
dividing the sub-mount into a plurality of individual light emitting device units so as to correspond to the respective light emitting structures, after separating the growth substrate from the plurality of light emitting structures.
- [Claim 3] The method of claim 1, further comprising:
forming a first electrode on an exposed region of the first conductive type semiconductor layer and a second electrode on the second conductive type semiconductor layer, before bonding the sub-mount, wherein the sub-mount is bonded onto the first and second electrodes.
- [Claim 4] The method of claim 3, wherein the first electrode comprises a first electrode pad and a first bump, and the second electrode comprises a second electrode pad and a second bump, and
an upper surface of the first electrode is flush with an upper surface of

- the second electrode.
- [Claim 5] The method of claim 3, wherein the sub-mount comprises a first lead and a second lead electrically connected to the first electrode and second electrode, respectively.
- [Claim 6] The method of claim 1, wherein the using of chemical lift-off comprises at least partially removing the mask pattern by chemical etching.
- [Claim 7] The method of claim 1, wherein partially removing the sacrificial layer to form the fine voids comprises etching the sacrificial layer via electrochemical etching (ECE), chemical etching (CE), or photo enhanced chemical etching (PEC).
- [Claim 8] The method of claim 7, wherein the voids are formed by combination or expansion of the fine voids.
- [Claim 9] The method of claim 1, wherein one surface of the first conductive type semiconductor layer exposed by separation of the growth substrate comprises a roughness structure.
- [Claim 10] The method of claim 9, further comprising:
forming a fine roughness structure on the one surface of the first conductive type semiconductor layer exposed by separation of the growth substrate.
- [Claim 11] The method of claim 10, wherein forming of the fine roughness structure comprises performing at least one of wet etching and dry etching on the exposed one surface of the first conductive type semiconductor layer.
- [Claim 12] The method of claim 10, further comprising:
removing the exposed one surface of the first conductive type semiconductor layer to a predetermined thickness, before forming the fine roughness structure.
- [Claim 13] The method of claim 1, wherein the growth substrate is a nitride substrate.
- [Claim 14] The method of claim 3, further comprising:
forming an insulation layer filling a space between the first electrode and side surfaces of the second conductive type semiconductor layer and the active layer.

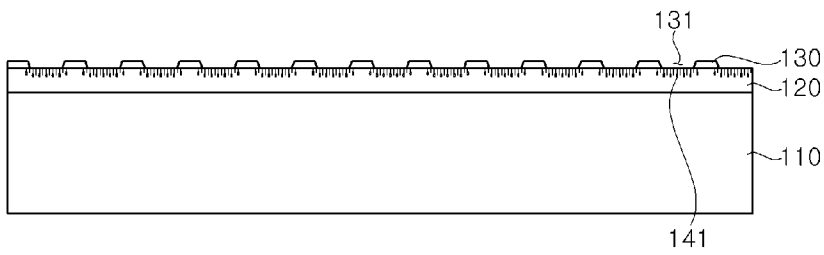
[Fig. 1]



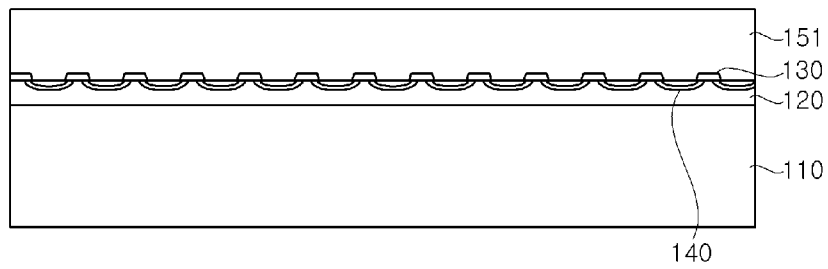
[Fig. 2]



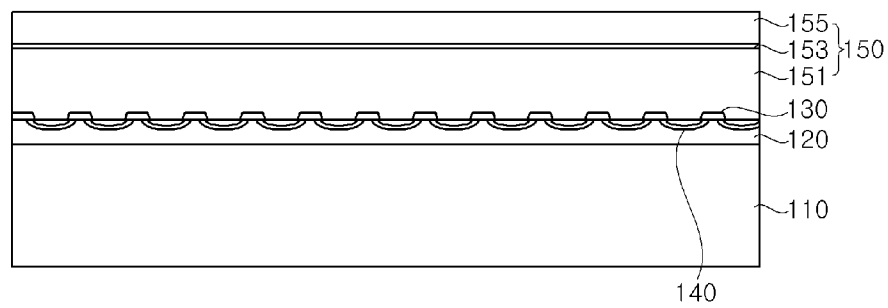
[Fig. 3]



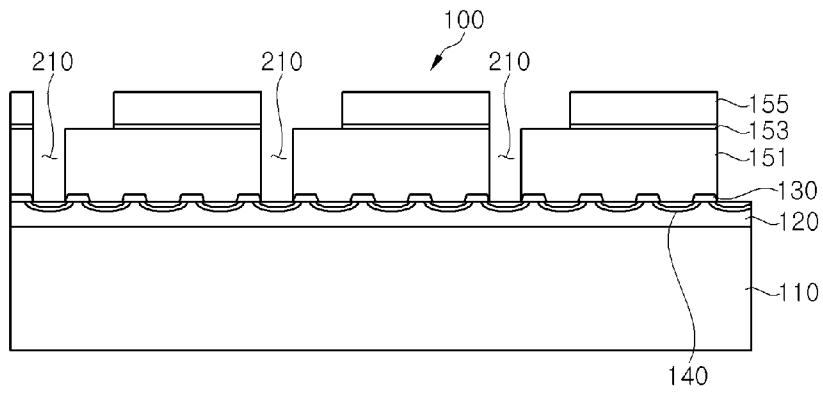
[Fig. 4]



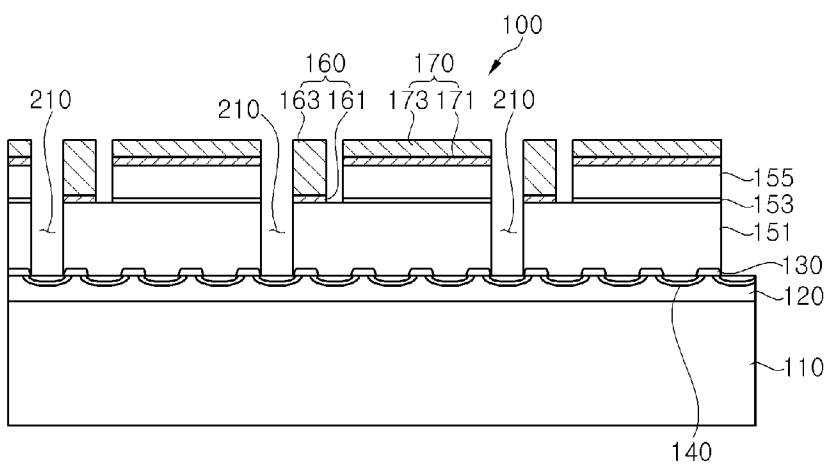
[Fig. 5]



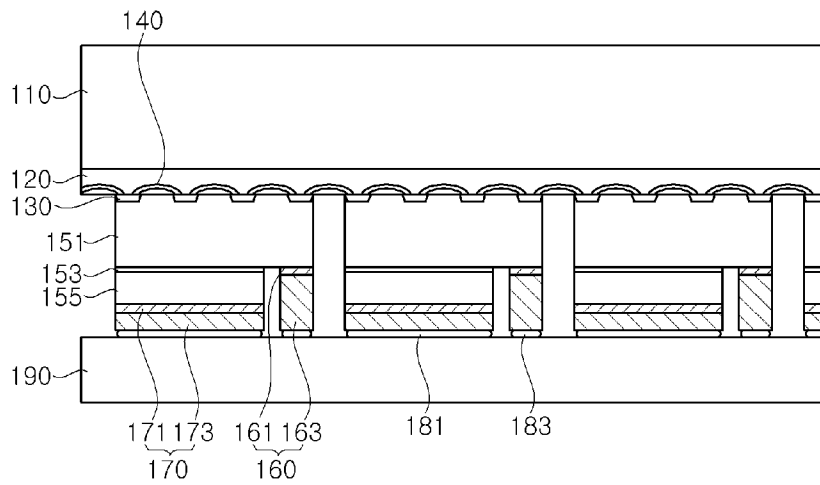
[Fig. 6]



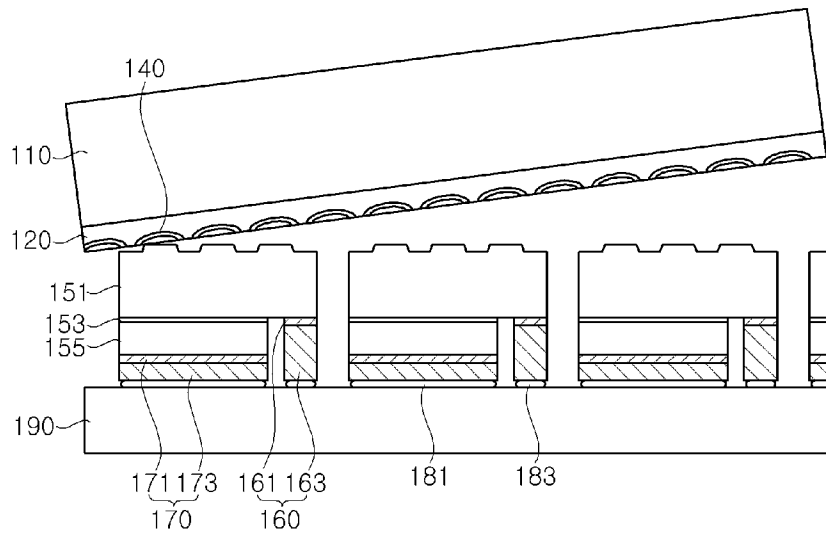
[Fig. 7]



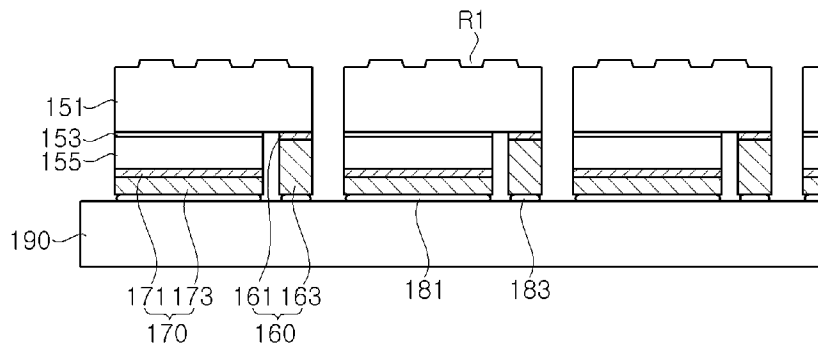
[Fig. 8]



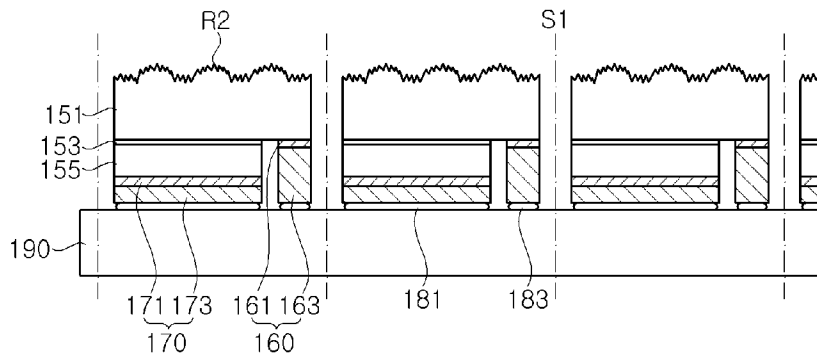
[Fig. 9]



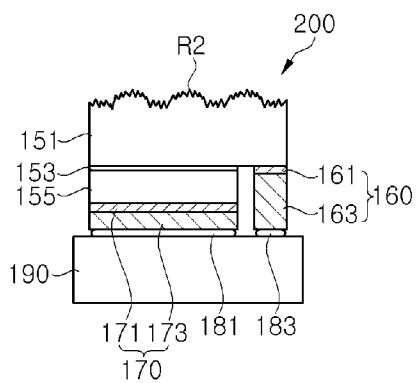
[Fig. 10]



[Fig. 11]



[Fig. 12]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2014/006091**A. CLASSIFICATION OF SUBJECT MATTER****H01L 33/12(2010.01)i, H01L 33/20(2010.01)i, H01L 33/22(2010.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 33/12; H01L 33/20; H01L 21/20; H01L 21/306; H01L 21/02; H01L 33/22; H01L 27/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: monolithical separation, sacrificial layer, void, mask pattern, lift-off

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 10-2013-0035685 A (SEOUL OPTO DEVICE CO., LTD.) 09 April 2013 See paragraphs 12-16, 24-27, claim 1 and figures 3-4.	1-14
A	KR 10-2009-0114870 A (SAMSUNG ELECTRO-MECHANICS CO., LTD.) 04 November 2009 See paragraphs 6-14, 17-25, claim 1 and figures 2a-2g.	1-14
A	US 2012-0309172 A1 (LINDA T. ROMANO et al.) 06 December 2012 See paragraphs 4, 24-31, claims 1-2 and figures 1-3.	1-14
A	US 2013-0052797 A1 (KUEI-SUNG CHANG et al.) 28 February 2013 See paragraphs 23-27, claim 1 and figure 17.	1-14
A	JP 2009-152387 A (SONY CORP.) 09 July 2009 See paragraphs 53-58, claim 1 and figure 15.	1-14



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

03 November 2014 (03.11.2014)

Date of mailing of the international search report

06 November 2014 (06.11.2014)

Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon Metropolitan City, 302-701,
Republic of Korea

Facsimile No. +82-42-472-7140

Authorized officer

PARK, Hye Lyun

Telephone No. +82-42-481-3463



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR2014/006091

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR 10-2013-0035685 A	09/04/2013	None	
KR 10-2009-0114870 A	04/11/2009	KR 10-0978568 B1	27/08/2010
US 2012-0309172 A1	06/12/2012	None	
US 2013-0052797 A1	28/02/2013	US 8796110 B2	05/08/2014
JP 2009-152387 A	09/07/2009	None	