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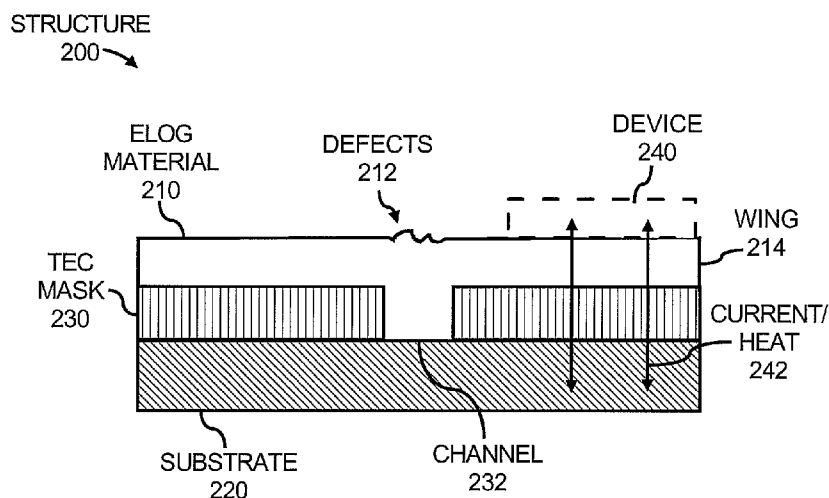


FIG. 2

(57) Abstract: A semiconductor structure includes a substrate, a thermally and electrically conductive mask positioned upon the substrate, and an epitaxial lateral over growth (ELOG) material positioned upon the thermally and electrically conductive mask.

SEMICONDUCTOR STRUCTURE HAVING AN ELOG ON A THERMALLY AND ELECTRICALLY CONDUCTIVE MASK

BACKGROUND

5 **[0001]** Heteroepitaxy is often used to create layered structures of different types of materials on substrates that are not lattice matched and otherwise would not form high quality epitaxial layers on the substrates. For instance, gallium nitride (GaN) does not form well on substrates made of sapphire (Al_2O_3) or silicon on sapphire (SOS) because of a relatively high level
10 of lattice mismatch between the GaN and the sapphire or silicon on sapphire. The lattice mismatch often results in defects and dislocations in the GaN. To overcome these problems, epitaxial lateral overgrowth (ELOG) is used to form the GaN material, or other material, on another material, typically, through a channel or aperture in a dielectric material on a crystalline substrate.

15 **[0002]** An example of a conventional structure 100 formed through heteroepitaxy of an epitaxial lateral overgrowth (ELOG) material 110, such as, GaN, indium phosphide (InP), gallium arsenide (GaAs), etc., and a substrate 120 is shown in FIG. 1. As shown therein, a cross-sectional view of the structure 100 illustrates that a mask 130 is created on the substrate 120 using
20 the dielectric material. The ELOG material 110 is shown without hash marks to more clearly show its position with respect to the mask 130.

[0003] The structure 100 is also depicted as including a channel 132, which is typically a few microns wide, in the dielectric mask 130. The ELOG material 110 is grown out of the channel 132 from seed material layer 120.
25 More particularly, the ELOG material 110 grows from the channel 132 and spreads out of the channel 132 and across parts of the dielectric mask 130, as shown in FIG. 1. The dielectric material is used to form the mask 130 because it is able to withstand the relatively high temperatures that are required to grow the ELOG material 110 and also enables a suitable surface on which the ELOG
30 material 110 laterally grows. As a comparison, conventional metals typically cannot be used as the mask 130 because the metals are prone to melting or

forming alloys with the ELOG material at the temperatures required for the ELOG material to properly grow.

[0004] One problem with the ELOG material 110 formation is that as the ELOG material 110 grows out of the channel 132, defects 112 are often created
5 in the transition from the vertical extension to the lateral overgrowth. However, material quality tends to increase as the layer spreads out over the dielectric mask 130. To avoid the defects 112, devices 140 are typically built upon wing portions 114 of the ELOG material 110, or the wing portions 114 form parts of the devices 140, which are generally laterally spaced from the defects 112.
10 This configuration results in some undesirable characteristics in the structure 100.

[0005] For instance, the insulating properties of the dielectric mask 130 cause current crowding and thermal crowding because electrical current must flow along the wings 114 of the ELOG material 110 and then through the
15 material 110 contained in the channel 132, as indicated by the arrows 142. In addition, heat generated in the devices 140 must also flow through this path to become dissipated through the substrate 120. This is not an ideal path for either the current or heat to flow because it constricts the heat and current flow and often results in overheating, which may impair the functioning of devices
20 140. In addition, the current crowding causes non-uniform current and the behavior of the devices 140 consequently suffers. The current and thermal crowding ultimately limits the flexibility of the devices that may be built using a dielectric mask and often requires additional heat dissipation solutions, which adds to the costs associated with implementing the structure 100, as well as the
25 size of the structure 100.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Embodiments are illustrated by way of example and not limited in the following figure(s), in which like numerals indicate like elements, in which:

[0007] FIG. 1 illustrates a cross-sectional side view of a portion of a
5 conventional semiconductor structure.

[0008] FIG. 2 illustrates a cross-sectional side view of a portion of a semiconductor structure, according to an embodiment of the invention;

[0009] FIGS. 3A and 3B, respectively, illustrate cross-sectional side views of portions of semiconductor structures, according to embodiments of the
10 invention;

[0007] FIG. 4 depicts a cross-sectional side view of a portion of a semiconductor structure, according to an embodiment of the invention; and

DETAILED DESCRIPTION

[0010] For simplicity and illustrative purposes, the principles of the embodiments are described by referring mainly to examples thereof. In the following description, numerous specific details are set forth in order to provide
5 a thorough understanding of the embodiments. It will be apparent however, to one of ordinary skill in the art, that the embodiments may be practiced without limitation to these specific details. In other instances, well known methods and structures are not described in detail so as not to unnecessarily obscure the description of the embodiments.

10 **[0011]** Disclosed herein are semiconductor structures that contain ELOG materials formed on thermally and electrically conductive masks. The thermally and electrically conductive masks may be formed of carbon nanostructures or graphene. The thermal and electrical conductive properties of the masks upon which the ELOG materials are formed generally enable heat and current to be
15 conducted more readily between devices positioned on the ELOG materials and a substrate upon which the thermally and electrical conductive masks are positioned as compared with conventional ELOG structures that employ dielectric masks.

[0012] With reference first to FIG. 2, there is shown a cross-sectional side
20 view of a portion of a semiconductor structure 200, in accordance with an embodiment. It should be understood that the portion of the semiconductor structure 200 may include additional components and that some of the components described herein may be removed and/or modified without departing from a scope of the semiconductor structure 200.

25 **[0013]** As shown in FIG. 2, the semiconductor structure 200 includes an epitaxial lateral overgrowth (ELOG) material 210, a substrate 220, and a thermally and electrically conductive (TEC) mask 230. The ELOG material 210 is generally composed of a growth material, such as, GaN, GaInN, GaAlN, AlN, InN, InP, InGaAsP, InGaAs, GaAs, AlGaAs, Si, SiGe, and all possible III-V
30 family and its alloys, etc., which grows lattice mismatched in the channel 232 on the substrate 220 initially vertically and then grows laterally and vertically over

the TEC mask 230. The ELOG material 210 has therefore been formed from vertical growth out of the channel 232 and through lateral spreading over parts of the TEC mask 230, in manners similar to those discussed above with respect to ELOG growth over the dielectric mask 130 (FIG. 1).

5 **[0014]** The substrate 220 is composed of any suitable crystalline material such as SiC, Sapphire, Si, Ge, and the like. The TEC mask 230 overlies the substrate 220 and provides adequate surfaces for the ELOG material 210 to form through an ELOG process from the channel 232 formed in the TEC mask 230. As the name implies, the TEC mask 230 is formed of one or more
10 materials that are capable of electrical and thermal conductance levels that exceed the dielectric materials used in conventional ELOG structures. Examples of suitable electrical and thermal conductance levels are, for instance, electrical and thermal conductance levels that are similar to or exceed the levels of metals, such as copper and the like. According to an embodiment,
15 the TEC mask 230 is composed of graphene or carbon nanostructures, such as, nanotubes or other shaped nano-scale structures, which are capable of conducting current and heat at much higher levels as compared with the dielectric material 130 (FIG. 1) employed in conventional structures.

[0015] According to a further embodiment, the TEC mask 230 is
20 composed of relatively high density carbon nanostructures to substantially prevent the ELOG material 210 from forming additional defects caused by vertical growth from the substrate 220. In this embodiment, therefore, the carbon nanostructures forming the TEC mask 230 have a sufficiently high density to substantially prevent wings 214 of the ELOG material 210 from
25 having a relatively large number of defects during the ELOG process. By way of example, carbon nanostructures are considered to be insufficiently dense if the wings 214 are formed with a number of defects due to wings 214 growing vertically from the substrate 220 in a manner that substantially prevents a device 240 from properly attaching to the wings 214. The device 240 may be
30 considered as being unable to properly attach to the wings 214, for instance, if

there is an insufficient amount of space between defects to enable the device 240 to be situated on the wings 214 without contacting the defects.

[0016] Through use of the carbon nanostructures or the graphene in the TEC mask 230, electrical and thermal conduction between a device 240 and the substrate 220 may occur more readily as compared with conventional structures. The increase in electrical and thermal conduction as compared with conventional structures occurs because current and heat are conducted through a much larger area (over the TEC mask 230) than the material contained in the channel 132 of a conventional structure 100. In addition, the carbon nanostructures and the graphene materials are suitable for the ELOG process because they are able to withstand the relatively high temperatures that often required for the ELOG process to occur.

[0017] In FIG. 2, the device 240 has been shown with dashed lines to indicate that the device 240 does not necessarily form part of the semiconductor structure 200. Instead, the structure 200 and the device 240 may form part of an apparatus, such as, a laser, a transistor, a photodetector, an optical amplifier, an optical waveguide, an optical modulator, etc., in which case, the structure 200 and the device 240 are components of the apparatus.

[0018] It should be understood that the portion of the semiconductor structure 200 depicted in FIG. 2 may form part of a larger semiconductor structure or may include additional elements to form a larger semiconductor structure. For instance, the semiconductor structure 200 may include additional channels 232 from which the ELOG material 210 grows. In this regard, the semiconductor structure 200 may be considered as a relatively larger structure having a number of wings 214 upon which devices 240 may be positioned. Additional embodiments pertaining to the semiconductor structure 200 are described with respect to the following figures.

[0019] Turning first to FIGS. 3A and 3B, there are shown cross-sectional side views of portions of semiconductor structures 300 and 350, in accordance with other embodiments. It should be understood that the portions of the

semiconductor structures 300 and 350 may include additional components and that some of the components described herein may be removed and/or modified without departing from scopes of the semiconductor structures 300 and 350.

5 **[0020]** The semiconductor structures 300 and 350 depicted in FIGS. 3A and 3B include many of the same elements as the semiconductor structure 200 depicted in FIG. 2. As such, only those elements that differ from the semiconductor structure 200 will be described with respect to the semiconductor structures 300 and 350.

10 **[0021]** As shown in FIG. 3A, the TEC mask 230 includes a plurality of dimples 310. The dimples 310 are formed on the surface opposite the substrate 220 and do not extend through the TEC mask 230. In addition, the dimples 310 may be formed on the TEC mask 230 surface through any reasonably suitable fabrication technique. Although the dimples 310 have been
15 depicted as having semi-circular cross-sectional shapes, the dimples 310 may have any other suitable shapes, such as, vertically extending side walls, horizontally extending bottom wall, one vertically extending side wall and wall curved side wall, etc. In one regard, use of the TEC mask 230 generally enables the ELOG material 210 to be formed on the TEC mask 230 without
20 requiring that the ELOG material 210 extend and directly contact the substrate 220.

[0022] According to an embodiment, seed material, such as nanocrystalline or micro-crystalline silicon or III-V materials that can initiate epitaxial growth for the ELOG material 210, may be placed in one or more of
25 the dimples 310 and may be grown laterally out of the dimples 310. In this embodiment, the ELOG material 210 grown from one dimple 310 may meet the ELOG material 210 grown from another dimple 310 at an interface 320. Although the interfaces 320 have been depicted as comprising vertically extending sections of ELOG materials 210, the ELOG materials 210 grown from
30 separate dimples 310 may become interfaced with one another in various other

patterns. In another embodiment, the dimples 310 may be spaced sufficiently apart from each other to enable the ELOG material 210 to grow from the dimples 310 without contacting each other. In any regard, when the ELOG material 210 growth is initiated from the dimples 310, the substrate 220 need
5 not be crystalline and may be non-single crystalline or even amorphous.

[0023] As further shown, defects 212 may occur during the transition of the vertical extension to the lateral extension of the ELOG material 210. As discussed above, it is beneficial to be able to place devices 240 on the wings 214 of the ELOG material 210 as opposed to the locations where defects 212
10 exist. In one regard, therefore, the dimples 310 may be spaced sufficiently apart from each other to enable sufficient space on the wings 214 for placement of at least portions of the devices 240.

[0024] Through implementation of the structure 300 depicted in FIG. 3A, the ELOG material 210 may be formed to be relatively thinner and to be formed
15 in a relatively less amount of time as compared with ELOG material 210 growth from the channel 232. For instance, the dimples 310 may be formed to have a relatively smaller size, such as, around tens of nanometers or less, than the channel 232 (FIG. 2), which may be about a micron wide.

[0025] Turning now to FIG. 3B, the semiconductor structure 350 includes
20 all of the elements of the semiconductor structure 300. In addition, however, the semiconductor structure 350 includes a channel 232 from which the ELOG material 210 grows. In this regard, the ELOG material 210 may grow into the dimples 310 as it is laterally extended across the wings 214 of the ELOG material 210.

[0026] With reference now to FIG. 4, there is shown a cross-sectional
25 side view of a portion of a semiconductor structure 400, in accordance with another embodiment. It should be understood that the portion of the semiconductor structure 400 may include additional components and that some of the components described herein may be removed and/or modified without
30 departing from a scope of the semiconductor structure 400.

[0027] The semiconductor structure 400 depicted in FIG. 4 includes many of the same elements as the semiconductor structure 200 depicted in FIG. 2. As such, only those elements that differ from the semiconductor structure 200 will be described with respect to the semiconductor structure 400.

5 [0028] As shown in FIG. 4, the TEC mask 410 is composed of a high density material. In this regard, the TEC mask 410 is composed of relatively high density carbon nanostructures or graphene. In addition, a low density TEC mask 420 is positioned in the channel 232. In this regard, the low density TEC mask 420 is composed of relatively low density carbon nanostructures or
10 graphene. According to an embodiment, the high density TEC mask 410 is composed of sufficiently high density material to substantially prevent deformations or other defects in the ELOG material 210 as it is grown. Likewise, the low density TEC mask 420 is composed of sufficiently low density material to enable seed material for the ELOG material 210 to be placed in
15 spaces between the material and for the ELOG material 210 to grow out of the spaces between the material. By way of example, the low density TEC mask 420 is formed to include spaces between vertically extending portions of the TEC mask 420 material, to thus enable the ELOG material 210 to grow vertically from the spaces. In addition, as the ELOG material 210 grows from
20 individual spaces in the low density TEC mask 420 and extends above the low-density TEC mask 420, the ELOG material 210 may become combined with the ELOG material 210 extending from other spaces as it is grown laterally across the high density TEC mask 410.

[0029] What has been described and illustrated herein is a preferred
25 embodiment of the invention along with some of its variations. The terms, descriptions and figures used herein are set forth by way of illustration only and are not meant as limitations. Those skilled in the art will recognize that many variations are possible within the scope of the invention, which is intended to be defined by the following claims -- and their equivalents -- in which all terms are
30 meant in their broadest reasonable sense unless otherwise indicated.

What is claimed is:

1. A semiconductor structure comprising:
a substrate;
a thermally and electrically conductive mask positioned upon said
5 substrate; and
an epitaxial lateral over growth (ELOG) material positioned upon said
thermally and electrically conductive mask.
2. The structure of claim 1, wherein said thermally and electrically
10 conductive mask comprises a material selected from the group consisting of
carbon nanostructures and graphene.
3. The structure of claim 1, wherein said thermally and electrically
conductive mask comprises a plurality of dimples.
- 15 4. The structure of claim 1, wherein said thermally and electrically
conductive mask contains at least one trench, wherein the ELOG material
contains a vertically extending section that extends from the at least one trench.
- 20 5. The structure of claim 4, wherein said thermally and electrically
conductive mask comprises a high density thermally and electrically conductive
mask and a low density thermally and electrically conductive mask, wherein the
at least one trench is formed in the high density thermally and electrically
conductive mask and said low density thermally and electrically conductive
25 mask is positioned in the at least one trench and containing a plurality of
spaces, said vertically extending section of the ELOG material extending from
the plurality of spaces.
6. An apparatus comprising:
30 a substrate;
a thermally and electrically conductive mask positioned upon said
substrate;

an epitaxial lateral over growth (ELOG) material positioned upon said thermally and electrically conductive mask; and
a device positioned upon the ELOG material.

5 7. The apparatus of claim 6, wherein said thermally and electrically conductive mask comprises a material selected from the group consisting of densely packed carbon nanostructures and graphene.

8. The apparatus of claim 6, wherein said thermally and electrically
10 conductive mask comprises a plurality of dimples.

9. The apparatus of claim 8, wherein the ELOG material has a surface and wherein the dimples are sufficiently spaced in at least one area to position at least a portion of the device upon said surface of the ELOG material.

15 10. The apparatus of claim 6, wherein said thermally and electrically conductive mask contains at least one trench, wherein the ELOG material contains a vertically extending section that extends from the at least one trench.

20 11. The apparatus of claim 10, wherein said thermally and electrically conductive mask comprises a high density thermally and electrically conductive mask and a low density thermally and electrically conductive mask, wherein the at least one trench is formed in the high density thermally and electrically conductive mask and said low density thermally and electrically conductive
25 mask is positioned in the at least one trench and containing a plurality of spaces, said vertically extending section of the ELOG material extending from the plurality of spaces.

12. The apparatus of claim 6, wherein said device comprises a component of
30 at least one of a semiconductor laser, transistor, photodetector, optical amplifier, optical waveguide, and optical modulator.

13. A semiconductor structure comprising:
a substrate;
a thermally and electrically conductive mask positioned on the substrate,
5 wherein said thermally and electrically conductive mask comprises a material
selected from the group consisting of densely packed carbon nanostructures
and graphene, wherein said thermally and electrically conductive mask contains
at least one trench; and
an epitaxial lateral over growth (ELOG) material positioned upon said
10 thermally and electrically conductive mask, and wherein the ELOG material
contains a vertically extending section that extends from the at least one trench.
14. The structure of claim 13, further comprising:
low density thermally and electrically conductive material positioned in
15 the at least one trench, said low density thermally and electrically conductive
material comprising spaces, and wherein the ELOG material extends from the
spaces.
15. The structure of claim 13, further comprising a device positioned on a
20 portion of the ELOG material, wherein the device is a component of an
electronic device.

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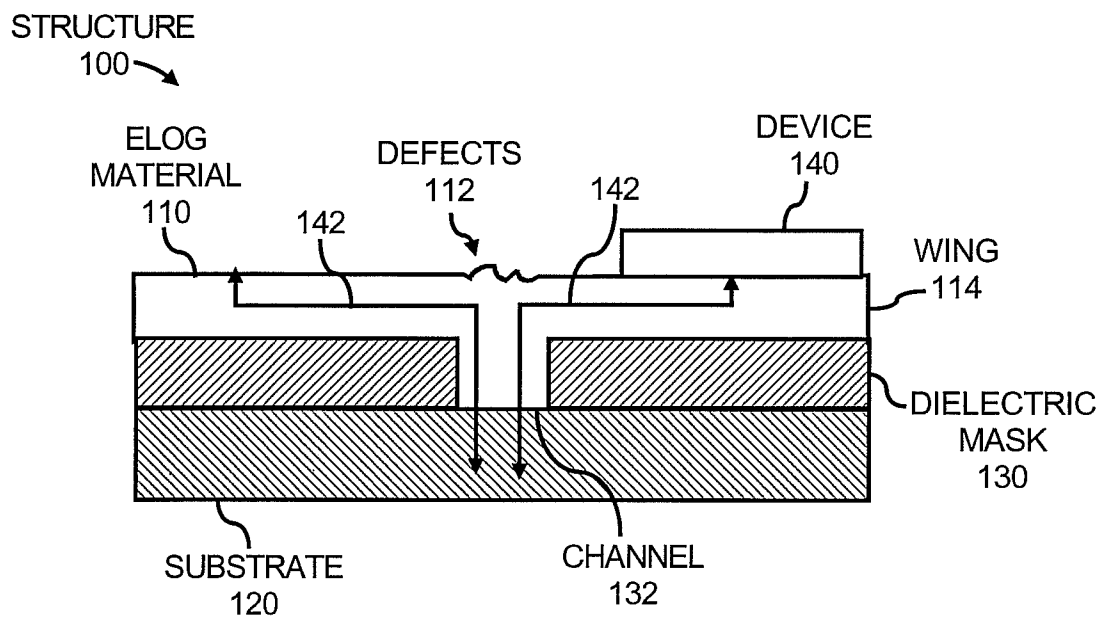


FIG. 1
(PRIOR ART)

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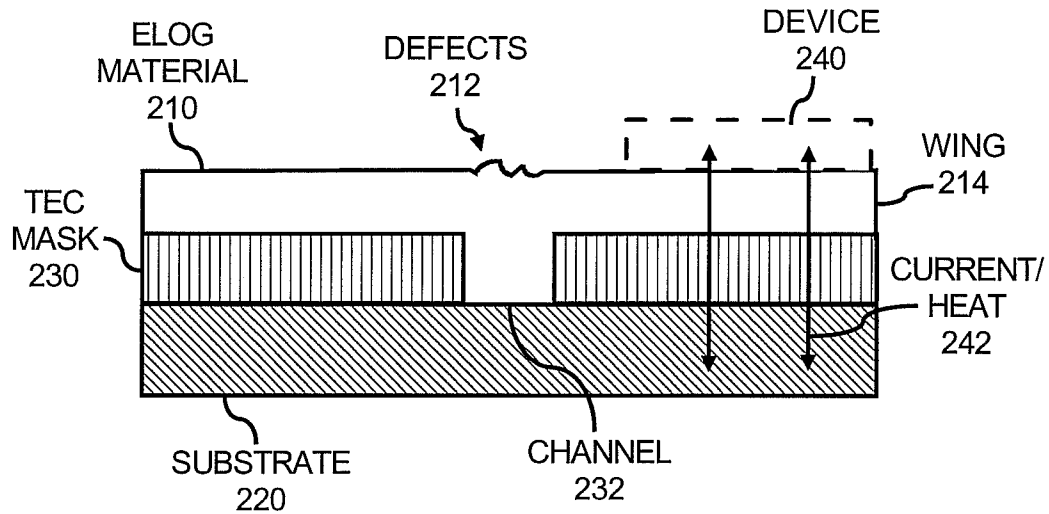
STRUCTURE
200

FIG. 2

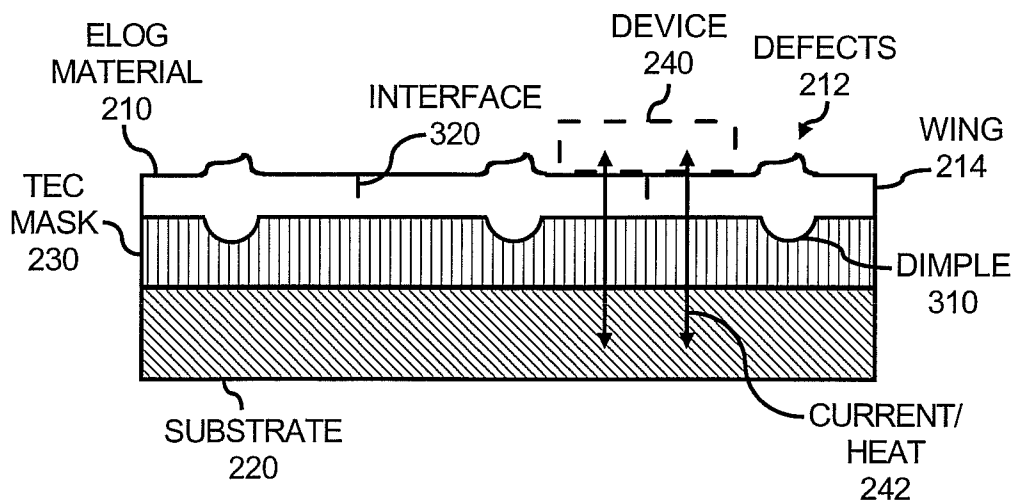
STRUCTURE
300

FIG. 3A

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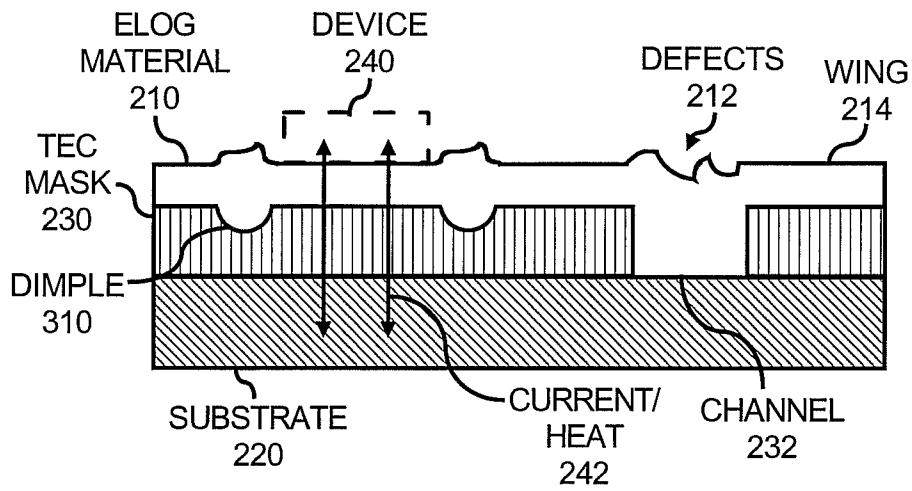
STRUCTURE
350

FIG. 3B

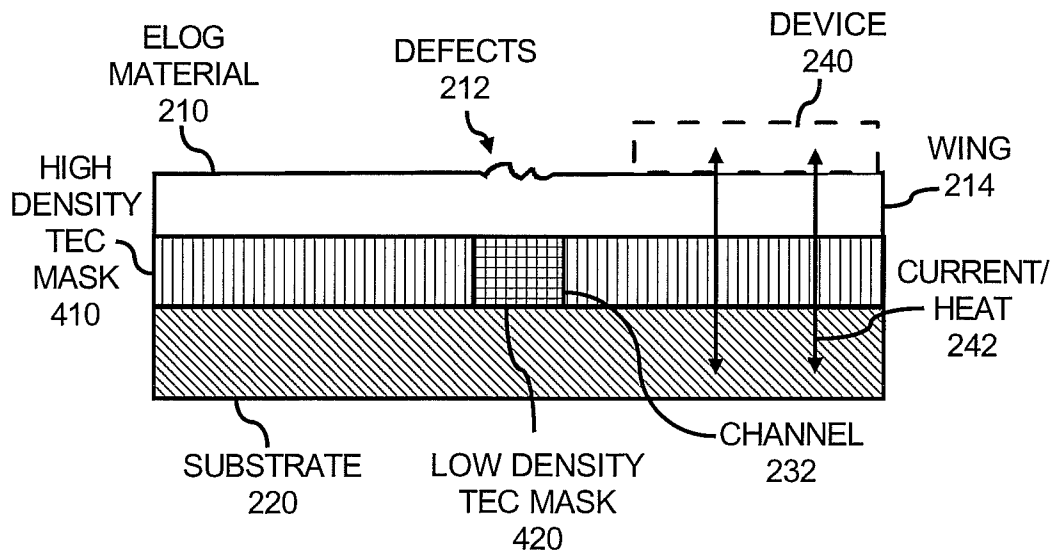
STRUCTURE
400

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2008/086991**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/20(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC : H01L 29/778, 21/338, 29/812, C30B 13/34, 1/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Utility models and applications for Utility models since 1975

Japanese Utility models and applications for Utility models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKIPASS(KIPO Internal) & Keyword: ELOG, thermal, electrical, conduct, carbon and mask

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	JP 14-134735 A (TOSHIBA CORP.) 10 May 2002 See Abstract; Figures5-7 and Claim1	1,6,12 2-5,7-11,13-15
A	US 05217564 A (CARL O. BOZLER et al.) 08 June 1993 See Abstract and Figures2A-2E	1-15
A	US 2004-0082150 A1 (HUA-SHUANG KONG et al.) 29 April 2004 See Abstract; Figures1-3 and Claim1	1-15

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"&" document member of the same patent family

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Name and mailing address of the ISA/KR

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Telephone No. 82-42-481-8496



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2008/086991

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 14-134735 A	10.05.2002	None	
US 05217564 A	08.06.1993	EP 0191504 A2	20.08.1986
		EP 0506146 A2	30.09.1992
		EP 0049286 A4	05.08.1982
		EP 0191504 A3	10.09.1986
		EP 0192280 A2	27.08.1986
		EP 0194495 A1	17.09.1986
		EP 0049286 B1	02.03.1988
		EP 0192280 A3	10.09.1986
		JP 02-283014 A	20.11.1990
		JP 02-584164 B2	21.11.1996
		JP 06-020945 A	28.01.1994
		US 04727047 A	23.02.1988
		US 04816420 A	28.03.1989
		US 04837182 A	06.06.1989
		US 05217564 A	08.06.1993
		US 05273616 A	28.12.1993
		US 05328549 A	12.07.1994
		US 05362682 A	08.11.1994
		US 05549747 A	27.08.1996
		US 05588994 A	31.12.1996
		US 05676752 A	14.10.1997
		WO 1981-002948 A1	15.10.1981
US 2004-0082150 A1	29.04.2004	US 06582986 B2	24.06.2003
		US 06764932 B2	20.07.2004
		US 06803602 B2	12.10.2004
		US 06812053 B1	02.11.2004
		US 06955977 B2	18.10.2005
		US 2002-0022290 A1	21.02.2002
		US 2002-0098693 A1	25.07.2002
		US 2003-0207518 A1	06.11.2003