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(54) MEMORY DEVICE HAVING HIGHLY INTEGRATED CELL STRUCTURE AND METHOD OF ITS FABRICATION

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(57) **ABSTRACT**

In an embodiment, a memory device, with a highly integrated cell structure, includes a mold insulating layer disposed on a semiconductor substrate. At least one conductive line is disposed on the mold insulating layer. Data storage elements self-aligned with the conductive line are interposed between the conductive line and the mold insulating layer. In this case, each of the data storage elements may include a resistor pattern and a barrier pattern, which are sequentially stacked, and the resistor pattern may be self-aligned with the barrier pattern.

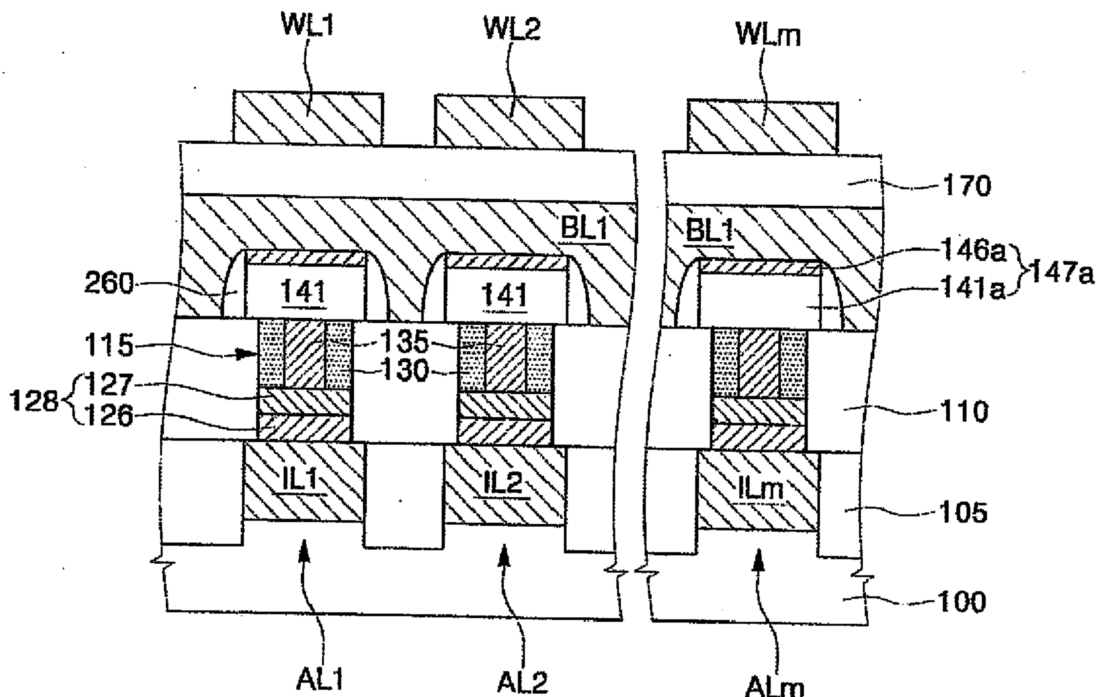


FIG. 1

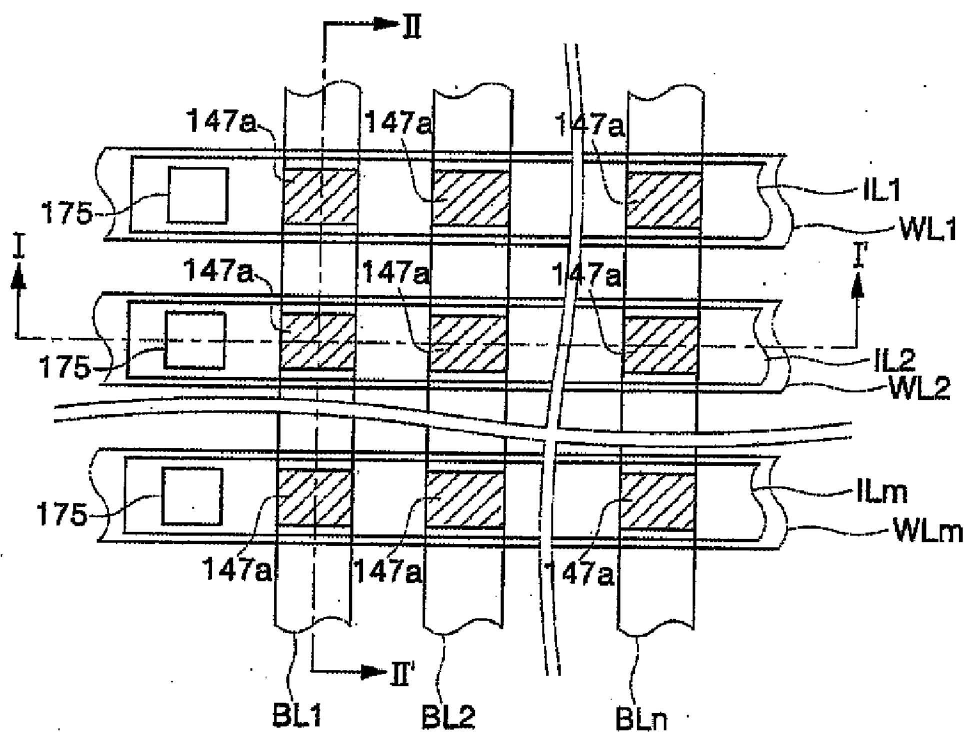


FIG. 2A

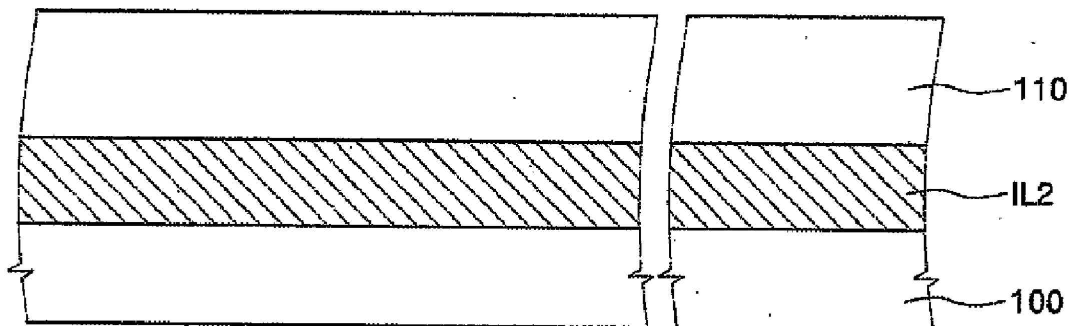


FIG. 2B

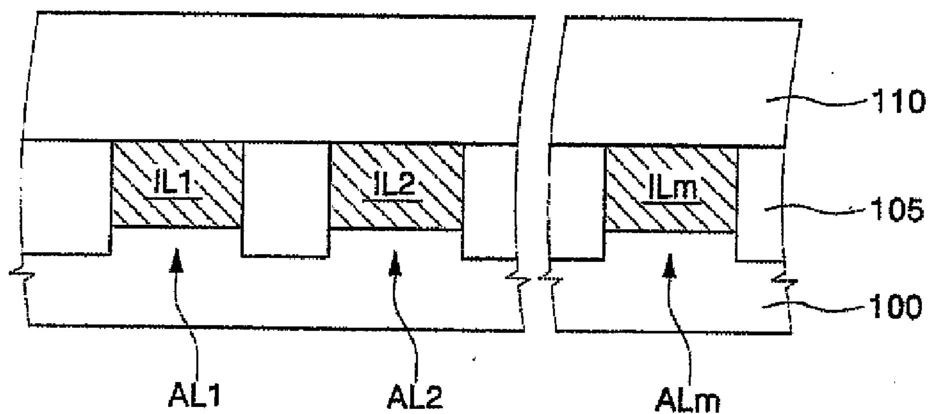


FIG. 3A

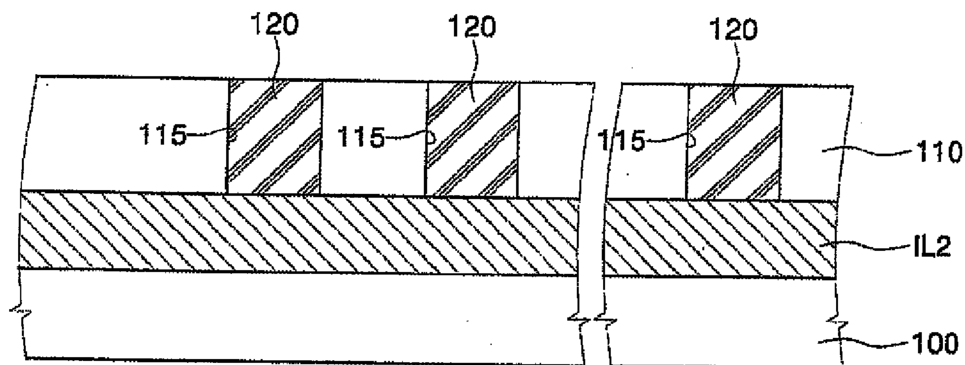


FIG. 3B

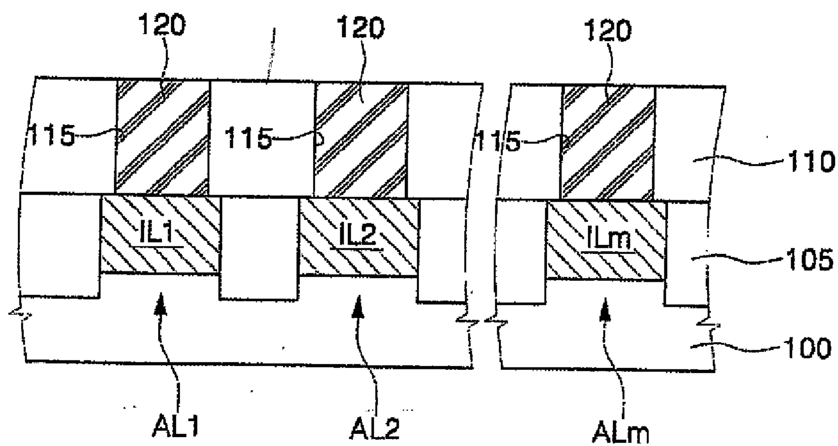


FIG. 4A

115
135
130
128
127
126
127
126
110
IL2
100

FIG. 4B

115
135
130
128
127
126
127
126
110
IL1
IL2
ILm
105
100
AL1
AL2
ALm

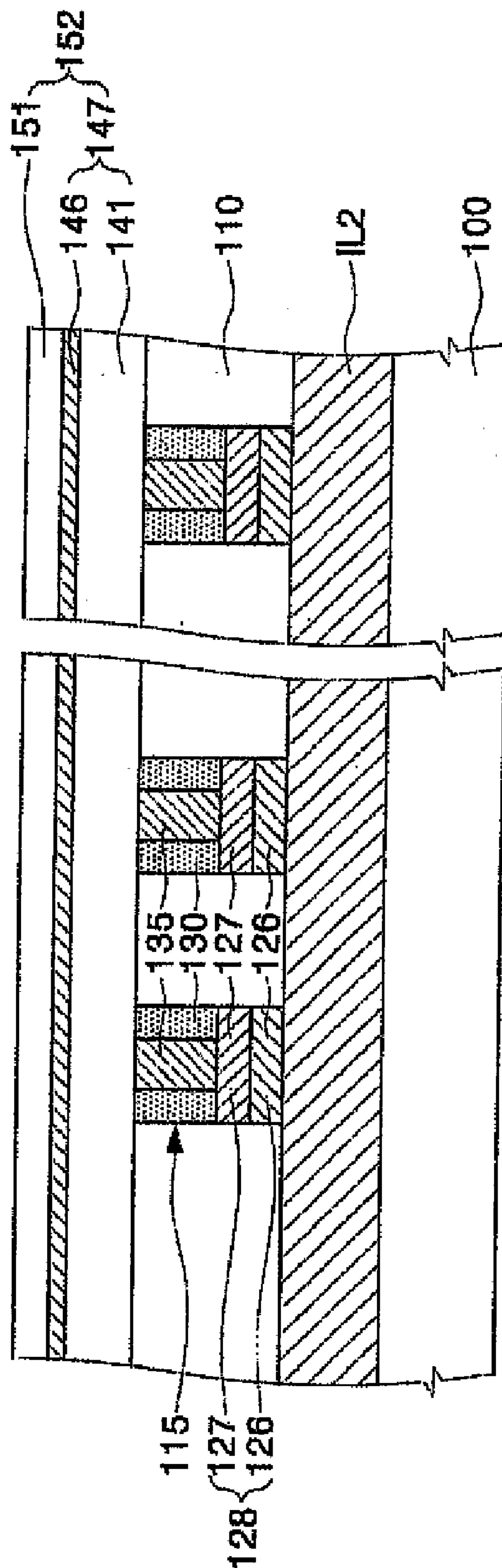


FIG. 5A
151
152
146
147
141
110
IL2
100
135
130
127
126
115
127
126
128

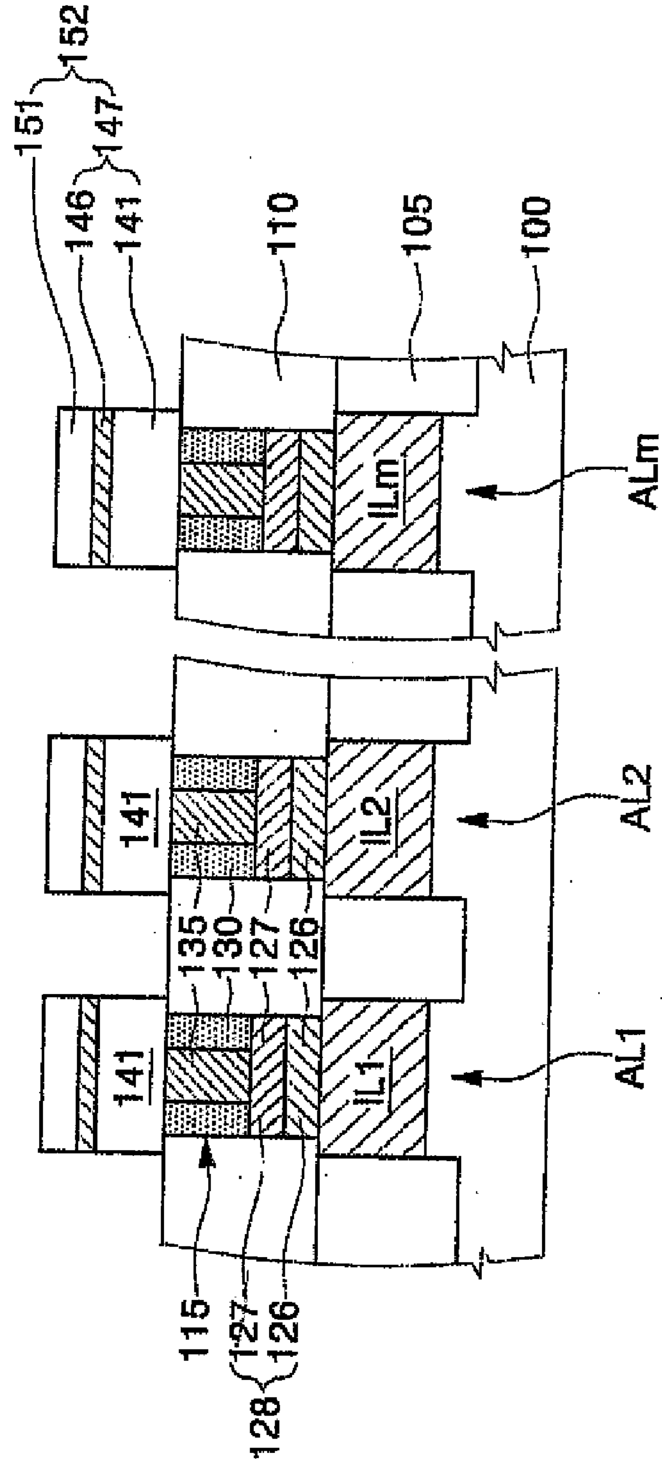


FIG. 5B
152
151
147
146
141
110
105
100
ILm
ALm
141
IL2
AL2
135
130
127
126
141
IL1
AL1
115
128
127
126

FIG. 6A

152
151
147
146
141
110
IL2
100
155
115
135
130
127
126
128

FIG. 6B

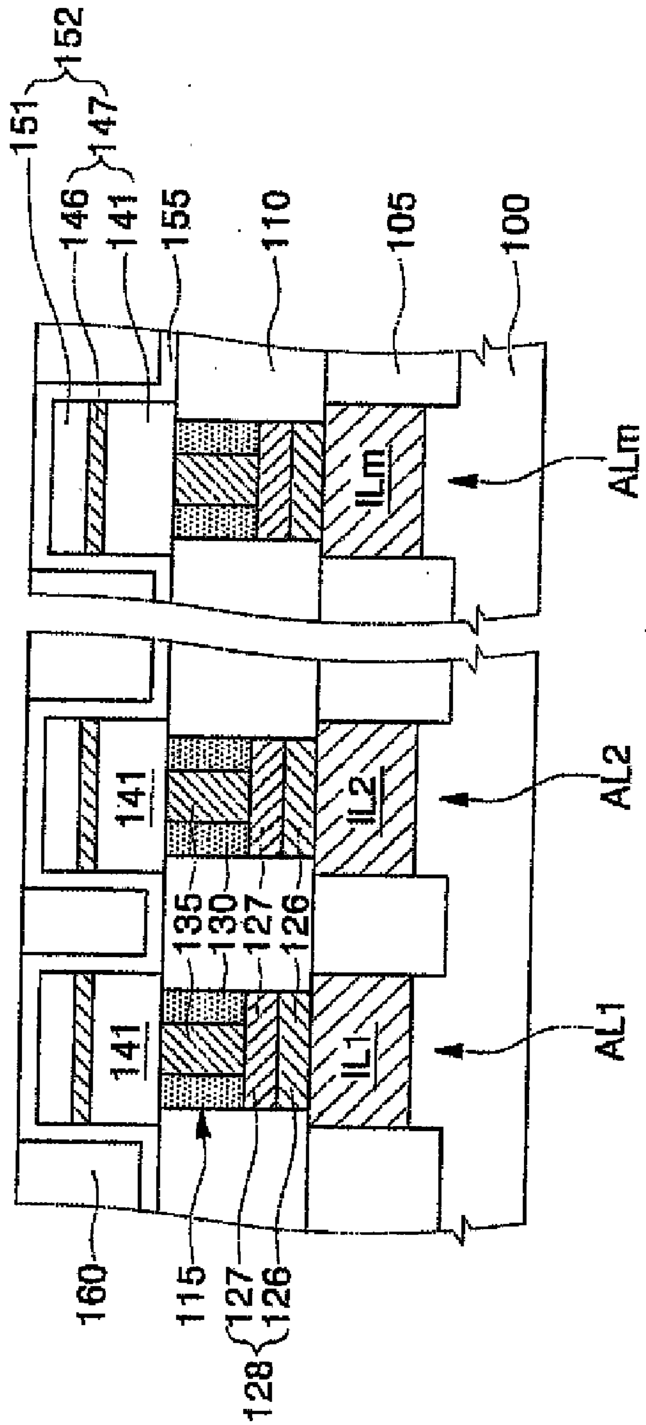


FIG. 6C

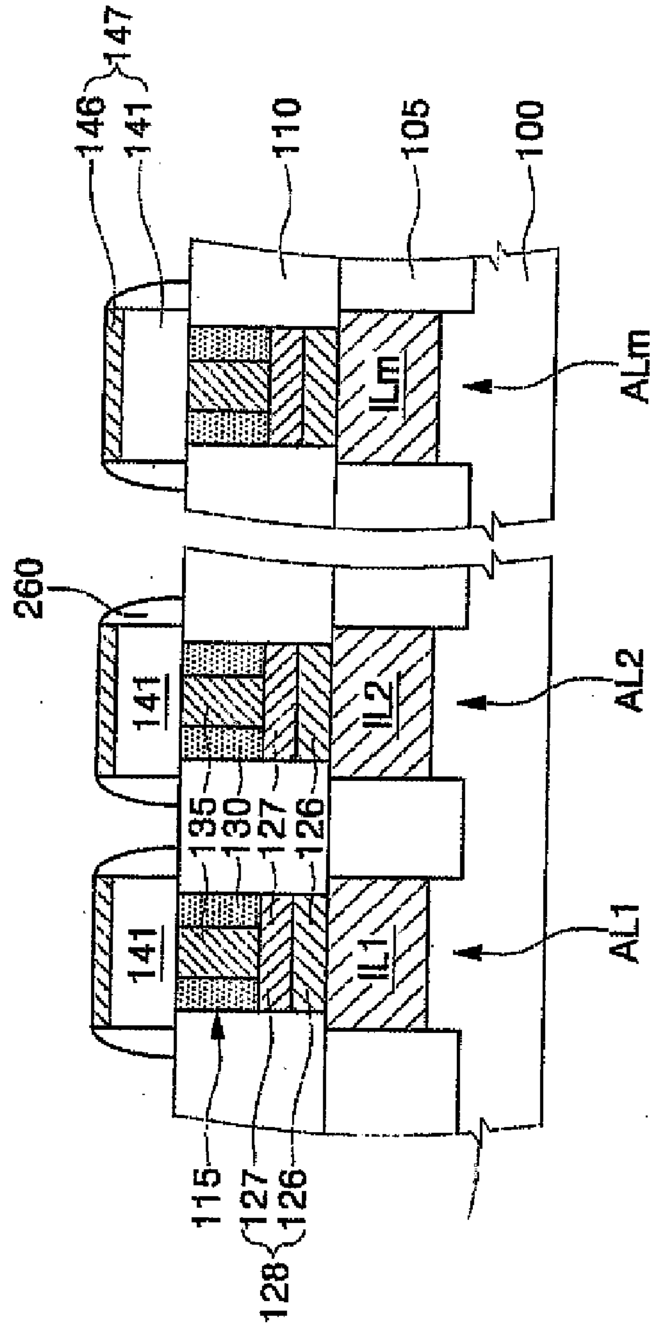


FIG. 7A

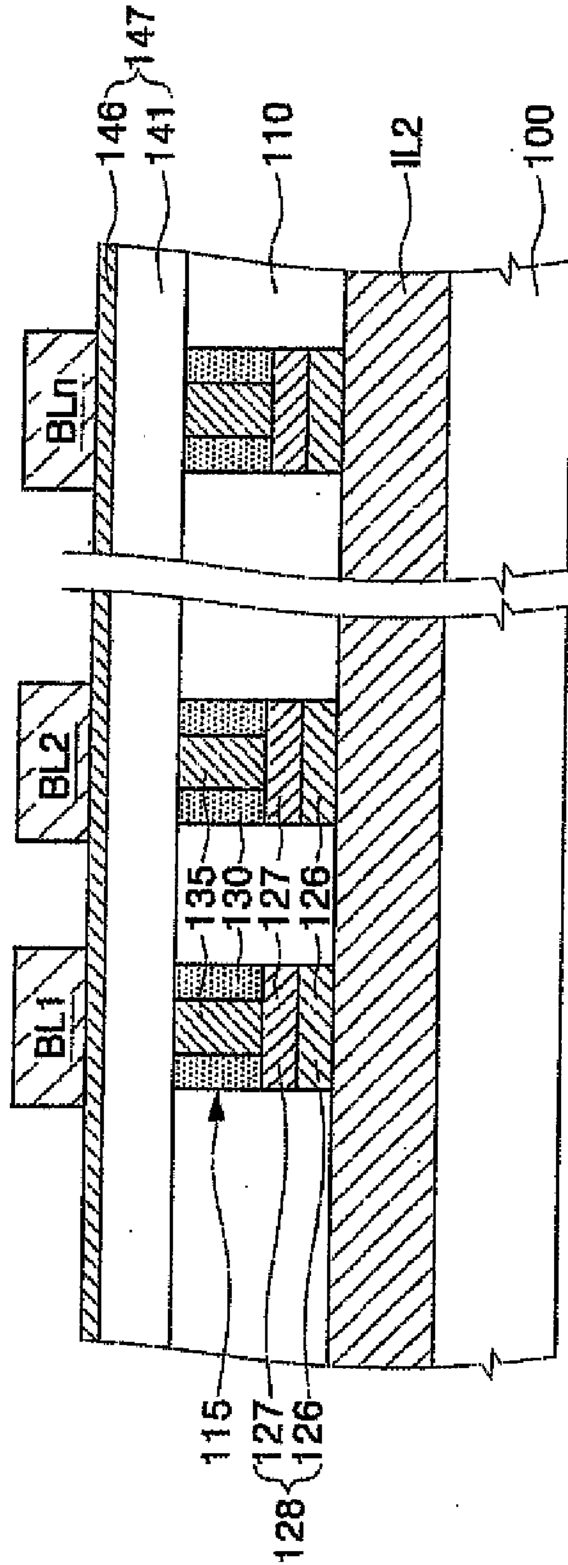


FIG. 7B

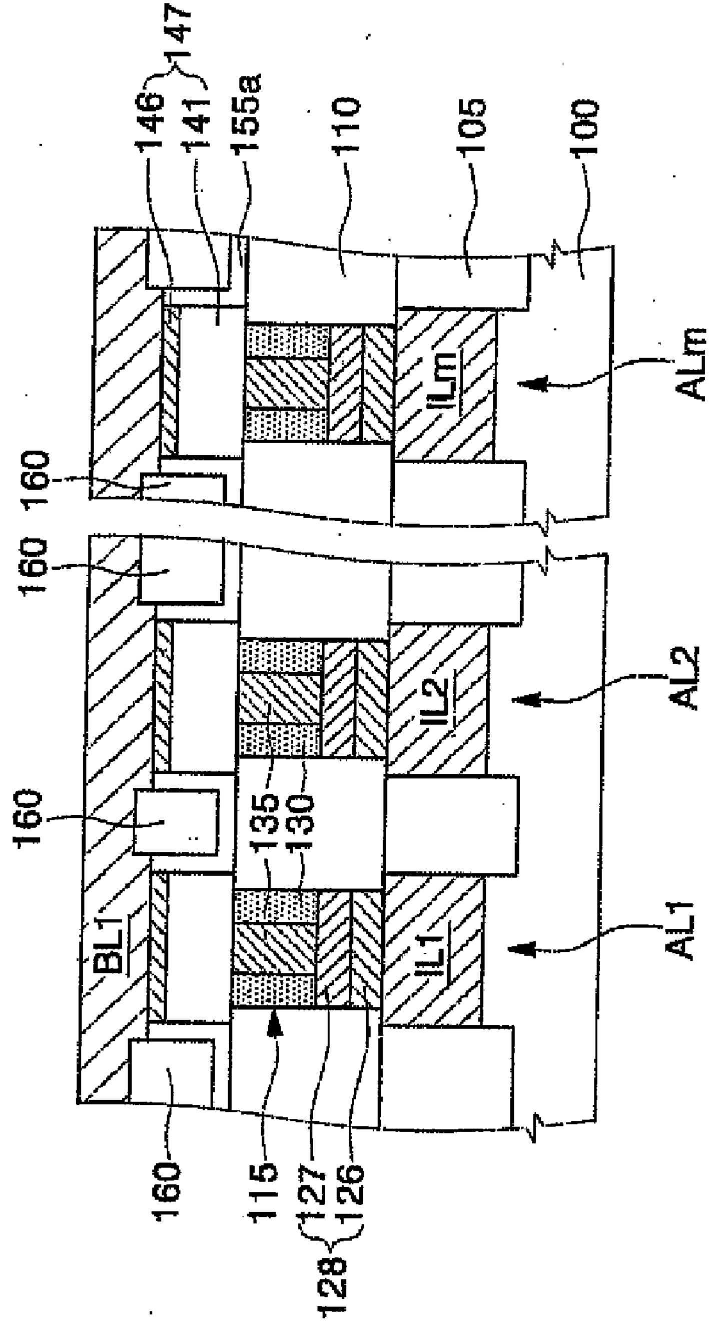
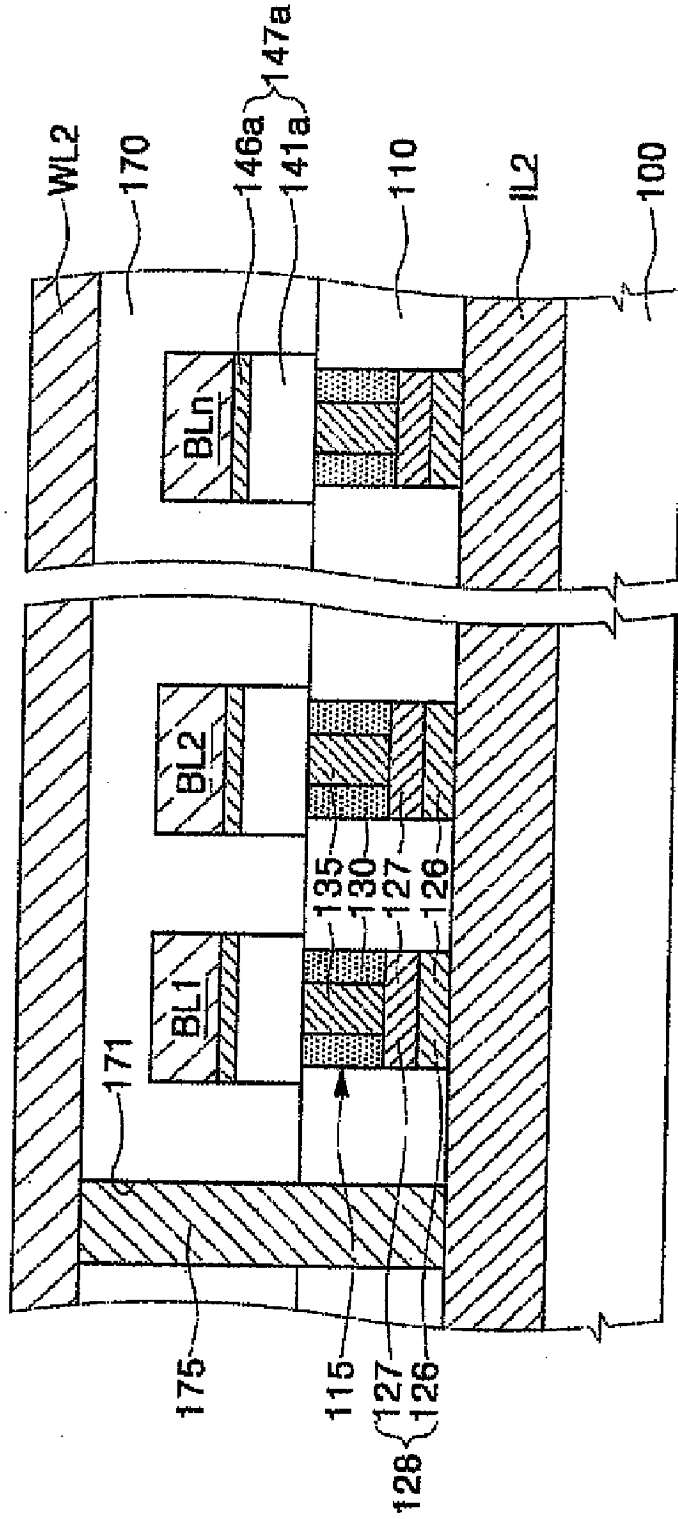


FIG. 7C

BL1 146 141 147 110 105 100 ILm ALm BL1 141 135 130 IL2 AL2 141 260 115 127 126 128 IL1 AL1

FIG. 8A



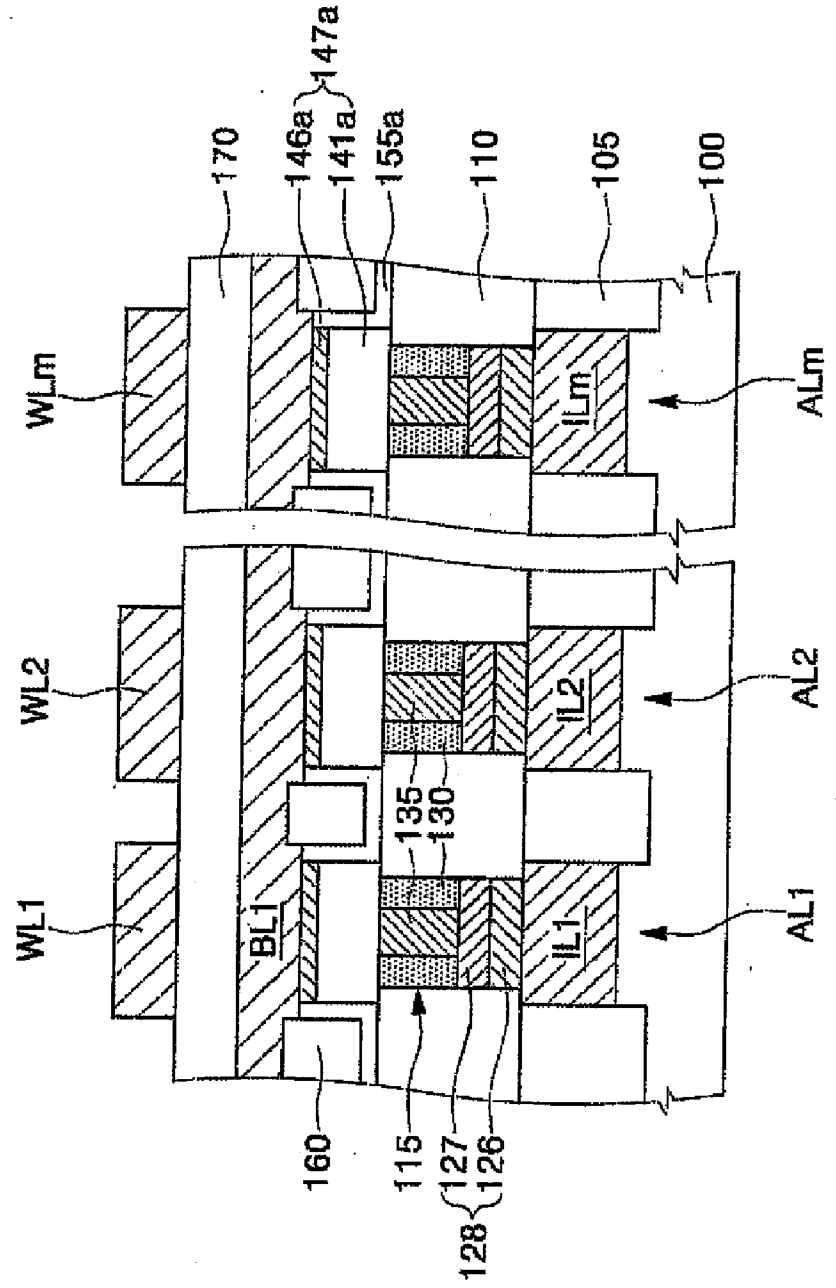


FIG. 8B
WL1
WL2
WLm
170
146a
141a
147a
155a
110
105
100
BL1
160
115
127
126
128
135
130
IL1
IL2
ILm
AL1
AL2
ALm

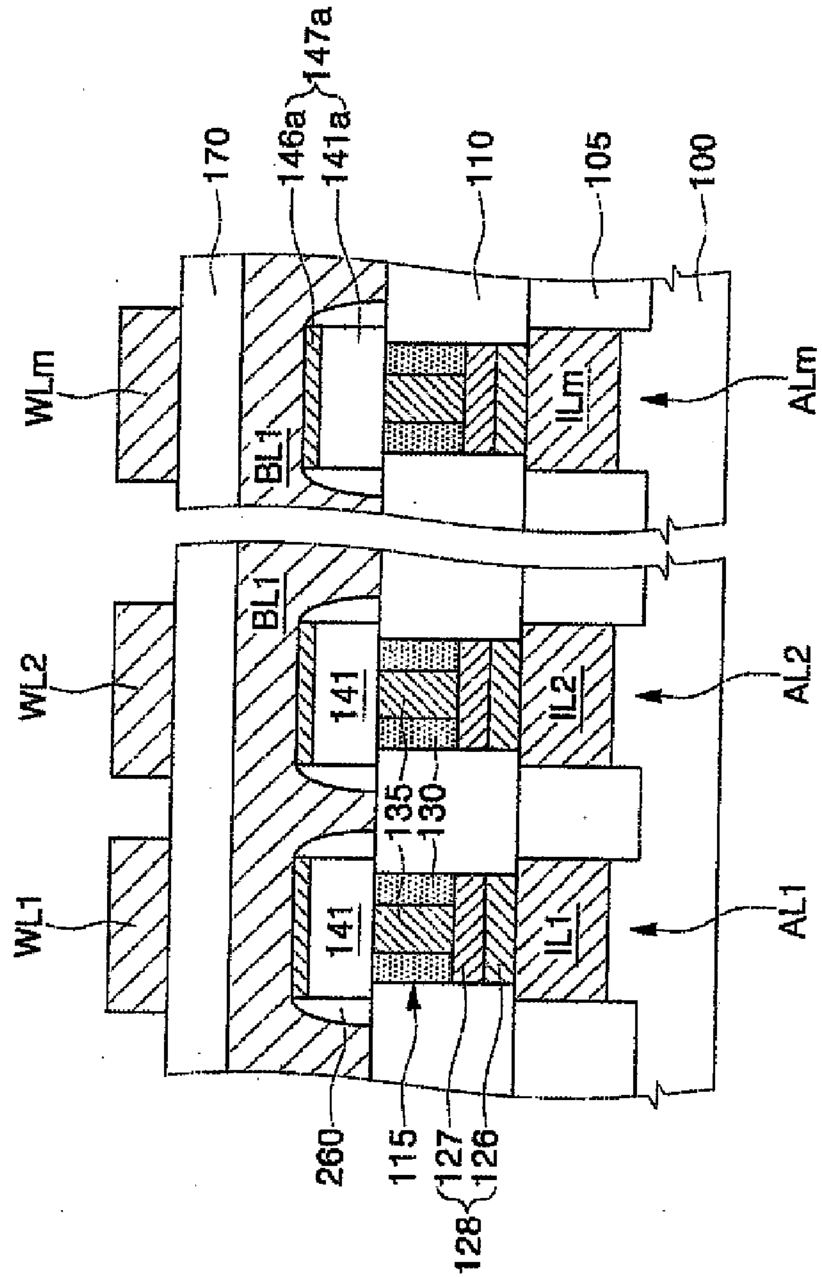


FIG. 8C

MEMORY DEVICE HAVING HIGHLY INTEGRATED CELL STRUCTURE AND METHOD OF ITS FABRICATION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of application Ser. No. 11/428,500, filed Jul. 3, 2006 which claims the benefit of Korean Patent Application No. 10-2005-0059414, filed on Jul. 1, 2005, the contents of which are hereby incorporated herein by reference in their entirety.

BACKGROUND

[0002] 1. Field of the Invention

[0003] The present invention relates to a semiconductor device and a method of its fabrication, and more particularly, to a memory device having a highly integrated cell structure and a method of its fabrication.

[0004] 2. Description of Related Art

[0005] Nonvolatile memory devices do not lose their stored data even if their power is interrupted. In general, nonvolatile memory devices employ flash memory cells having a stacked gate structure. The stacked gate structure includes a tunnel oxide layer, a floating gate, an inter-gate dielectric layer, and a control gate electrode, which are sequentially stacked on a channel. Accordingly, the tunnel oxide layer should have improved film quality and the coupling ratio of the flash memory cells should be increased to enhance the reliability and programming efficiency of the flash memory cells.

[0006] Novel nonvolatile memory devices, for example, phase-change memory devices, have been proposed as a substitute to conventional flash memory devices. In the phase-change memory devices, a unit cell includes a cell switching device and a phase-change material layer connected to the cell switching device. In this case, an upper electrode and a lower electrode are provided on and under the phase-change material layer, respectively. The lower electrode may be electrically connected to the cell switching device, and the upper electrode may be electrically connected to a bit line provided on the phase-change material layer. The cell switching device may be an active device, such as a MOS transistor.

[0007] Particularly in recent years, semiconductor devices are highly integrated. Accordingly, to enhance the integration density of a memory device, it is necessary to reduce the area occupied by a unit cell of the memory device.

[0008] A large program current, which is supplied through the MOS transistor, of at least several mA is required to program the phase-change memory cell. To reduce the area occupied by the unit cell of the memory device, the area of the MOS transistor used as the switching device needs to be reduced. However, it is technically difficult to reduce its area.

[0009] Also, the phase-change material layer should be formed to a small size to scale down the unit cell of the memory device. In particular, when the phase-change material layer is formed in an island form using typical photolithography and etching processes, there is a technical limit in reducing its size.

[0010] Furthermore, as the integration density of the memory devices increases, since the area of the unit cells of the memory device correspondingly decreases, it may be difficult to form the upper electrode contacting a top surface of the phase-change material layer. In particular, as the size of the phase-change material layer decreases, the margin of the process of forming the upper electrode interposed between the phase-change material layer and the bit line provided on the phase-change material layer also decreases, and thus the process of forming the upper electrode becomes difficult. Specifically, the upper electrode, which is interposed between the phase-change material layer and the bit line and in contact with the top surface of the phase-change material layer, may include a top electrode contact (TEC) and a contact plug. In forming the TEC, which contacts the top surface of the phase-change material layer, and the contact plug, which connects the TEC and the bit line, the phase-change material layer may be misaligned with the contact plug as a consequence of the downscaling of the phase-change material layer. Thus, the phase-change material layer may be misaligned with the bit line.

[0011] Therefore, it is necessary to develop a novel structure and method for reducing the area occupied by the unit cells of the memory device to increase the integration density of the memory device.

SUMMARY

[0012] Embodiments of the invention provide a memory device having a highly integrated cell structure.

[0013] Other embodiments of the inventions provide methods of fabricating a memory device having a highly integrated cell structure.

[0014] In one embodiment, the memory device includes a mold insulating layer disposed on a semiconductor substrate. At least one conductive line is disposed on the mold insulating layer. Data storage elements are interposed between the conductive line and the mold insulating layer to be self-aligned with the conductive line.

[0015] In some embodiments of the present invention, each of the data storage elements may include a resistor pattern and a barrier pattern, which are sequentially stacked, and the resistor pattern may be self-aligned with the barrier pattern. The resistor pattern may be a phase-change material layer pattern. The barrier pattern may include a metal nitride layer.

[0016] In other embodiments, the conductive line may include a metal nitride layer and a metal layer, which are sequentially stacked.

[0017] In still other embodiments, the memory device may further include insulating material layer patterns covering sidewalls of the data storage elements, which are substantially parallel to a widthwise direction of the conductive line. The insulating material layer patterns may be arranged in lines such that the insulating material layer patterns fill regions between the data storage elements and cross the conductive line. The memory device may further include protective insulating layer patterns interposed between the insulating material layer patterns and the data storage elements and between the insulating material layer patterns and the mold insulating layer.

[0018] In yet other embodiments, the memory device may further include a semiconductor pattern and a lower electrode interposed between the semiconductor substrate and the data storage element. The semiconductor pattern and the lower electrode may be sequentially stacked on the semiconductor substrate through the mold insulating layer. The semiconductor pattern may constitute a vertical-contact-type cell diode. The memory device may further include an insulating contact spacer interposed between the mold insulating layer and the lower electrode.

[0019] Another aspect of the present invention is directed to a method of fabricating a memory device having a highly integrated cell structure. The method includes forming a mold insulating layer on a semiconductor substrate. A plurality of parallel data storage element lines is formed on the mold insulating layer. At least one conductive line is formed across the data storage element lines. The data storage element lines are etched using the conductive line as an etch mask, thereby forming data storage elements self-aligned with the conductive line at intersections between the conductive line and the data storage elements lines.

[0020] In some embodiments of the present invention, each of the data storage element lines may be formed by sequentially stacking a resistor line and a barrier layer. The resistor line may include a phase-change material layer. The barrier layer may include a metal nitride layer.

[0021] In other embodiments, the conductive line may be formed by sequentially stacking a metal nitride layer and a metal layer.

[0022] In still other embodiments, after the data storage element lilies are formed, insulating protective spacers may be further formed to cover sidewalls of the data storage element lines.

[0023] In yet other embodiments, after the data storage element lines are formed, interlayer dielectric layer patterns may be further formed between the data storage element lines. The formation of the interlayer dielectric layer patterns may include forming an interlayer dielectric layer on the semiconductor substrate having the data storage element lines, and planarizing the interlayer dielectric layer. Before the interlayer dielectric layer is formed, a protective insulating layer may be further formed on the semiconductor substrate having the data storage element lines.

[0024] Still another aspect of the present invention is directed to a method of fabricating a memory device having a highly integrated cell structure. The method includes forming a mold insulating layer on a semiconductor substrate. Cell diode holes are formed through the mold insulating layer. A semiconductor pattern and a lower electrode are sequentially stacked in each of the cell diode holes. The cell diode holes are covered by a plurality of parallel data storage element lines. At least one conductive line is formed across the data storage element lines to be substantially aligned with upper portions of the cell diode holes in a vertical direction. The data storage element lines are etched using the conductive line as an etch mask, thereby forming data storage elements self-aligned with the conductive line at intersections between the conductive line and the data storage element lines.

[0025] In some embodiments of the present invention, the semiconductor pattern may constitute a vertical-contact-type cell diode.

[0026] In other embodiments, before the lower electrode is formed, insulating contact spacers may be further formed on sidewalls of the cell diode holes, which are exposed due to a step difference between a top surface of the mold insulating layer and a surface of the semiconductor pattern.

[0027] In still other embodiments, each of the data storage element lines may be formed by sequentially stacking a resistor line and a barrier layer. The resistor line may include a phase-change material layer. The barrier layer may include a metal nitride layer.

[0028] In yet other embodiments, the conductive line may be formed by sequentially stacking a metal nitride layer and a metal layer.

[0029] In still other embodiments, after the data storage element lines are formed, insulating protective spacers may be further formed to cover sidewalls of the data storage element lines.

[0030] In yet other embodiments, after the data storage element lines are formed, interlayer dielectric layer patterns may be further formed between the data storage element lines. The formation of the interlayer dielectric layer patterns may include forming an interlayer dielectric layer on the semiconductor substrate having the data storage elements, and planarizing the interlayer dielectric layer.

BRIEF DESCRIPTION

[0031] The foregoing and other objects, features and advantages of the invention will be apparent from the more particular description of exemplary embodiments of the invention, as illustrated in the accompanying drawings. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

[0032] FIG. **1** is a plan view of a memory device according to exemplary embodiments of the present invention.

[0033] FIGS. **2**A, **3**A, **4**A, **5**A, **6**A, **7**A, and **8**A are cross-sectional views taken along line I-I' of FIG. **1**, illustrating a memory device according to exemplary embodiments of the present invention.

[0034] FIGS. **2**B, **3**B, **4**B, **5**B, **6**B, **713**, and **8**B are cross-sectional views taken along line II-II' of FIG. **1**, which illustrate a memory device according to exemplary embodiments of the present invention.

[0035] FIGS. **6**C, **7**C, and **8**C are cross-sectional views taken along line II-II', of FIG. **1**, illustrating a memory device according to other exemplary embodiments of the present invention.

DETAILED DESCRIPTION

[0036] The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. This invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure is thorough and complete and fully conveys the scope of the invention to those skilled in the art. In the drawings, the thicknesses of layers and regions are exaggerated for clarity. The same reference numerals are used to denote the same elements.

[0037] FIG. **1** is a plan view of a memory device according to exemplary embodiments of the present invention. FIGS. **2**A, **3**A, **4**A, **5**A, **6**A, **7**A, and **8**A are cross-sectional views taken along line I-I' of FIG. **1**, illustrating a memory device according to exemplary embodiments of the present invention. FIGS. **2**R, **3**B, **4**B, **5**B, GB, **7**R, and **8**B are cross-sectional views taken along line II-II of FIG. **1**, illustrating a memory device according to exemplary embodiments of the present invention. FIGS. **6**C, **7**C, and **8**C are cross-sectional views taken along line II-II, of FIG. **1**, illustrating a memory device according to other exemplary embodiments of the present invention.

[0038] First, a memory device according to exemplary embodiments of the present invention will now be described with reference to FIGS. **1**, **8**A, and **8**B.

[0039] Referring to these figures, a plurality of impurity regions. e.g., an m-number of impurity regions IL**1**, IL**2**, . . .

, and ILm, may be disposed parallel to each other on predetermined regions of a semiconductor substrate **100** of a first conductivity type. A separation layer **105** may be disposed between the impurity regions IL**1**, IL**2**, . . . , and ILm to separate the impurity regions IL1, IL2, . . . , and ILm from each other. The separation layer **105** may be a trench isolation layer formed in a predetermined region of the semiconductor substrate **100**. In this case, the impurity regions IL1, IL2, . . . , and ILm may be provided in a plurality of active regions, respectively, each of which is defined by the trench isolation layer. The active regions may be an m-number of active regions AL**1**, AL**2**, . . . , and ALm. The active regions AL1, AL**2**, . . . , and ALm may be cell active regions defined in a cell region of the memory device. The impurity regions IL**1**, IL2, . . . , and ILm may have a second conductivity type different from the first conductivity type.

[0040] In exemplary embodiments of the present invention, it is assumed that the first and second conductivity types are a p-type and an n-type, respectively, for clarity of explanation. However, the first and second conductivity types may be an n-type and a p-type, respectively.

[0041] A mold insulating layer **110** is disposed on the semiconductor substrate **100** having the impurity regions IL**1**, IL2, . . . , and ILm and the separation layer **105**. Predetermined regions of the impurity regions IL**1**, IL**2**, . . . , and ILm are exposed by a plurality of cell diode holes **115** that penetrate the mold insulating layer **110**. Lower regions of the cell diode holes **115** may be filled with semiconductor patterns **128**, respectively. Each of the semiconductor patterns **128** may include a first semiconductor pattern **126** and a second semiconductor pattern **127** that are sequentially stacked. The second semiconductor patterns **127** may have the second conductivity type, and the first semiconductor patterns **126** may have the first or second conductivity type. When the first semiconductor patterns **126** have the first conductivity type, the first and second semiconductor patterns **126** and **127**, which are sequentially stacked in the cell diode holes **115**, constitute cell diodes, respectively. Alternatively when both the first and second semiconductor patterns **126** and **127** have the first conductivity type, the first semiconductor patterns **126** and the impurity regions IL**1**, IL**2**, . . . , and ILm that contact the first semiconductor patterns **126**, constitute cell diodes, respectively. Therefore, the cell diodes may be vertical-contact-type cell diodes.

[0042] Cell diode electrodes (not shown) may be provided on top surfaces of the second semiconductor patterns **127**, respectively. The cell diode electrodes may be include a metal silicide layer, and have surfaces lower than the top surface of the mold insulating layer **110**. Lower electrodes **135** are respectively disposed in the cell diode holes **115** on the cell diode electrodes. Surfaces of the lower electrodes **135** may be substantially the same level as, or lower than, the top surface of the mold insulating layer **110**.

[0043] At least one conductive line is disposed on the mold insulating layer **110**. In exemplary embodiments of the present invention, a plurality of other conductive lines may be provided parallel to the conductive line. That is, a plurality of parallel conductive lines may be disposed on the mold insulating layer **110**.

[0044] Hereinafter, for clarity of explanation, the conductive lines will be referred to as bit lines. The bit lines comprise an n-number of bit lines BL**1**, BL**2**, . . . , and BLn. The bit lines BL**1**, BL**2**, . . . , and BLn are formed of a conductive material layer. For example, they may be formed of a single metal layer, or a sequentially stacked metal nitride layer and a metal layer. The metal nitride layer may be a titanium nitride layer.

[0045] Data storage elements **147***a*, self-aligned with the bit lines BL**1**, BL**2**, . . . , and BLn, are interposed between the mold insulating layer **110** and the bit lines. In other words, the data storage elements **147***a* are each self-aligned with one selected bit line, and disposed under that selected bit line. When viewed in a plan view, each of the data storage elements **147***a* may have a substantially tetragonal shape. That is, each of the data storage elements **147***a* may have four sidewalls. A pair of opposite sidewalls of the data storage elements **147***a* are self-aligned with the bit lines BL**1**, RL**2**, . . . , and BLn to be parallel to a lengthwise direction of the bit lines. The other pair of opposite sidewalls of the data storage elements **147***a* may be parallel to a widthwise direction of the bit lines. In other words, one pair of opposite sidewalls is generally parallel to the bit lines, while the other pair of sidewalls is perpendicular to the bit lines.

[0046] The data storage elements **147***a* are spaced apart from each other. That is, the data storage elements **147***a* may be island shaped, spaced apart from each other. The data storage elements **147***a* respectively cover the lower electrodes **135**. Accordingly, the bit lines BL**1**, BL**2**. . . . , and BLn may pass over the lower electrodes **135**.

[0047] The data storage elements **147***a* include resistor patterns **141***a* and barrier patterns **146***a* that are sequentially stacked. The resistor patterns **141***a* may include a material layer whose resistance varies with current. For instance, the resistor patterns **141***a* may include a phase-change material layer with a resistance that depends on a phase of the phase-change material layer, and the resistance varies with current flowing through the resistor patterns **141***a*. For example, the phase-change material layer may include a chalcogenide layer. Thus, the resistor patterns **141***a* can be realized as a variable resistor. The barrier patterns **146***a* may comprise a metal nitride layer, such as a titanium nitride layer, and may serve as an upper electrode.

[0048] Insulating material layer patterns cover the opposite sidewalls of the data storage elements **147***a* that are substantially parallel to the widthwise direction of the bit lines BL**1**, BL**2**, . . . , and BLn. When viewed from above, the insulating material layer patterns may be arranged in parallel lines that cross the bit lines. In this case, the insulating material layer patterns are disposed below the bit lines at intersections between the insulating material layer patterns and the bit lines. Specifically, regions between the data storage elements **147***a* disposed under one selected bit line may be filled with the insulating material layer patterns, as shown in FIG. **8**B. In this case, the insulating material layer patterns may be interlayer dielectric patterns **160**. That is, the interlayer dielectric patterns **160** may fill the regions between the data storage elements **147***a* and be disposed under the bit lines BL**1**, BL**2**, . . . , and BLn so that the bit lines overlap the interlayer dielectric patterns **160**. The interlayer dielectric patterns **160** may be substantially vertically aligned with the separation layer **105**. Further, protective insulating layer patterns **155***a* may be interposed between the interlayer dielectric patterns **160** and the data storage elements **147***a* and between the interlayer dielectric patterns **160** and the mold insulating layer **110**.

[0049] Meanwhile, according to another embodiment, as shown in FIG. **8**C, the insulating material layer patterns covering the opposite sidewalls of the data storage elements **147***a*

that are parallel to the widthwise direction of the bit lines BL**1**, . . . , and BLn, may be insulating protective spacers **260**.

[0050] An inter-metal dielectric layer **170** covers the bit lines BL**1**, BL**2**, . . . , and BLn. Thus, the inter-metal dielectric layer **170** may cover the sidewalls of the data storage elements **147***a* that are parallel to the lengthwise direction of the bit lines, and the insulating material layer patterns may cover the sidewalls of the data storage elements **147***a* that are parallel to the widthwise direction of the bit lines. That is, the sidewalls of the data storage elements **147***a* that are substantially parallel to the widthwise direction of the bit lines may be covered by the interlayer dielectric patterns **160** or the protective insulating layer patterns **155***a*, as shown in FIG. **8**B, or covered by the insulating protective spacers **260**, as shown in FIG. **8**C.

[0051] Conductive plugs **175** are formed through the inter-metal dielectric layer **170**. The conductive plugs **175** may be in ohmic contact with the predetermined regions of the impurity regions IL**1**, IL**2**, . . . , and ILm. Metal interconnections may be disposed on the inter-metal dielectric layer **170** to cover the conductive plugs **175**. The metal interconnections may function as word lines. That is, a plurality of parallel word lines, i.e., an m-number of word lines WL**1**, WL**2**, . . . , and WLm may be disposed on the inter-metal dielectric layer **170**. The word lines WL**1**, WL**2**, . . . , and WLm may cover the conductive plugs **175** and cross the bit lines BL**1**, BL**2**, . . . , and BLn, It is obvious to one skilled in the art that the connection structure of the word lines WL**1**, WL**2**, . . . , and WLm can be modified according to design conditions.

[0052] As described above, a unit cell may include a vertical-contact-type cell diode, a lower electrode **135**, and a data storage element **147***a* that are vertically aligned with each other and sequentially stacked on the semiconductor substrate **100**. As a result, the integration density of the cell can be increased. Further, each of the bit lines BL**1**, BL**2**, . . . , and BLn, which covers the data storage elements i**47***a*, is self-aligned with the data storage elements **147***a*. That is, the data storage elements **147***a*, which are disposed under the bit lines, are arranged to be self-aligned with the bit lines, thus increasing the integration density of the cell. Accordingly, it is possible to minimize the planar area of the unit cell including at least one data storage element self-aligned with at least one selected bit line under the selected bit line, a lower electrode contacting a bottom surface of the data storage element, and a cell diode connected to a bottom surface of the lower electrode. As a result, the cell structure can be highly integrated.

[0053] Hereinafter, methods of fabricating a memory device according to exemplary embodiments of the present invention will be described with reference to FIGS. **1**, **2**A, **3**A, **4**A, **5**A, **6**A, **7**A, **8**A, **2**B, **3**B, **4**B, **5**B, **6**B, **7**B, and **8**B.

[0054] Referring to FIGS. **1**, **2**A and **2**B, a semiconductor substrate **100** of a first conductivity type is prepared. A separation layer, for example, an isolation layer **105**, may be formed in predetermined regions of the semiconductor substrate **100** to define a plurality of active regions. The isolation layer **105** may be a shallow trench isolation layer. The active regions may be an m-number of active regions AL**1**, AL**2**, . . . , and ALm. The active regions may be defined to be substantially parallel to each other. Impurity ions of a second conductivity type different from the first conductivity type are implanted into the active regions AL**1**, AL**2**, . . . , and ALm, thereby forming impurity regions **11**,**1**, IL**2**, . . . , and ILm of the second conductivity type. As a result, the isolation layer **105** serves to electrically isolate the impurity regions of the second conductivity type from each other. The first and second conductivity types may be p and n-type, respectively, or vise versa.

[0055] A mold insulating layer **110** is formed on the entire surface of the semiconductor substrate **100** having the impurity regions IL**1**, IL**2**, . . . , and ILm of the second conductivity type. The mold insulating layer **110** may include a silicon oxide layer.

[0056] Referring to FIGS. **1**, **3**A, and **3**B, the mold insulating layer **110** is patterned to form cell diode holes **115** that expose predetermined regions of the impurity regions IL**1**, IL**2**, . . . , and ILm of the second conductivity type.

[0057] A semiconductor layer is formed to fill the cell diode holes **115**. The semiconductor layer may be obtained using a selective epitaxial growth (SEG) technique, which employs the exposed regions of the impurity regions IL**1**, IL**2**, . . . , and ILm of the second conductivity type as seed layers. Therefore, when the impurity regions of the second conductivity type have a single crystalline structure, the semiconductor layer also may be formed to have a single-crystalline structure. When the SEG technique makes use of a silicon source gas, the semiconductor layer may be a silicon layer. The semiconductor layer may have a top surface higher than a top surface of the mold insulating layer **110**. In this case, the semiconductor layer may be planarized to leave semiconductor patterns **120** in the cell diode holes **115**. As a result, the semiconductor patterns **120** may have flat surfaces at the same level as the top surface of the mold insulating layer **110**.

[0058] Alternatively, the semiconductor layer may be obtained using a solid phase epitaxial (SPE) technique. **111** this case, the semiconductor patterns **120** may be formed by planarizing the semiconductor layer obtained using the SPE technique.

[0059] Referring to FIGS. **1**, **4**A and **4**B, the semiconductor patterns **120** are partially etched to form recessed semiconductor patterns **128** having surfaces lower than the top surface of the mold insulating layer **110**. As a result, upper regions of the cell diode holes **115** are exposed to form upper cell diode holes. Impurity ions of the first or second conductivity type are implanted into lower regions of the recessed semiconductor patterns **128**, thereby forming first semiconductor patterns **126**. Accordingly, the first semiconductor patterns **126** may have the first or second conductivity type. Also, impurity ions of the first conductivity type are implanted into upper regions of the recessed semiconductor patterns **128**, thereby forming second semiconductor patterns **127**. Thus, the second semiconductor patterns **127** may have the first conductivity type. The ion implantation process for forming the first semiconductor patterns **126** may be performed after the ion implantation process for forming the second semiconductor patterns **127**.

[0060] When the first semiconductor patterns **126** are doped with the impurity ions of the second conductivity type, the first and second semiconductor patterns **126** and **127**, which are sequentially stacked in the cell diode holes **115**, constitute cell diodes, respectively. Alternatively, when the first semiconductor patterns **126** are doped with the impurity ions of the first conductivity type, the impurity regions IL**1**, IL**2**, . . . , and ILm of the second conductivity type and the first semiconductor patterns **126**, which contact the impurity regions, constitute cell diodes, respectively. Therefore, the cell diodes may be formed as vertical-contact-type cell diodes.

[0061] Although not shown in the drawings, cell diode electrodes may be formed on surfaces of the second semiconductor patterns **127**. The cell diode electrodes may include a metal silicide layer, such as a cobalt silicide layer, a nickel silicide layer, or a titanium silicide layer. The metal silicide layer may be formed using a typical self-aligned silicide (salicide) technique. In this case, the cell diode electrodes may still have surfaces lower than the top surface of the mold insulating layer **110**.

[0062] Insulating contact spacers **130** may be formed to cover the exposed sidewalls of the upper cell diode holes. The insulating contact spacers **130** may include a silicon oxide layer or a silicon nitride layer. Subsequently, a conductive layer is formed on the semiconductor substrate **100** having the insulating contact spacers **130** to fill the upper cell diode holes. The conductive layer is planarized until the top surface of the mold insulating layer **110** is exposed, thereby forming lower electrodes **135** remaining in each of the upper cell diode holes. Specifically, the planarization of the conductive layer may be performed using a chemical mechanical polishing (CMP) technique until the top surface of the mold insulating layer **110** is exposed. As a result, surfaces of the lower electrodes **135** may be substantially level with the top surface of the mold insulating layer **110**. Alternatively, the conductive layer may be planarized by an etch back process to expose the top surface of the mold insulating layer **110**, in which case the surfaces of the lower electrodes **135** may be lower than the top surface of the mold insulating layer **110**.

[0063] The lower electrodes **135** may include a conductive layer that does not react with phase-change material layers, which will be formed in a subsequent process. For example, the lower electrodes **135** may comprise a metal nitride layer, such as a titanium nitride layer.

[0064] Referring to FIGS. **1**, **5**A and **5**B, a plurality of parallel memory patterns **152** are formed on the semiconductor substrate having the lower electrodes **135** to cover the lower electrodes **135**, respectively. The memory patterns **152** may be formed by sequentially stacking data storage element lines **147** and sacrificial insulating layer patterns **151**. The data storage element lines **147** may be obtained by sequentially stacking resistor lines **141** and barrier layers **146**. The resistor lines **141** may include a material layer with a resistance that varies with current. For example, the resistor lines **141** may include a phase-change material layer with a resistance that depends on a phase of the phase-change material layer. As an example, the phase-change material layer may be a chalcogenide layer. The barrier layers **146** may include a material that does not react with the resistor lines **141**. For example, the barrier layers **146** may comprise a metal nitride layer such as a titanium nitride layer. The sacrificial insulating layer patterns **151** may include a silicon nitride layer.

[0065] The sacrificial insulating layer patterns **151** may be omitted. If so then the memory patterns **152** may include only the data storage element lines **147**, i.e., the resistor lines **141** and the barrier layers **146** that are sequentially stacked.

[0066] Referring to FIGS. **1**, **6**A, and **6**B, a protective insulating layer **155** may be conformably formed on the semiconductor substrate having the sacrificial insulating layer patterns **151**. An interlayer dielectric layer is formed on the entire surface of the semiconductor substrate having the protective insulating layer **155**. The interlayer dielectric layer may include a material having an etch selectivity with respect to the sacrificial insulating layer patterns **151**. For example, when the sacrificial insulating layer patterns **151** are formed of a silicon nitride layer, the interlayer dielectric layer may be a silicon oxide layer. In this case, the protective insulating layer **155** may include a material having a different polishing rate from the interlayer dielectric layer. For example, when the interlayer dielectric layer is formed of a silicon oxide layer, the protective insulating layer **155** may include a silicon nitride.

[0067] The interlayer dielectric layer is planarized, thereby forming interlayer dielectric layer patterns **160** that remain between the memory patterns **152**. When the protective insulating layer **155** is formed or a material having a different polishing rate from the interlayer dielectric layer, the interlayer dielectric layer may be planarized using the protective insulating layer **155** as a planarization stop layer.

[0068] The protective insulating layer **155** may be omitted. If so then the interlayer dielectric layer may include a material having a different polishing rate from, and an etch selectivity with respect to, the sacrificial insulating layer patterns **151**. For example, when the sacrificial insulating layer patterns **151** are formed of a silicon nitride layer, the interlayer dielectric layer may be a silicon oxide layer.

[0069] Meanwhile, according to another embodiment, as shown in FIG. **6**C, after the data storage element lines **147** are formed, insulating protective spacers **260** may be formed to cover sidewalls of the data storage element lines **147**. Specifically, an insulating layer may be conformably formed on the semiconductor substrate having the data storage element lines **147**. Subsequently, the insulating layer may be anisotropically etched to form the insulating protective spacers **260** covering the sidewalls of the data storage element lines **147**. As a result, the sidewalls of the data storage element lines **147** may be covered by the insulating protective spacers **260**, and top surfaces of the data storage element lines **147** may be exposed.

[0070] Referring to FIGS. **1**, **7**A, and **7**B, a process of exposing the top surfaces of the data storage element lines **147** is carried out. The top surfaces of the data storage element lines **147** may be exposed by an etching process. Specifically, when the sacrificial insulating layer patterns (**151** of FIGS. **6**A and **6**B) and the protective insulating layer (**155** of FIGS. **6**A and **6**R) are formed on the data storage element lines **147**, the protective insulating layer (**155** of FIGS. **6**A and **6**B) and the sacrificial insulating layer patterns (**151** of FIGS. **6**A and **6**B) are selectively removed on the data storage element lines **147**. As a result, the top surfaces of the data storage element lines **147** may be exposed. In this case, protective insulating layer patterns **155***a* may be formed to cover not only a bottom surface and sidewalls of the interlayer dielectric layer patterns **160**, but also sidewalls of the data storage element lines **147**.

[0071] Alternatively, when the protective insulating layer (**155** of FIGS. **6**A and **6**B) is omitted, the sacrificial insulating layer patterns (**151** of FIGS. **6**A and **6**B) are selectively removed on the data storage element lines **147**. As the top surfaces of the data storage element lines **147** are exposed, top surfaces of the interlayer dielectric layer patterns **160** may be lowered to some extent. However, the top surfaces of the interlayer dielectric layer patterns **160** may still be higher than the top surfaces of the data storage element lines **147**.

[0072] Thereafter, a conductive layer is formed on the entire surface of the semiconductor substrate **100** having the data storage element lines **147** and the interlayer dielectric layer patterns **160**. The conductive layer is patterned to form at least one conductive line crossing the data storage element lines **147** and the interlayer dielectric layer patterns **160**.

[0073] Meanwhile, a hard mask layer may be formed on the conductive layer. Thus, a hard mask pattern (not shown) may be formed on the conductive line. The conductive line may be a bit line. The bit line may be plurally formed. That is, a plurality of parallel bit lines may be formed across the data storage element lines **147** and the interlayer dielectric layer patterns **160**. The bit lines may be formed to include an n-number of bit lines BL**1**, BL**2**, . . . , and BLn.

[0074] Meanwhile, when insulating protective spacers **260** are formed, as shown in FIG. **6**C, the parallel bit lines BL**1**, BL**2**, . . . , and BLn may be formed across the insulating protective spacers **260** and the data storage element lines **147**, as shown in FIG. **7**C. As a result, the sidewalls of the data storage elements **147***a* (yet to be formed, as in FIGS. **8**A and **8**B), which are substantially parallel to a widthwise direction of the bit lines BL**1**, BL**2**, . . . , and BLn, may be covered by the bit lines. In this case, the bit lines may be formed by sequentially stacking a metal nitride layer and a metal layer. Here, the data storage element lines **147** may include resistor lines **14 1**. The metal nitride layer can prevent the resistor lines **141** from reacting with 5 the metal layer.

[0075] Referring to FIGS. **1**, **8**A, and **8**B, the data storage element lines (**147** of FIGS. **7**A and **7**B) are etched using the bit lines BL**1**, BL**2**, . . . , and BLn as an etch mask. Thus, data storage elements **147***a* are formed at intersections between the bit lines and the data storage element lines **147** to be self-aligned with the bit lines. As a result, sidewalls of the data storage elements **147***a*, which are parallel to a lengthwise direction of the bit lines BL**1**, BL**2**, . . . , and BLn. may be exposed as shown in FIG. **8**A. Each of the data storage elements **147***a* may be formed in an island shape spaced apart from each other. The sidewalls of the data storage elements **147***a*, which are substantially parallel to the widthwise direction of the bit lines BL**1**, BL**2**, . . . , and BLn, may be covered by the interlayer dielectric layer patterns **160** or the protective insulating patterns **155** a as shown in FIG. **8**B.

[0076] Alternatively, the sidewalls of the data storage elements **147***a*, which are substantially parallel to the widthwise direction of the bit lines BL**1**, BL**2**, . . . , and BLn. may be covered by the insulating protective spacers **260** as shown in FIG. **8**C. That is, the sidewalls of the data storage elements **147***a*, which are substantially parallel to the widthwise direction of the bit lines, may be covered by insulating material layer patterns.

[0077] Meanwhile, when the formation of the insulating material layer patterns is omitted, the sidewalls of the data storage elements **147***a*, which are substantially parallel to the widthwise direction of the bit lines, may be covered by the bit lines. In this case, the bit lines may be formed by sequentially stacking a metal nitride layer and a metal layer.

[0078] As described above, the formation of the data storage elements **147** may be performed by a photolithography process for forming the bit lines BL**1**, BL**2**, . . . , and BLn. The data storage elements **147***a* may be substantially formed by photolithography processes for forming line patterns. As a result, the size of the data storage elements **147***a* and a distance between the data storage elements **147***a* may be determined by a photolithography process that can minimize line widths. Accordingly, the area occupied by the data storage elements **147***a* can be minimized. As a result, the area of a unit cell can be reduced, thus the integration density of a memory device can be improved. Also, since the data storage elements **147***a* can be formed to be self-aligned with the bit lines BL**1**, BL**2**, . . . , and BLn, any misalignment between the data storage elements **147***a* and the bit lines can be solved.

[0079] The data storage elements **147***a* may be formed by sequentially stacking resistor patterns **141***a* and barrier patterns **146***a*. Thus, the resistor patterns **141***a* and the barrier patterns **146***a* are formed by substantially the same process. Accordingly, the resistor patterns **14 1** a can be self-aligned with the barrier patterns **146***a*.

[0080] An inter-metal dielectric layer **170** is formed on the semiconductor substrate having the data storage elements **147***a*. The inter-metal dielectric layer **170** may include silicon oxide. The inter-metal dielectric layer **170** may be patterned to form openings **171** that expose predetermined regions of the impurity regions IL**1**, IL**2**, . . . , and ILm, respectively. The openings **171** may be filled with conductive plugs **175**, respectively.

[0081] Thereafter, a plurality of parallel metal interconnections may be formed on the inter-metal dielectric layer **170** to cover the conductive plugs **175** and cross the bit lines BL**1**, BL**2**, . . . , and BLn. The metal interconnections may serve as word lines that include an m-number of word lines WL**1**, WL**2**, . . . , and WLm.

[0082] Meanwhile, when the bit lines BL**1**, BL**2**, . . . , and BLn are formed on the semiconductor substrate having the insulating protective spacers **260**, as described with reference to FIG. **7**C, the data storage element lines (**147** of FIGS. **7**A and **7**C) are selectively removed using the bit lines BT,**1**, BL**2**, . . . , and BLn as a mask as shown in FIG. **8**C. Thus, final data storage elements **147***a* are formed at intersections between the bit lines and the data storage element lines (**147** of FIGS. **7**A and **7**C) to be self-aligned the bit lines. Accordingly, the sidewalls of the data storage elements **147***a*, which are parallel to the lengthwise direction of the bit lines, may be exposed. Subsequently, as described above with reference to FIGS. **8**A and **8**B, the inter-metal dielectric layer **170** covering the bit lines, the conductive plugs **175** passing through the inter-metal dielectric layer **170**, and the word lines WL**1**, WL**2**, . . . , and WLm covering the conductive plugs **175** may be sequentially formed.

[0083] According to the present invention, as described above, a unit cell may include a vertical-contact-type cell diode, a lower electrode, and a data storage element, which arc sequentially stacked on a semiconductor substrate and self-aligned with each other in a vertical direction. The data storage element is self-aligned with a bit line that covers and crosses the data storage element. The data storage element may include a resistor pattern and a barrier pattern, which are sequentially stacked. The resistor pattern and the barrier pattern can be formed using substantially the same process. That is, the resistor pattern can be self-aligned with the barrier pattern. Since the data storage element is formed to be self-aligned with the bit line, the size of the data storage element can be minimized. This results in the minimization of the planar area of a memory cell that includes the data storage element self-aligned with the bit line under the bit line, the lower electrode connected to, and disposed under, the data storage element, and the cell diode connected to, and disposed under, the lower electrode. Thus, a cell structure can be highly integrated. Consequently, the exemplary embodiments of the present invention can provide memory devices having a highly integrated cell structure.

[0084] Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection

with the embodiment is included in at least one embodiment of the present invention. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

[0085] Exemplary embodiments of the present invention have been disclosed herein and, although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. Accordingly, it will be understood by those of ordinary skill in the art that various changes in form and details may be made without departing from the spirit and scope of the present invention as set forth in the following claims.

What is claimed is:

1. A memory device comprising:

a mold insulating layer disposed over a semiconductor substrate;

a conductive line having sides disposed over the mold insulating layer; and

a data storage element interposed between the conductive line and the mold insulating layer so that sides of the data storage elements are aligned with the sides of the conductive line.

2. The memory device according to claim **1**, wherein the data storage element includes a resistor pattern and a barrier pattern that are sequentially stacked, the resistor pattern being self-aligned with the barrier pattern.

3. The memory device according to claim **2**, wherein the resistor pattern includes a phase-change material layer.

4. The memory device according to claim **2**, wherein the barrier pattern comprises a metal nitride layer.

5. The memory device according to claim **1**, wherein the conductive line includes a metal nitride layer and a metal layer that are sequentially stacked.

6. The memory device according to claim **1**, further comprising an insulating material layer pattern that covers opposite sidewalls of the data storage elements, the opposite sidewalls being substantially parallel to a widthwise direction of the conductive line.

7. The memory device according to claim **6**, wherein the insulating material layer pattern is arranged in a line to fill regions between the data storage elements, and to cross the conductive line.

8. The memory device according to claim **7**, further comprising a protective insulating layer pattern interposed between the insulating material layer pattern and the data storage element and between the insulating material layer pattern and the mold insulating layer.

9. The memory device according to claim **1**, further comprising a semiconductor pattern and a lower electrode interposed between the semiconductor substrate and the data storage element wherein the semiconductor pattern and the lower electrode are sequentially stacked on the semiconductor substrate through the mold insulating layer.

10. The memory device according to claim **9**, wherein the semiconductor pattern constitutes a vertical-contact-type cell diode.

11. The memory device according to claim **9**, further comprising an insulating contact spacer interposed between the mold insulating layer and the lower electrode.

12. A memory device comprising:

a mold insulating layer disposed on a semiconductor substrate;

a cell diode hole disposed in the mold insulating layer and including a cell diode;

a lower electrode disposed on the cell diode and in the cell diode hole;

a bit line disposed over the cell diode; and

a data storage element interposed between the bit line and the cell diode, the data storage element self-aligned with the bit line.

13. The memory device according to claim **12**, wherein the data storage element includes a resistor pattern and a barrier pattern that are sequentially stacked, the resistor pattern being self-aligned with the barrier pattern.

14. The memory device according to claim **13**, wherein the resistor pattern includes a phase-change material layer.

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