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(54) **Title:** METHOD AND APPARATUS FOR CIRCUIT WITH LOW IC POWER DISSIPATION AND HIGH DYNAMIC RANGE

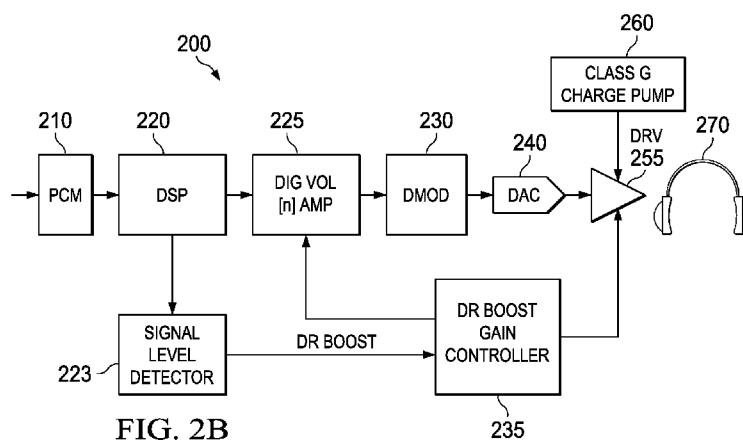


FIG. 2B

(57) **Abstract:** An apparatus comprises a selected volume detector (223) that detects a selected output volume; an analog output signal amplifier (255); a digital volume amplifier (225); a boost gain control element (235) coupled to the selected volume detector, the analog output signal amplifier and the digital volume amplifier. The boost gain control element is configured to keep a gain of a path of the digital volume amplifier and the analog output signal amplifier substantially constant. The boost gain control element can adjust both a gain of the digital volume control and a gain of the analog output signal amplifier; to keep the gain of the path of the digital volume amplifier and the analog output signal substantially constant and equal to the selected output volume.

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METHOD AND APPARATUS FOR CIRCUIT
WITH LOW IC POWER DISSIPATION AND HIGH DYNAMIC RANGE

[0001] This is directed, in general, to an integrated circuit (IC) that has an audio channel that plays back audio signals encoded in any digital format compressed (such as MP3) or uncompressed (such as PCM), and more particular, to an audio channel with a low IC power dissipation and a high dynamic range (DR) is desired simultaneously.

BACKGROUND

[0002] Generally, as understood by the inventors, state of the art audio ICs for audio playback can have several limitations that can create engineering and user trade-offs between power dissipation and signal to noise ratio (SNR) as well as dynamic range (DR). In one instance, a best in class portable audio CODEC (i.e. capable of encoding or decoding a digital data stream or signal) has reported a MPEG-1 or MPEG-2 Audio Layer III (MP3) quiescent power at 4 milliwatts, and a best SNR is 101dB (Amplitude.) However, these parameters are not achieved simultaneously.

[0003] For example, turning to FIG. 1, a circuit 100, a prior art digital to analog (DAC) headphone playback channel, is illustrated. In the circuit 100, a pulse code modulation (PCM) codec 110 is coupled to a digital signal processor (DSP) 120. The DSP 120 is then oversampled at a demodulator (DMOD) 130, an output of which is coupled to an input of a digital to analog converter (ADC) 140. An analog signal of the DAC 140 is then conveyed to the driver 150, which is powered by a class “G” charge pump 160. This in turn, is used to power a pair of headphones 170.

[0004] However, as recognized by the Present Inventors, there are problems with this prior art circuit 100. Generally, the prior art circuit 100, as well as other circuits used for portable IC for an audio playback for a headphone (HP), encounter a problem of noise, be it white noise

or other, within the DMOD 120, the DAC 140, and the HP 170, that forces tradeoffs between power dissipation, die size, and so on, versus a dynamic range of the circuit 100.

[0005] Certain patents do generally address power savings in a prior art circuit 100, used for portable IC for an audio playback for a headphone (HP). For example, please see U.S. Patent No. 7,808,324 “Operating environment and process position selected charge-pump operating mode in an audio power amplifier integrated circuit” to Woodford et al, which is generally directed towards Class G efficiency, but not SNR or power of DAC, HP amp. U.S. Patent Application No. 11/610496 “Energy-Efficient Consumer Device Audio Power Output Stage” to Tucker et al, is generated directed to a low power audio playback path focused on CP mode control, but no description of dynamic range improvement or power reduction occurring simultaneously. U.S. Patent No. 7,622, 984, “Charge pump circuit and methods of operation thereof” to Lesso, et al, describes charge pump circuits to generate a plurality of positive and negative outputs using a single CFLY, but simultaneous DR improvement and power reduction is not addressed. U.S. Patent No. 7,714,660, entitled “Amplifier circuit and methods of operation thereof” to Lesso et al, which is generally directed to a charge pump and headphone amplifier circuit which is directed toward improving “efficiency”, but does not address dynamic range, instead 660 is used to control CP mode of operation to track the signal amplitude. Other references are U.S. App. No. 2011/0123048 “Class G Audio Amplifiers and Associated Methods of Operation” to Wang et al., and U.S. Pat App No. 2011.0084760 A1 to Guo, et al, may be directed to class G amplifiers, but they do not address a dynamic range improvement or power reduction occurring simultaneously.

[0006] Therefore, there is a need in the art to address at least some of the issues associated with dynamic range improvement or power reduction occurring simultaneously.

SUMMARY

[0007] A first aspect provides an apparatus, comprising: a selected volume detector that detects a selected output volume; an analog output signal amplifier; a digital volume amplifier; a digital gain control element coupled to the selected volume detector; the analog output signal amplifier; and the digital volume amplifier; wherein the gain control element is configured to: keep a channel gain of a path of the digital volume amplifier and an analog output signal amplifier substantially constant, wherein the digital gain control element can adjust both: a) a gain of the digital volume amplifier; and b) a gain of the analog output signal amplifier; to keep

the gain of the path of the digital volume amplifier and the analog output signal amplifier substantially constant and equal to the selected output volume designated for a suitable listening level.

[0008] A second aspect provides an apparatus, comprising: a selected volume detector that detects a selected output volume; an analog output signal amplifier; a digital volume amplifier; a gain control element coupled to a) the selected volume detector; b) the analog output signal amplifier; and the digital volume amplifier; wherein the gain control element is configured to: keep a gain of a path of the digital volume amplifier and the analog output signal amplifier substantially constant, wherein the boost gain control element can adjust both: a) a gain of the digital volume control; and b) a gain of the analog output signal amplifier; to keep the gain of the path of the digital volume amplifier and the analog output signal substantially constant and equal to the selected output volume, wherein the boost gain control element is further configured to: compare the selected output volume to a threshold value. If the selected output volume is below the threshold, then the gain control element can: a) adjust upwards a digital volume of the digital volume amplifier; and b) adjust downwards a volume of the amplifier, to keep the gain of the path of the digital volume amplifier and the analog output signal substantially constant and equal to the selected output volume.

[0009] In the third aspect, the digital gain control element in stated apparatus is adapted to adjust both a) and b) to be higher or lower in discrete steps of programmable magnitude such that the sum remains substantially constant. It is implied that the adjustment of a) and b) is complementary in direction or polarity to achieve the requirements of a substantially constant gain. The number of steps is also programmable in the apparatus. Programmability may be designed in the factory or made adjustable in the field. No explicit limits on the resolution or range of the gains are imposed by the apparatus.

[0010] In a fourth aspect, a method is provided determining if a selected output volume is greater than a volume threshold; increasing a gain of a digital amplifier if the selected output volume is not greater than the threshold volume; decreasing a gain of an amplifier if the selected output volume is not greater than the threshold volume; and wherein the gain of a path of the digital volume amplifier and the analog output signal substantially constant and seeks to be equal to the selected output volume.

BRIEF DESCRIPTION OF THE DRAWINGS

- [0011] FIG. 1 illustrates a prior art DAC-headphone playback channel;
- [0012] FIG. 2A illustrates a first analysis for dynamic allocation of a digital/analog gain partition of a DAC channel;
- [0013] FIG. 2B illustrates a second analysis for dynamic allocation of a digital/analog gain partition of a DAC channel
- [0014] FIG. 3 is an illustration of a usage of a dynamic allocation circuit of FIG. 2A and 2B with multiple outputs;
- [0015] FIG. 4 is an example of a method of using the dynamic allocation circuit of FIG. 2A and 2B;
- [0016] FIG. 5A is a graph of a dynamic digital/analog gain partition of a DAC channel circuit when entering a boost mode;
- [0017] FIG. 5B is a graph of a dynamic digital/analog gain partition of a DAC channel circuit when exiting a boost mode;
- [0018] FIGS. 6A and 6B are example silicon results of a dynamic digital/analog gain partition of a DAC channel circuit;
- [0019] FIG. 7A and FIG. 7B are example silicon results of a dynamic digital/analog gain partition of a DAC channel circuit when applied to a Fast Fourier Transform (FFT);
- [0020] FIG. 8 is a graph of the dynamic range measurement with and without the use of the apparatus described. Industry standard measurements of dynamic range are performed at an output amplitude of -60dBFS (read as 60 decibels below full scale); and
- [0021] FIG. 9 a graph of how the transition of the signal amplitude above and below the selected volume level of -18dBFS (read as 18 decibels below full scale) results in changes to the supply voltage level facilitating lower IC power dissipation.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0022] Turning to FIG. 2A, illustrated is one aspect of an example dynamic range boost circuit 200 constructed according to the principles of the present Application. In the circuit 200, a block diagram of a DAC headphone playback channel with dynamic range enhancement is illustrated.

[0023] Generally, the circuit 200 is directed towards an approach of a dynamic boost for a high dynamic range that also has a lower power dissipation occurring substantially

simultaneously for a DAC headphone playback on a single IC. The headphone may be replaced by any other load such as a loudspeaker, an external audio amplification apparatus without altering the behavior of the stated apparatus.

[0024] The circuit 200 uses a dynamic allocation, and in some preferred embodiments, an optimization, of a digital/ analog gain partitioning of an audio signal. In other words, the circuit 200 can partition gain between a digital volume amplifier 225 and an analog amplifier 255 to nonetheless convey a selected output volume to a headphone or a listener. In other words, an absolute path gain is unchanged, and the digital/analog gain partitioning is altered.

[0025] Partitioning the gain such that the digital gain is maximized and the analog gain is minimized reduces DMOD, DAC and Amplifier circuit noise, and therefore benefits dynamic range of the circuit 200. Additionally according to the principles of the present Application, regarding digital to analog conversion, partitioning can proceed without introduction of undesirable distortion as long as the elements DMOD, DAC and Analog Amplifier are maintained in their linear region of operation. Enhanced dynamic range using above principles can be employed within the present Application.

[0026] Generally, dynamic range is the ratio of the signal amplitude at a designated output terminal to the totality of the noise at the same output terminal. Hence constant signal amplitude with lower noise in effect enhances dynamic range. Enhanced dynamic range provides a higher fidelity audio listening experience which is highly desirable.

[0027] The circuit 200 has a number of advantages when compared to prior art headphone drivers. The circuit 200 helps to reduce or eliminate audible artifacts. One such artifact is that, if noise is generated earlier on in an audio system, that noise is also amplified by later amplifiers. But there can be other considerations, such as relative power consumptions of various electronic elements.

[0028] However, earlier stages of a headphone driver can be more power consuming. Therefore, the circuit 200 allocates and optimizes between the digital volume amplifier 225 and the analog amplifier 255. The circuit 200 has two primary modes of operation: a “boost” mode, and a “reverse dynamic boost (“normal”)” mode.

[0029] In the boost mode, when an amplitude at a driver output, such as at a headphone (HP), is under a designated digital threshold, such as -18dBFS, a digital gain before the DAC is increased by a value ΔG_D (for example, as high as +12dB), whereas an analog

amplifier/headphone driver gain is reduced by the same amount to as low as -12dB. Again, an absolute path gain is unchanged, yet the digital/analog gain portioning is altered. In the circuit 200, the noise of the DSP ramps up less than linearly, so while a gain of a system may be constant, the noise itself is not.

[0030] This reduces DMOD, DAC and Amp noise, and therefore benefits dynamic range of the circuit 200.

[0031] In the normal mode, when a signal stabs above the threshold, the digital gain before the DAC ramps downward, and the analog amplifier/headphone driver gain ramps up to register settings.

[0032] In the circuit 200, a PCM CODEC 210 is coupled to a digital signal processor (DSP) 120. In one example of the circuit 200, the PCM output bits at a rate of 48kilo bits per second. The DSP 230 is then oversampled at a DMOD 220, a digital filter, which can be an eight times over-sampling, an output of which is coupled to an input of a digital to analog converter (DAC) 140. An analog signal of the DAC 140 is then conveyed to the driver 150, which is then powered by a class “G” charge pump 160. This in turn, is used to power an example pair of headphones 170.

[0033] In the circuit 200, an output of the DFILT 220, is then conveyed to a digital amplifier 255. The digital amplifier 225 can digitally amplify or de-amplify a received digital signal. In one example, a range of amplification or de-amplification can be from -63 dB to +16dB.

[0034] FIG. 2B illustrates the circuit 200 in more detail. In the circuit 2500, a PCM CODEC 210 is coupled to a DSP 220. In one example of the circuit 250, the PCM 210 output bits at a rate of 48kilo bits per second. The DSP 220 also has a signal level detect 223 coupled to it. The signal level detector detects the actual equivalent volume amplification of the digital signal.

[0035] The signal level detect 223 is also coupled to a dynamic range boost gain control 235. The DRBGC 235 is coupled to the digital volume 225 and the driver 255. The DRBDCC 235 allocates, as a function of an output of the signal level detector 235, comparative amplifications between the digital volume 225 and the driver 225.

[0036] In the boost mode, when an amplitude at a driver output, such as at a headphone (HP), is under a digital threshold, such as -18dBFS, a digital gain before the DAC is increased

(for example, as high as +12dB), whereas an analog amplifier/headphone driver gain is reduced to as much as -12dB. Again, an absolute path gain is unchanged, yet the digital/analog gain portioning is altered. In the circuit 200, the noise of the DSP ramps up less than linearly, so while a gain of a system may be constant, the noise itself is not. In the normal mode, when a signal stabs above the threshold, the digital gain ramps down, and the driver gain ramps up to register settings.

[0037] FIG. 3 illustrates a part of an integrated circuit 300 that employs aspects of the circuit 200 in a context of multiple end user amplifiers 355-337. An algorithm for determining how to control the gain of the digital volume amplifier 225 or the amplifier can be embedded within a DR boost gain controller 335.

[0038] As an example the DR boost gain controller 335 could be used to enhance the dynamic range of a stereophonic audio channel comprising of separate left and right channels. Another example could be that of a surround sound channel comprising of left, right and a third channel of low frequency commonly known as a sub-woofer channel. The intent of these illustrative examples is to show that the DR boost controller 335 principle is applicable to a plurality of channels concurrently or individually.

[0039] Generally, as described above regarding FIG. 2A-3, a plurality of different number of thresholds against which the output volume may be compared and consequent gain adjustments can be made is employed. The apparatus 300, described above with single threshold, is hence to be treated as a subset of implementations that could have multiple thresholds.

[0040] FIG. 4 illustrates an example method 400 for determining a dynamic partition of a gain of a digital amplifier, such as the digital amplifier 225, and a gain of a driver such as the driver 255, can be partitioned.

[0041] After a start step 401, in a step 410, a gain of the digital amplifier is set to "0."

[0042] In a step 420, a command is received that audio is to be played. This command can be received at the PCM 210 of FIG. 2B, for example. The method 400 then advances to a step 430.

[0043] In step 430, it is determined whether the overall volume level desired, V_{out} , is greater than a $V_{threshold}$, such as -18dBfs. If yes, the method 400 advances to a normal mode 403 in a step 455. If no, the method 400 advances to a boost mode 407 in a step 440.

[0044] In the boost mode 407, in step 440, it is then determined if the gain of the amplifier, such as the amplifier 255, is greater than a minimum gain, such as -12dB. If not, then step 440 loops back to step 420. However, if the gain of the amplifier is greater than the minimum gain of the amplifier, step 440 advances to step 450.

[0045] In step 450, it is determined if the selected V_{out} is less than the V_{out} threshold for less than a certain amount of time, such as 21.2 milliseconds. If not, then step 450 loops back to step 420. However, if the selected V_{out} is less than the V_{out} threshold for less than a certain amount of time, the method advances to step 460. Generally, the amount of delay time in milliseconds is chosen so that the method 400 does not introduce any substantial audible artifacts into the audio signal.

[0046] In step 460, it is determined if the last digital gain amplifier update occurred less than a second time period ago, such as 41.66 μs ago. If not, then step 450 loops back to step 420. However, if the last digital gain amplifier update occurred less than a second time period ago then the digital amplifier amplification is increased a dB step gain, such as 2dB, and the amplifier gain is decreased by 2 db. Step 470 then loops back to step 420. Generally, the amount of gain ramp time in μs is chosen so that the method 400 does not introduce any substantial audible artifacts into the audio signal.

[0047] In one aspect, the dynamic boost 407, if an overall threshold volume level is not exceeded, increases a digital gain amplifier and decreases an analog output gain, thereby maintaining the same overall volume. As the threshold volume is not above a certain level, the method 400 saves power on the analog amplifier by changing amplification to the earlier digital amplifier and allowing the analog amplifier to be operated from a lower supply voltage; moreover, as the amplification is below the threshold, this means that the listener will not have a great of an amplification of any previous noise of pops, clicks, etc. from earlier on in an amplification circuit 200.

[0048] In the normal mode 403, in, it is determined whether the gain of the digital amplifier is greater than 0dB. If not, then step 445 loops back to step 420. However, if the gain of the digital amplifier is greater than 0dB, then step 445 advances to step 455.

[0049] Step 455, it is determined whether a last update to the digital amplifier has occurred within a third time period, such as 10 μs . If not, then step 445 loops back to step 420.

However, if the last update to the digital amplifier has occurred within a third time period, step 445 advances to a step 465.

[0050] In the step 465, the gain of the digital amplifier is decreased by a given amount, such as 2 decibels, and the gain of the analog amplifier is increased by the same given amount, such as 2 decibels. Step 465 then loops back to step 420. According to the principles of the present Application, the step 465 is generally designed to have the amount of increase or decrease in the respective amplifiers substantially equal.

[0051] In one aspect, the normal 407, if an overall threshold volume level is exceeded, decreases the gain of a digital gain amplifier and increases an analog output gain, thereby maintaining the same overall volume. As the threshold volume is above a certain level, the method 400 saves power on the analog amplifier by changing amplification to the earlier digital amplifier; moreover, as the amplification is above the threshold, this means that the listener will have a greater tolerance of amplifications of any previous noise of pops, clicks, etc. from earlier on in an amplification circuit 200.

[0052] The following Table is to be used in conjunction with the timing diagrams of FIGS 5A and 5B. The HSLDRV and HSRDRV refer to a stereo amplifier driver combination HS – headset or headphone L/R – left/right DRV – driver:

Term	Description	Example Values
VTHP(N)	Voltage threshold for DR Boost Operation	-18dBfs
X	Gain step, analog and digital mismatch < 0.03dB	2 dB
G0, A	Initial HSDRV gain	4 dB
G0, D	Initial digital gain	0 dB
GMIN, A	Min HSDRV gain	-12 dB
GMAX, D	Max digital gain	+16 dB
TDELAY	Digital and HSDRV gain change latency; 9 CLK cycles of DAC_CLK	2.34 μ s
TRELEASE	Gain step time when signal is below VTH, Synchronized to frame sync 4cycles of 96KHz	41.6 μ s
TATTACK	Gain step time when signal is above VTH, Synchronized to frame sync 1 cycle of 96KHz	10.6 μ s
THOLD	Hold time after the signal crosses the threshold; Charge pump (CP) is switched at THOLD/2	40 ms

[0053] FIG. 5A illustrates a timing diagram, such as can be used in conjunction with the circuit 200 and the method 400, when the circuit 200 enters the boost mode, such as the boost mode 407.

[0054] As is illustrated, the output amplitude crosses below as V_{THP} threshold level boost level, wherein the 'boost' can be thought of as the digital amplifier boost. To avoid frequent changes in gain, the method defines a wait time to ensure that the signal stays below the pre-defined threshold V_{THP} for a designated amount of time T_{hold} . After completion of designated fraction of this time, T_{hold} , a charge pump supply voltage used for the analog output amplifier, such as the class G charge pump 260, is then switched a lower voltage. The use of a lower supply voltage with same or reduced current drawn from the analog output amplifier reduces overall power drawn from the supply. After the time threshold T_{hold} . T_{hold} is used, as within boost mode, an analog amplifier gain can then be reduced in steps, and simultaneously a digital amplifier gain can be increased in steps by the DR boost controller using method in FIG 4.

[0055] Prior to gain change occurrence, the state of the signal `CHARGE_PUMP_HV_TO_LV` is to be altered for further power savings for the apparatus. The signal `CHARGE_PUMP_HV_TO_LV` is set to a logic level '1' implying an asserted signal. This permits the supply to the analog output amplifier to be transitioned safely to a lower output value without danger of undesirable distortion or in the extreme - signal saturation.

[0056] It is noted that the power supply transition just described above is not relied upon to achieve dynamic range enhancement. Thereby the two approaches can be implemented together or separately without prejudice to either approach. If they are implemented together, then the principles of the present Application detailed in this section, and in others below, how the two approaches are to be combined to achieve the twin objectives of dynamic range enhancement and lower power dissipation in a manner that advances prior art.

[0057] Then, after a T_{delay} , which is a latency period for the digital amplifier and the analog amplifier to be capable of changing their amplifier states, as is illustrated, the AMP signal, wherein the user has an overall amplification level of "G", changes in G_{0-x} , when x is, say 2 decibels, and the digital amplifier increases its output by 2 decibels. This continues in after steps until a minimum level of the amplifier is made, and a maximum digital gain is made. It is to be carefully noted that the supply control for reduced power dissipation and the gain control

for enhanced dynamic range are being exercised by the DR boost controller concurrently as stated in the application previously. Typical audio signals have positive and negative swings. Hence $V_{TH} = -18\text{dBFS} = |V_{THP}| = |V_{THN}|$ where $V_{THP} = -V_{THN}$ to handle audio signals that have positive and negative excursions around 0V.

[0058] FIG. 5B illustrates a timing diagram, such as can be used in conjunction with the circuit 200 and the method 400, when the circuit 200 enters a reverse boost mode, such as the reverse boost mode 403.

[0059] As is illustrated, the output amplitude crosses as V_{TH} threshold level reverse boost level, wherein the reverse 'boost' can be thought of as the digital amplifier unboost and the amplifier reboost. During this time, T_{attack} , the gain of the digital amplifier is decreased by X, say 2 decibels, as the gain of the amplifier is increased by 2 decibels.

[0060] After the time threshold T_{hold} , T_{hold} is used, as within boost mode, an analog amplifier is powered up, and a digital amplifier is powered down.

[0061] FIG. 6A is an example measurement of the sweep of Signal to Noise + Distortion (SNDR) versus output amplitude showing that a silicon embodiment of the principle and method does not adversely alter the behavior of the channel in its performance relative to prior art while enhancing the signal to noise ratio for signals that conform to the range $\leq V_{TH}$ (example-18dBFS). The method does not limit the choice of V_{TH} . The use of an example value of -18dBFS is to illustrate that for a specific situation of interest, greatest enhancement is obtained in the dynamic range of the channel for this choice of V_{TH} . For other situations a different value of V_{TH} may be chosen without prejudice.

[0062] FIGS. 6B, 7A and 7B are examples of Fast Fourier Transforms (FFT) of measured spectra of silicon embodiment of the principle and method showing specific points on the sweep of FIG 6. These specific points are chosen to be -1dBFS -3dBFS and -60dBFS. At the former level the distortion of the circuit is considered to determine channel performance while at -60dBFS the noise is considered to determine channel performance. It is evident that no adverse effects are observed at -1dBFS and -3dBFS as discussed earlier wherein it was alluded to above that the principle does not increase undesirable distortion or introduce audible artifacts. Similarly the beneficial aspects of lower noise as discussed earlier above are clearly seen at -60dBFS spectrum where the SNDR is measured to be 45dB. The dynamic range is therefore $60+45=105\text{dB}$ which is higher than prior art by at least 4 decibels equivalent to a linear figure of

37% lower noise. As stated in the prior art the highest performance claimed for similar class of audio channels is 101dB.

[0063] FIG. 8 further reinforces a comparison of prior art with described principle and method where the GREEN curve represents the signal-to-noise (SNR) without applying stated principle and method while the RED curve represents the SNR applying stated principle and method.

[0064] FIG. 9 shows an example output signal as the silicon embodiment transitions between the boost and the reverse boost mode. It is duly noted to those familiar in the art of audio signal amplification and reproduction that the signal shows no obvious audible artifacts as discussed above. The inventors note that the resolution of a plot is finite and not easily amenable to indicate the complete absence of such artifacts whose amplitudes are known to be of very small magnitude. Hence it is noted that the above advantages has been verified by the inventors using quantitative measurement tests and subjective listening tests widely adopted across the field of audio integrated circuits with appropriate test equipment of adequate resolution.

[0065] Those skilled in the art to which this application relates will appreciate that modifications may be made to the described embodiments, and that many other embodiments are possible within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. An apparatus, comprising:
 - a selected volume detector that detects a selected output volume;
 - an analog output signal amplifier;
 - a digital volume amplifier; and
 - a boost gain control element coupled to the selected volume detector,the analog output signal amplifier and the digital volume amplifier;
 - wherein the boost gain control element is configured to:
 - keep a gain of a path of the digital volume amplifier and the analog output signal amplifier substantially constant, wherein the boost gain control element can adjust both:
 - a) a gain of the digital volume control; and
 - b) a gain of the analog output signal amplifier;
 - to keep the gain of the path of the digital volume amplifier and the analog output signal substantially constant and equal to the selected output volume.
2. The apparatus of Claim 1, wherein the boost gain control element is further configured to:
 - compare the selected output volume to a threshold value;
 - if the selected output volume is below the threshold, then the boost gain control element can:
 - a) adjust upwards a digital volume of the digital volume amplifier; and
 - b) adjust downwards a volume of the amplifier,
 - to keep the gain of the path of the digital volume amplifier and the analog output signal substantially constant and equal to the selected output volume.
3. The apparatus of Claim 2, wherein the boost gain control element is further configured to:
 - compare the selected volume to a threshold value;

if the given volume of amplitude is above the threshold, then
the boost gain control element can:

a) adjust downwards a digital volume of the digital volume
amplifier; and

b) adjust upwards a volume of the amplifier,

to keep the gain of the path of the digital volume amplifier and the analog output signal
substantially constant and equal to the selected output volume.

4. The apparatus of Claim 1, further comprising a digital signal processor, wherein an
output of the digital signal processor coupled to an input of the digital volume amplifier.

5. The apparatus of Claim 1, wherein the output signal amplifier is a “Class G” charge
pump.

6. The apparatus of Claim 1, wherein the selected volume detector is coupled to a digital
signal processor that receives a selected volume signal.

7. The apparatus of Claim 1, wherein

a) the threshold of the boost amplifier is substantially 18 decibels of
amplification; and

a dynamic range of the digital volume amplifier is an increase of substantially
twelve dB; and

a dynamic range of the analog output signal amplifier as adjusted by the boost
gain control is substantially minus twelve dB.

8. The apparatus of Claim 7, wherein there is a transition period between a unity
amplification of a digital amplifier and a 12 db value, wherein both the driver transition at a
substantial 1 dB change.

9. The apparatus of Claim 1, wherein the boost gain control element is further configured
to:

compare the selected output volume to a threshold value;
if the selected output volume is below the threshold, then the boost gain control element can:
a) adjust upwards a digital volume of the digital volume amplifier; and
b) adjust downwards a volume of the amplifier,
to keep the gain of the path of the digital volume amplifier and the analog output signal substantially constant and equal to the selected output volume.

10. The apparatus of Claim 9, wherein the boost gain control element is further configured to:

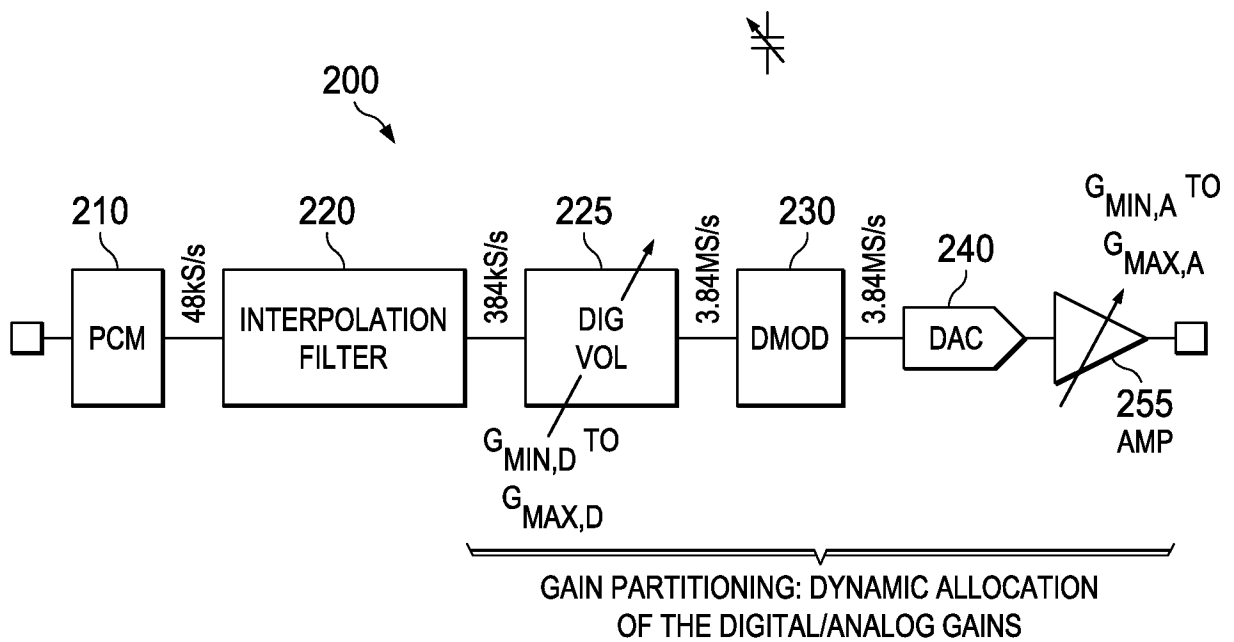
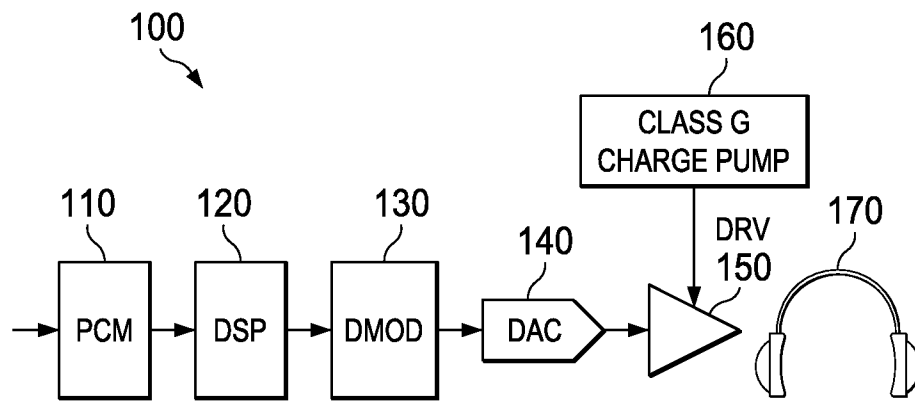
compare the selected output volume to a threshold value;
if the selected output volume is below the threshold, then the boost gain control element can:
a) adjust upwards a digital volume of the digital volume amplifier; and
b) adjust downwards a volume of the amplifier,
to keep the gain of the path of the digital volume amplifier and the analog output signal substantially constant and equal to the selected output volume.

11. The apparatus of Claim 10, wherein the boost gain control element is further configured to:

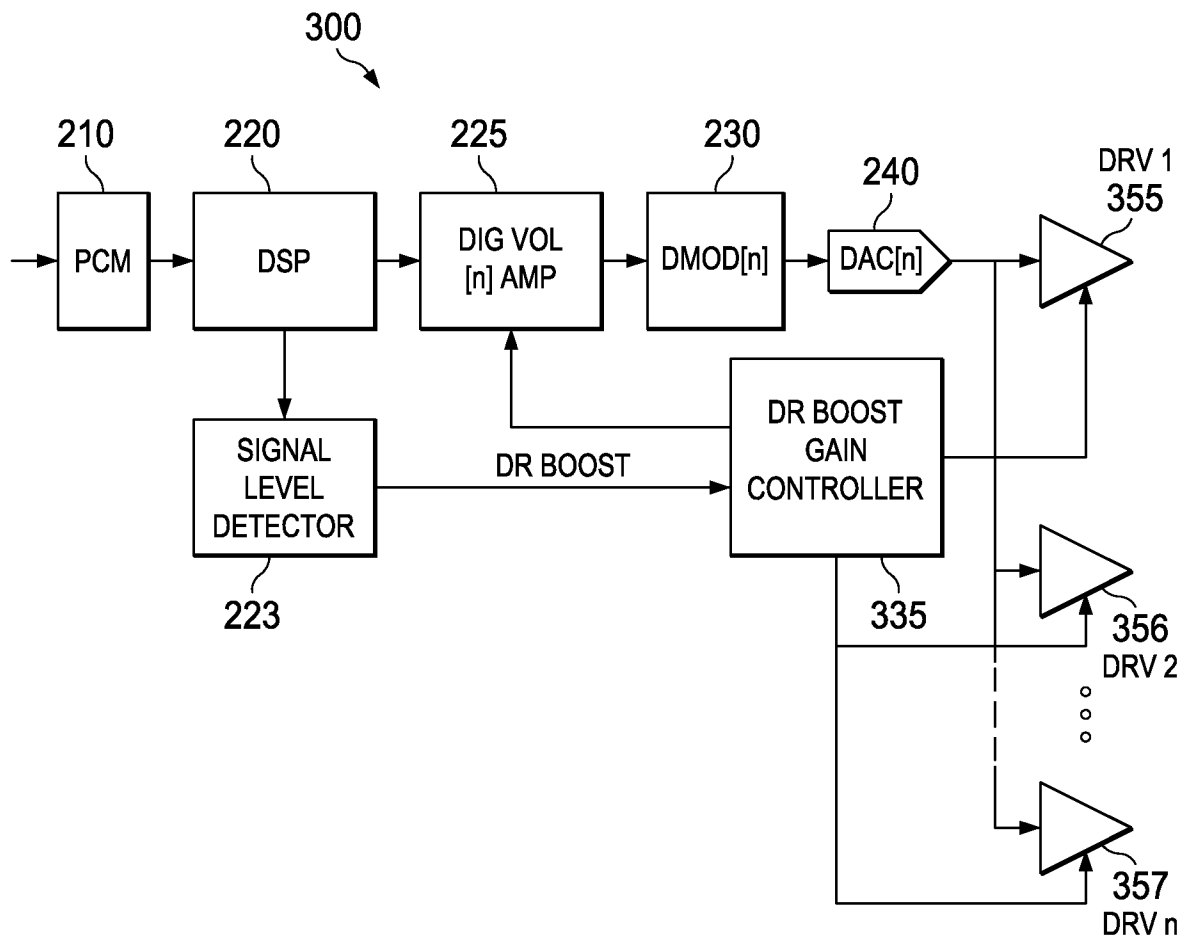
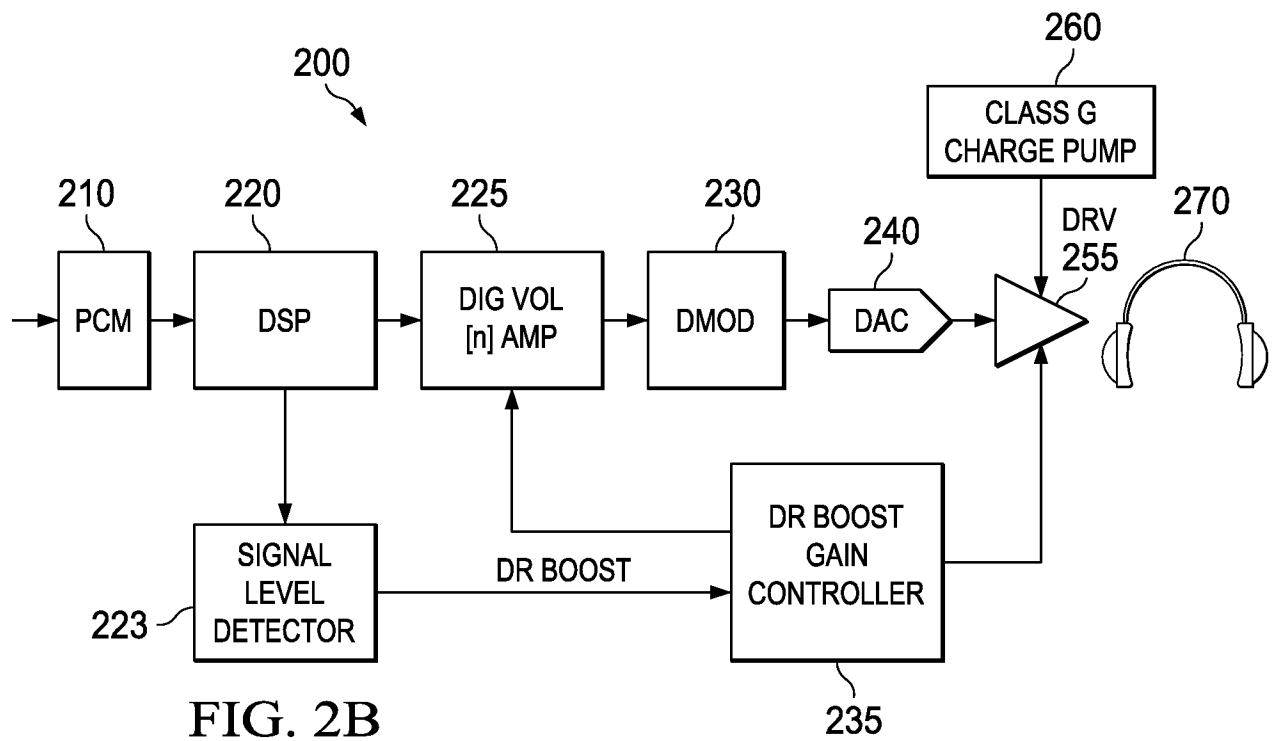
compare the selected volume to a threshold value;
if the given volume of amplitude is above the threshold, then the boost gain control element can:
a) adjust downwards a digital volume of the digital volume amplifier; and
b) adjust upwards a volume of the amplifier,
to keep the gain of the path of the digital volume amplifier and the analog output signal substantially constant and equal to the selected output volume.

12. A method, comprising:
determining if a selected output volume is greater than a volume threshold;
increasing a gain of a digital amplifier if the selected output volume is not greater than the threshold volume;
decreasing a gain of an amplifier if the selected output volume is not greater than the threshold volume; and
wherein the gain of a path of the digital volume amplifier and the analog output signal substantially constant and seeks to be equal to the selected output volume.
13. The method of Claim 12, further comprising:
playing an audio stream at the selected output volume.
14. The method of Claim 12, further comprising:
determining if a gain of an amplifier is greater than an allowable gain of the amplifier if the selected output volume is not greater than the volume threshold.
15. The method of Claim 12, further comprising
determining if the output volume is less than the volume threshold for a first time lapse;
and
determining in an update of an amplifier value of at least one of the digital amplifier and the analog amplifier occurred with a second time lapse ago.

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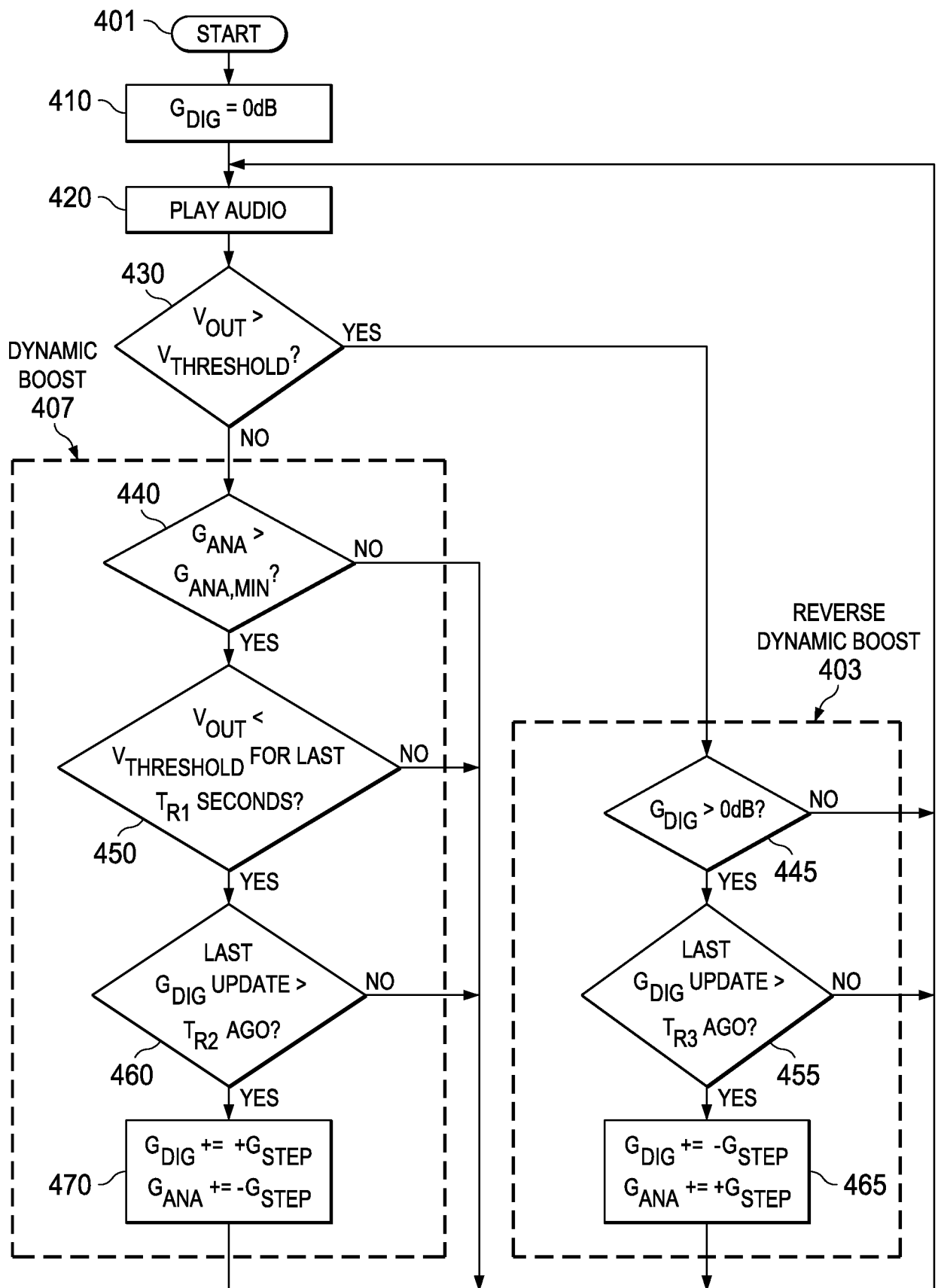


FIG. 4

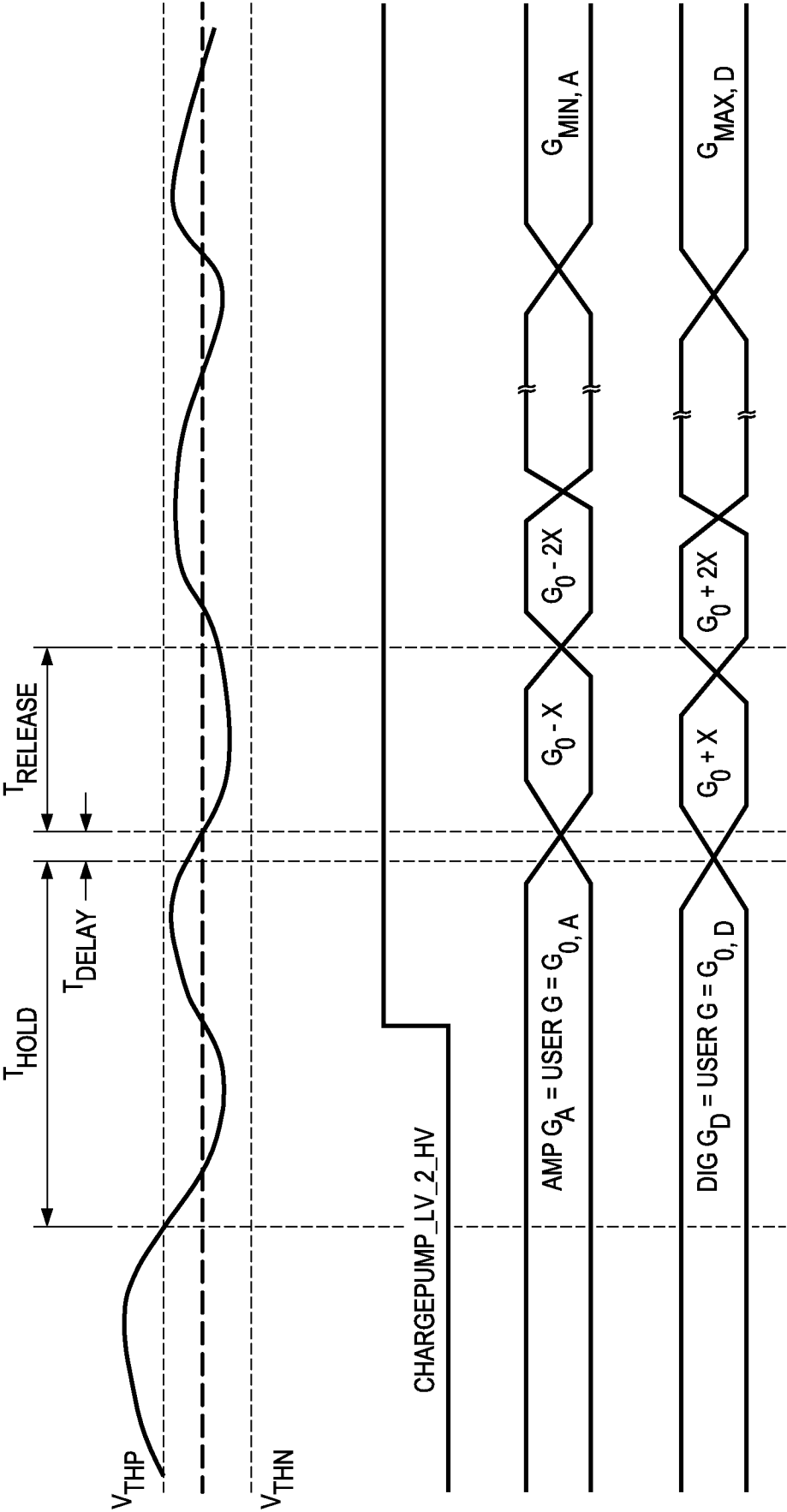


FIG. 5A

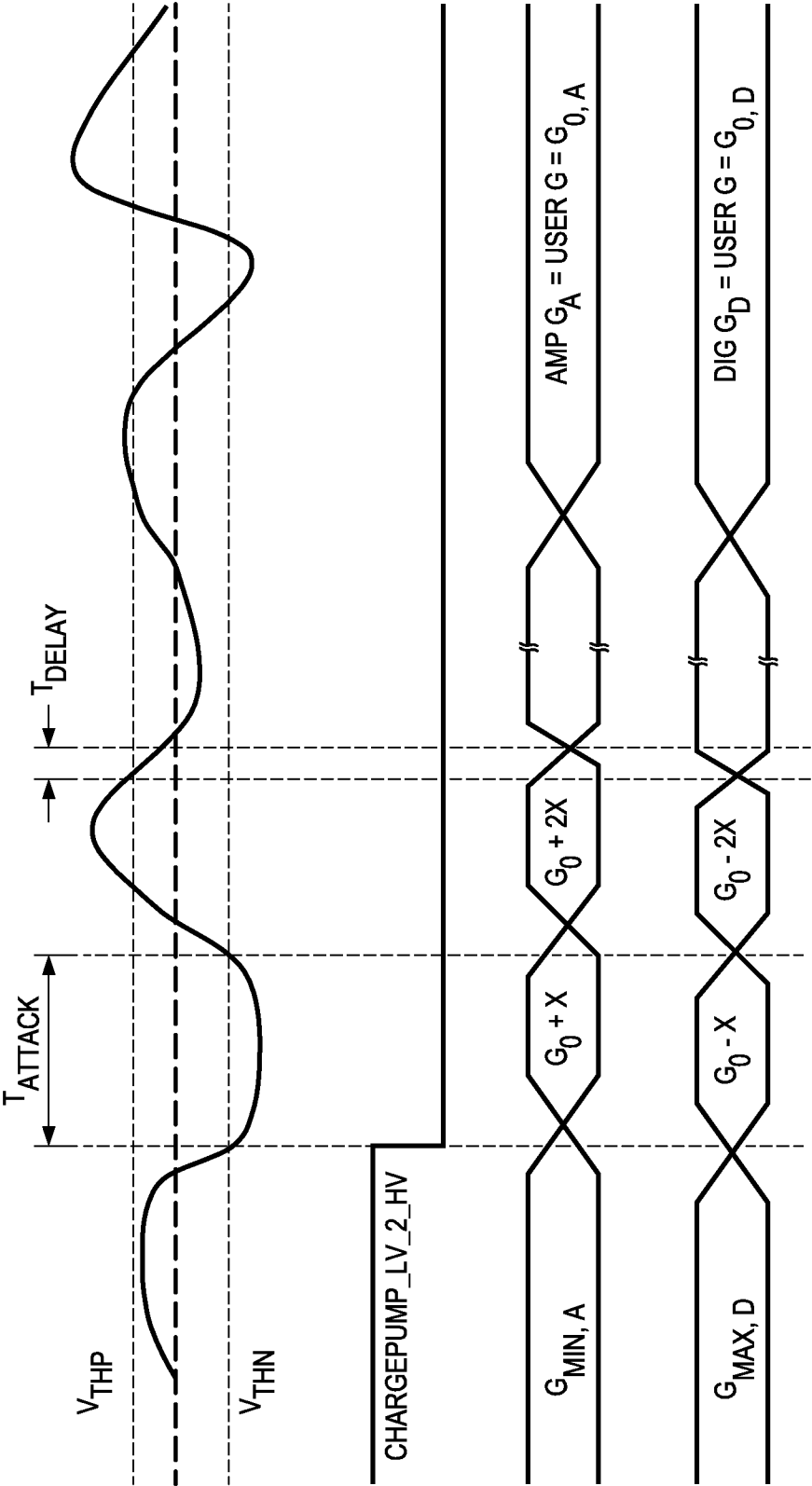
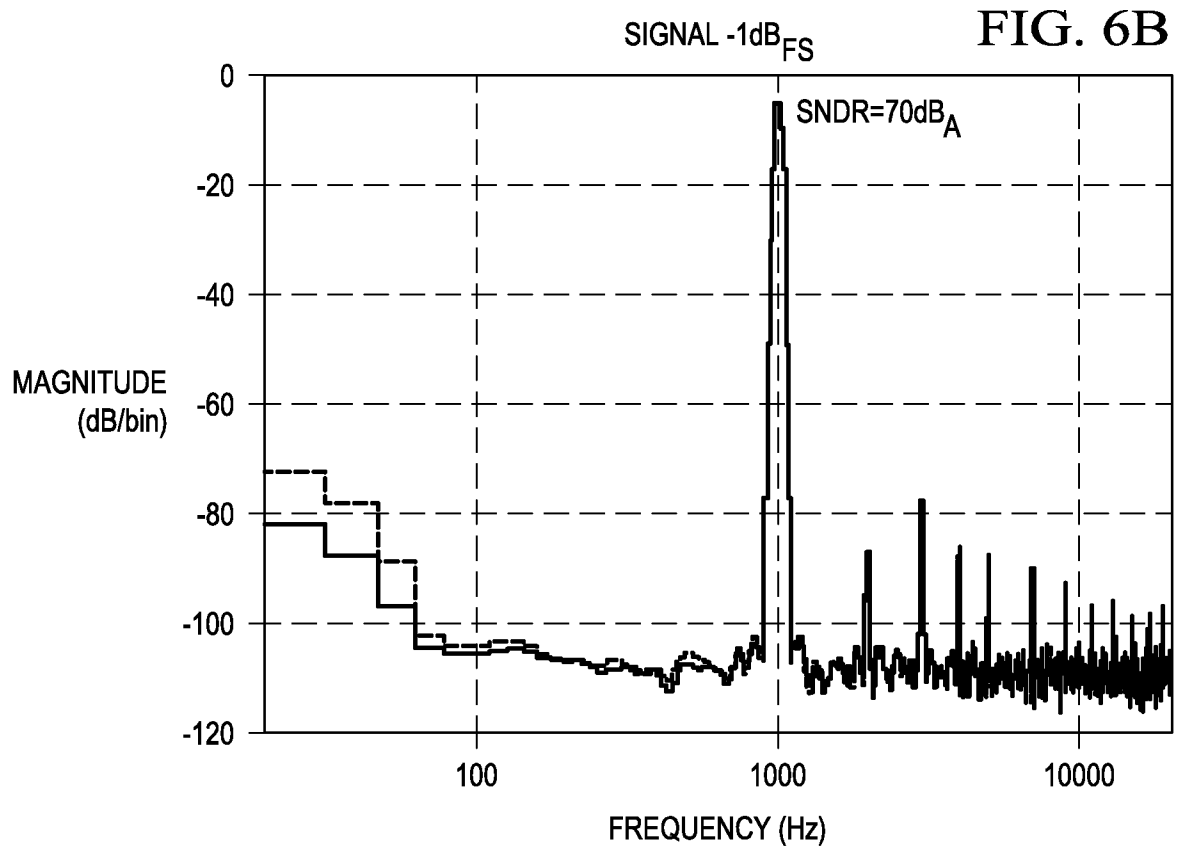
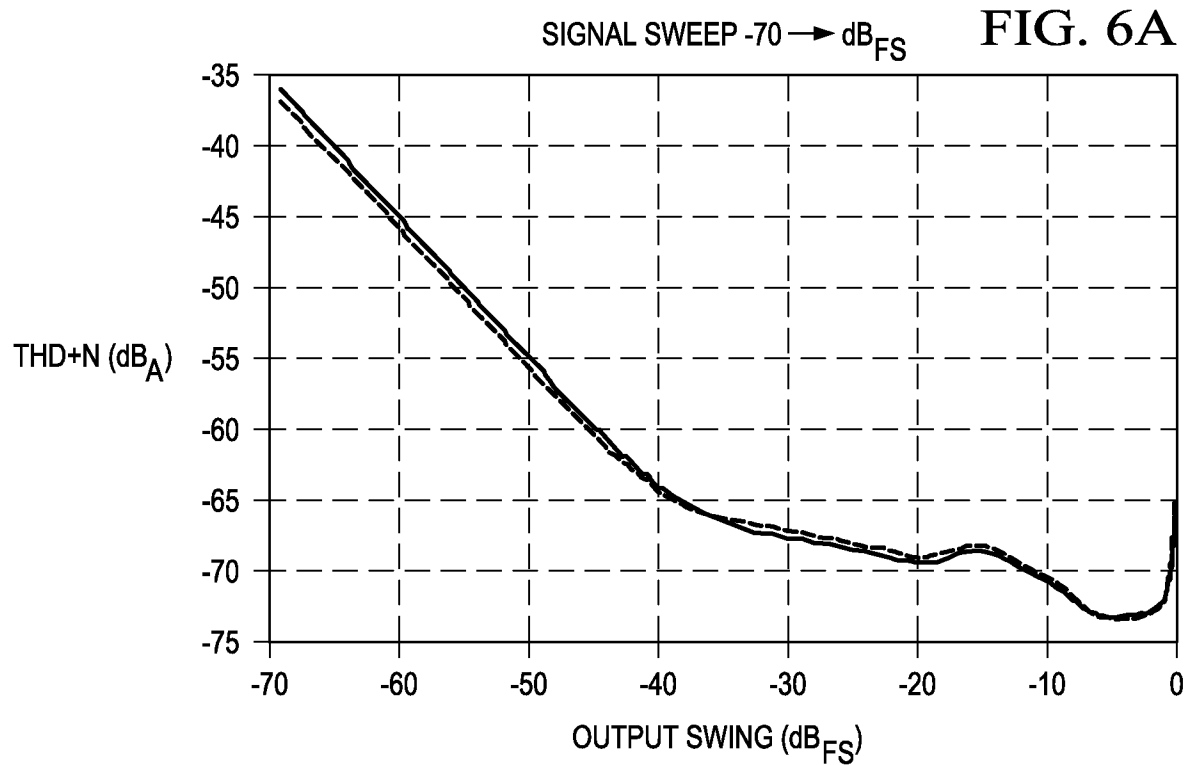
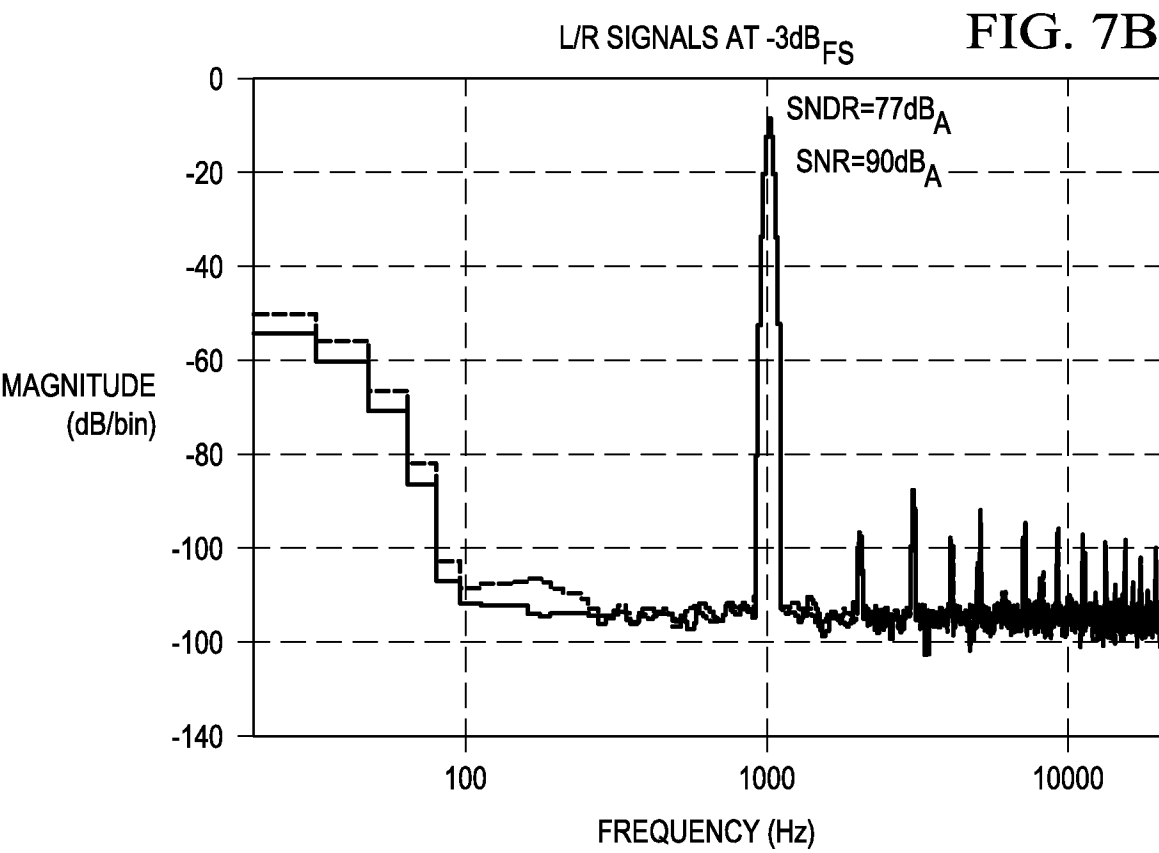
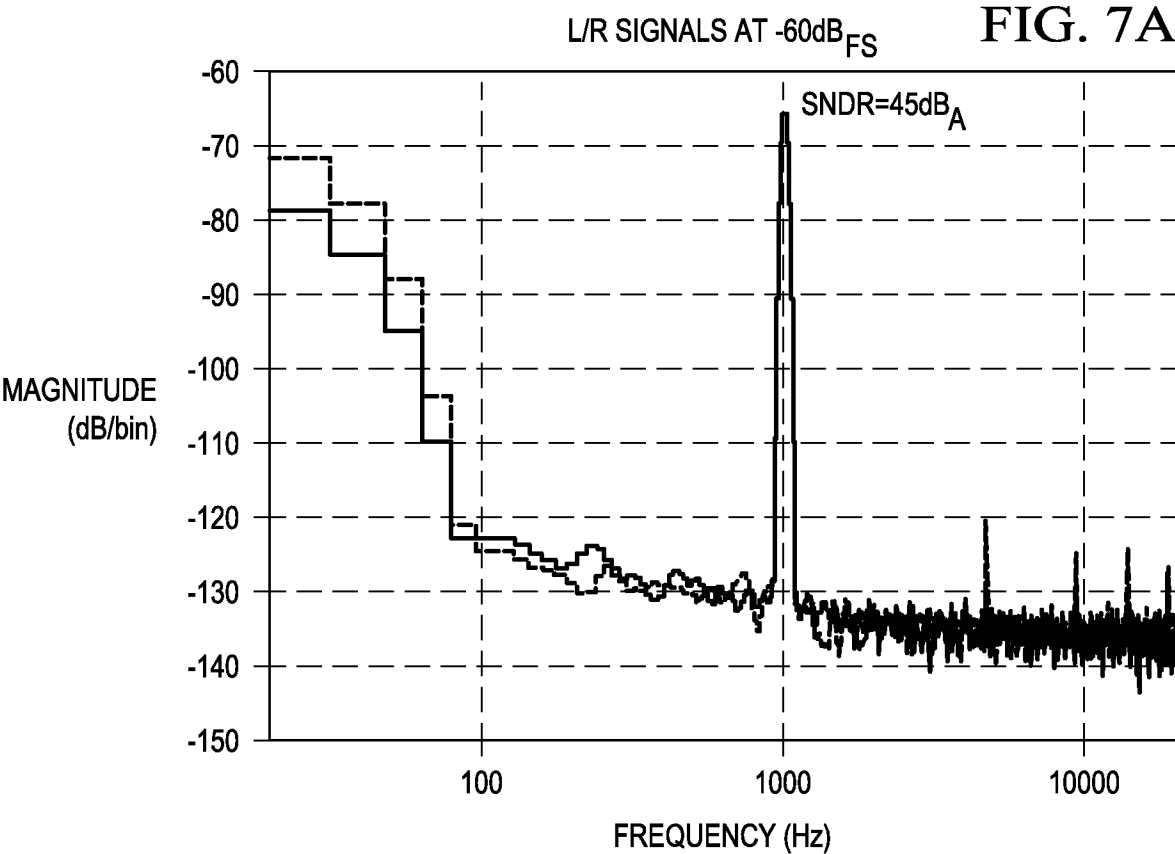
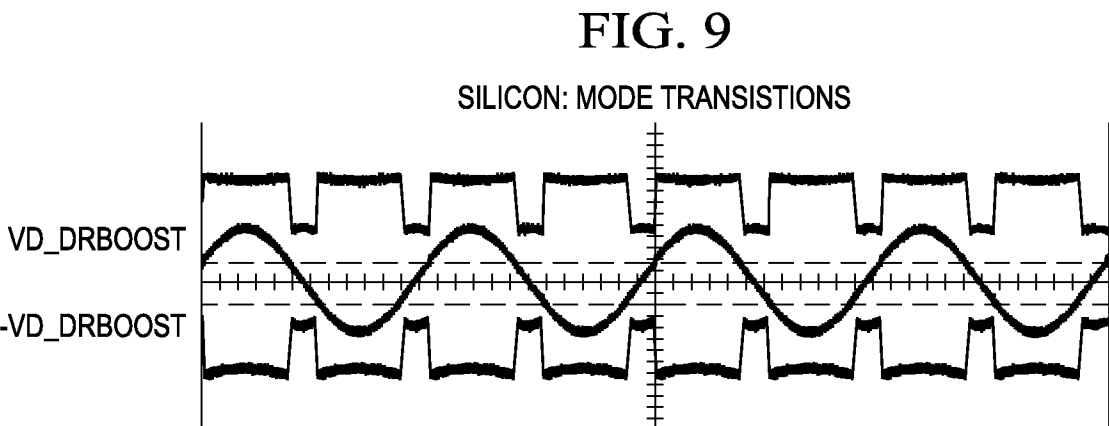
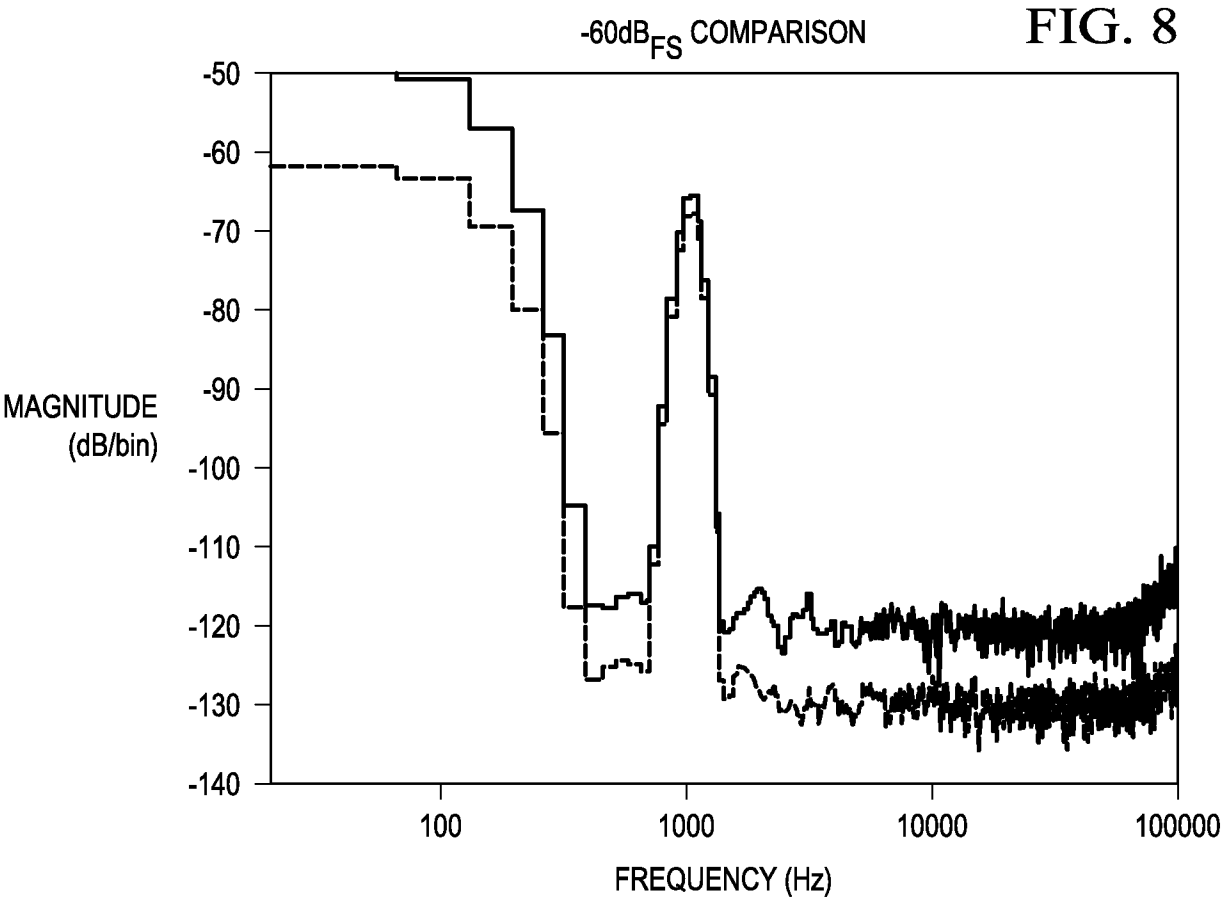


FIG. 5B

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A. CLASSIFICATION OF SUBJECT MATTER***H03G 9/00(2006.01)i, H04R 3/00(2006.01)i***

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03G 9/00; H04R 25/00; H03G 7/00; H03F 21/00; H03G 3/20; H03G 11/00; G10L 21/04

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: circuit, power dissipation, dynamic range, amplifier, volume detector, threshold, digital, analog

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2010-0215194 A1 (BHATTACHARYA) 26 August 2010 See paragraphs [0020]-[0030], and figures 1-3.	1-15
A	US 2011-0075861 A1 (WU et al.) 31 March 2011 See paragraphs [0015]-[0022], and figures 1-3.	1-15
A	US 2008-0044041 A1 (TUCKER et al.) 21 February 2008 See abstract, paragraphs [0015]-[0020], and figures 1,2.	1-15
A	US 2009-0257599 A1 (SAND JENSEN et al.) 15 October 2009 See abstract, paragraphs [0029]-[0033], and figure 1.	1-15
A	JP 2000-102098 A (YAMAHA CORPORATION) 7 April 2000 See abstract, paragraphs [0021]-[0027], and figures 1-4.	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

14 May 2013 (14.05.2013)

Date of mailing of the international search report

15 May 2013 (15.05.2013)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/023160

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