



(51) International Patent Classification:
H01L 27/105 (2006.01) *H01L 21/8247* (2006.01)

(21) International Application Number:
PCT/US2011/000152

(22) International Filing Date:
27 January 2011 (27.01.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/701,885 8 February 2010 (08.02.2010) US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— without international search report and to be republished upon receipt of that report (Rule 48.2(g))

(54) Title: RESISTIVE MEMORY AND METHODS OF PROCESSING RESISTIVE MEMORY

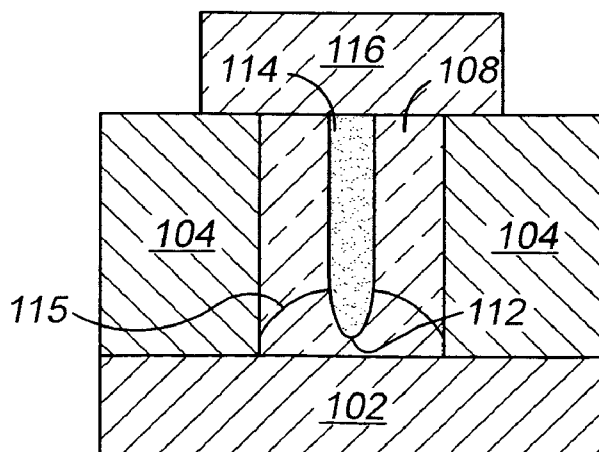


Fig. 1G

(57) Abstract: Resistive memory and methods of processing resistive memory are described herein. One or more method embodiments of processing resistive memory include conformally forming a cell material in an opening in an interlayer dielectric such that a seam is formed in the cell material, forming a conductive pathway by modifying the seam, and forming an electrode on the cell material and the seam.

RESISTIVE MEMORY AND METHODS OF PROCESSING RESISTIVE MEMORY

Technical Field

[0001] The present disclosure relates generally to semiconductor memory devices and methods, and systems, and more particularly, to resistive memory and methods of processing resistive memory.

Background

[0002] Memory devices are typically provided as internal, semiconductor, integrated circuits in computers or other electronic devices. There are many different types of memory, including random-access memory (RAM), read only memory (ROM), dynamic random access memory (DRAM), synchronous dynamic random access memory (SDRAM), flash memory, and resistive, e.g., resistance variable, memory, among others. Types of resistive memory include programmable conductor memory, phase change random access memory (PCRAM), and resistive random access memory (RRAM), among others.

[0003] Memory devices are utilized as non-volatile memory for a wide range of electronic applications in need of high memory densities, high reliability, and low power consumption. Non-volatile memory may be used in, for example, personal computers, portable memory sticks, solid state drives (SSDs), digital cameras, cellular telephones, portable music players such as MP3 players, movie players, and other electronic devices.

[0004] Memory devices may include a number of memory cells arranged in a matrix, e.g., array. For example, an access device, such as a diode, a field effect transistor (FET), or bipolar junction transistor (BJT), of the memory cells may be coupled to an access line, e.g., word line, forming a “row” of the array. The memory elements of each memory cell may be coupled to a data line, e.g., bit line, in a “column” of the array. In this manner, the access device of a memory cell may be accessed through a row decoder activating a row of memory cells by selecting the word line coupled to their gates. The programmed state of a row of selected memory cells may be determined, e.g., sensed, by

causing different currents, to flow in the memory elements depending on the resistance associated with a programmed state for a particular memory cell.

[0005] Memory cells may be programmed, e.g., written, to a desired state. That is, one of a number of programmed states, e.g., resistance levels, can be set for a memory cell. For example, a single level cell (SLC) can represent one of two logic states, e.g., 1 or 0. Resistive memory cells can also be programmed to one of more than two programmed states, such as to represent more than two binary digits, e.g., 1111, 0111, 0011, 1011, 1001, 0001, 0101, 1101, 1100, 0100, 0000, 1000, 1010, 0010, 0110, or 1110. Such cells may be referred to as multi state memory cells, multi-digit cells, or multilevel cells (MLCs).

[0006] Resistive memory such as RRAM may store data by varying the resistance level of a resistive memory element. Data may be programmed to a selected RRAM cell by applying sources of energy, such as positive or negative electrical pulses, e.g., positive or negative voltage or current pulses, to a particular resistive memory element for a predetermined duration. RRAM cells may be programmed to a number of resistance levels by application of voltages or currents of various magnitudes, polarities, and durations.

[0007] Methods for processing, e.g., fabricating, RRAM cells may include planar fabrication of RRAM cells. That is, RRAM cells may have a planar structure. However, RRAM cells having a planar structure may be large, e.g., RRAM cells having a planar structure may increase the size of an RRAM device. Further, RRAM cells having a planar structure may operate inconsistently or erroneously, e.g., the sensed resistance level of an RRAM cell having a planar structure may be different than the resistance level to which that cell was programmed.

Brief Description of the Drawings

[0008] Figures 1A-1G illustrate process steps associated with forming a resistive memory cell in accordance with a number of embodiments of the present disclosure.

[0009] Figure 2 illustrates a functional block diagram of a resistive memory in accordance with a number of embodiments of the present disclosure.

Detailed Description

[0010] Resistive memory and methods of processing resistive memory are described herein. One or more method embodiments of processing resistive memory include conformally forming a cell material in an opening in an interlayer dielectric such that a seam is formed in the cell material, forming a conductive pathway by modifying the seam, and forming an electrode on the cell material and the seam.

[0011] Processing resistive memory, e.g., resistive memory cells, in accordance with a number of embodiments of the present disclosure can decrease the size of the resistive memory cells and/or memory devices associated with the resistive memory cells. Processing resistive memory in accordance with a number of embodiments of the present disclosure can also increase the consistency and reliability of the resistive memory. For example, processing resistive memory in accordance with embodiments of the present disclosure can decrease the number of erroneous data reads associated with resistive memory.

[0012] In the following detailed description of the present disclosure, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration how a number of embodiments of the disclosure may be practiced. These embodiments are described in sufficient detail to enable those of ordinary skill in the art to practice a number of embodiments of this disclosure, and it is to be understood that other embodiments may be utilized and that process, electrical, or mechanical changes may be made without departing from the scope of the present disclosure.

[0013] As will be appreciated, elements shown in the various embodiments herein can be added, exchanged, and/or eliminated so as to provide a number of additional embodiments of the present disclosure. In addition, as will be appreciated, the proportion and the relative scale of the elements provided in the figures are intended to illustrate the embodiments of the present invention, and should not be taken in a limiting sense. As used herein, “a number of” something can refer to one or more such things. For example, a number of memory devices can refer to one or more memory devices.

[0014] Figures 1A-1G illustrate process steps associated with forming a resistive memory cell in accordance with a number of embodiments of the present disclosure. Figure 1A illustrates a schematic cross-sectional view of an

interlayer dielectric 104 on an electrode 102, with an opening 106 in interlayer dielectric 104. Electrode 102 can be, for example, tungsten or platinum.

Interlayer dielectric 104 can be, for example, an oxide dielectric, such as silicon dioxide (SiO_2). Interlayer dielectric 104 could also be, for example, a nitride dielectric, such as silicon nitride (Si_3N_4). Embodiments of the present disclosure are not limited to a particular type of interlayer dielectric material or electrode.

[0015] Interlayer dielectric 104 can be formed on electrode 102 in a number of ways, including chemical vapor deposition (CVD) or atomic layer deposition (ALD), as will be appreciated by one of skill in the art. A portion of interlayer dielectric 104 can then be removed, e.g., etched and/or patterned, to form opening 106. Opening 106 is adjacent to electrode 102, as shown in Figure 1.

[0016] In a number of embodiments, opening 106 can have a diameter of 10 to 30 nanometers. For example, opening 106 can have a diameter of approximately 22 nanometers, approximately 25 nanometers, or approximately 27 nanometers. However, embodiments are not limited to a particular diameter for opening 106.

[0017] Figure 1B illustrates a schematic cross-section view of the structure shown in Figure 1A after a subsequent processing step. Figure 1B includes a resistive memory cell material 108 formed on interlayer dielectric 104 and in opening 106 in interlayer dielectric 104. In a number of embodiments, resistive memory cell material 108 can be conformally formed on interlayer dielectric 104 and in opening 106. Resistive memory cell material 108 can be conformally formed on interlayer dielectric 104 and in opening 106 in a number of ways, including ALD, CVD, and plating. Further, the method of conformal formation can include having a portion of resistive memory cell material 108 that is in bottom up fill or selective mode. However, embodiments of the present disclosure are not limited to a particular method of conformal formation. The method of conformal formation used can depend on, for example, the material used for resistive memory cell material 108.

[0018] Resistive memory cell material 108 can be, for example, a resistance random access memory (RRAM) cell material. RRAM cell materials can include, for example, Ge_xSe_y , a binary metal oxide such as Cu_xO_y , WO_x , Nb_2O_5 , Al_2O_3 , Ta_2O_5 , TiO_x , ZrO_x , Ni_xO , and Fe_xO , and/or other materials that

can support solid phase electrolyte behavior. Other RRAM cell materials can include perovskite oxides such as doped or undoped SrTiO_3 , SrZrO_3 , and BaTiO_3 , colossal magnetoresistive materials such as $\text{Pr}_{(1-x)}\text{Ca}_x\text{MnO}_3$ (PCMO), $\text{La}_{(1-x)}\text{Ca}_x\text{MnO}_3$ (LCMO), and $\text{Ba}_{(1-x)}\text{Sr}_x\text{TiO}_3$, and polymer materials such as Bengala Rose, AlQ_3Ag , Cu-TCNQ, DDQ, TAPA, and Fluorescein-based polymers, among other types of RRAM cell materials.

[0019] In a number of embodiments, resistive memory cell material 108 can be conformally formed, e.g., conformally deposited, on interlayer dielectric 104 and in opening 106 such that a seam, e.g., seams 110-1 and 110-2 shown in Figure 1B, is formed in resistive memory cell material 108. As shown in Figure 1B, the seam can be an opening in resistive memory cell material 108, e.g., a region where the opposite sides of resistive memory cell material 108 approach each other such that resistive memory cell material 108 does not completely fill opening 106. That is, resistive memory cell material 108 can be formed on interlayer dielectric 104 and in opening 106 such that resistive memory cell material conforms to interlayer dielectric 104 and forms a seam in resistive memory cell material 108. In a number of embodiments, the seam formed in resistive memory cell material 108 can be modified to form a conductive pathway in resistive memory cell material 108, as will be further described herein.

[0020] Figure 1B illustrates a first and a second seam, e.g., seams 110-1 and 110-2, that can result from conformal formation of resistive memory cell material 108 in accordance with a number of embodiments of the present disclosure. As shown in Figure 1B, seams 110-1 and 110-2 have different characteristics. Differentiating characteristics can include surface, or near surface, modification as part of the terminating portion of a deposition procedure.

[0021] The characteristics of the seam formed in resistive memory cell material 108 can depend on the amount of time for which the conformal formation of resistive memory cell material 108 occurs. For example, the diameter and/or depth of the seam can decrease as the amount of time for which the conformal formation of resistive memory cell material 108 occurs increases. In the embodiments illustrated in Figure 1B, the amount of time for which the conformal formation that results in the formation of seam 110-1 occurs can be

greater than the amount of time for which the conformal formation that results in the formation of seam 110-2 occurs. For example, the diameter d1 of seam 110-1 is less than the diameter d2 of seam 110-2, as will be further described herein. Additionally, the depth D1 of seam 110-1 is less than the depth D2 of seam 110-2, e.g., bottom portion 112-2 of seam 110-2 is closer to electrode 102 than bottom portion 112-1 of seam 110-1, as shown in Figure 1B.

[0022] In a number of embodiments, resistive memory cell material 108 can be conformally formed in opening 106 such that there is resistive memory cell material 108 between the bottom of the seam and electrode 102, e.g., such that the seam is not in contact with electrode 102. For example, as shown in Figure 1B, seams 110-1 and 110-2 are conformally formed such that there is resistive memory cell material 108 between bottom portions 112-1 and 112-2 of seams 110-1 and 110-2, e.g., such that seams 110-1 and 110-2 are not in contact with electrode 102.

[0023] The distance between the bottom of the seam and electrode 102 can depend on the amount of time for which the conformal formation of resistive memory cell material 108 occurs. For example, the distance between the bottom of the seam and electrode 102 can increase as the amount of time for which the conformal formation of resistive memory cell material 108 occurs increases. In the embodiments illustrated in Figure 1B, the amount of time for which the conformal formation that results in the formation of seam 110-1 occurs can be greater than the amount of time for which the conformal formation that results in the formation of seam 110-2 occurs. For example, the distance between bottom portion 112-1 and electrode 102 is greater than the distance between bottom portion 112-2 and electrode 102, as shown in Figure 1B. In a number of embodiments, the distance between the bottom of the seam and electrode 102 can be in the range of 3 Angstroms to 15 Angstroms. However, embodiments of the present disclosure are not so limited. For example, the distance between the bottom of the seam and electrode 102 can be up to 100 Angstroms.

[0024] Figure 1C illustrates a schematic top view of resistive memory cell material 108 having seams 110-1 and 110-2 formed therein. That is, Figure 1C illustrates a schematic top view of the conformal formations of resistive memory cell material 108 shown in Figure 1B. As shown in Figure 1C, the diameter d1 of seam 110-1 is less than the diameter d2 of seam 110-2.

[0025] In a number of embodiments, the seam formed in resistive memory cell material 108, e.g., seams 110-1 and 110-2, can have a diameter of 0.5 to 5.0 nanometers. For example, the seam can have a diameter of approximately 1 nanometer. The diameter of the seam can be measured, for example, at the top of the seam.

[0026] The characteristics of the seam formed in resistive memory cell material 108, e.g., the depth and/or diameter of the seams, and/or the distance between the bottom of the seam and electrode 102, can result from the conformal formation of resistive memory cell material 108 on interlayer dielectric 104 and in opening 106, in accordance with a number of embodiments of the present disclosure. However, these characteristics of the seam may not be achievable using previous approaches, e.g., planar fabrication.

[0027] Figure 1D illustrates a schematic cross-sectional view of the structure shown in Figures 1B and 1C after a subsequent processing step. Figure 1D includes a filament 114 formed on resistive memory cell material 108 and in, e.g., within, a seam 110 in resistive memory cell material 108. Filament 114 can be a modifier material that is a different material than resistive memory cell material 108 and/or forms a conductive pathway in seam 110 such that seam 110 is a conductive pathway. That is, forming filament 114 in seam 110 can modify seam 110 to form a conductive pathway in resistive memory cell material 108. Filament 114 can be, for example, a metal, such as silver and copper, or a metal oxide, such as copper oxide and silver oxide. That is, filament 114 can be, for example, a metal, such as copper and silver, that is readily oxidized or reduced in solid phase. Filament 114 can be part of an additional, e.g., top, electrode structure, such as electrode 116 described in connection with Figure 1G.

[0028] In a number of embodiments, filament 114 can be a filament source material. That is, filament 114 can contain atoms that can form a filament within resistive memory cell material 108.

[0029] Filament, e.g., filament source material, 114 can be formed on resistive memory cell material 108 and in seam 110 in a number of ways, including spin-coating, spray, ALD, CVD, and condensation. Forming filament source material 114 in seam 110 can increase the concentration of atoms in filament source material 114. Because the concentration of atoms in filament source material 114 can be increased, filament source material 114 can be a thin

material, e.g., filament source material 114 can have a thickness that is less than the thickness of resistive memory cell material 108, as shown in Figure 1D.

[0030] As shown in Figure 1D, filament source material 114 can be formed in seam 110 such that an end of filament source material 114 is adjacent to bottom portion 112 of seam 110. Because the end of filament source material 114 can be adjacent to bottom portion 112 of seam 110, there can be resistive memory cell material 108 between the end of filament source material 114 and electrode 102, filament source material 114 may not be in contact with electrode 102, and/or the distance between the end of filament source material 114 and electrode 102 can be in the range of 3 Angstroms to 15 Angstroms. Filament source material 114 can also be formed in seam 110 such that filament source material 114 completely fills seam 110, as shown in Figure 1D.

[0031] In a number of embodiments, filament source material 114 can be heated after it is formed on resistive memory cell material 104 and in seam 110. Heating filament source material 114 can diffuse atoms from filament source material 114 into resistive memory cell material 104.

[0032] As previously described herein, forming filament source material 114 in seam 110 can modify seam 110 to form a conductive pathway in resistive memory cell material 108. This conductive pathway can be formed without forming any additional material between the end of filament source material 114 and bottom electrode 102 to couple the end of filament source material 114 to bottom electrode 102. Rather, the conductive pathway can include a conductive path that extends through region 115 in resistive memory cell material 108, along a path from the end of filament source material 114 to bottom electrode 102. That is, the conductive pathway can be formed with only resistive memory cell material 108 formed between the end of filament source material 114 and bottom electrode material 102, e.g., with only resistive memory cell material 108 in region 115.

[0033] Figure 1E illustrates a schematic cross-sectional view of the structure shown in Figure 1D after a subsequent processing step. In Figure 1E, a portion of resistive memory cell material 108 and a portion of filament source material 114 are removed. The removed portions of resistive memory cell material 108 and filament source material 114 can be removed, e.g., etched

and/or patterned, in a number of ways, including chemical mechanical polishing (CMP) and blanket etching.

[0034] The removed portion of resistive memory cell material 108 can include, for example, the portion of resistive memory cell material 108 that is not in opening 106. The removed portion of filament source material 114 can include, for example, the portion of filament source material 114 that is not in seam 110. Removing these portions of resistive memory cell material 108 and filament source material 114 can expose interlayer dielectric 104, as shown in Figure 1E.

[0035] Figure 1F illustrates a schematic top view of Figure 1E. In a number of embodiments, filament source material 114 can have a diameter d of 0.5 to 5.0 nanometers. For example, filament source material 114 can have a diameter d of approximately 1 nanometer. The diameter d of filament source material 114 can correspond to the diameter of seam 110. For example, in embodiments in which filament source material 114 completely fills seam 110, the diameter d of filament source material 114 can correspond to the diameter of seam 110 at the top of seam 110.

[0036] Figure 1G illustrates a schematic cross-sectional view of the structure shown in Figures 1E and 1F after a subsequent processing step. Figure 1G includes an electrode 116 formed on interlayer dielectric 104, resistive memory cell material 108, and filament source material 114. Electrode 116 can be, for example, tungsten or platinum. Electrode 116 can be formed, e.g., deposited and patterned, on interlayer dielectric 104, resistive memory cell material 108, and filament source material 114 in a number of ways, as will be appreciated by one of skill in the art. In a number of embodiments, filament source material 114 can be part of the structure of electrode 116, as previously described herein.

[0037] The structure illustrated in Figure 1G can be a component, e.g., portion, of a resistive memory cell. For example, the structure illustrated in Figure 1G can be a component of an RRAM cell, e.g., memory cell 212 shown in Figure 2.

[0038] Resistive memory cells, e.g., RRAM cells, processed in accordance with a number of embodiments of the present disclosure can decrease the size of the resistive memory cells and/or memory devices associated

with the resistive memory cells. Resistive memory cells processed in accordance with a number of embodiments of the present disclosure can also have increases consistency and reliability. For example, resistive memory cells processed in accordance with a number of embodiments of the present disclosure can have increased reliability as compared to memory cells processed in accordance with previous approaches, e.g., planar fabrication.

[0039] As one example, the distance between bottom portion 112 of seam 110 in resistive memory cell material 108, e.g., the end of filament source material 114, and electrode 102, can be in the range of 3 Angstroms to 15 Angstroms, as previously described herein, which can decrease the size of the resistive memory cell. This distance can also improve the performance of filament source material 114, which can increase the consistency and reliability of the resistive memory cell, e.g., memory cell 212 shown in Figure 2. This distance can result from the conformal formation of resistive memory cell material 108 on interlayer dielectric 104 and in opening 106, in accordance with a number of embodiments of the present disclosure. However, this distance may not be achievable using previous approaches, e.g., planar fabrication.

[0040] Additionally, opening 106 can have a diameter of 10 to 30 nanometers, as previously described herein. Further, seam 110 in resistive memory cell material 108, e.g., filament source material 114, can have a diameter of 0.5 to 5.0 nanometers, as previously described herein. These dimensions can also decrease the size of the resistive memory cell. These dimensions can result from the conformal formation of resistive memory cell material 108 and interlayer dielectric 104 and in opening 106, in accordance with a number of embodiments of the present disclosure. However, these dimensions may not be achievable using previous approaches, e.g., planar fabrication.

[0041] Resistive memory cells processed in accordance with a number of embodiments of the present disclosure can also decrease the effect of grain boundaries in resistive memory cell material 108. For example, resistive memory cell material 108 may contain grain boundaries, and filament source material 114 may diffuse faster along the grain boundaries. However, embodiments of the present disclosure can restrict the grain boundary interaction area to the central point of filament source material 114, e.g., the central point of seam 110 in resistive memory cell material 108. This can reduce failures

associated with the grain boundaries, which can increase the consistency and reliability of the resistive memory cell. This grain boundary area interaction restriction can result from the conformal formation of resistive memory cell material 108 on interlayer dielectric 104 and in opening 106, in accordance with a number of embodiments of the present disclosure. However, this grain boundary area interaction restriction may not be achievable using previous approaches, e.g., planar fabrication.

[0042] Figure 2 illustrates a functional block diagram of a resistive memory 200 in accordance with a number of embodiments of the present disclosure. As shown in Figure 2, resistive memory 200 includes resistive memory structure 202. Resistive memory structure 202 can be a structure processed in accordance with a number of embodiments of the present disclosure. For example, resistive memory structure 202 can be the structure illustrated in Figure 1G.

[0043] In Figure 2, access device 210 is coupled in series with resistive memory structure 202 to form memory cell 212. Memory cell 212 is coupled to data line, e.g., bit line, 220 and source line 222. Access device 210 can serve as a switch for enabling and disabling current flow through resistive memory structure 202. Access device 210 can be, for example, a transistor, such as a field effect transistor (FET) or bipolar junction transistor (BJT), with a gate coupled to access line, e.g., word line, 224. Thus, when word line 224 is energized, access device 210 can be turned on, thereby completing the circuit between source line 222 and bit line 220 through resistive memory structure 202.

[0044] In a number of embodiments, bit line 220 and source line 222 are coupled to logic for sensing, e.g., reading, from, and logic for programming, e.g., writing, memory cell 212. For example, as shown in Figure 2, read/write control multiplexer 230 has an output coupled to bit line 220. Read/write control multiplexer 230 can be controlled by read/write control logic line 232 to select between a first input coupled to bipolar write pulse generator 226, and a second input coupled to read sensing logic 228. The magnitude, polarity, and/or duration of voltage or current applied to resistive memory structure 202 for programming can be controlled by application thereof between bit line 220 and source line 222 associated with memory cell 212.

[0045] In a number of embodiments, during a write operation, bias generator 229 can establish, through bipolar write pulse generator 226, a write bias voltage potential difference between bit line 220 and source line 222, e.g., a fixed voltage, associated with memory cell 212. The write bias voltage can cause a particular magnitude of current to flow through resistive memory structure 202, which can change the resistance of resistive memory structure 202 to a particular resistance. The particular resistance can correspond to the programmed state of resistive memory structure 202.

[0046] In a number of embodiments, during a read operation, bias generator 129 can establish, through read sensing logic 228, a read bias voltage potential difference between bit line 220 and source line 222, e.g., a fixed voltage, associated with memory cell 212. The read bias voltage can cause a particular magnitude of current to flow corresponding to the resistance of resistive memory structure 202. For example, the greater the resistance of resistive memory structure 202, the smaller the current that flows for a given read bias voltage according to Ohm's law. The amount of current flowing through resistive memory structure 202 during a read operation (or a voltage proportional thereto) can be sensed by read sensing logic 228, e.g., a sense amp (not shown) can compare a circuit-derived input to a reference input that corresponds to a boundary condition between two programmed states, to determine an output corresponding to the programmed state represented by the present resistance of resistive memory structure 202.

[0047] In a number of embodiments, a read current can be applied through resistive memory structure 202 causing a corresponding voltage to be developed, which can be sensed and compared to a reference voltage. From the comparison, the resistance of resistive memory structure 202 can be determined, e.g., based on the principles of Ohm's law.

[0048] Although Figure 2 illustrates, and the discussion above describes, a particular read and write logic arrangement, one of skill in the art will appreciate that a number of embodiments of the present disclosure can be implemented using other configurations of logic for switching and/or programming resistive memory structure 202. Further, resistive memory 200 can include additional elements and/or circuitry not shown in Figure 2 so as not

to obscure embodiments of the present disclosure, as will be appreciated by one of skill in the art.

Conclusion

[0049] Resistive memory and methods of processing resistive memory are described herein. One or more method embodiments of processing resistive memory include conformally forming a cell material in an opening in an interlayer dielectric such that a seam is formed in the cell material, forming a conductive pathway by modifying the seam, and forming an electrode on the cell material and the seam.

[0050] Although specific embodiments have been illustrated and described herein, those of ordinary skill in the art will appreciate that an arrangement calculated to achieve the same results can be substituted for the specific embodiments shown. This disclosure is intended to cover adaptations or variations of various embodiments of the present disclosure. It is to be understood that the above description has been made in an illustrative fashion, and not a restrictive one. Combination of the above embodiments, and other embodiments not specifically described herein will be apparent to those of skill in the art upon reviewing the above description. The scope of the various embodiments of the present disclosure includes other applications in which the above structures and methods are used. Therefore, the scope of various embodiments of the present disclosure should be determined with reference to the appended claims, along with the full range of equivalents to which such claims are entitled.

[0051] In the foregoing Detailed Description, various features are grouped together in a single embodiment for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the disclosed embodiments of the present disclosure have to use more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter lies in less than all features of a single disclosed embodiment. Thus, the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment.

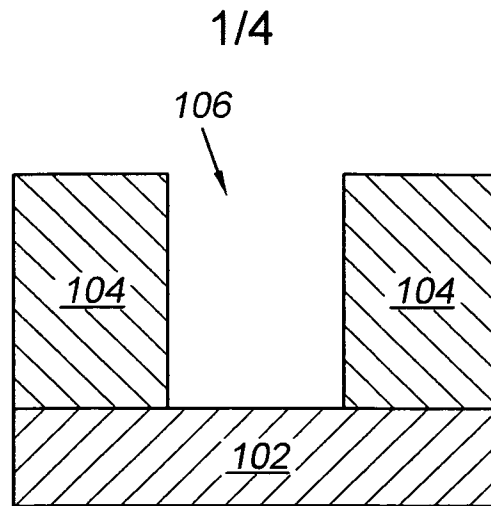
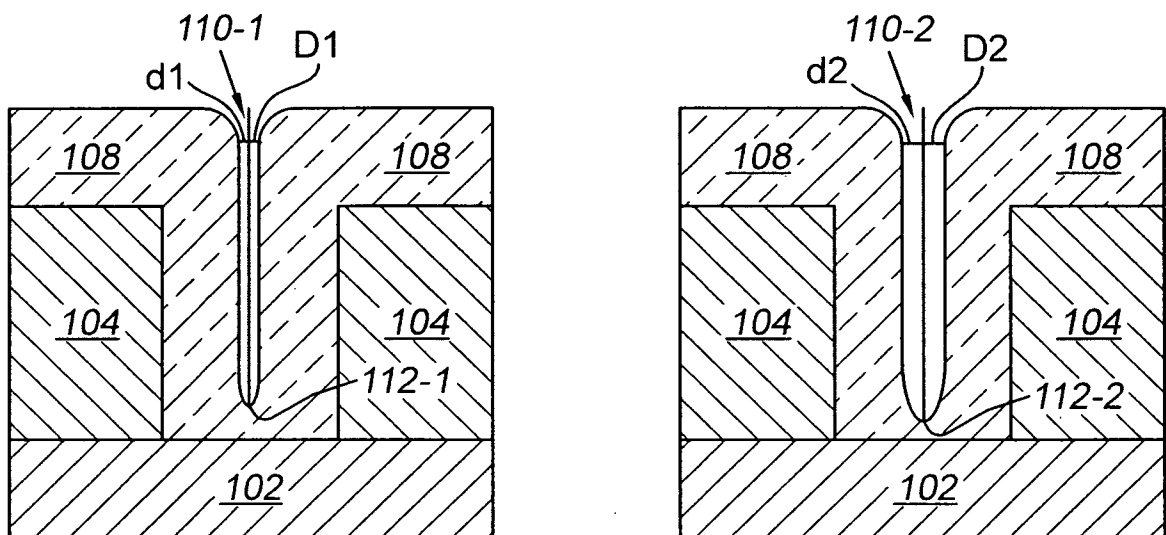
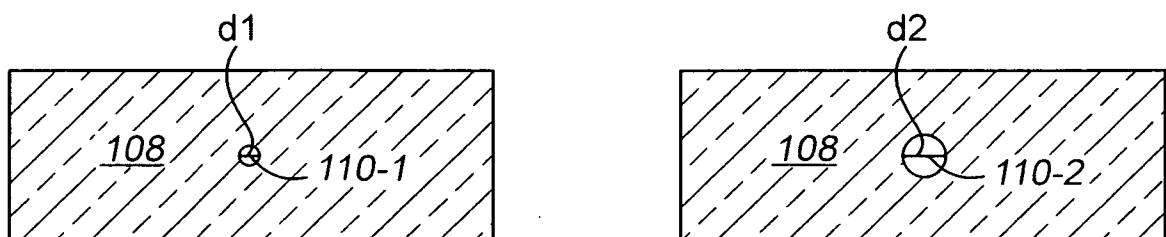
What is claimed is:

1. A method of processing a resistive memory cell, comprising:
conformally forming a cell material in an opening in an interlayer dielectric such that a seam is formed in the cell material;
forming a conductive pathway by modifying the seam; and
forming an electrode on the cell material and the seam.
2. The method of claim 1, wherein modifying the seam includes forming a filament in the seam.
3. The method of claim 2, wherein the method includes heating the filament after the filament is formed in the seam.
4. The method of claim 2, wherein the filament is a filament source material.
5. The method of any one of claims 1-4, wherein the method includes:
conformally forming the cell material in the opening such that cell material is formed between a bottom of the seam and an additional electrode adjacent the opening; and
forming the conductive pathway does not include forming an additional material that couples the bottom of the seam to the bottom electrode.
6. A method of processing a resistive random access memory (RRAM) cell, comprising:
forming a seam in a cell material by conformally depositing the cell material in an opening in an interlayer dielectric;
forming a conductive pathway in the cell material by modifying the seam; and
forming an electrode on the cell material and the seam.
7. The method of claim 6, wherein modifying the seam includes forming a filament in the seam.

8. The method of any one of claims 6-7, wherein the method includes conformally depositing the cell material in the opening such that cell material is formed between a bottom of the seam and an additional electrode adjacent the opening.
9. The method of claim 8, wherein only cell material is formed between the bottom of the seam and the additional electrode.
10. The method of any one of claims 6-7, wherein the method includes removing a portion of the cell material before forming the electrode on the cell material and the seam.
11. A method of processing a resistive memory cell, comprising:
 - conformally forming a resistive memory cell material in an opening in an interlayer dielectric such that a seam is formed in the resistive memory cell material;
 - forming a filament in the seam; and
 - forming an electrode on the resistive memory cell material and filament.
12. The method of claim 11, wherein the method includes forming the filament with a different material than the resistive memory cell material.
13. The method of claim 11, wherein the method includes diffusing atoms from the filament into the resistive memory cell material after the filament is formed in the seam and before the electrode is formed on the resistive memory cell material and filament.
14. The method of claim 13, wherein the method includes diffusing atoms from the filament by heating the filament.
15. The method of any one of claims 11-14, wherein the method includes conformally forming the resistive memory cell material in the opening such that the seam is not in contact with an additional electrode adjacent the opening.

16. The method of any one of claims 11-14, wherein the method includes forming the filament in the seam such that the filament completely fills the seam.
17. A resistive memory cell, comprising:
 - an interlayer dielectric having an opening;
 - a cell material conformally formed in the opening;
 - a conductive pathway in the cell material; and
 - an electrode on the cell material and the conductive pathway.
18. The resistive memory cell of claim 17, wherein the conductive pathway includes a filament.
19. The resistive memory cell of claim 18, wherein the filament is a metal or a metal oxide.
20. The resistive memory cell of any one of claims 17-19, wherein the cell material is a metal oxide.
21. The resistive memory cell of any one of claims 17-19, wherein the conductive pathway has a diameter of 0.5 nanometers to 5.0 nanometers.
22. The resistive memory cell of any one of claims 17-19, wherein the opening has a diameter of 10 to 30 nanometers.
23. A resistive random access memory (RRAM) cell, comprising:
 - an interlayer dielectric having an opening;
 - a resistive memory cell material conformally formed in the opening such that the cell material includes a seam;
 - a filament in the seam; and
 - an electrode on the resistive memory cell material and filament.
24. The RRAM cell of claim 23, wherein the filament is a different material than the resistive memory cell material.

25. The RRAM cell of claim 23, wherein the resistive memory cell material is Ge_xSe_y .
26. The RRAM cell of claim 23, wherein:
the RRAM cell includes an additional electrode adjacent the opening in the interlayer dielectric; and
an end of the filament in the seam is a distance of 3 Angstroms to 15 Angstroms from the additional electrode.
27. The RRAM cell of claim 26, wherein the RRAM cell includes only resistive memory cell material between the additional electrode and the end of the filament.
28. The RRAM cell of claim 23, wherein the filament has a diameter of approximately 1 nanometer.
29. The RRAM cell of any one of claims 23-28, wherein the filament is a filament source material.

**Fig. 1A****Fig. 1B****Fig. 1C**

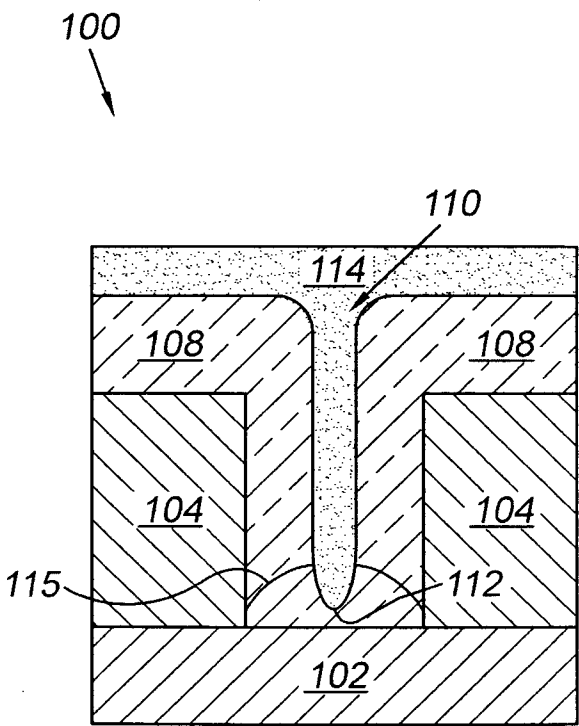


Fig. 1D

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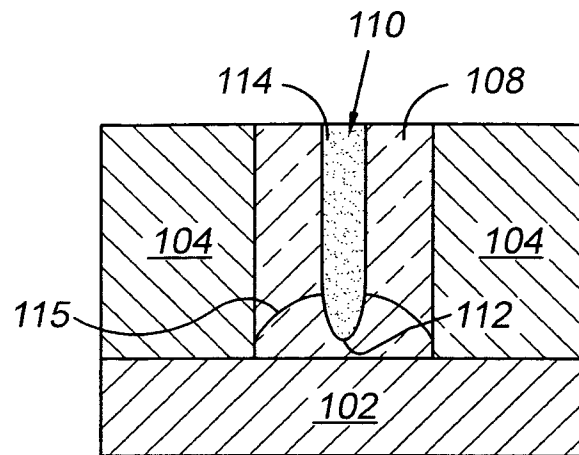


Fig. 1E

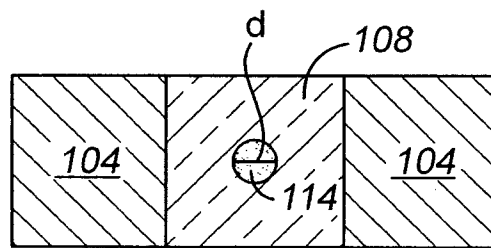


Fig. 1F

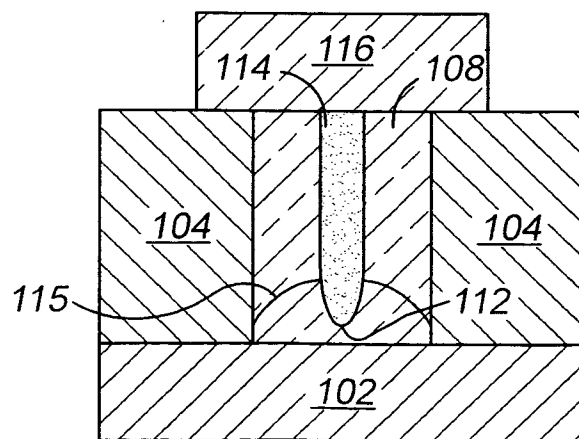


Fig. 1G

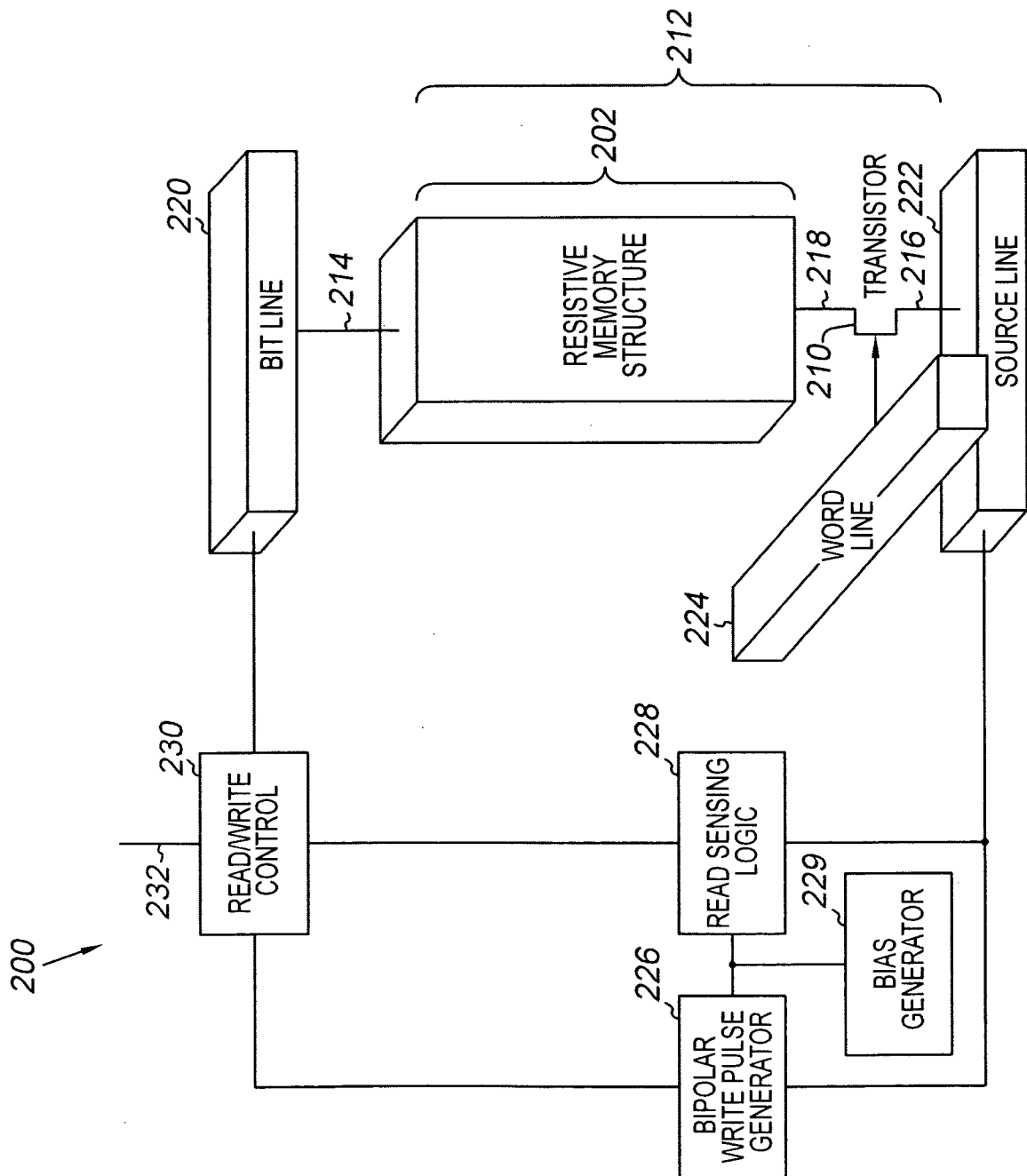


Fig. 2