SEMICONDUCTOR MEMORY DEVICE AND SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

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ABSTRACT

A leakage current of the MOS transistor of a power control section at a standby time is drastically reduced and the reduction of the consumption power is achieved. A memory module is provided with power control sections. When either of the memory mats is not selected, the power control sections stop the power supply voltage to a non-selected memory mat, a word driver, an input-output circuit, a control circuit and an output circuit. At the standby time of the memory module, the power control section stops a power supply to power control sections, a control circuit, a predecoder circuit, and an input circuit. In this manner, the leakage current of the MOS transistor of the power control sections at the standby time can be drastically reduced.
FIG. 4
SEMICONDUCTOR MEMORY DEVICE AND SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

CROSS-REFERENCE TO RELATED APPLICATION


TECHNICAL FIELD OF THE INVENTION

[0002] The present invention relates to a technique for reducing power consumption in a semiconductor integrated circuit device, and more in particular, it relates to a technique which is effective when applied to the reduction of a leakage current at a standby time in a semiconductor memory such as an SRAM (Static Random Access Memory) and the like.

BACKGROUND OF THE INVENTION

[0003] In general, a memory module such as the SRAM is contained in a semiconductor integrated circuit device such as a system LSI.

[0004] Some of these memory modules mentioned above are provided with a power control section for reducing power consumption by cutting off the power during a period when a circuit operation is not needed. This power control section is provided, for example, in each divided memory mat.

[0005] The power control section consists of a memory mat, an input-output circuit, a control circuit, a plurality of MOS (Metal Oxide Semiconductor) transistors provided between the power supply voltages supplied to peripheral circuits such as a word driver, a predecoder circuit and the like, and a power control circuit for controlling the on and off of these MOS transistors.

[0006] The power control circuit cuts off the power supply voltage supplied to the memory mat, the input-output circuit, and the peripheral circuits by turning off the MOS transistors at the standby time of the semiconductor integrated circuit device.

SUMMARY OF THE INVENTION

[0007] However, the inventors of the present invention have found out that the above-described technique for reducing the consumption power in the semiconductor integrated circuit device has the following problem.

[0008] That is, with the increase of the capacity of the memory module and the increase of the number of the divided memory mats, the number of MOS transistors of the power control section tends to increase, and a standby current of the semiconductor integrated circuit device becomes large due to the increase of a subthreshold current in the MOS transistors.

[0009] An object of the present invention is to provide a semiconductor memory device and a semiconductor integrated circuit device capable of reducing the power consumption by drastically reducing the leakage current of the MOS transistors at a standby time.

[0010] The above and other objects and novel characteristics of the present invention will be apparent from the description of this specification and the accompanying drawings.

[0011] The typical one of the inventions disclosed in this application will be briefly described as follows.

[0012] The semiconductor memory device according to the present invention comprises: memory mats obtained by dividing a memory array into at least two portions; a first peripheral circuit which is provided for each of the respective memory mats, controls the memory mats, and performs a data transfer with the memory mat; a second peripheral circuit for performing overall control of each of the peripheral circuits; a first power control section for controlling a power supply in a non-selected first peripheral circuit when one of the memory mats divided into at least two portions is selected and operated; and a second power control section for controlling a power supply in the first power control section and the second peripheral circuit when either of the memory mat divided into at least two portions is not selected.

[0013] Also, the semiconductor integrated circuit device according to the present invention comprises: a memory module which includes: memory mats obtained by dividing a memory array into at least two portions; a first peripheral circuit which is provided for each of the respective memory mats, controls the memory mats, and performs a data transfer with the memory mat; a second peripheral circuit for performing overall control of each of the peripheral circuits; a first power control section for controlling a power supply in a non-selected first peripheral circuit when one of the memory mats divided into at least two portions is selected and operated; and a second power control section for controlling a power supply in the first power control section and the second peripheral circuit when either of the memory mats divided into at least two portions is not selected.

[0014] The effects obtained by the representative one of the inventions disclosed in this application will be briefly described as follows.

[0015] 1. It is possible to drastically reduce the consumption current at a standby time by cutting off the power supply at a standby time in a first power control section.

[0016] 2. It is also possible to further drastically reduce the consumption current at a standby time since the power supply to first and second peripheral circuits at a standby time can be reliably cut off.

[0017] 3. Since it is possible to reduce the consumption current of the semiconductor memory device and the semiconductor integrated circuit device by the above 1 and 2, the performance and the reliability of an electronic system formed by using these semiconductor memory device and semiconductor integrated-circuit device can be improved.

BRIEF DESCRIPTIONS OF THE DRAWINGS

[0018] FIG. 1 is a block diagram of a semiconductor integrated circuit device according to a first embodiment of the present invention;

[0019] FIG. 2 is a block diagram of a semiconductor memory module provided in the semiconductor integrated circuit device of FIG. 1;

[0020] FIG. 3 is a circuit diagram showing a connection configuration in a power control section provided in the memory module of FIG. 2;

[0021] FIG. 4 is a chip layout view in the power control section of FIG. 3;

[0022] FIG. 5 is a circuit diagram showing the connection configuration of the power control section provided in the memory module according to a second embodiment of the present invention;
FIG. 6 is a circuit diagram showing the connection configuration of the power control section provided in the memory module according to a third embodiment of the present invention; and

FIG. 7 is a circuit diagram showing the connection configuration of the power control section provided in the semiconductor integrated circuit device according to a fourth embodiment of the present invention.

DESCRIPTIONS OF THE PREFERRED EMBODIMENTS

Hereinafter, embodiments of the present invention will be described in detail with reference to the accompanying drawings. Note that components having the same function are denoted by the same reference symbols throughout the drawings for describing the embodiments, and the repetitive description thereof will be omitted.

First Embodiment

FIG. 1 is a block diagram of a semiconductor integrated circuit device according to the first embodiment of the present invention, FIG. 2 is a block diagram of a memory module provided in the semiconductor integrated circuit device of FIG. 1, FIG. 3 is a circuit diagram showing a connection configuration in a power control section provided in the memory module of FIG. 2, and FIG. 4 is a chip layout diagram in the power control section of FIG. 3.

In this first embodiment, the semiconductor integrated circuit device 1 is a microcomputer for processing various multimedia applications used in the electronic system such as a mobile phone and the like.

As shown in FIG. 1, the semiconductor integrated circuit device 1 is composed of an XY memory controller 2, an XY memory 3, a user memory controller 4, a user memory 5, a cache memory controller 6, a cache memory 7, a memory management unit 8, an address conversion buffer 9, an interrupt controller 10, a clock oscillator 11, a CPU (Central Processing Unit) 12, a DSP (Digital Signal Processor) 13, an SCI (Serial Control Interface) 14, a BSC (Bus State Controller) 15, a DMAC (Direct Memory Access Controller) 16, an SCI (Serial Communication Interface) 17, a USB (Universal Serial Bus) 18, an A/D converter 19, an external bus interface 20, and the like.

FIG. 2 is a block diagram showing the configuration of the memory module 25.

The memory module 25 has a memory array 26 in which memory cells which are the smallest unit of memory are regularly arranged in an array. This memory array 26 has, for example, a dual architecture provided with two memory mats 26a and 26b.

The memory mat 26a, and the memory mat 26b, are connected to word drivers (first peripheral circuits) 27 and 28, respectively. These word drivers 27 and 28 select word lines in a row direction in the memory mat 26a, and the memory mat 26b.

Further, the memory mat 26a, and the memory mat 26b, are connected to input-output circuits (first peripheral circuits) 29 and 30, respectively. The input-output circuits 29 and 30 control an input-output timing of the data in the memory mats 26a and 26b.

The input-output circuits 29 and 30 are connected to control circuits (first peripheral circuits) 31 and 32, respec-
The control circuit 31 is connected to the word driver 27 and the control circuit (second peripheral circuit) 33, respectively, and the control circuit 32 is connected to the word driver 28 and the control circuit 33, respectively.

[0047] Further, the control circuits 31 to 33 are connected to a predecoder circuit (second peripheral circuit) 34, and the predecoder circuit 34 is connected to an input circuit (second peripheral circuit) 35. The input-output circuits 29 and 30 are connected to output circuits 36 and 37, respectively.

[0048] Address and various types of command signals are inputted from the input circuit 35. The predecoder circuit 34 decodes the address inputted via the input circuit 35 and outputs the same to the control circuits 31 to 33.

[0049] The control circuit 33 performs the overall control in the memory module 25 and selects either of the control circuits 31 or 32 based on the inputted address and command signals, and at the same time, outputs a control signal obtained by decoding the command signal. The control circuits 31 and 32 supply the decode signal to the word drivers 27 and 28 based on the control signals outputted from the control circuit 33.

[0050] Further, the word driver 27, the input-output circuit 29, and the control circuit 31 are connected to a power control section (first power control section) 38, respectively, and the word driver 28, the input-output circuit 30, and the control circuit 32 are connected to a power control section (first power control section) 39, respectively.

[0051] The power control section 38 stops the power supply voltage to the word driver 27, the input-output circuit 29, and the control circuit 31 when the memory mat 26, is not selected.

[0052] The power control section 39 stops the power supply voltage to the word driver 28, the input-output circuit 30, and the control circuit 32 when the memory mat 26, is not selected.

[0053] Further, the control circuit 33, the predecoder circuit 34, the input circuit 35, and the power control sections 38 and 39 are connected to a power control section (second power control section) 40, respectively. The power control section 40 stops the power supply voltage to the control circuit 33, the predecoder circuit 34, the input circuit 35, and the power control sections 38 and 39 when both the memory mats 26, and 26, are not selected.

[0054] FIG. 3 is an explanatory diagram of the circuit configuration of the power control sections 38 to 40.

[0055] The power control section 38 is composed of a power control circuit (first switch control circuit) 38, and transistors (first switch section) 38, and 38. The transistor 38, consists of an N channel MOS, and the transistor 38, consists of a P channel MOS.

[0056] The input-output circuit 29 and the control circuit 31 are connected between the power supplies via the transistor 38, and the word driver 27 is connected between the power supplies via the transistor 38. The memory mat 26, and the output circuit 36 are directly connected between the power supplies.

[0057] The transistor 38, is connected between the input-output circuit 29 and a reference potential GND and between the control circuit 31 and the reference potential GND. Also, the transistor 38, is connected between the word driver 27 and a power supply voltage VDD.

[0058] The power control circuit 38, controls the on and off of the transistors 38, and 38, based on a selection signal (for example, a high-order address of the addresses to be inputted from the CPU 12) for selecting the memory mat outputted from the predecoder circuit 34.

[0059] The power control section 39 is composed of a power control circuit (first switch control circuit) 39, and transistors (first switch sections) 39, and 39. The transistor 39, consists of the N channel MOS and the transistor 39, consists of the P channel MOS.

[0060] The input-output circuit 30 and the control circuit 32 are connected between the power supplies via the transistor 39, and the word driver 28 is connected between the power supplies via the transistor 39. The memory mat 26, and the output circuit 37 are directly connected between the power supplies.

[0061] The transistor 39, is connected between the input-output circuit 30 and the reference potential GND and between the control circuit 32 and the reference potential GND, and the transistor 39, is connected between the word driver 28 and the power supply voltage VDD.

[0062] The power control circuit 39, controls the on and off of the transistors 39, and 39, based on the memory mat selection signal outputted from the predecoder circuit 34.

[0063] When the transistors 39, and 39, are turned off, connections between the input-output circuit 30 and the reference potential GND and between the control circuit 32 and the reference potential GND, and between the power supply voltage VDD and the word driver 28 are shut off, and the power supply is stopped.

[0064] Here, the reason why the power supply to the memory mats 26, and 26, is not stopped is to hold the data of the memory mats 26, and 26, and the reason why the power supply to the output circuits 36 and 37 is not stopped is to prevent the output of the memory module 25 from becoming a high impedance.

[0065] Further, since the word drivers 27 and 28 output Hi signals at an active time, the power supply voltage VDD is shut off and the reference potential GND is connected by the word drivers 27 and 28. By doing so, it is possible to prevent the malfunction of the memory mats 26, and 26.

[0066] The power control section (second power control section) 40 is composed of a power control circuit (second switch control circuit) 40, and transistors (second switch sections) 40, to 40. The transistors 40, to 40, are composed of the N channel MOS.

[0067] The transistor 40, is connected between the power control circuit 38, and the reference potential GND, and the transistor 40, is connected between the power control circuit 38, and the reference potential GND. The transistor 40, is connected between the predecoder circuit 34, the input circuit 35, and the control circuit 33 and the reference potential GND.

[0068] The power control circuit 40, controls the on and off of the transistors 40, to 40, based on a standby signal inputted externally from the CPU 12 (FIG. 1) and the like. When the standby signal is inputted to the power control circuit 40, the power control circuit 40, outputs a Lo signal and turns off the transistors 40, to 40.

[0069] Next, the operation of the power control sections 38 to 40 in the first embodiment will be described.

[0070] During the time when a memory mat selection signal outputted from the predecoder circuit 34 selects the memory mat 26, the power control circuit 38, outputs a control signal to turn on the transistors 38, and 38, and the power control circuit 39, outputs a control signal to turn off the transistors 39, and 39. In this manner, the power supply
to the word driver 28, the input-output circuit 30, and the control circuit 32, operations of which are not needed is shut off.

Further when the standby signal is inputted and the memory module 25 is put into a standby state, the power control circuit 40, outputs a Lo signal to turn off the transistors 40, to 40, Therefore, not only the power supply to the control circuit 33, the predecoder circuit 34 and the input circuit 35 but also the power supply to the power control circuits 38, and 39 are shut off, and the leakage current and the like of the MOS transistors which form the power control circuits 38, and 39, can be drastically reduced.

Fig. 4 is an explanatory drawing of the layout of the power control sections 38 to 40 in a semiconductor chip C1.

As shown in Fig. 4, a wiring area HR in which wiring patterns are formed is provided in the central region. An input-output circuit 29 extending from above to below is formed on the left side of the wiring area HR, and an input-output circuit 30 extending from above to below is formed on the right side of the wiring area HR.

The memory mat 26 is formed on the left side of the input-output circuit 29 and the memory mat 26 is formed on the right side of the input-output circuit 30.

The power control circuit 38, and the control circuit 31 are formed above the input-output circuit 29 and the power control circuit 39, and the control circuit 32 are formed below the input-output circuit 30.

The word drivers 27 and 28 are formed above the memory mats 26 and 26, The transistors 38, and 39, are formed on the left and right of the word drivers 27 and 28. These transistors 38, and 39, are composed of a large number of transistors connected in parallel.

The transistors 40, to 40, are formed on the left side of the memory mat 26, and the input circuit 35 and the output circuits 36 and 37 are formed on the left side of the area where the transistors 40, to 40, are formed.

The control circuit 33, the predecoder circuit 34, and the power control circuit 40, are formed below the memory mat 26, The transistors 40, to 40, are formed below the memory mat 26, These transistors 40, to 40, are also composed of a large number of transistors connected in parallel.

The transistor 38, is formed on the right side of the input-output circuit 29 and the transistor 39, is formed on the left side of the input-output circuit 30. These transistors 38, and 39, are also composed of a large number of transistors connected in parallel.

In this manner, according to this first embodiment, since the power supply to the power control circuits 38, and 39, is also shut off at the standby time of the memory module 25, the current at the standby time in the memory module 25 can be drastically reduced.

Second Embodiment

Fig. 5 is a circuit diagram showing a connection configuration of a power control section provided in a memory module according to a second embodiment of the present invention.

In this second embodiment, similar to the memory module 25 (Fig. 2) of the first embodiment, a memory module 25a is composed of a memory array 26 consisting of a memory mat 26, and a memory mat 26, word drivers 27 and 28, input-output circuits 29 and 30, control circuits 31 to 33, the predecoder circuit 34, the input circuit 35, output circuits 36 and 37, power control sections 38a and 39a (first power control sections), and a power control section 40, As shown in Fig. 5, the power control section 40 is different from that transistors 40, 40a, and 40 (second switch sections) are provided to the same configuration as the first embodiment (Fig. 3) composed of the power control circuit 40, and the transistors 40, 40a, and 40.

The transistor 40, is connected between the control circuit 31 and a reference potential GND and between the input-output circuit 29 and the reference potential GND, and the transistor 40, is connected between the word driver 27 and the power supply voltage VDD.

As shown in Fig. 6, the power control section 40 is different from that in the first embodiment, the description thereof will be omitted.

During the time when a selection signal outputted from the predecoder circuit 34 selects the memory mat 26a, a Hi signal is outputted to the transistor 38, from the output section of the power control circuit 38, and a Lo signal is outputted to the transistor 39, from the output section of the power control circuit 39.

At this time, since a standby signal is not inputted to the power control circuit 40, the Hi signal is outputted so as to turn on the transistors 40, to 40, and the Lo signal is inputted through an inverter to the transistor 40, so as to turn on the transistor 40.

Consequently, the transistors 38a, 38a, 40a, and 40a are turned on and the transistors 39a and 39a are turned off, and thus, the power supply to the word driver 28, the input-output circuit 30, and the control circuit 32 is shut off.

Further, when the standby signal is inputted to the memory module 25a, the Lo signal is outputted from the power control circuit 40, to turn off and the transistors 40, to 40, and 40, is that the signal is outputted through the inverter to turn off the transistors 40, and 40.

When the transistors 40, and 40, are turned off, the power is not supplied to the power control circuits 38, and 39, and the output signal from the power control circuits 38, and 39, becomes uncertain. However, as described above, since the transistors 40, to 40, are turned off by the signal from the power control circuit 40, it is possible to shut off the power supply to the power control circuits 38, and 39, the word drivers 27 and 28, the input-output circuits 29 and 30, and the control circuits 31 and 32.

Thus, in this second embodiment, even if the power supply to the power control circuits 38, and 39, is stopped, it is possible to turn off the transistors 40, 40, 40, and 40, so as to reduce the consumption current of the memory module 25a at the standby time.

Third Embodiment

Fig. 6 is a circuit diagram showing a connection configuration of a power control section provided in a memory module according to a third embodiment of the present invention.

In this third embodiment, similar to the memory module 25 (Fig. 2) of the first embodiment, a
memory module 25b is composed of a memory array 26 consisting of a memory mat 26a and a memory mat 26b, word drivers 27 and 28, input-output circuits 29 and 30, control circuits 31 to 33, a predecoder circuit 34, an input circuit 35, output circuits 36 and 37, power control sections 38a and 39a (first power control sections), and a power control section 40. [0096] Further, as shown in Fig. 6, the power control sections 38a and 39a are different in that the NAND circuits (switch control sections) 38a and 39a and AND circuits (switch control sections) 38a and 39a are provided to the same configuration as the first embodiment (Fig. 3) composed of the power control circuits 38a and 39a and the transistors 38a, 38b, 38c, 39a, and 39b.

[0097] The output section of the power control circuit 38a is connected to each one of the input sections of the NAND circuits 38a and 38c, respectively, and the output section of the power control circuit 38a is connected to each one of the input sections of the NAND circuit 39a and the AND circuit 39a, respectively.

[0098] The output section of the power control circuit 40a, the output section of the power control circuit 40b, is connected to the output section of the power control circuit 40a, respectively. The gate of the transistor 38a is connected to the output section of the NAND circuit 38a, and the gate of the transistor 38a is connected to the output section of the AND circuit 38a.

[0099] The gate of the transistor 39a is connected to the output section of the NAND circuit 39a, and the gate of the transistor 39a is connected to the output section of the AND circuit 39a. Further, since the other circuit connection configuration is identical to that in Fig. 3 of the first embodiment, the description thereof will be omitted.

[0100] Next, the operation of the power control sections 38a and 39a in the third embodiment will be described.

[0101] During the time when a selection signal outputted from the predecoder circuit 34 selects the memory mat 26a, a Hi signal is outputted to each one of the other input sections of the NAND circuit 38a and the AND circuit 38a, from the output section of a power control circuit 39a. On the other hand, a Lo signal is outputted to each one of the input sections of the NAND circuit 39a and the AND circuit 39a, from the output section of the power control circuit 39a.

[0102] At this time, since a standby signal is not inputted to the power control circuit 40a, the Hi signal is outputted so as to turn on the transistors 40a to 40c and the Hi signal is inputted to the other input sections of the NAND circuits 38a and 39a and the AND circuits 38a and 39a, respectively.

[0103] Consequently, the transistors 38a, 38b, and 38c, are turned on and the transistors 39a, 39b, and 39c, are turned off, and thus, the power supply to the word driver 28, the input-output circuit 30 and the control circuit 32 is shut off.

[0104] Further, when the standby signal is inputted to the memory module 25a, the Lo signal is outputted from the power control circuit 40a to turn off the transistors 40a to 40c. The Lo signal is inputted to the other input sections of the NAND circuits 38a and 39a and the AND circuits 38a, and 39a, respectively.

[0105] When the transistors 40a and 40b are turned off, the power is not supplied to the power control circuits 38a and 39a, and the output signal from the power control circuits 38a and 39a becomes uncertain. However, as described above, since the Lo signal is inputted to the other input sections of the NAND circuits 38a and 39a and the AND circuits 38a, and 39a, respectively, the NAND circuits 38a and 39a output the Hi signal and the AND circuits 38c and 39c output the Lo signal, and thus, the transistors 38a, 38b, 39a, and 39b, can be reliably turned off.

[0106] Consequently, in this third embodiment, even if the power supply to the power control circuits 38a and 39a is stopped, it is possible to reliably turn off the transistors 38a, 38b, 39a, and 39b, and also possible to further reduce the consumption current of the memory module 25a at the standby time.

Fourth Embodiment

[0107] FIG. 7 is a diagram in the fourth embodiment, in which the second embodiment is applied to the semiconductor integrated circuit device shown in FIG. 1.

[0108] Each circuit module constituting a semiconductor integrated circuit device is composed of, for example, an XY memory controller (block 1) 2, a CPU (block 2) 12, and a USB (block 13) 18.

[0109] A power control section 38c is composed of the power control circuit 38a and the transistor 38b, and in the case where a circuit module in the block 1 becomes a target of the power supply shut off, the transistor 38a is controlled to be turned off by the control signal of a first state from the CPU 12. In this manner, the power supply to the circuit module in the block 1 is shut off.

[0110] The power control section 40a is composed of the power control circuit 40a and a transistor (second switch section) 40b. The transistor 40b is connected between each circuit module contained in the blocks 1 and 2 and the power control circuit 38a and the reference potential GND, and the Lo signal is outputted from the power control circuit 40b by, for example, the control signal of a second state showing a standby state of the CPU 12 so as to turn off the transistor 40b. By doing so, it is possible to control the shut off of the power supply to the blocks 1 and 2. Further, the transistor 40b is not limited to the configuration of FIG. 7 and can be provided by each circuit module and the power control circuit 38a, as shown in FIG. 5.

[0111] The circuit module contained in the block 3 includes, for example, an interrupt controller 10, communication units 17 and 18, a timer unit (not shown), and the like. These circuits perform the input-output of the signals with the outside of the semiconductor integrated circuit device and never become the targets of the control of the power supply shut off in order to always be in a state ready to receive the signal.

[0112] The circuit module contained in the block 1 includes, for example, an XY memory 3, a user memory controller 4, and the like, and in the case where the semiconductor integrated circuit device is in a mode not to access a built-in memory or there is no need to perform the operation for a fixed period of time, it is possible to shut off the power supply by the power control section 38c regardless of the operation of other circuit modules.

[0113] The circuit module contained in the block 2 includes, for example, the DSP 13. These blocks share the power control section 40a with other blocks, and in the case where they are in a state not being accessed even in the period when the semiconductor integrated circuit device is in an operating state, it is possible to shut off the power supply by the power control section 40a.

[0114] By these controls of the power supply, it is possible to reduce the consumption current at the operation time and the standby time. Further, since the power supply is shut off
and the unnecessary operations of the circuit modules are prevented, it is possible to reduce a power supply noise in the semiconductor integrated circuit device.

[0115] Further, these blocks can be composed of a plurality of blocks. Further, it is also possible to provide the power control section commonly used by a plurality of circuit modules.

[0116] Further, the configuration of the power control circuit is not limited to the above-described embodiments, and the configuration similar to that of the third embodiment in which the power supply control is performed by the NAND circuit (switch control section) and the AND circuit is also available.

[0117] In the foregoing, the invention made by the inventors of the present invention has been concretely described based on the embodiments. However, it is needless to say that the present invention is not limited to the foregoing embodiments and various modifications and alterations can be made within the scope of the present invention.

1-12. (canceled)

13. A semiconductor integrated circuit device on a single semiconductor chip, comprising:
a central processing unit; and
an internal memory operated between a power supply voltage and a reference potential and including:
an input circuit coupled to the central processing unit, a first memory mat,
a first input and output circuit coupled between the input circuit and the first memory mat,
a first switching transistor provided between the power supply voltage and the reference potential via the first input and output circuit,
a first power control circuit coupled to the first switching transistor and controlling an operation of the first switching transistor in response to a selection or a non-selection of the first memory mat,
a second switching transistor provided between the power supply voltage and the reference potential via the first power control circuit,
a third switching transistor provided between the power supply voltage and the reference potential via the input circuit, and
a second power control circuit coupled to the second and third switching transistors and controlling operations of the second and third switching transistors in response to a standby signal from the central processing unit.

14. A semiconductor integrated circuit according to claim 13,
wherein the first switching transistor is turned on by the first power control circuit when the first memory mat is selected, and
wherein the first switching transistor is turned off by the first power control circuit when the first memory mat is unselected.

15. A semiconductor integrated circuit according to claim 14,
wherein the second and third switching transistors are turned off by the second power control circuit when the second power control circuit receives the standby signal.

16. A semiconductor integrated circuit according to claim 13,
wherein the second and third switching transistors are turned off by the second power control circuit when the second power control circuit receives the standby signal.

17. A semiconductor integrated circuit, according to claim 13,
wherein the internal memory further includes:
a second memory mat,
a second input and output circuit coupled between the input circuit and the second memory mat,
a fourth switching transistor provided between the power supply voltage and the reference potential via the second input and output circuit,
a third power control circuit coupled to the fourth switching transistor and controlling an operation of the fourth switching transistor, and
a fifth switching transistor provided between the power supply voltage and the reference potential via the third power control circuit, an operation of the fifth switching transistor being controlled by the second power control circuit.

18. A semiconductor integrated circuit according to claim 17,
wherein the fourth switching transistor is turned on by the third power control circuit when the second memory mat is selected, and
wherein the fourth switching transistor is turned off by the third power control circuit when the second memory mat is unselected.

19. A semiconductor integrated circuit according to claim 18,
wherein the first switching transistor is turned on by the first power control circuit when the first memory mat is selected, and
wherein the first switching transistor is turned off by the first power control circuit when the first memory mat is unselected.

20. A semiconductor integrated circuit according to claim 19,
wherein the second, third and fifth switching transistors are turned off by the second power control circuit when the second power control circuit receives the standby signal.

21. A semiconductor integrated circuit device on a single semiconductor chip, comprising:
a central processing unit; and
an internal memory operated between a power supply voltage and a reference potential and including:
an input circuit coupled to the central processing unit, a first memory mat,
a first input and output circuit coupled between the input circuit and the first memory mat,
a first switching transistor provided between the power supply voltage and the reference potential via the first input and output circuit,
a first power control circuit coupled to the first switching transistor and controlling an operation of the first switching transistor in response to a selection or a non-selection of the first memory mat,
a second switching transistor provided between the power supply voltage and the reference potential via the first power control circuit.
a second input and output circuit coupled between the input circuit and the second memory mat,
a third switching transistor provided between the power supply voltage and the reference potential via the second input and output circuit,
a second power control circuit coupled to the third switching transistor and controlling an operation of the third switching transistor,
a fourth switching transistor provided between the power supply voltage and the reference potential via the second power control circuit,
a fifth switching transistor provided between the power supply voltage and the reference potential via the input circuit, and
a third power control circuit coupled to the second, fourth and fifth switching transistors and controlling operations of the second, fourth and fifth switching transistors in response to a standby signal from the central processing unit.

22. A semiconductor integrated circuit according to claim 21,
wherein the first switching transistor is turned on by the first power control circuit when the first memory mat is in a selection state,
wherein the first switching transistor is turned off by the first power control circuit when the first memory mat is in a non-selection state,
wherein the third switching transistor is turned on by the second power control circuit when the second memory mat is in a selection state, and
wherein the third switching transistor is turned off by the second power control circuit when the second memory mat is in a non-selection state.

23. A semiconductor integrated circuit according to claim 22,
wherein second, fourth and fifth switching transistors are turned off by the third power control circuit when the third power control circuit receives the standby signal.

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