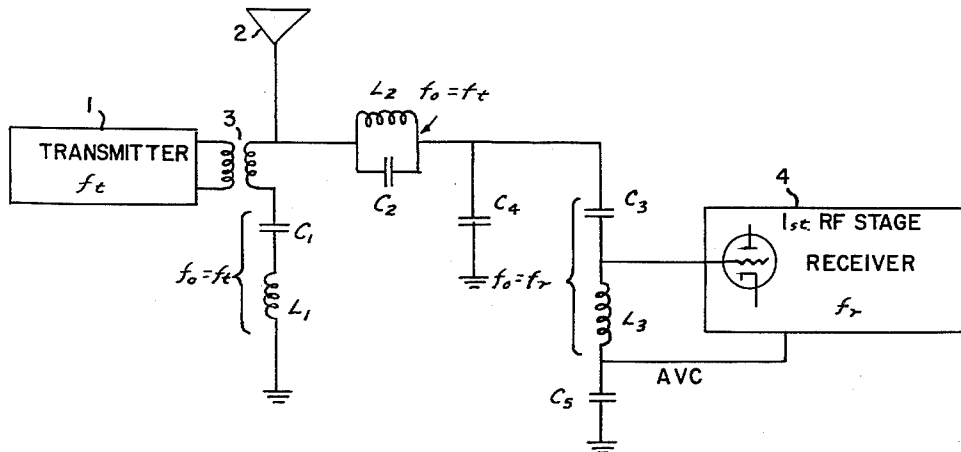


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WAVE TRAP ENABLING SIMULTANEOUS RECEIVING
AND TRANSMITTING FROM SAME ANTENNA
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WAVE TRAP ENABLING SIMULTANEOUS RECEIVING AND TRANSMITTING FROM SAME ANTENNA

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1 Claim. (Cl. 343-180)

(Granted under Title 35, U.S. Code (1952), sec. 266)

The invention described herein may be manufactured and used by or for the United States Government for governmental purposes without payment to me of any royalty thereon.

The purpose of this invention is to provide a circuit for coupling the output of a transmitter and the input of a receiver to a common antenna for simultaneous transmitting and receiving at different but not widely separated frequencies without undue loss of transmitter power or overloading of the receiver input.

The details of the invention will be explained with reference to the accompanying drawing which shows a schematic diagram of the coupling circuit.

Transmitter 1, operating at a frequency f_t , is coupled to the antenna 2 through transformer 3. Receiver 4, operating at a frequency f_r , which differs from f_t , has the grid of its first R.F. stage coupled to the antenna 2 by means of a circuit comprising a series resonant circuit L_3-C_3 tuned to f_r , a shunt condenser C_4 , a parallel resonant circuit L_2-C_2 tuned to f_t and a series resonant circuit L_1-C_1 tuned to f_t . Condenser C_5 serves as a by-pass condenser around the AVC circuit of the receiver which is connected to the grid of the first R.F. stage through L_3 .

Since the resonant frequency f_0 of circuit L_1-C_1 is f_t , this series resonant circuit offers negligible impedance to the transmitter frequency and substantially all of the transmitter output voltage at the secondary of transformer 3 is applied between the antenna and ground as desired for maximum radiation. The purpose of circuit L_2-C_2 , condenser C_4 and circuit L_3-C_3 is to reduce this voltage enough before it reaches the receiver input to prevent overloading of the receiver. As seen from the drawing, the antenna voltage during transmission is also applied across the series circuit consisting of parallel resonant circuit L_2-C_2 and condenser C_4 . Since the L_2-C_2 circuit is tuned to f_t it presents a high impedance to currents of this frequency. The magnitude of this impedance equals $2\pi f_t L_2 Q$, where $Q=2\pi f_t L_2/R_2$, R_2 being the radio frequency resistance of L_2 at f_t , and may be made very large by the use of an inductance L_2 of high Q . Condenser C_4 is made large enough to have an impedance at f_t that is very low relative to the impedance of L_2-C_2 at this frequency. Therefore, a very small fraction of the voltage of frequency f_t appearing between the antenna and ground appears across C_4 .

The radio frequency voltage across C_4 is also applied across series circuit L_3-C_3 . Condenser C_5 is a relatively large by-pass condenser so that the lower end of L_3 is effectively connected to ground for radio frequencies. The resonant frequency f_0 of circuit L_3-C_3 is made equal to the receiving frequency f_r . With sufficient separation

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of f_r and f_t , the f_t voltage across L_3 may be reduced to a magnitude comparable to the f_t signal magnitude across C_4 .

When f_t is lower than f_r the position of L_3 and C_3 should be as shown in the drawing since the greater f_t voltage appears across C_3 . For an f_t greater than f_r the positions of C_3 and L_3 should be interchanged since the greater f_t voltage will then be developed across L_3 .

The operation of the circuit coupling the antenna to the receiver input will now be considered for the receiving frequency f_r . Since the circuit L_1-C_1 is tuned to f_t it has a relatively high impedance at f_r . This prevents the relatively low output impedance of the transmitter from loading the antenna at f_r . The receiving frequency antenna voltage, in the same manner as the transmitting frequency voltage, is applied across the series circuit consisting of circuit L_2-C_2 and C_4 . However, circuit L_2-C_2 , which is tuned to f_t , has a relatively low impedance at f_r so that a greater portion of the antenna f_r voltage is developed across C_4 than was the case for the f_t voltage. Further, circuit L_3-C_3 , which is tuned to series resonance at f_r , develops voltages across L_3 and C_3 that are far greater than the voltage across C_4 , being Q times this voltage. Therefore, if an inductance L_3 of very high Q is used, the f_r voltage developed across L_3 and applied to the input of the receiver will be many times the voltage of this frequency across C_4 .

From the foregoing it is seen that high attenuation of voltages of frequency f_t occurs between the antenna and the receiver input. This, together with the fact that the receiver is tuned to receive f_r and reject f_t , prevents the transmitter from overloading the receiver. On the other hand, the f_r signal is conveyed from the antenna to the receiver input with little or no attenuation, the loss introduced by L_2-C_2 and C_4 being made up by the voltage amplification produced by series resonant circuit L_3-C_3 .

I claim:

A circuit for coupling an antenna to the output circuit of a transmitter and the input circuit of a receiver, comprising: a transformer having a primary winding coupled to the output circuit of said transmitter and a secondary winding; a first series inductance-capacitance circuit resonant at a predetermined transmitting frequency; means connecting one terminal of said secondary winding to said antenna and the other terminal through said first series inductance-capacitance circuit to a point of reference potential; a shunt capacitor having one terminal connected to said point of reference potential; a parallel inductance-capacitance circuit resonant at said transmitting frequency connected between said antenna and the other terminal of said shunt capacitor; a second series inductance-capacitance circuit resonant at a predetermined receiving frequency different from said transmitting frequency connected in parallel to said shunt capacitor; and means coupling the input of said receiver across one of the elements of said second series inductance-capacitance circuit.

References Cited in the file of this patent

UNITED STATES PATENTS

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