(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
8 January 2009 (08.01.2009)

PCT

(10) International Publication Number
WO 2009/005696 A1

(51) International Patent Classification:
H05K 3/46 (2006.01)

(21) International Application Number:
PCT/US2008/007978

(22) International Filing Date: 23 June 2008 (23.06.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/824,484 29 June 2007 (29.06.2007) US

(71) Applicant *(for all designated States except US)*: **TESSERA, INC.** [US/US]; 3099 Orchard Drive, San Jose, CA 95134 (US).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **HABA, Belgacem** [US/US]; C/o Tessera, Inc., 3099 Orchard Drive, San Jose, CA 95134 (US).

(74) Agents: **CAPATI, April, M.** et al.; Lerner, David, Littenberg, Krumholz & Mentlik, LLP, 600 South Avenue West, Westfield, NJ 07090 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

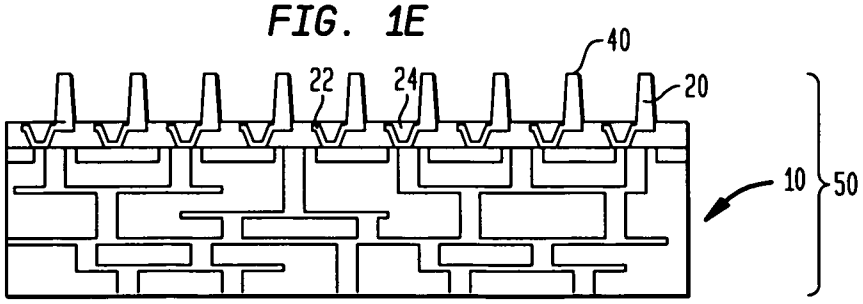
— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report*

(54) Title: MULTILAYER WIRING ELEMENT HAVING PIN INTERFACE

FIG. 1E



(57) Abstract: A method of forming contacts for an interconnection element (10), includes (a) joining a conductive element (16) to an interconnection element 10 having multiple wiring layers, (b) patterning the conductive element (16) to form conductive pins (20), and (c) electrically interconnecting the conductive pins (20) with conductive features of the interconnection element (10). A multiple wiring layer interconnection element (10) having an exposed pin interface, includes an interconnection element (10) having multiple wiring layers separated by at least one dielectric layer (24), the wiring layers including a plurality of conductive features exposed at a first face of the interconnection element (10), a plurality of conductive pins (20) protruding in a direction away from the first face, and metal features (22) electrically interconnecting the conductive features with the conductive pins (20).

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MULTILAYER WIRING ELEMENT HAVING PIN INTERFACE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims the benefit of Application Serial No. 11/824,484, filed June 29, 2007, entitled MULTILAYER WIRING ELEMENT HAVING PIN INTERFACE, the disclosure of which is hereby incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] The present invention relates generally to interconnecting microelectronic devices and supporting interconnection elements, especially multilayer wiring elements.

[0003] In the flip-chip mounting technique, the front or contact-bearing surface of a microelectronic device is mounted face-down to an interconnection element such as a chip carrier or other interconnection element, e.g., substrate. Each contact on the device is joined by a solder bond to the corresponding contact pad on the substrate, as by positioning solder balls on the substrate or device, juxtaposing the device with the substrate in the front-face-down orientation and momentarily reflowing the solder. The flip-chip technique yields a compact assembly, which occupies an area of the substrate no larger than the area of the chip itself.

[0004] However, thermal stress presents significant challenges to the design of flip-chip assemblies. The solder bonds between the device contacts and the supporting substrate are substantially rigid. Changes in the relative sizes of the device and the supporting substrate due to thermal expansion and contraction in service create substantial stresses in these rigid bonds, which in turn can lead to fatigue failure of the bonds. Moreover, it is difficult to test the chip before attaching it to the substrate, and hence difficult to maintain the required outgoing quality level in the finished

assembly, particularly where the assembly includes numerous chips.

[0005] As the number of interconnections per microelectronic device increases, the issue of interconnection planarity continues to grow as well. If the interconnections are not planar with respect to each other, it is likely that many of the interconnections will not electrically contact their juxtaposed contact pads on a supporting substrate, such as a standard printed wiring board. Therefore, a method of making coplanar pins on existing multilayer interconnection elements is desired.

SUMMARY OF THE INVENTION

[0006] In an embodiment of the present invention, a method of forming contacts for an interconnection element, includes (a) joining a conductive element to an interconnection element having multiple wiring layers, (b) patterning the conductive element to form conductive pins, and (c) electrically interconnecting the conductive pins with conductive features of the interconnection element.

[0007] In another embodiment of the present invention, a multiple wiring layer interconnection element having an exposed pin interface, includes an interconnection element having multiple wiring layers separated by at least one dielectric layer, the wiring layers including a plurality of conductive features exposed at a first face of the interconnection element, a plurality of conductive pins protruding in a direction away from the first face, and metal features electrically interconnecting the conductive features with the conductive pins.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figs. 1A-1E illustrate an embodiment of a method of assembling an electronic interconnect of the present invention.

[0009] Figs. 2A-2E illustrate another embodiment of a method of assembling an electronic interconnect of the present invention.

[0010] Fig. 3 schematically illustrates a side view of microelectronic pins.

[0011] Fig. 4 schematically illustrates a top view of microelectronic pins.

[0012] Figs. 5A-5B schematically illustrate a side view of microelectronic pins.

[0013] Figs. 6A-6E illustrate another embodiment of a method of assembling an electronic interconnect of the present invention.

[0014] Figs. 7A-7C illustrate an embodiment of an assembly of the invention joined to other electronic structures.

DETAILED DESCRIPTION

[0015] A method of making coplanar pins on existing multilayer interconnection elements is herein described. A multilayer interconnection element 10 is shown in Fig. 1, having dielectric portions 12 and conductive portions 14. The conductive portions may be in the form of wires, bond pads or the like.

[0016] The multilayer interconnection element 10 may be formed of a single metal substrate or a multilayer substrate with dielectric such as polyimide, ceramic, FR4, BT resin and the like. The multilayer interconnection element 10 may also be an interconnection element with multiple wiring layers or the like. Reference is also made to U.S. Pat. No. 6,528,784 which discusses the manufacture of a multilayer interconnection element, which is hereby incorporated by reference.

[0017] In one embodiment of the present invention, a metallic layer 16 is laminated onto the multilayer interconnection element 10 using an adhesive 18 as illustrated in Fig. 1B. The metallic layer 16 may be any suitable metal

as known in the art. For example, the metal may be any conductive metal, such as copper. Thereafter, the metallic layer 16 may be used to form microelectronic contacts or pins 20 as shown in Fig. 1C.

[0018] The microelectronic pins 20 may be formed as known in the art. For example, the microelectronic pins 20 may be formed by photolithographically patterning a resist layer on metallic layer 16 and transferring the resist patterns to the metallic layer 16 by etching.

[0019] Once the microelectronic pins 20 are formed, where the adhesive layer 18 acts as an etch stop layer, the adhesive 18 may have portions removed from it to permit electrical connections to be formed between the microelectronic pins 20 and the conductive portions 14 of the multilayer interconnection element 10, as shown in Fig. 1D. The adhesive 18 may be selectively removed using photolithographic techniques or the like, as known in the art.

[0020] Then, as shown in Fig. 1E, electrical connections 22 are formed adjacent the portions removed from the adhesive 18. For example, sputtering, also known as physical vapor deposition, or electroless plating may be followed by photolithographic patterning or laser drilling to define locations of the connections. Once the electrical connections 22 have been formed, they may be electroplated to increase their thickness to an amount desired. This then results in electrical connections 22 being formed between the multilayer interconnection element 10 and the microelectronic pins 20. Lastly, a protective dielectric layer or film 24 (Fig. 1E) may be deposited onto the multilayer interconnection element 10 covering the electrical connections 22 and lower portions of the microelectronic pins 20 to form the assembly 50 is not damaged. This protective layer 24 can also assist in maintaining co-planarity of the top surfaces 40 of the microelectronic pins 20 because the dielectric protective

layer 24 reduces flexure when the assembly 50 is handled because it holds the pins 20 in a stiff fashion. Example protective layer materials include a solder mask or the like.

[0021] In another embodiment of the present invention, a multilayer interconnection element 10 is illustrated as shown in Fig. 2A. Thereafter, as shown in Fig. 2B, a layered metallic structure 26 is joined to the multilayer interconnection element 10 using an adhesive 18. The layered metallic structure 26 may include a first metallic layer 28, an etch stop layer 30 and a second metallic layer 32. The first metallic layer 28, preferably, has a greater thickness than the second metallic layer 32. Although a trimetal structure is illustrated, the layered metallic structure 26 may include any number of layers.

[0022] Microelectronic pins 20 may be formed from the first metallic layer 28, as shown in Fig. 2C using techniques such as photolithographic patterning, or the like. However, the etch-stop layer remains.

[0023] A method of fabricating the pins 20 will now be described with reference to the following figures. As shown in FIG. 3, a plurality of conductive pins 200 are formed to protrude above a surface of a continuous metal wiring layer 210. The pins 200 can be formed by a variety of different processes. Exemplary processes are described in U.S. Patent No. 6,884,709, as well as in the U.S. Provisional Application entitled, "Chip Capacitor Embedded PWB" having serial number 60/875,730 and a file date of January 11, 2007, the disclosures of which are incorporated by reference herein.

[0024] In one such process, an exposed metal layer of a multi-layer metal structure is etched in accordance with a photolithographically patterned photoresist layer to form pins 200, the etching process stopping on an interior metal layer 220 of the structure. The interior metal layer 220 includes one or more metals different from that of the exposed metal

layer, the interior metal layer 220 being of such composition that it is not attacked by the etchant used to etch the exposed metal layer. For example, the metal layer from which the pins 200 are etched can consist essentially of copper, the continuous metal layer 210 can also consist essentially of copper, and the interior metal layer 220 can consist essentially of nickel. Nickel provides good selectivity relative to copper to avoid the nickel layer from being attacked when the metal layer is etched to form pins 200.

[0025] After forming the pins 200, a different etchant is then applied to remove the exposed interior metal layer 220 by a process which is selective to the underlying metal layer 210. Alternatively, another way that the pins 200 can be formed is by electroplating, in which pins are formed by plating a metal onto a base metal layer 210 through openings patterned in a dielectric layer such as a photoresist layer.

[0026] As indicated in plan view in FIG. 4, the pins can have a variety of different shapes and sizes. For example, when viewed from the top, the pins can have a shape which is circular 300, square or rectangular 310, or oval shape 320. When pins have a star shape, it may allow them to compress more easily or less easily than when other shapes are used. The height of the pins 200 above the plane of the underlying metal layer typically ranges between about 15 microns (μm) and about 250 microns (μm) and the width ranges for the tip of the pins is about 30 microns and above.

[0027] FIGS. 5A and 5B illustrate exemplary alternative structures that the pins can take. For example, as illustrated in FIG. 5A, a pin 400 is formed by etching a first metal layer selective to an etch stop metal layer 420 which overlies a base metal layer 440, the pin 400 being coated with a second metal layer 410. The second metal layer can include the same metal as the first metal layer, one or more other metals, or a combination of a metal included in the first

metal layer with another metal. In a particular embodiment, the second metal layer 410 includes a metal such as gold which is resistant to corrosion and which may also facilitate the formation of a diffusion bond between the second metal layer and a metal layer of another feature in contact therewith. In another particular embodiment, the second metal layer includes a low melting temperature metal such as tin or a low melting temperature metal alloy such as solder or a eutectic composition. Additional examples of one or more metals usable as a second metal layer include nickel, aluminum or nickel/gold.

[0028] As illustrated in FIG. 5B, only the tip of a conductive pin 450 may be coated with a second metal layer 460, and the body of the conductive pin may contact the adhesive layer 470 directly, without an intervening etch stop layer.

[0029] Thereafter, as shown in Fig. 2D, portions of the etch stop layer 30, the second metallic layer 32 and the adhesive 18 may be removed. The etch stop layer 30, the second metallic layer 32 and the adhesive 18 may be removed either simultaneously or sequentially, as desired. Removal of these layers permits electrically connecting the microelectronic pins 20 with the conductive portions 14 of the multilayer interconnection element 10, as stated herein. Lastly, a protective dielectric layer 24 such as described above (Fig. 1E) may then be deposited atop the completed structure.

[0030] In yet another embodiment of the present invention, as illustrated in Figs. 6A-6E a layered metallic structure 26 may be joined to a multilayer interconnection element 10 using an adhesive 18. However, prior to this step, the second metallic layer 32 has portions removed therefrom, such that when the layered metallic structure 26 is attached to the multilayer interconnection element 10 using the adhesive, some

of the adhesive may then rise into the removed portions of the second metallic layer 32, as shown in Figs. 6B and 6C. Thus, the second metallic layer 32 may already be patterned prior to affixing the layered metallic structure 26 to the multilayer interconnection element 10.

[0031] Thereafter, microelectronic pins 20 are formed in a manner as stated previously. Next, portions of the etch stop layer 30 and the adhesive 18 are removed as shown in Fig. 6D. Then, electrical connections 22 are formed which electrically connect the microelectronic pins 20 with the conductive portions 14 of the multilayer interconnection element 10. Lastly, a protective layer 24 may be deposited to form the assembly 50.

[0032] The methods and structures described herein are advantageous for flip-chip mounting of a chip, having a land grid array ("LGA") or ball grid array ("BGA"), to the exposed pin interface such as that shown in Fig. 7A. A chip may also be mounted to the assembly 50 on a side opposite the microelectronic pins 20, as shown in Fig. 7B. Further, the methods and structures are also advantageous for flip chip or wire bond microcontacts as shown in Fig. 7C. The finished assembly may be a circuit panel or may be a circuit panel joined to a chip. Further, the finished assembly may be meant for interconnection to another circuit panel or a chip.

[0033] Although the invention herein has been described with reference to particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present invention. It is therefore to be understood that numerous modifications may be made to the illustrative embodiments and that other arrangements may be devised without departing from the spirit and scope of the present invention as defined by the appended claims.

CLAIMS

1. A method of forming contacts for an interconnection element, comprising:

(a) joining a conductive element to an interconnection element having multiple wiring layers;

(b) patterning the conductive element to form conductive pins; and

(c) electrically interconnecting the conductive pins with conductive features of the interconnection element.

2. The method of claim 1, wherein step (a) includes joining the conductive element to the interconnection element with a dielectric layer.

3. The method of claim 2, wherein the dielectric layer includes an adhesive.

4. The method of claim 2, wherein step (c) includes forming openings in the dielectric layer and forming traces interconnecting the conductive features with the conductive pins.

5. The method of claim 1, wherein the conductive element includes a single metal sheet.

6. The method of claim 1, wherein the conductive element includes a layered metal structure.

7. The method of claim 6, wherein the layered metal structure includes an outer metal layer, an inner metal layer facing the interconnection element and a third metal layer between the inner and outer metal layers, step (b) further includes etching the outer metal layer selectively with respect to the third metal layer, and step (c) includes interconnecting the conductive features with portions of the inner metal layer.

8. The method of claim 7, wherein step (c) further includes forming openings in the third metal layer and inner metal layer, the openings being aligned with the conductive features.

9. The method of claim 7, wherein the inner metal layer has first openings and step (c) further includes forming through openings in the third metal layer, the through openings being aligned with the first openings and the conductive features.

10. A method of forming a packaged chip including the method of forming contacts for an interconnection element as claimed in claim 1, further comprising:

(d) electrically interconnecting contacts of a microelectronic element with the conductive pins.

11. A method of forming a packaged chip including the method of forming contacts for an interconnection element as claimed in claim 1, wherein the conductive pins project from a first face of the interconnection element, the method further comprising:

(d) electrically interconnecting contacts of a microelectronic element with second conductive features of the interconnection element exposed at a second face of the interconnection element, the second face being remote from the first face.

12. A multiple wiring layer interconnection element having an exposed pin interface, comprising:

an interconnection element having multiple wiring layers separated by at least one dielectric layer, the wiring layers including a plurality of conductive features exposed at a first face of the interconnection element;

a plurality of conductive pins protruding in a direction away from the first face; and

metal features electrically interconnecting the conductive features with the conductive pins.

13. The element of claim 12, wherein the interconnection element is joined to the conductive pins with an adhesive.

14. The element of claim 13, wherein the adhesive includes openings through which the metal features extend.

15. The element of claim 12, wherein the conductive pins are formed from a layered metal structure having an outer metal layer, an inner metal layer facing the interconnection element and a third metal layer between the inner and outer metal layers.

16. The element of claim 15, wherein conductive pins are formed from the outer metal layer.

17. The element of claim 15, wherein the metal features interconnect the conductive features with portions of the inner metal layer.

18. An assembly including the element of claim 12, further comprising a microelectronic element having contacts interconnected with the conductive pins.

19. An assembly including the element of claim 12, further comprising a microelectronic element having contacts interconnected with the conductive features of the interconnecting element.

20. The assembly of claim 19, wherein the conductive features are at a second face remote from the conductive pins.

21. An interconnection element, comprising:

a multilayer substrate having a plurality of conductive pads;

a plurality of posts;

a joining layer positioned between the multilayer substrate and the plurality of posts, the joining layer having first and second surfaces and a plurality of metallized vias extending between the first and second surfaces, the plurality of metallized vias are positioned to electrically couple the plurality of posts to the plurality of conductive pads on the multilayer substrate.

22. The element of claim 21, wherein the posts are formed from a layered metal structure having an outer metal layer, an inner metal layer facing the joining layer and a third metal layer between the inner and outer metal layers.

23. The element of claim 22, wherein the posts are formed from the outer metal layer.

24. An assembly including the element of claim 21, further comprising a microelectronic element having contacts interconnected with the posts.

25. An assembly including the element of claim 21, further comprising a microelectronic element having contacts interconnected with second conductive pads of the multilayer substrate exposed at a second face of the multilayer substrate.

26. The assembly of claim 25, wherein the second conductive pads are at the second face being remote from a first face of the multilayer substrate adjacent the joining layer.

27. The element of claim 21, wherein the joining layer is an adhesive.

28. A method of forming an interconnection element, comprising:

providing a multilayer substrate having a plurality of contact pads;

securing a metal layer to the multilayer substrate with a joining layer;

forming a plurality of posts from the metal layer; and

forming a plurality of metallized vias within the joining layer, the metallized vias electrically coupling the contact pads of the multilayer substrate with the plurality of posts.

29. The method of claim 28, wherein the joining layer comprises a dielectric layer.

30. The method of claim 29, wherein the dielectric layer comprises an adhesive.

31. The method of claim 28, wherein the metal layer includes a single metal sheet.

32. The method of claim 28, wherein the metal layer includes a layered metal structure.

33. A method of forming a packaged chip including the method of forming contacts for an interconnection element as claimed in claim 28, further comprising:

electrically interconnecting contacts of a microelectronic element with the posts.

34. A method of forming a packaged chip including the method of forming contacts for an interconnection element as claimed in claim 28, wherein the posts project from a first face of the interconnection element, the method further comprising:

electrically interconnecting contacts of a microelectronic element with second conductive pads of the multilayer substrate exposed at a second face of the multilayer substrate, the second face being remote from the first face.

FIG. 1A

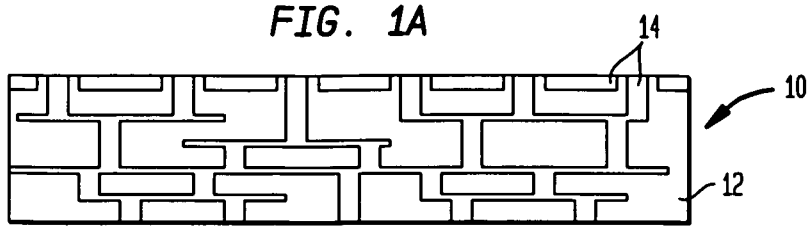


FIG. 1B

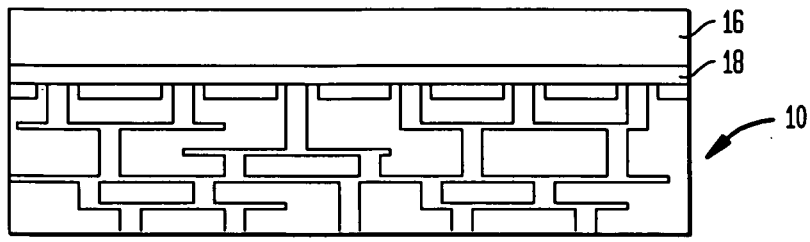


FIG. 1C

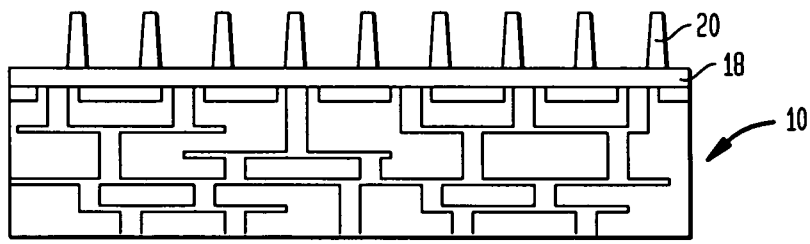


FIG. 1D

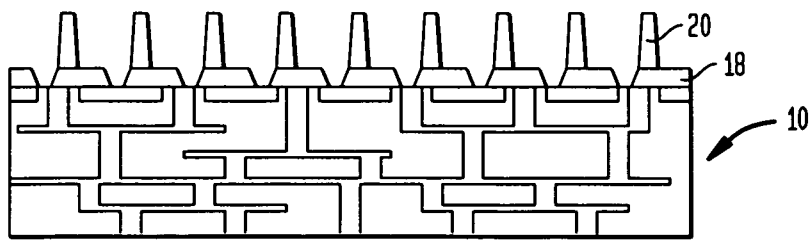


FIG. 1E

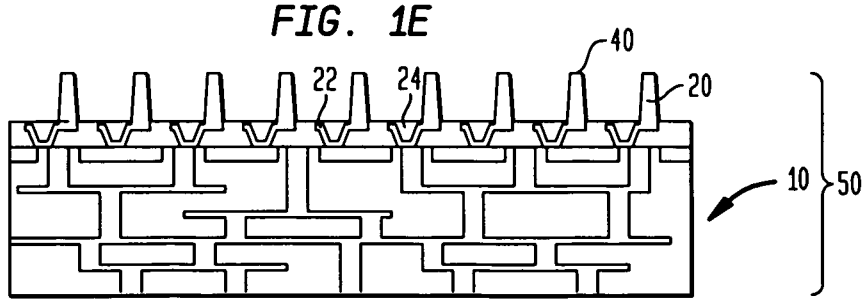


FIG. 2A

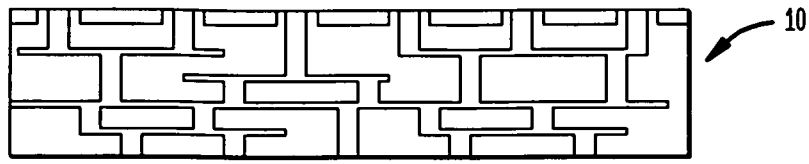


FIG. 2B

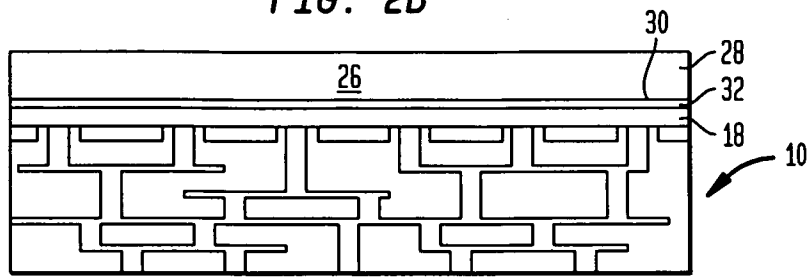


FIG. 2C

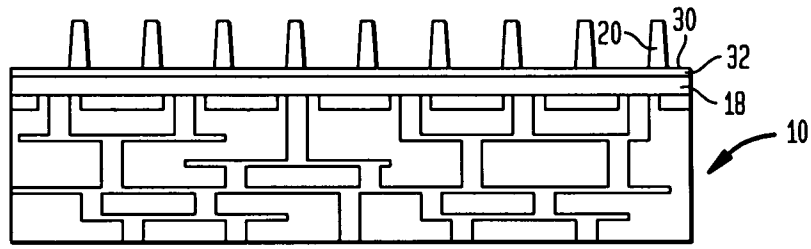


FIG. 2D

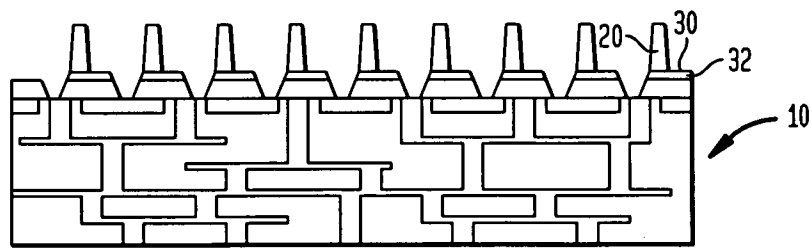


FIG. 2E

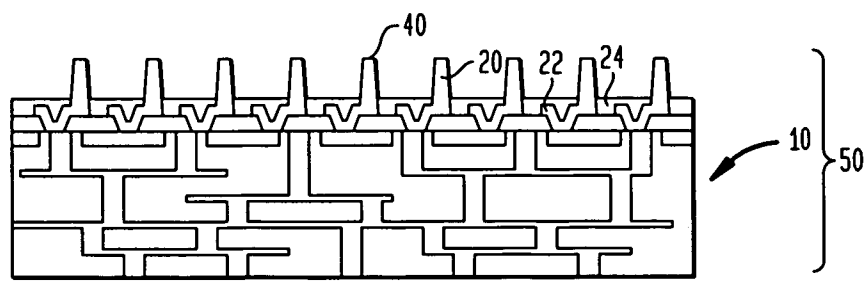


FIG. 3

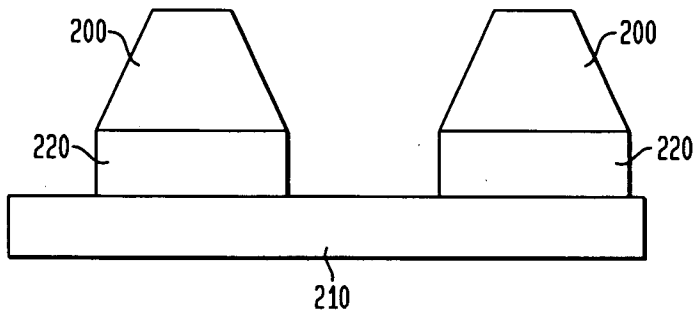


FIG. 4

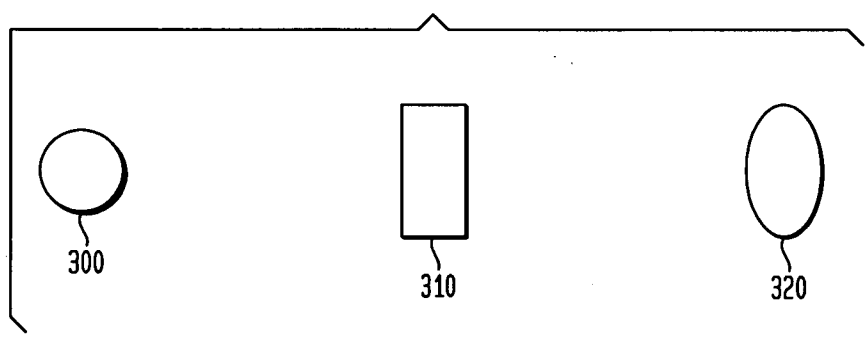


FIG. 5A

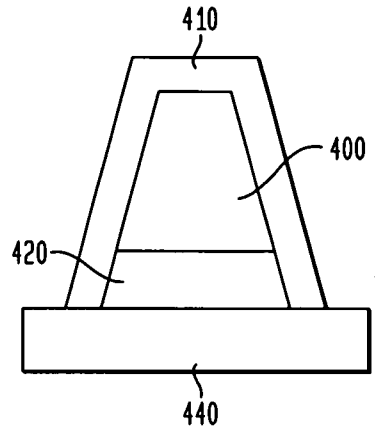


FIG. 5B

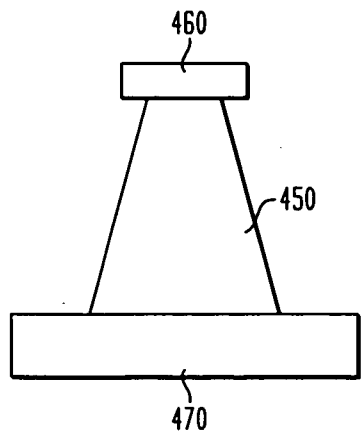


FIG. 6A

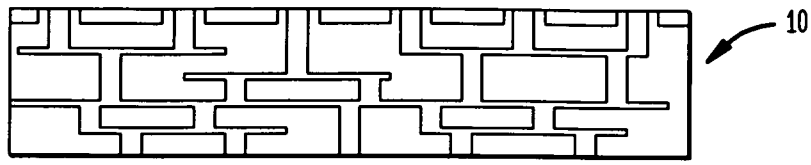


FIG. 6B

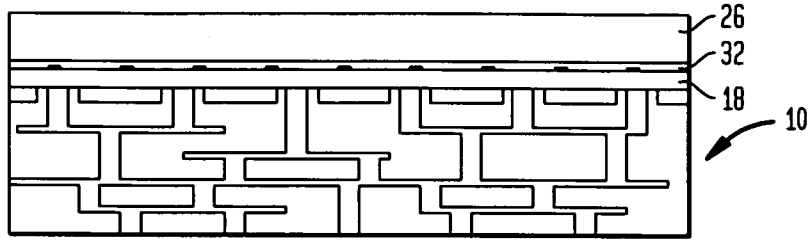


FIG. 6C

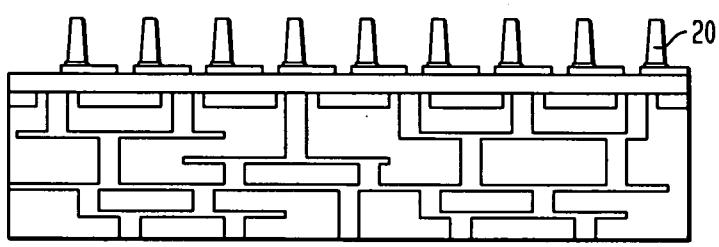


FIG. 6D

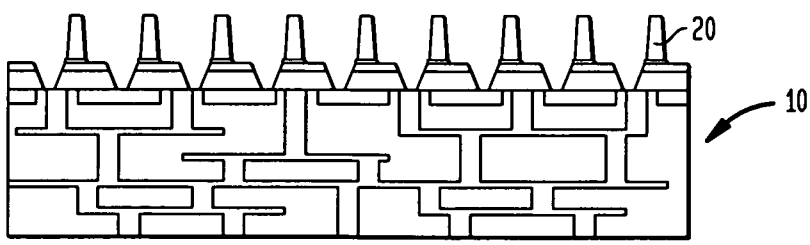


FIG. 6E

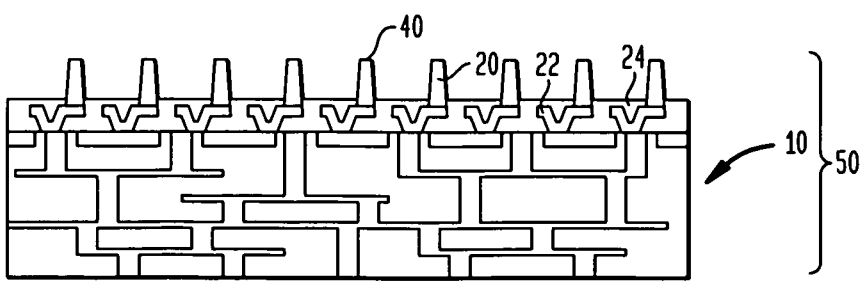


FIG. 7A

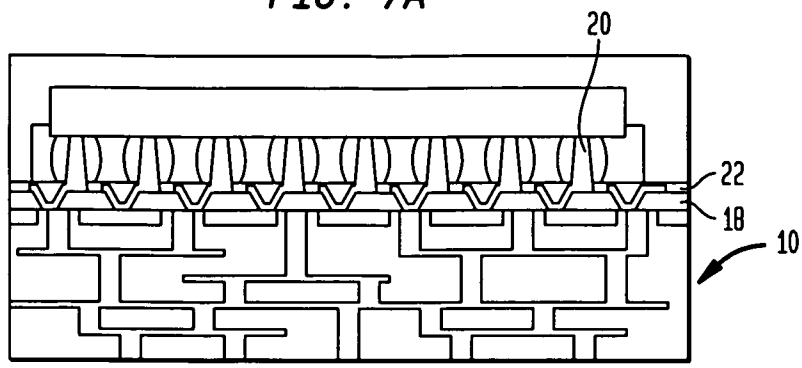


FIG. 7B

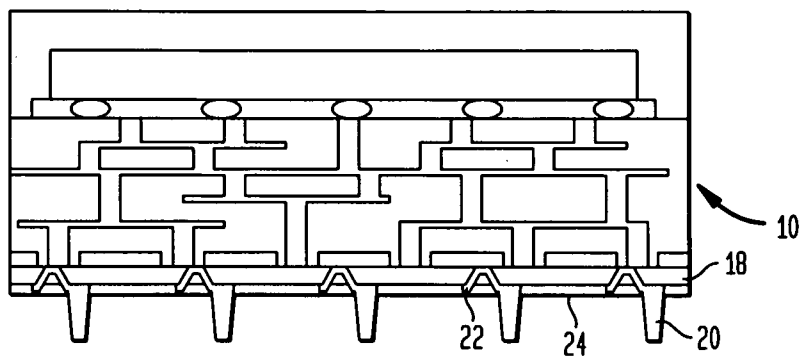
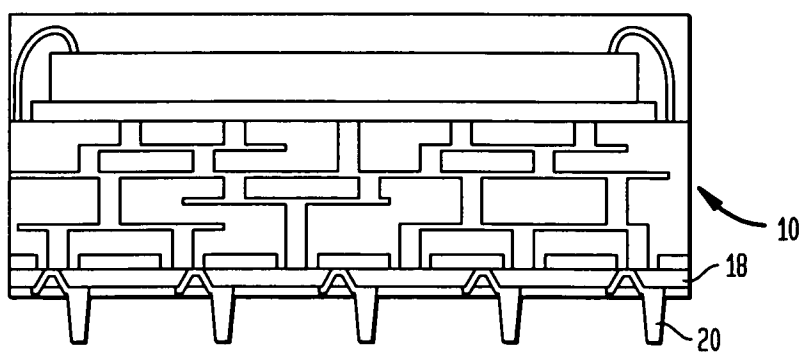


FIG. 7C



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2008/007978

A. CLASSIFICATION OF SUBJECT MATTER

H05K 3/46(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 8: H05K, H01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Utility models and applications for Utility models since 1975

Japanese Utility models and applications for Utility models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKIPASS(KIPO internal) & Keyword: "interconnection, conductive pin"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 59-198747 A (NEC CORP.) 10 November 1984 See the Abstract	1-34
A	JP 59-178752 A (HITACHI LTD.) 11 October 1984 See the Abstract	1-34
A	JP 01-308057 A (MATSUSHITA ELECTRIC IND. CO., LTD.) 12 December 1989 See the Abstract	1-34

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
06 OCTOBER 2008 (06.10.2008)	**06 OCTOBER 2008 (06.10.2008)**

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Korean Intellectual Property Office
Government Complex-Daejeon, 139 Seonsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

KIM, Jong Hee

Telephone No. 82-42-481-8500

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2008/007978

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 59-198747 A	10.11.1984	None	
JP 59-178752 A	11.10.1984	None	
JP 01-308057 A	12.12.1989	None	