



(12) **United States Design Patent**
Chowdhury et al.

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(54) **GROUNDING RING OF A PROCESS KIT FOR SEMICONDUCTOR SUBSTRATE PROCESSING**

37/32897; H01J 37/3414; H01J 37/3423; H01L 21/00; H01L
(Continued)

(71) Applicant: **Applied Materials, Inc.**, Santa Clara, CA (US)

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Primary Examiner — Nicole C Shiflet
Assistant Examiner — Karen M. Jones

(74) *Attorney, Agent, or Firm* — Moser Taboada

(57) **CLAIM**

The ornamental design for a grounding ring of a process kit for semiconductor substrate processing, as shown and described.

DESCRIPTION

FIG. 1 is a top isometric view of a grounding ring of a process kit for semiconductor substrate processing, according to the novel design.

FIG. 2 is a bottom isometric view thereof.

FIG. 3 is a top plan view thereof.

FIG. 4 is a bottom plan view thereof.

(Continued)

(72) Inventors: **Abhishek Chowdhury**, Bangalore (IN); **Nataraj Bhaskar Rao**, Bangalore (IN); **Edwin C. Suarez**, Pleasanton, CA (US); **Harisha Sathyanarayana**, Bangalore (IN); **Diego Ramiro Puente Sotomayor**, Phoenix, AZ (US); **Qanit Takmeel**, Mesa, AZ (US); **Mohammad Kamruzzaman Chowdhury**, Phoenix, AZ (US); **Arun Chakravarthy Chakravarthy**, Tamil Nadu (IN)

(73) Assignee: **APPLIED MATERIALS, INC.**, Santa Clara, CA (US)

(**) Term: **15 Years**

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(51) **LOC (15) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D15/138**; D13/182

(58) **Field of Classification Search**
USPC D15/138, 140, 141, 144, 144.1, 144.2, D15/199; D13/118, 182, 184, 199
CPC H01J 37/32623; H01J 37/32633; H01J 37/32642; H01J 37/32715; H01J 37/32733; H01J 37/32743; H01J

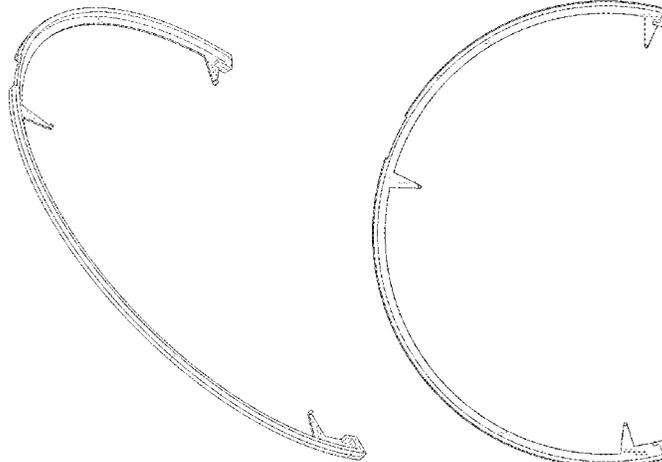


FIG. 5 is a left elevation view thereof.
 FIG. 6 is a right elevation view thereof.
 FIG. 7 is a back elevation view thereof, enlarged to more clearly show details; and,
 FIG. 8 is a front elevation view thereof, enlarged to more clearly show details.

1 Claim, 6 Drawing Sheets

(58) **Field of Classification Search**

CPC 21/0226; H01L 21/02263; H01L 21/02266;
 H01L 21/02269; H01L 21/02271; H01L
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 C23C 16/00; C23C 16/458; C23C 16/44;
 C23C 16/04; C23C 16/4582; C23C
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See application file for complete search history.

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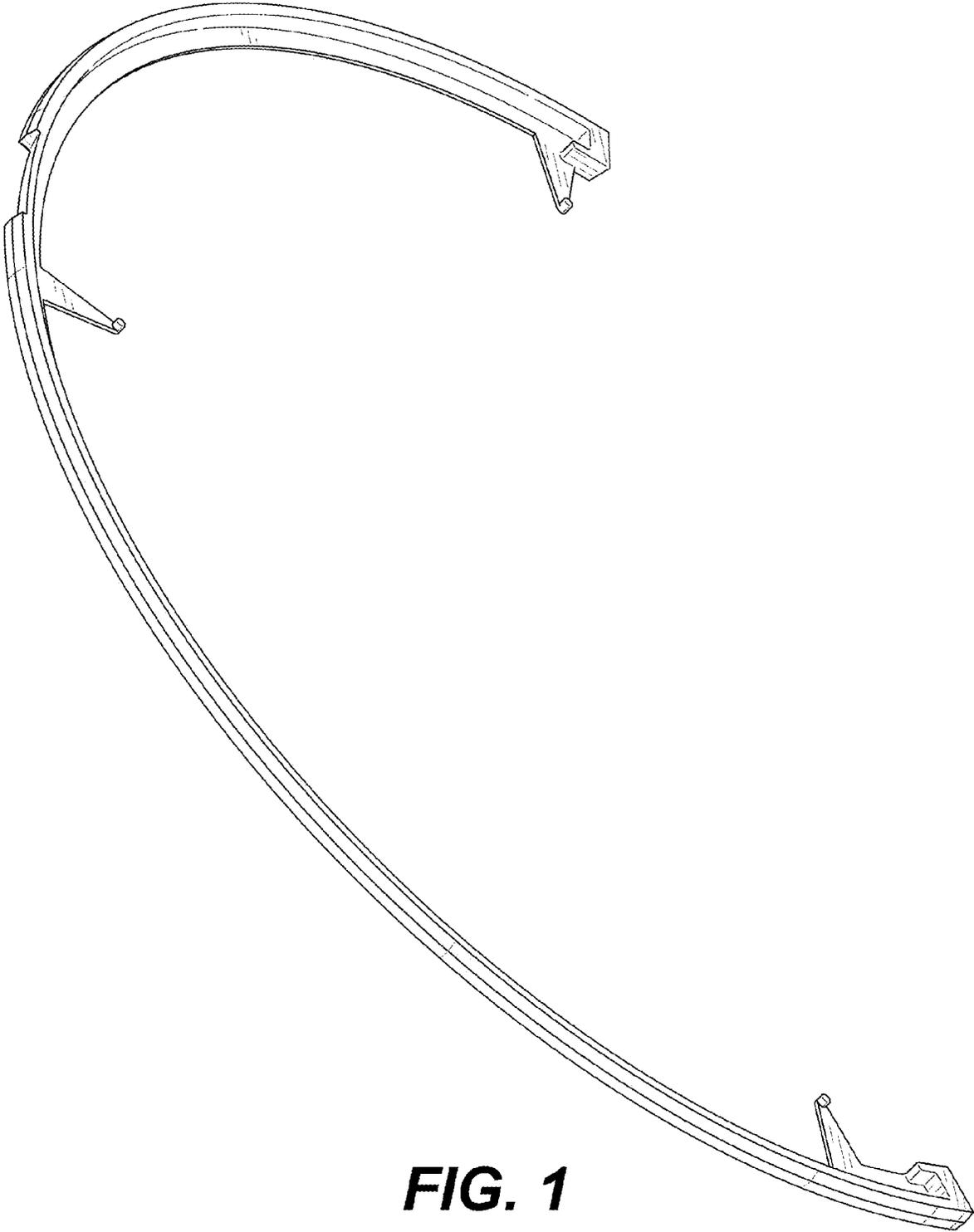


FIG. 1

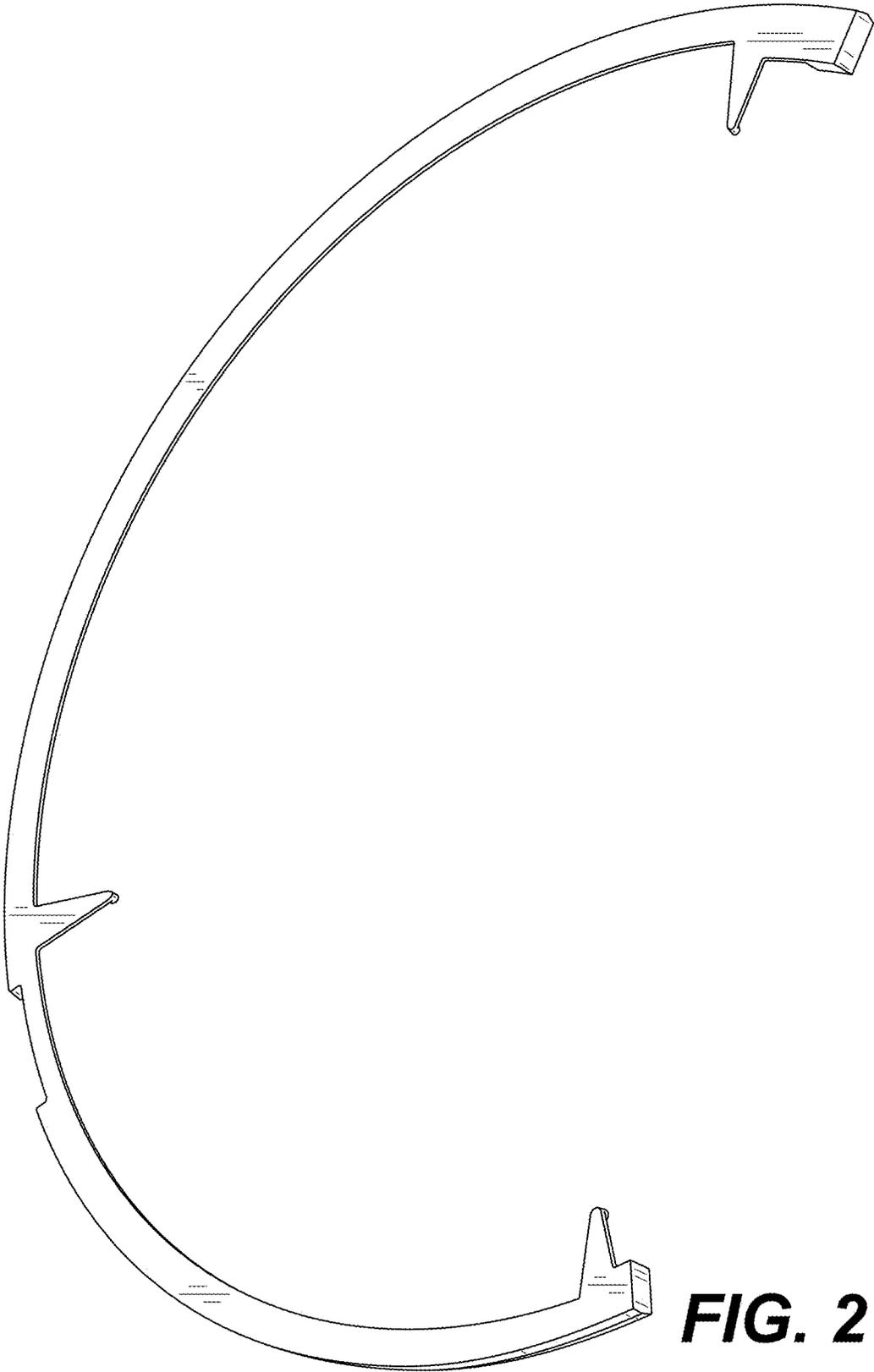


FIG. 2

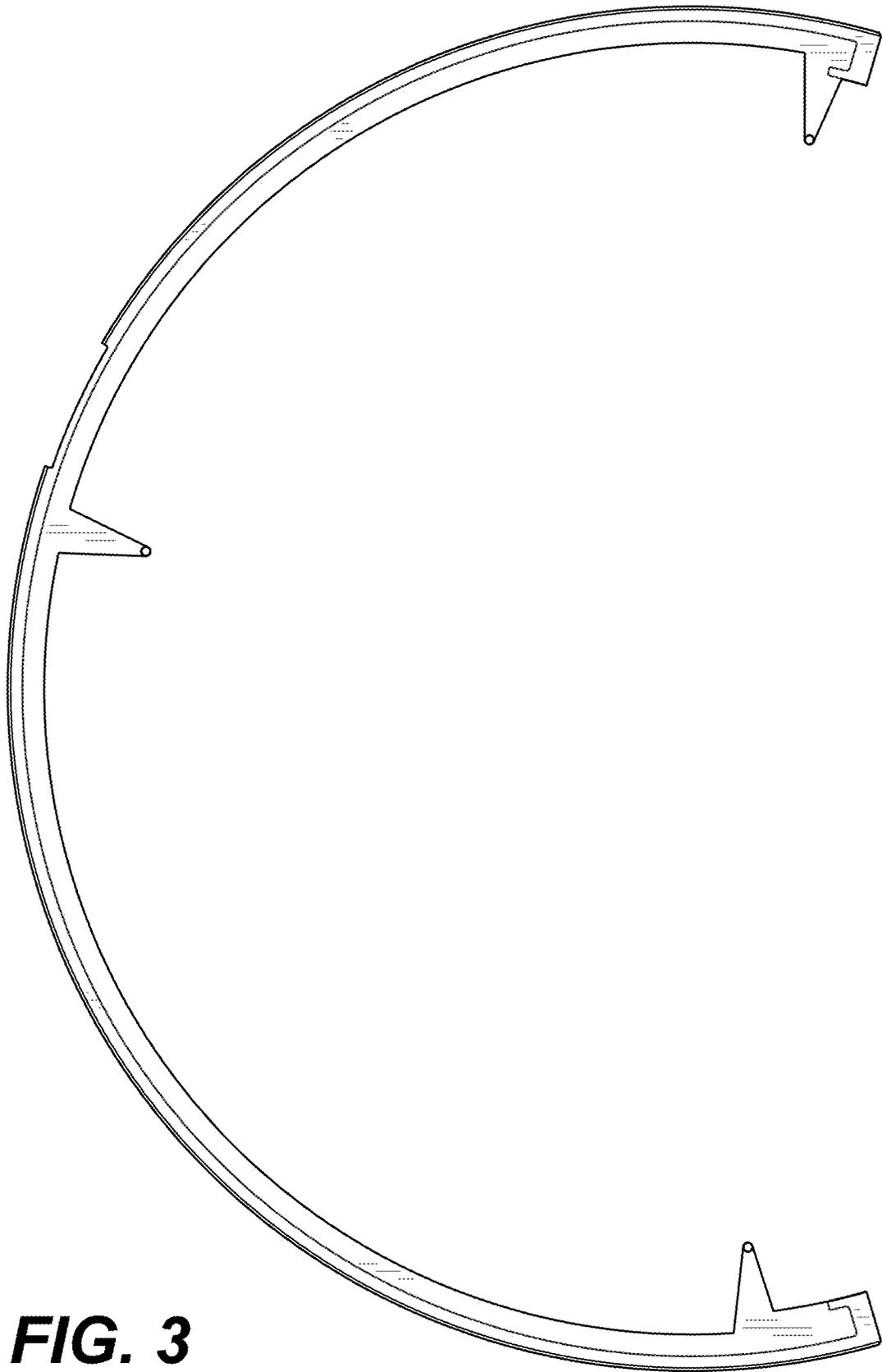


FIG. 3

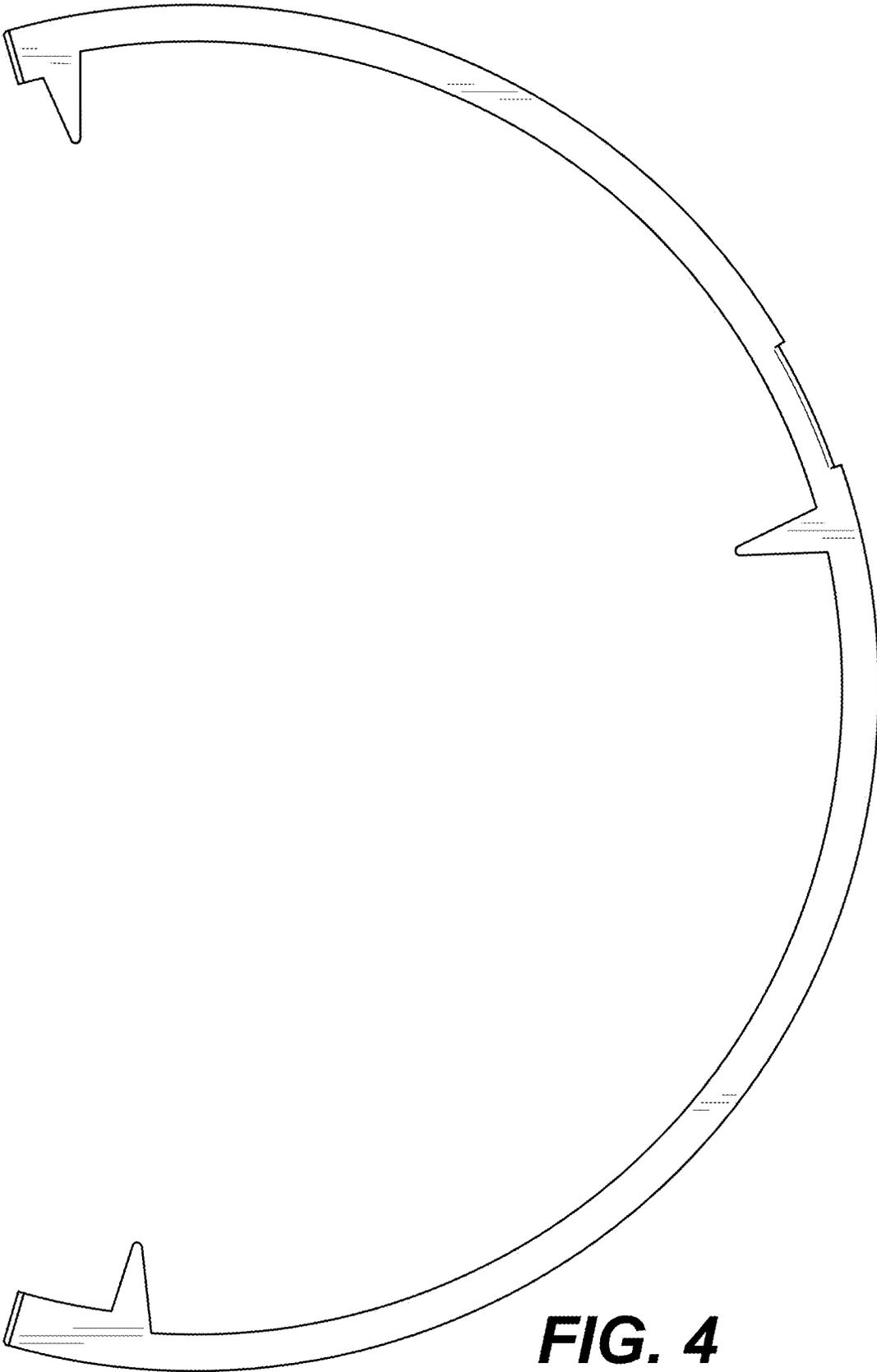


FIG. 4



FIG. 5



FIG. 6

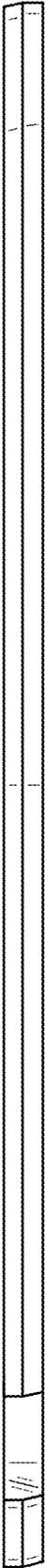


FIG. 7

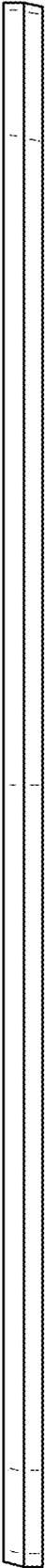


FIG. 8